

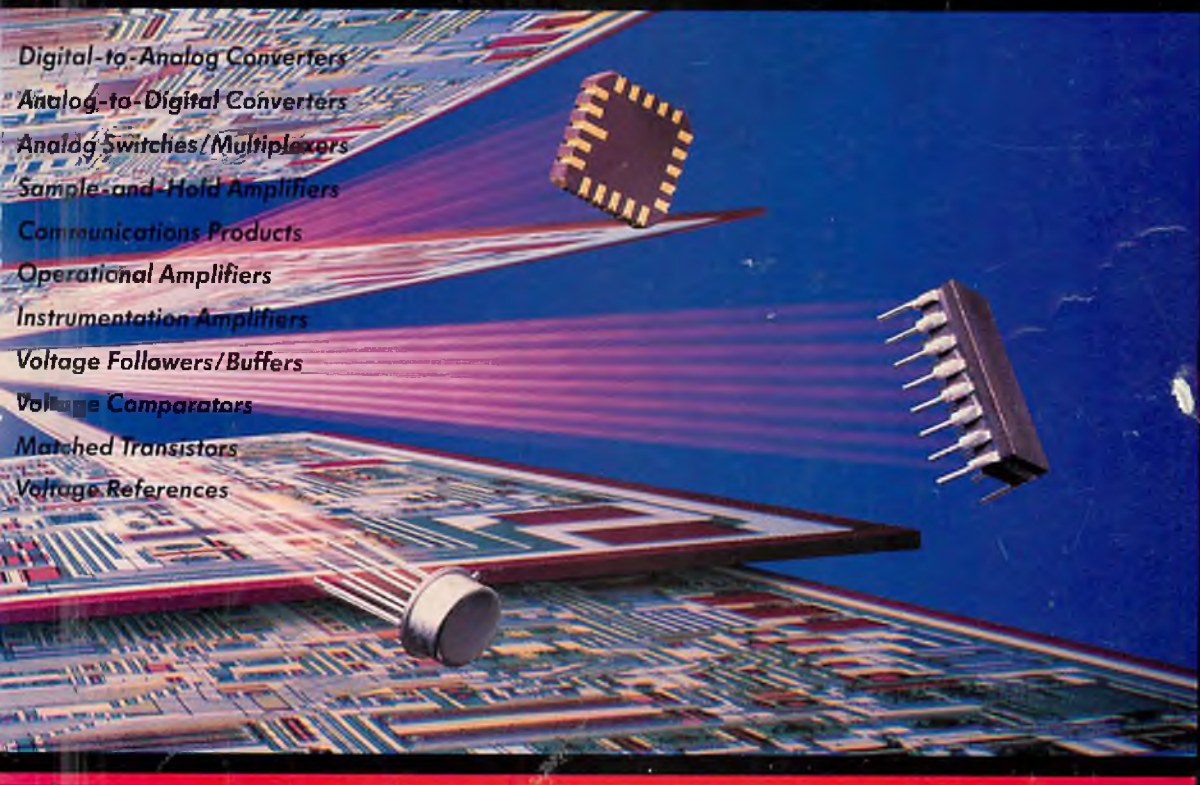


DATABOOK

PRECISION ANALOG INTEGRATED CIRCUITS

1988

Digital-to-Analog Converters
Analog-to-Digital Converters
Analog Switches/Multiplexers
Sample-and-Hold Amplifiers
Communications Products
Operational Amplifiers
Instrumentation Amplifiers
Voltage Followers/Buffers
Voltage Comparators
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Voltage References



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Analog IC Data Book

1988

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Application Notes

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- AB-2** OP-10 Instrumentation Amplifier CMRR vs. Frequency Improvement
- AB-3** Digital Nulling of Precision Op Amps
- AB-4** REF-02 Temperature Controller
- AB-6** Single Supply Operation of the DAC-08 and DAC-20
- AB-9** Dual Precision Voltage Reference
- AB-101** Precision Audio Switch
- AB-102** 12-Bit 4 Quadrant Multiplying D/A Converter
- AB-103** Low-Drift Micropower Instrumentation Amplifier
- AB-104** Single-Supply Micropower Instrumentation Amplifier
- AB-105** Low Input-Current Operational Amplifier
- AB-106** Transimpedance Amplifier
- AB-107** Two-Wire, 4-20mA Current Transmitter
- AB-108** A Micropower Single-Supply Precision Rectifier
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- AB-110** Logarithmic Converter
- AB-111** Single-Supply Wien-Bridge Oscillator
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- AB-113** Precision Ramp Generator
- AB-114** Precision Current Regulator
- AB-115** Micropower 1.23V Bandgap Reference
- AN-6** A Low-Cost, High-Performance Tracking A/D Converter
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- AN-23** D/A Converter Generates Hyperbolic Functions
- AN-24** The OP-17, OP-16, OP-15 as Output Amplifiers for High Speed D/A Converters
- AN-25** Applying the OP-06 Op Amp as a High Precision Comparator
- AN-27** Polarity Programmable Peak Detector
- AN-28** Audio Applications for the DAC-86 Companding D/A Converter
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- AN-35** Understanding Crosstalk in Analog Multiplexers
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- AN-41** Improved Shared-Channel CODEC Design with PMI's Companding DACs
- AN-42** A 1kHz, 0dBm0 Standard Signal Generator
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- AN-48** Designing Digital Repeaters with ICs
- AN-50** A Variable-Frequency, Clock-Recovery Circuit using the RPT-82 or RPT-83
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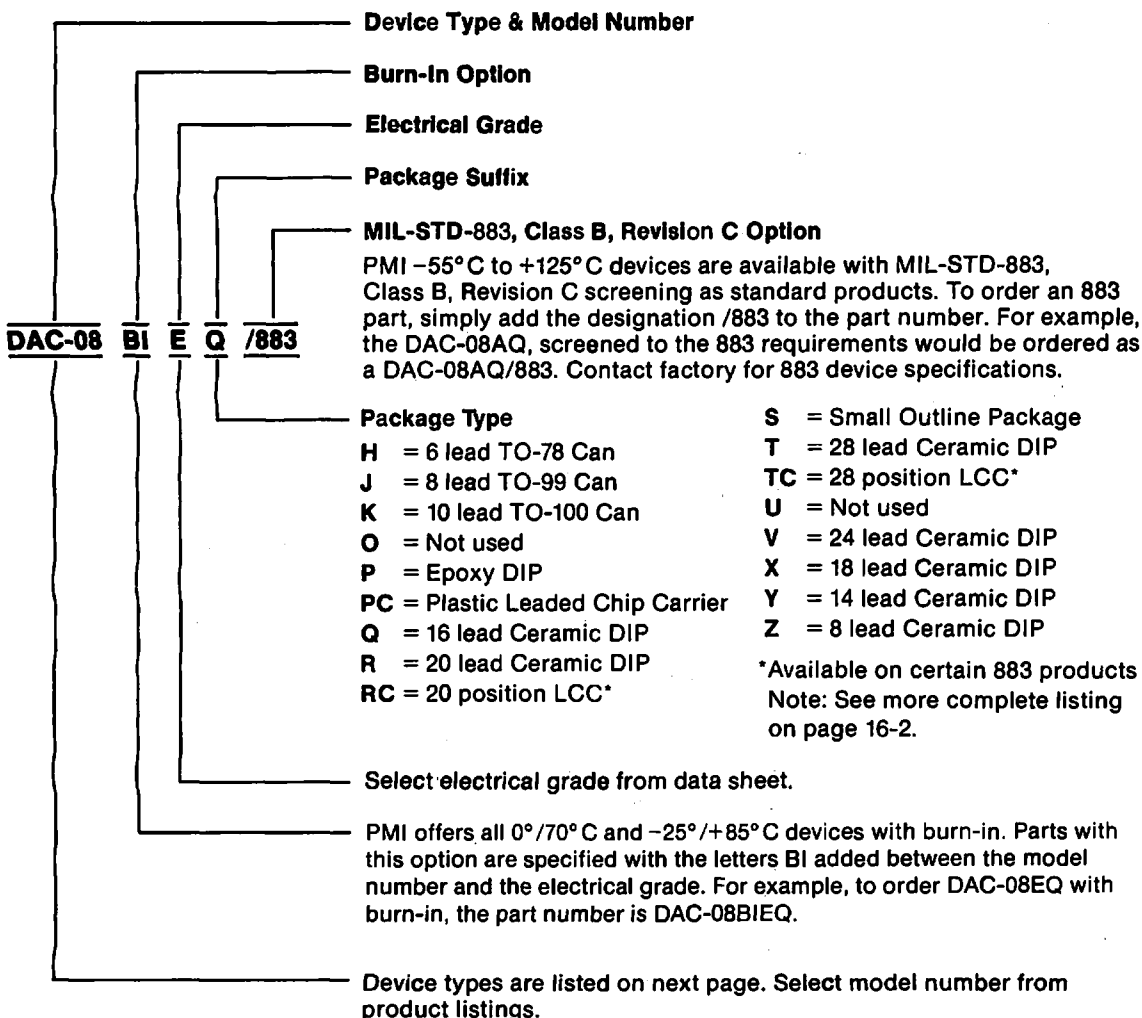
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PACKAGED PRODUCTS PART NUMBERING SYSTEM

2

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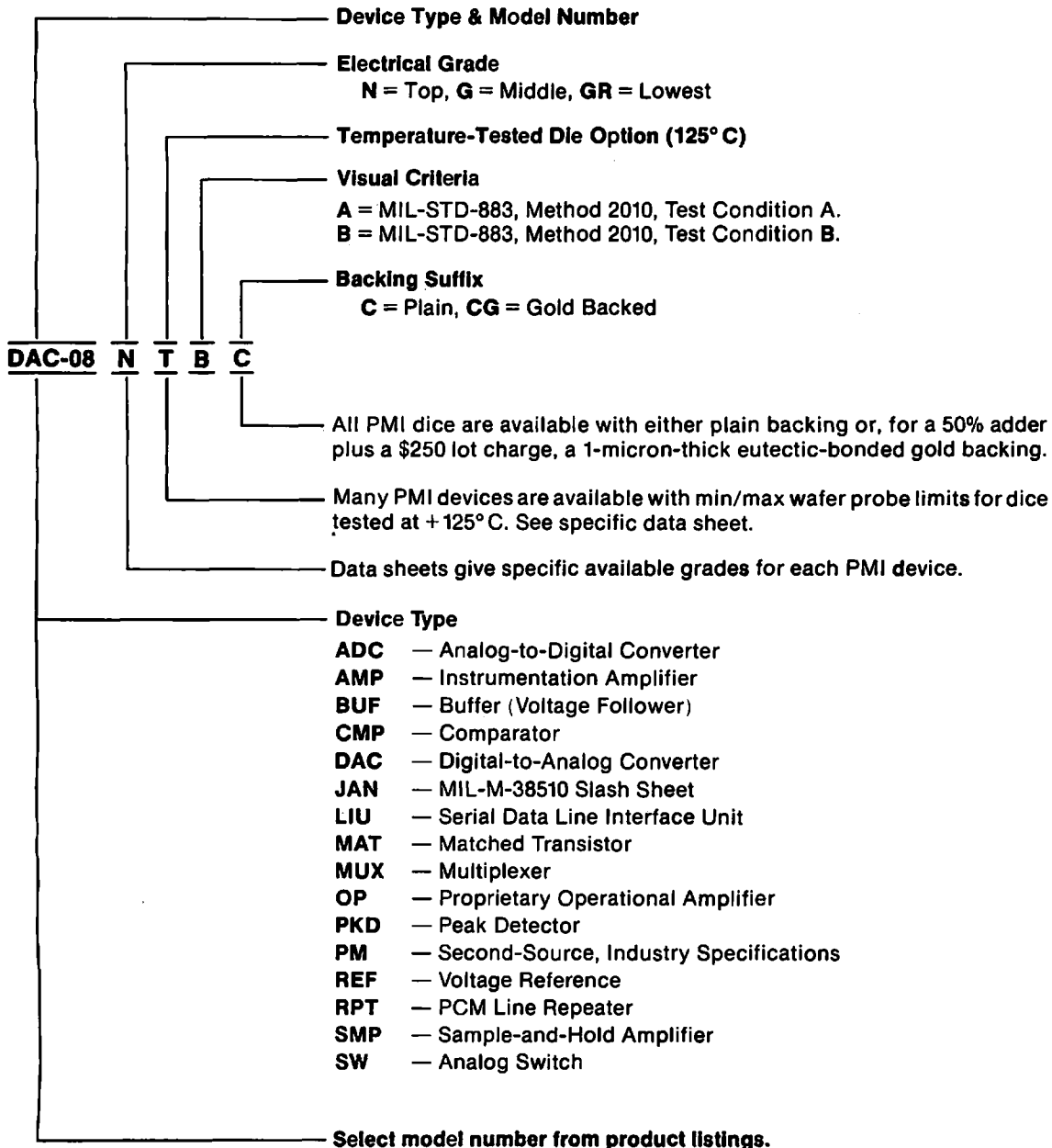




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DICE PART NUMBERING SYSTEM





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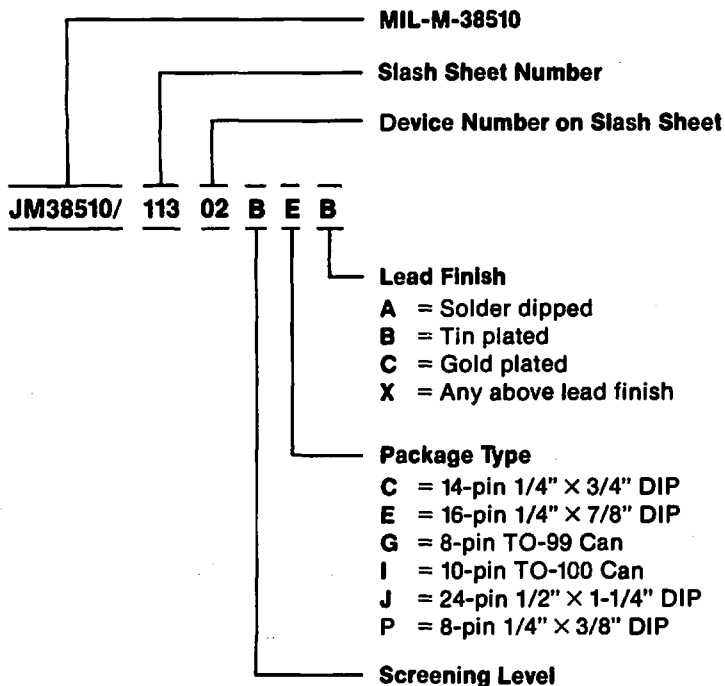
Precision Monolithics Inc.

JAN PRODUCTS PART NUMBERING SYSTEM

MIL-M-38510

PMI's factory is certified to produce JAN parts per MIL-M-38510. PMI currently has JAN Qualifications on the following devices: 741A, 747A, LM108A, LH2108, 4136, LF155A, LF156A, LF157A, LF155, LF156, LF157, OP-07A, OP-07, OP-27A, DAC-08A, DAC-08, LM111 and LM139. These devices are in full compliance with the military detail specifications and are listed on the Qualified Products List (QPL).

SLASH SHEET PART NUMBERING SYSTEM



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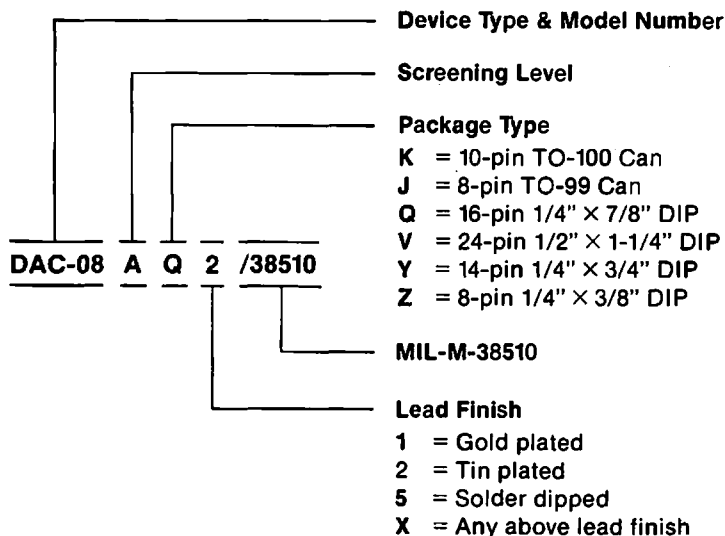
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ORDERING INFORMATION

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JAN PART NUMBERING SYSTEM



MILITARY DRAWINGS

Precision Monolithics offers compliant 883C products tested to military drawing requirements. Those devices currently available are listed in the table below. New devices are being added to the military drawing system as program needs are identified. If your program has a use for products which are not currently on this list, PMI will assist you in preparing a military drawing for your requirement. Please call PMI direct for assistance.

Generic Part Number Military Drawing Number

MUX-08AQ/883	5962-8771601EX
MUX-08BQ/883	5962-8771602EX
MUX-08BRC/883	5962-87716022X
MUX-16AT/883	5962-8771701XX
MUX-16BT/883	5962-8771702XX
MUX-16BTC/883	5962-87717023X
MUX-24AQ/883	5962-8771801EX
MUX-24BQ/883	5962-8771802EX
OP-07AJ/883	5962-8203601GX
OP-07ARC/883	5962-82036012X
OP-07AZ/883	5962-8203601PX
OP-07J/883	5962-8203602GX
OP-07RC/883	5962-82036022X

Generic Part Number Military Drawing Number

OP-07Z/883	5962-8203602PX
OP-14AJ/883	5962-8771401GX
OP-14AZ/883	5962-8771401PX
OP-14BJ/883	5962-8771402GX
OP-14BZ/883	5962-8771402PX
OP-17AJ/883	5962-8770601GX
OP-17AZ/883	5962-8770601PX
OP-17BJ/883	5962-8770602GX
OP-17BZ/883	5962-8770602PX
OP-77AJ/883	5962-8773801GX
OP-77AZ/883	5962-8773801PX
OP-207AY/883	5962-8771501CX
OP-207BY/883	5962-8771502CX
OP-227AY/883	5962-8688701CX
OP-400ATC/883	5962-87771013X
OP-400AY/883	5962-8777101CX
PM-139ARC/883	5962-87739012X
PM-139AY/883	5962-8773901CX
PM-7226AR/883	5962-8780201RX
PM-7524AQ/883	5962-87770001EX
PM-7524ARC/883	5962-87700012X
PM-7524BQ/883	5962-8770002EX
PM-7524BRC/883	5962-87700022X
PM-7528AR/883	5962-8770101RX
PM-7528ARC/883	5962-87701012X



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ORDERING INFORMATION

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ORDERING INFORMATION

Generic Part Number Military Drawing Number

PM-7528BR/883	5962-8770102RX
PM-7528BRC/883	5962-87701022X
PM-7545AR/883	5962-8770201RX
PM-7545ARC/883	5962-87702012X
PM-7545BR/883	5962-8770202RX
PM-7545BRC/883	5962-87702022X
REF-02AJ/883	5962-8551401GX
REF-02AZ/883	5962-8551401PX

DICE INFORMATION

Triple Passivation

Triple Passivation is a three-step process which provides superior reliability and protection for all PMI integrated circuits. First, a specially treated thermal silicon dioxide layer is grown. This protects the junctions and also attracts any residual ionic impurities to the top surface of the oxide, where they are held fixed. Next, a layer of silicon nitride is applied to prevent the entry of any potential contamination or impurities. The third step is the thick glass overcoat layer which leaves only the bonding pads exposed. This "glassivation" protects the die from damage during assembly and is especially important in minimizing yield loss during shipment and assembly of dice for hybrid circuits.

Quality Assurance

PMI believes that quality and reliability must be built into the product; no amount of testing can replace these inherent properties. For this reason, devices are fabricated and processed with many exclusive processes and controls added to improve quality and reliability. The integrity of aluminum metallization is confirmed by sampling wafer lots using Scanning Electron Microscope (SEM) examinations per Method 2018 specifications.

Mechanical Information

Aluminum metallization with a nominal thickness of 10,000 angstroms is standard for all devices. Die thickness is 19 mils minimum to 21 mils maximum. Minimum bonding pad size is 4.0 mils X 4.0 mils for all devices.

Visual Inspection

All dice are 100% visually inspected to the applicable visual criteria per MIL-STD-883 Method 2010, Condition B.

Electrical Connections

The back side of dice should be electrically isolated from adjacent voltages. If it is necessary to connect the die-attach area to a voltage, the following conditions apply:

1. All bipolar technology die substrates should be connected to the negative power supply voltage (V-).
2. All CMOS technology die substrates should be connected to the positive power supply voltage (V_{DD}).

Electrical Testing

All dice are 100% tested to the 25°C DC wafer test limits shown in this catalog before the wafer is separated into individual dice. Due to variations in assembly methods and normal yield loss, PMI does not guarantee specifications after packaging for standard dice. Sample assembly and testing in standard PMI packages to specified LTPD's and min/max specifications are available at extra cost. Consult factory for dice lot qualification negotiation.

Shipping

Protection during shipment is provided by a wafer carrier with anti-static shield and cushioning strip. In addition, the wafer carrier is vacuum sealed in a polyethylene bag.

Military/Aerospace Applications

PMI devices are widely used in military and aerospace programs. A partial listing includes:

Military Aircraft (Electronic Systems)

B-1B	F-14
A-10	F-16
F-15	F-5
F-18	

Missile/Spacecraft

Harm Missile	ADATS
Sparrow Missile	Maverick
Minuteman	Milstar
TOW	Stinger Missile
GOES	Cruise Missile
FAADS	Space Shuttle



ORDERING INFORMATION

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RELIABILITY INFORMATION

MIL-STD-883C

PMI standard "883" parts are manufactured to be in full compliance with all MIL-STD-883 requirements. See Section 3 for more details.

Specials

At PMI, we have a proven track record for handling "customer specials". Many IC manufacturers shy away from processing precision linear ICs to the unique in-house specifications of their customers. PMI recognizes your special needs and welcomes the opportunities provided by the military/aerospace industry. The Military and Aerospace industry is a cornerstone of PMI's business and we will continue to offer the extra processing that your applications require.

Radiation Resistance

As a leading supplier of precision linear ICs to the military/aerospace industry, PMI is suppor-

tive of the system designer's needs for readily available, standard components that are radiation resistant. A number of standard PMI linear integrated circuits have characteristically demonstrated good resistance to radiation. These devices have been subjected to radiation levels necessary to perform effectively in military/aerospace radiation environments, and they are now being used in a number of demanding military and space programs.

Experiments to isolate the processing mechanisms that led to PMI's increased radiation hardness characteristics have pointed heavily toward the use of a silicon nitride passivation layer. While we do not believe that this process is the only radiation hardening advantage of PMI devices, it does add a great deal to survivability.

For more information request PMI's "Radiation Resistance" brochure.



Precision Monolithics Inc.

ORDERING INFORMATION

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ORDERING INFORMATION

ALTERNATE REPLACEMENTS FOR DISCONTINUED ELECTRICAL GRADES AND PACKAGE TYPES

PMI has discontinued certain electrical grades and/or package options. The guide below is provided to help the designer select an appropriate alternate device. **Exact**

Replacements are drop-in replacements with identical packaging and electrical specifications, equal to or better than the original device.

Similar Replacements will serve the same basic function, but electrical specifications or packaging may vary.

Packaged Products

Part Number	Alternate Device Type
AMP01BTC	EXACT REPLACEMENT — AMP01BTC/883C
CMP02CZ	SIMILAR REPLACEMENT — CMP02CP
CMP02EJ	SIMILAR REPLACEMENT — CMP01EP
CMP02EZ	SIMILAR REPLACEMENT — CMP02EP
CMP02J	SIMILAR REPLACEMENT — CMP02EP
CMP02J/883C	SIMILAR REPLACEMENT — CMP01J/883C
CMP02Z	SIMILAR REPLACEMENT — CMP02EP
CMP02Z/883C	SIMILAR REPLACEMENT — CMP01Z/883C
DAC01AY	SIMILAR REPLACEMENT — DAC01FY
DAC01AY/883C	SIMILAR REPLACEMENT — DAC01Y/883C
DAC01BY	SIMILAR REPLACEMENT — DAC01FY
DAC01FY/883C	EXACT REPLACEMENT — DAC01Y/883C
DAC01Y	EXACT REPLACEMENT — DAC01Y/883C
DAC02BCX1	EXACT REPLACEMENT — DAC02ACX1
DAC03BDX1	EXACT REPLACEMENT — DAC03ADX1
DAC03BDX2	EXACT REPLACEMENT — DAC03ADX2
DAC03DDX1	EXACT REPLACEMENT — DAC03CDX1
DAC03DDX2	EXACT REPLACEMENT — DAC03CDX2
DAC05CX1	EXACT REPLACEMENT — DAC05AX1
DAC05CX1/883C	EXACT REPLACEMENT — DAC05AX1/883C
DAC05GX1	EXACT REPLACEMENT — DAC05EX1
DAC06CX	EXACT REPLACEMENT — DAC06BX
DAC06CX/883C	EXACT REPLACEMENT — DAC06BX/883C
DAC06GX	EXACT REPLACEMENT — DAC06FX
DAC08RC	EXACT REPLACEMENT — DAC08RC/883C
DAC10CX/883C	EXACT REPLACEMENT — DAC10BX/883C
DAC100BBQ6/883C	EXACT REPLACEMENT — DAC100ACQ6/883C
DAC100BCQ6/883C	EXACT REPLACEMENT — DAC100ACQ6/883C
DAC100BCQ8	EXACT REPLACEMENT — DAC100BBQ8
DAC100CCQ8	EXACT REPLACEMENT — DAC100BBQ8
DAC100DDQ4	EXACT REPLACEMENT — DAC100CCQ4
DAC100DDQ8	EXACT REPLACEMENT — DAC100BBQ8

Packaged Products

Part Number	Alternate Device Type
DAC208AX	SIMILAR REPLACEMENT — DAC210
DAC208AX/883C	SIMILAR REPLACEMENT — DAC210
DAC208BX	SIMILAR REPLACEMENT — DAC210
DAC208BX/883C	SIMILAR REPLACEMENT — DAC210
DAC208EX	SIMILAR REPLACEMENT — DAC210
DAC208FX	SIMILAR REPLACEMENT — DAC210
DAC210ASX	SIMILAR REPLACEMENT — DAC210EX
DAC210ASX/883C	SIMILAR REPLACEMENT — DAC210EX
DAC210AX	SIMILAR REPLACEMENT — DAC210EX
DAC210AX/883C	SIMILAR REPLACEMENT — DAC210EX
DAC210BSX	SIMILAR REPLACEMENT — DAC210FX
DAC210BSX/883C	SIMILAR REPLACEMENT — DAC210FX
DAC210BX	SIMILAR REPLACEMENT — DAC210FX
DAC210BX/883C	SIMILAR REPLACEMENT — DAC210FX
DAC210ESX	SIMILAR REPLACEMENT — DAC210EX
DAC210FSX	SIMILAR REPLACEMENT — DAC210FX
DMX88EQ	SIMILAR REPLACEMENT — MUX88FQ
DMX88FQ	SIMILAR REPLACEMENT — MUX88FQ
GAP01AX	SIMILAR REPLACEMENT — PKD01
GAP01AX/883C	SIMILAR REPLACEMENT — PKD01
GAP01BX	SIMILAR REPLACEMENT — PKD01
GAP01BX/883C	SIMILAR REPLACEMENT — PKD01
GAP01EP	SIMILAR REPLACEMENT — PKD01
GAP01EX	SIMILAR REPLACEMENT — PKD01
GAP01FP	SIMILAR REPLACEMENT — PKD01
GAP01FX	SIMILAR REPLACEMENT — PKD01
MAT02BRC	EXACT REPLACEMENT — MAT02BRC/883C
MUX08BRC	EXACT REPLACEMENT — MUX08BRC/883C
MUX16BTC	EXACT REPLACEMENT — MUX16BTC/883C
MUX28AT	NOT RECOMMENDED FOR NEW DESIGNS
MUX28AT/883C	NOT RECOMMENDED FOR NEW DESIGNS
MUX28BT	NOT RECOMMENDED FOR NEW DESIGNS
MUX28BT/883C	NOT RECOMMENDED FOR NEW DESIGNS
MUX88EQ	SIMILAR REPLACEMENT — MUX88FQ
OP01GJ/883C	EXACT REPLACEMENT — OP01J/883C
OP01GZ	SIMILAR REPLACEMENT — OP01HZ
OP01GZ/883C	SIMILAR REPLACEMENT — OP01J/883C
OP01Z	SIMILAR REPLACEMENT — OP01J
OP01Z/883C	SIMILAR REPLACEMENT — OP01J/883C
OP02BZ	EXACT REPLACEMENT — OP02AZ
OP02BZ/883C	EXACT REPLACEMENT — OP02AZ/883C
OP02DJ	EXACT REPLACEMENT — OP02CJ
OP02DZ	EXACT REPLACEMENT — OP02CZ
OP02Z	EXACT REPLACEMENT — OP02AZ
OP04AK	EXACT REPLACEMENT — OP04AK/883C
OP04BK	EXACT REPLACEMENT — OP04K/883C
OP04BK/883C	EXACT REPLACEMENT — OP04K/883C
OP04BY	EXACT REPLACEMENT — OP04Y
OP04BY/883C	EXACT REPLACEMENT — OP04Y/883C
OP04CK	EXACT REPLACEMENT — OP04K/883C
OP04K	EXACT REPLACEMENT — OP04K/883C



Precision Monolithics Inc.

ORDERING INFORMATION

Packaged Products

Part Number	Alternate Device Type
OP05AY	SIMILAR REPLACEMENT — OP05AZ
OP05AY/883C	SIMILAR REPLACEMENT — OP05AZ/883C
OP05CY	SIMILAR REPLACEMENT — OP05CZ
OP05EY	SIMILAR REPLACEMENT — OP05EZ
OP05Y	SIMILAR REPLACEMENT — OP05Z
OP05Y/883C	SIMILAR REPLACEMENT — OP05Z/883C
OP06AZ	SIMILAR REPLACEMENT — OP06AJ
OP06AZ/883C	SIMILAR REPLACEMENT — OP06AJ/883C
OP06BZ	SIMILAR REPLACEMENT — OP06BJ
OP06BZ/883C	SIMILAR REPLACEMENT — OP06BJ/883C
OP06CJ	EXACT REPLACEMENT — OP06BJ
OP06CZ	SIMILAR REPLACEMENT — OP06BJ
OP06EJ	SIMILAR REPLACEMENT — OP06EZ
OP07AY	SIMILAR REPLACEMENT — OP07AZ
OP07AY/883C	SIMILAR REPLACEMENT — OP07AZ/883C
OP07CY	SIMILAR REPLACEMENT — OP07CZ
OP07DY	SIMILAR REPLACEMENT — OP07DZ
OP07EY	SIMILAR REPLACEMENT — OP07EZ
OP07RC	EXACT REPLACEMENT — OP07RC/883C
OP07Y	SIMILAR REPLACEMENT — OP07Z
OP07Y/883C	SIMILAR REPLACEMENT — OP07Z/883C
OP08CJ	EXACT REPLACEMENT — OP08AJ
OP08CJ/883C	EXACT REPLACEMENT — OP08AJ/883C
OP08CZ	EXACT REPLACEMENT — OP08AZ
OP08GJ	EXACT REPLACEMENT — OP08EJ
OP08GP	EXACT REPLACEMENT — OP08EP
OP09BY	EXACT REPLACEMENT — OP09AY
OP09BY/883C	EXACT REPLACEMENT — OP09AY/883C
OP11ARC	EXACT REPLACEMENT — OP11ARC/883C
OP11CY	EXACT REPLACEMENT — OP11BY
OP11GY	EXACT REPLACEMENT — OP11FY
OP12AJ	EXACT REPLACEMENT — PM1012AJ
OP12AJ/883C	EXACT REPLACEMENT — PM1012AJ/883C
OP12AZ/883C	EXACT REPLACEMENT — PM1012AZ/883C
OP12BJ	EXACT REPLACEMENT — PM1012AJ
OP12BJ/883C	EXACT REPLACEMENT — PM1012AJ/883C
OP12BZ/883C	EXACT REPLACEMENT — PM1012AZ/883C
OP12CJ	EXACT REPLACEMENT — PM1012AJ
OP12CJ/883C	EXACT REPLACEMENT — PM1012AJ/883C
OP12CZ/883C	EXACT REPLACEMENT — PM1012AZ/883C
OP12FZ	EXACT REPLACEMENT — PM1012GZ
OP14BJ	EXACT REPLACEMENT — OP14AJ
OP14BJ/883C	EXACT REPLACEMENT — OP14AJ/883C
OP14BZ	EXACT REPLACEMENT — OP14AZ
OP14BZ/883C	EXACT REPLACEMENT — OP14AZ/883C
OP14DJ	EXACT REPLACEMENT — OP14CJ
OP15BZ/883C	EXACT REPLACEMENT — OP15AZ/883C
OP15CJ	EXACT REPLACEMENT — OP15BJ
OP15CJ/883C	EXACT REPLACEMENT — OP15BJ/883C
OP15CZ	EXACT REPLACEMENT — OP15BZ
OP15CZ/883C	EXACT REPLACEMENT — OP15AZ/883C

Packaged Products

Part Number	Alternate Device Type
OP16AZ	SIMILAR REPLACEMENT — OP16AJ
OP16AZ/883C	SIMILAR REPLACEMENT — OP16BZ/883C
OP16BZ	SIMILAR REPLACEMENT — OP16BJ
OP16CJ	EXACT REPLACEMENT — OP16BJ
OP16CJ/883C	EXACT REPLACEMENT — OP16BJ/883C
OP16CZ	SIMILAR REPLACEMENT — OP16BJ
OP17AZ	SIMILAR REPLACEMENT — OP17AJ
OP17BJ	EXACT REPLACEMENT — OP17AJ
OP17BZ	SIMILAR REPLACEMENT — OP17AJ
OP17CJ/883C	EXACT REPLACEMENT — OP17AJ/883C
OP17CZ	SIMILAR REPLACEMENT — OP17CJ
OP17CZ/883C	EXACT REPLACEMENT — OP17BZ/883C
OP20BJ/883C	SIMILAR REPLACEMENT — OP20BJ
OP20BZ/883C	SIMILAR REPLACEMENT — OP20BZ
OP20CJ/883C	SIMILAR REPLACEMENT — OP20CJ
OP20CZ/883C	SIMILAR REPLACEMENT — OP20CZ
OP21AJ/883C	SIMILAR REPLACEMENT — OP21AJ
OP21AZ/883C	SIMILAR REPLACEMENT — OP21AZ
OP21BJ/883C	SIMILAR REPLACEMENT — OP21BJ
OP21BZ/883C	SIMILAR REPLACEMENT — OP21BZ
OP21EP	SIMILAR REPLACEMENT — OP21FP
OP21FJ	SIMILAR REPLACEMENT — OP21FZ
OP21GZ	SIMILAR REPLACEMENT — OP21GJ
OP22AZ	SIMILAR REPLACEMENT — OP32AZ
OP22BJ	SIMILAR REPLACEMENT — OP32BZ
OP22BJ/883C	SIMILAR REPLACEMENT — OP32BZ/883C
OP22BZ	SIMILAR REPLACEMENT — OP32BZ
OP22BZ/883C	SIMILAR REPLACEMENT — OP32BZ/883C
OP22FJ	SIMILAR REPLACEMENT — OP22FZ
OP22HJ	SIMILAR REPLACEMENT — OP22HZ
OP27BRC	EXACT REPLACEMENT — OP27BRC/883C
OP27CJ/883C	EXACT REPLACEMENT — OP27BJ/883C
OP27CZ/883C	EXACT REPLACEMENT — OP27BZ/883C
OP32BRC	EXACT REPLACEMENT — OP32BRC/883C
OP37BRC	EXACT REPLACEMENT — OP37BRC/883C
OP37CZ/883C	EXACT REPLACEMENT — OP37BZ/883C
OP207BY	EXACT REPLACEMENT — OP207AY
OP207BY/883C	EXACT REPLACEMENT — OP207AY/883C
OP215AY	SIMILAR REPLACEMENT — OP215AZ
OP215AY/883C	SIMILAR REPLACEMENT — OP215AZ/883C
OP215BY	SIMILAR REPLACEMENT — OP215BZ
OP215BY/883C	SIMILAR REPLACEMENT — OP215BZ/883C
OP215CJ	SIMILAR REPLACEMENT — OP215CZ
OP215CY	SIMILAR REPLACEMENT — OP215BZ
OP215CY/883C	SIMILAR REPLACEMENT — OP215CZ/883C
OP215CZ	EXACT REPLACEMENT — OP215BZ
OP215EY	SIMILAR REPLACEMENT — OP215EZ
OP215FY	SIMILAR REPLACEMENT — OP215FZ
OP215GJ	EXACT REPLACEMENT — OP215FJ
OP215GY	SIMILAR REPLACEMENT — OP215GZ



Precision Monolithics Inc.

ORDERING INFORMATION

Packaged Products

Part Number Alternate Device Type

OP220AZ/883C	SIMILAR REPLACEMENT — OP220AJ/883C
OP220BJ/883C	EXACT REPLACEMENT — OP220AJ/883C
OP220BZ	EXACT REPLACEMENT — OP220AZ
OP220BZ/883C	SIMILAR REPLACEMENT — OP220AJ/883C
OP220CZ/883C	SIMILAR REPLACEMENT — OP220CJ/883C
OP220EJ	SIMILAR REPLACEMENT — OP220EZ
OP220FJ	SIMILAR REPLACEMENT — OP220FZ
OP220HJ	SIMILAR REPLACEMENT — OP220FZ
OP220HZ	SIMILAR REPLACEMENT — OP220FZ
OP221AJ	SIMILAR REPLACEMENT — OP221AZ
OP221AJ/883C	SIMILAR REPLACEMENT — OP221AZ
OP221AZ/883C	SIMILAR REPLACEMENT — OP221AZ
OP221BJ	SIMILAR REPLACEMENT — OP221AZ
OP221BJ/883C	SIMILAR REPLACEMENT — OP221AZ
OP221BZ	EXACT REPLACEMENT — OP221AZ
OP221BZ/883C	SIMILAR REPLACEMENT — OP221AZ
OP221CJ/883C	SIMILAR REPLACEMENT — OP221CJ
OP221CZ	SIMILAR REPLACEMENT — OP221CJ
OP221CZ/883C	SIMILAR REPLACEMENT — OP221CJ
OP221EJ	SIMILAR REPLACEMENT — OP221EZ
OP221FJ	SIMILAR REPLACEMENT — OP221EZ
OP221FZ	EXACT REPLACEMENT — OP221EZ
OP227BY	EXACT REPLACEMENT — OP227AY
OP227BY/883C	EXACT REPLACEMENT — OP227AY/883C
OP227CY	EXACT REPLACEMENT — OP227AY
OP420CRC	EXACT REPLACEMENT — OP420CRC/883C
PM108AJ	EXACT REPLACEMENT — PM108AJ/883C
PM108ARC	EXACT REPLACEMENT — PM108ARC/883C
PM108AZ/883C	SIMILAR REPLACEMENT — PM108AJ/883C
PM108J	EXACT REPLACEMENT — PM108J/883C
PM108Z/883C	SIMILAR REPLACEMENT — PM108J/883C
PM111RC	EXACT REPLACEMENT — PM111RC/883C
PM139ARC	EXACT REPLACEMENT — PM139ARC/883C
PM148Y/883C	EXACT REPLACEMENT — OP11BY/883C
PM155ARC	EXACT REPLACEMENT — PM155ARC/883C
PM155AZ	SIMILAR REPLACEMENT — PM155AJ
PM156ARC	EXACT REPLACEMENT — PM156ARC/883C
PM157AJ	EXACT REPLACEMENT — PM157AJ/883C
PM208J	EXACT REPLACEMENT — PM208AJ
PM357AJ	EXACT REPLACEMENT — PM157AJ/883C
PM357AZ	EXACT REPLACEMENT — PM157AZ
PM725CJ	SIMILAR REPLACEMENT — OP06
PM725CP	SIMILAR REPLACEMENT — OP06
PM725CZ	SIMILAR REPLACEMENT — OP06
PM725J	SIMILAR REPLACEMENT — OP06
PM725Z	SIMILAR REPLACEMENT — OP06
PM2108AQ	SIMILAR REPLACEMENT — PM2108AQ2/38510
PM2108AQ/883C	SIMILAR REPLACEMENT — PM2108AQ2/38510
PM2108Q	SIMILAR REPLACEMENT — PM2108AQ2/38510
PM2108Q/883C	SIMILAR REPLACEMENT — PM2108AQ2/38510

Packaged Products

Part Number Alternate Device Type

PM4136RC	EXACT REPLACEMENT — PM4136RC/883C
REF01RC	EXACT REPLACEMENT — REF01RC/883C
REF02DJ	EXACT REPLACEMENT — REF02CJ
REF02DZ	EXACT REPLACEMENT — REF02CZ
REF02RC	EXACT REPLACEMENT — REF02RC/883C
SMP11BRC	EXACT REPLACEMENT — SMP11BRC/883C
SW02BQ	SIMILAR REPLACEMENT — SW01BQ
SW02BQ/883C	SIMILAR REPLACEMENT — SW01BQ/883C
SW05BK	NOT RECOMMENDED FOR NEW DESIGNS
SW05BK/883C	NOT RECOMMENDED FOR NEW DESIGNS
SW05BY	NOT RECOMMENDED FOR NEW DESIGNS
SW05BY/883C	NOT RECOMMENDED FOR NEW DESIGNS
SW05FK	NOT RECOMMENDED FOR NEW DESIGNS
SW05FY	NOT RECOMMENDED FOR NEW DESIGNS
SW05GP	NOT RECOMMENDED FOR NEW DESIGNS
SW06BRC	EXACT REPLACEMENT — SW06BRC/883C
SW06GQ	SIMILAR REPLACEMENT — SW06GP
SW201BQ	SIMILAR REPLACEMENT — SW06BQ
SW201FQ	SIMILAR REPLACEMENT — SW201GP
SW202BQ	SIMILAR REPLACEMENT — SW06BQ
SW202BQ/883C	SIMILAR REPLACEMENT — SW06BQ/883C
SW202FQ	SIMILAR REPLACEMENT — SW202GP

Dice Products

Part Number Alternate Device Type

AMP01GAC	SIMILAR REPLACEMENT — AMP01GBC
AMP01NAC	SIMILAR REPLACEMENT — AMP01NBC
BUF03GAC	SIMILAR REPLACEMENT — BUF03GBC
BUF03NAC	SIMILAR REPLACEMENT — BUF03NBC
CMP01GRAC	SIMILAR REPLACEMENT — CMP01GRBC
CMP01NAC	SIMILAR REPLACEMENT — CMP01NBC
CMP02GRAC	SIMILAR REPLACEMENT — CMP02GRBC
CMP02NAC	SIMILAR REPLACEMENT — CMP02NBC
CMP04GAC	SIMILAR REPLACEMENT — CMP04GBC
CMP04NAC	SIMILAR REPLACEMENT — CMP04NBC
DAC01GAC	SIMILAR REPLACEMENT — DAC01GBC
DAC01NAC	SIMILAR REPLACEMENT — DAC01NBC
DAC02GAC	SIMILAR REPLACEMENT — DAC02GBC
DAC02NAC	SIMILAR REPLACEMENT — DAC02NBC
DAC08GAC	SIMILAR REPLACEMENT — DAC08GBC
DAC08GRAC	SIMILAR REPLACEMENT — DAC08GRBC
DAC08GTAC	SIMILAR REPLACEMENT — DAC08GTBC
DAC08NAC	SIMILAR REPLACEMENT — DAC08NBC
DAC08NTAC	SIMILAR REPLACEMENT — DAC08NTBC
DAC10GAC	SIMILAR REPLACEMENT — DAC10GBC
DAC10NAC	SIMILAR REPLACEMENT — DAC10NBC

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ORDERING INFORMATION



Precision Monolithics Inc.

ORDERING INFORMATION

Dice Products

Part Number	Alternate Device Type
DAC20GAC	SIMILAR REPLACEMENT — DAC20GBC
DAC210GAC	SIMILAR REPLACEMENT — DAC210GBC
DAC210GRAC	SIMILAR REPLACEMENT — DAC210GRBC
DAC210NAC	SIMILAR REPLACEMENT — DAC210NBC
DAC312GAC	SIMILAR REPLACEMENT — DAC312GBC
DAC312NAC	SIMILAR REPLACEMENT — DAC312NBC
DAC888GAC	SIMILAR REPLACEMENT — DAC888GBC
DAC888NAC	SIMILAR REPLACEMENT — DAC888NBC
DAC1408A—GAC	SIMILAR REPLACEMENT — DAC1408A—GBC
DMX88GBC	SIMILAR REPLACEMENT — MUX88GBC
DMX88NBC	SIMILAR REPLACEMENT — MUX88NBC
GAP01NAC	SIMILAR REPLACEMENT — PKD01NBC
GAP01NBC	SIMILAR REPLACEMENT — PKD01NBC
MAT01NAC	SIMILAR REPLACEMENT — MAT01NBC
MAT02NAC	SIMILAR REPLACEMENT — MAT02NBC
MUX08GAC	SIMILAR REPLACEMENT — MUX08GBC
MUX08NAC	SIMILAR REPLACEMENT — MUX08NBC
MUX08NTAC	SIMILAR REPLACEMENT — MUX08NTBC
MUX16GAC	SIMILAR REPLACEMENT — MUX16GBC
MUX16GTAC	SIMILAR REPLACEMENT — MUX16GTBC
MUX16NAC	SIMILAR REPLACEMENT — MUX16NBC
MUX16NTAC	SIMILAR REPLACEMENT — MUX16NTBC
MUX24GAC	SIMILAR REPLACEMENT — MUX24GBC
MUX24NAC	SIMILAR REPLACEMENT — MUX24NBC
MUX24NTAC	SIMILAR REPLACEMENT — MUX24NTBC
MUX28GAC	SIMILAR REPLACEMENT — MUX28GBC
MUX28GTAC	SIMILAR REPLACEMENT — MUX28GTBC
MUX28NAC	SIMILAR REPLACEMENT — MUX28NBC
MUX28NTAC	SIMILAR REPLACEMENT — MUX28NTBC
OP01GAC	SIMILAR REPLACEMENT — OP01GBC
OP01GRAC	SIMILAR REPLACEMENT — OP01GRBC
OP01GTAC	SIMILAR REPLACEMENT — OP01GTBC
OP01NAC	SIMILAR REPLACEMENT — OP01NBC
OP01NTAC	SIMILAR REPLACEMENT — OP01NTBC
OP02GAC	SIMILAR REPLACEMENT — OP02GBC
OP02GRAC	SIMILAR REPLACEMENT — OP02GRBC
OP02GTAC	SIMILAR REPLACEMENT — OP02GTBC
OP02NAC	SIMILAR REPLACEMENT — OP02NBC
OP02NTAC	SIMILAR REPLACEMENT — OP02NTBC
OP04GAC	SIMILAR REPLACEMENT — OP04GBC
OP04NAC	SIMILAR REPLACEMENT — OP04NBC
OP05GAC	SIMILAR REPLACEMENT — OP05GBC
OP05GRAC	SIMILAR REPLACEMENT — OP05GRBC
OP05GTAC	SIMILAR REPLACEMENT — OP05GTBC
OP05NAC	SIMILAR REPLACEMENT — OP05NBC
OP05NTAC	SIMILAR REPLACEMENT — OP05NTBC
OP06GAC	SIMILAR REPLACEMENT — OP06GBC
OP06GRAC	SIMILAR REPLACEMENT — OP06GRBC
OP06GTAC	SIMILAR REPLACEMENT — OP06GTBC
OP06NAC	SIMILAR REPLACEMENT — OP06NBC
OP06NTAC	SIMILAR REPLACEMENT — OP06NTBC

Dice Products

Part Number	Alternate Device Type
OP07GAC	SIMILAR REPLACEMENT — OP07GBC
OP07GRAC	SIMILAR REPLACEMENT — OP07GRBC
OP07GTAC	SIMILAR REPLACEMENT — OP07GTBC
OP07NAC	SIMILAR REPLACEMENT — OP07NBC
OP07NTAC	SIMILAR REPLACEMENT — OP07NTBC
OP08GAC	SIMILAR REPLACEMENT — OP08GBC
OP08GRAC	SIMILAR REPLACEMENT — OP08GRBC
OP08GTAC	SIMILAR REPLACEMENT — OP08GTBC
OP08NAC	SIMILAR REPLACEMENT — OP08NBC
OP08NTAC	SIMILAR REPLACEMENT — OP08NTBC
OP09GRAC	SIMILAR REPLACEMENT — OP09GRBC
OP09GTAC	SIMILAR REPLACEMENT — OP09GTBC
OP09NAC	SIMILAR REPLACEMENT — OP09NBC
OP09NTAC	SIMILAR REPLACEMENT — OP09NTBC
OP11GAC	SIMILAR REPLACEMENT — OP11GBC
OP11GRAC	SIMILAR REPLACEMENT — OP11GRBC
OP11GTAC	SIMILAR REPLACEMENT — OP11GTBC
OP11NAC	SIMILAR REPLACEMENT — OP11NBC
OP11NTAC	SIMILAR REPLACEMENT — OP11NTBC
OP12GAC	SIMILAR REPLACEMENT — OP12GBC
OP12GRAC	SIMILAR REPLACEMENT — OP12GRBC
OP12GTAC	SIMILAR REPLACEMENT — OP12GTBC
OP12NAC	SIMILAR REPLACEMENT — OP12NBC
OP12NTAC	SIMILAR REPLACEMENT — OP12NTBC
OP14GAC	SIMILAR REPLACEMENT — OP14GBC
OP14GRAC	SIMILAR REPLACEMENT — OP14GRBC
OP14NAC	SIMILAR REPLACEMENT — OP14NBC
OP15GAC	SIMILAR REPLACEMENT — OP15GBC
OP15GRAC	SIMILAR REPLACEMENT — OP15GRBC
OP15GTAC	SIMILAR REPLACEMENT — OP15GTBC
OP15NAC	SIMILAR REPLACEMENT — OP15NBC
OP15NTAC	SIMILAR REPLACEMENT — OP15NTBC
OP16GAC	SIMILAR REPLACEMENT — OP16GBC
OP16GRAC	SIMILAR REPLACEMENT — OP16GRBC
OP16GTAC	SIMILAR REPLACEMENT — OP16GTBC
OP16NAC	SIMILAR REPLACEMENT — OP16NBC
OP16NTAC	SIMILAR REPLACEMENT — OP16NTBC
OP17GAC	SIMILAR REPLACEMENT — OP17GBC
OP17GRAC	SIMILAR REPLACEMENT — OP17GRBC
OP17GTAC	SIMILAR REPLACEMENT — OP17GTBC
OP17NAC	SIMILAR REPLACEMENT — OP17NBC
OP17NTAC	SIMILAR REPLACEMENT — OP17NTBC
OP20GAC	SIMILAR REPLACEMENT — OP20GBC
OP20GRAC	SIMILAR REPLACEMENT — OP20GRBC
OP20NAC	SIMILAR REPLACEMENT — OP20NBC
OP21GAC	SIMILAR REPLACEMENT — OP21GBC
OP21GRAC	SIMILAR REPLACEMENT — OP21GRBC
OP21GTAC	SIMILAR REPLACEMENT — OP21GTBC
OP21NAC	SIMILAR REPLACEMENT — OP21NBC
OP21NTAC	SIMILAR REPLACEMENT — OP21NTBC
OP22GAC	SIMILAR REPLACEMENT — OP22GBC
OP22GRAC	SIMILAR REPLACEMENT — OP22GRBC
OP22NAC	SIMILAR REPLACEMENT — OP22NBC



Precision Monolithics Inc.

ORDERING INFORMATION

Dice Products

Part Number	Alternate Device Type
OP27GAC	SIMILAR REPLACEMENT — OP27GBC
OP27GRAC	SIMILAR REPLACEMENT — OP27GRBC
OP27GTAC	SIMILAR REPLACEMENT — OP27GTBC
OP27NAC	SIMILAR REPLACEMENT — OP27NBC
OP27NTAC	SIMILAR REPLACEMENT — OP27NTBC
OP32GAC	SIMILAR REPLACEMENT — OP32GBC
OP32GRAC	SIMILAR REPLACEMENT — OP32GRBC
OP32NAC	SIMILAR REPLACEMENT — OP32NBC
OP37GAC	SIMILAR REPLACEMENT — OP37GBC
OP37GRAC	SIMILAR REPLACEMENT — OP37GRBC
OP37NAC	SIMILAR REPLACEMENT — OP37NBC
OP50GAC	SIMILAR REPLACEMENT — OP50GBC
OP77GAC	SIMILAR REPLACEMENT — OP77GBC
OP77NAC	SIMILAR REPLACEMENT — OP77NBC
OP215GAC	SIMILAR REPLACEMENT — OP215GBC
OP215GRAC	SIMILAR REPLACEMENT — OP215GRBC
OP215GTAC	SIMILAR REPLACEMENT — OP215GTBC
OP215NAC	SIMILAR REPLACEMENT — OP215NBC
OP215NTAC	SIMILAR REPLACEMENT — OP215NTBC
OP220GAC	SIMILAR REPLACEMENT — OP220GBC
OP220GRAC	SIMILAR REPLACEMENT — OP220GRBC
OP220NAC	SIMILAR REPLACEMENT — OP220NBC
OP221GAC	SIMILAR REPLACEMENT — OP221GBC
OP221GRAC	SIMILAR REPLACEMENT — OP221GRBC
OP221NAC	SIMILAR REPLACEMENT — OP221NBC
OP420GAC	SIMILAR REPLACEMENT — OP420GBC
OP420GRAC	SIMILAR REPLACEMENT — OP420GRBC
OP420NAC	SIMILAR REPLACEMENT — OP420NBC
OP421GAC	SIMILAR REPLACEMENT — OP421GBC
OP421GRAC	SIMILAR REPLACEMENT — OP421GRBC
OP421NAC	SIMILAR REPLACEMENT — OP421NBC
PKD01NAC	SIMILAR REPLACEMENT — PKD01NBC

Dice Products

Part Number	Alternate Device Type
PM562GAC	SIMILAR REPLACEMENT — PM562GBC
REF01GAC	SIMILAR REPLACEMENT — REF01GBC
REF01GTAC	SIMILAR REPLACEMENT — REF01GTBC
REF01NAC	SIMILAR REPLACEMENT — REF01NBC
REF01NTAC	SIMILAR REPLACEMENT — REF01NTBC
REF02GAC	SIMILAR REPLACEMENT — REF02GBC
REF02GTAC	SIMILAR REPLACEMENT — REF02GTBC
REF02NAC	SIMILAR REPLACEMENT — REF02NBC
REF02NTAC	SIMILAR REPLACEMENT — REF02NTBC
SMP10GAC	SIMILAR REPLACEMENT — SMP10GBC
SMP10NAC	SIMILAR REPLACEMENT — SMP10NBC
SMP11GAC	SIMILAR REPLACEMENT — SMP11GBC
SMP11NAC	SIMILAR REPLACEMENT — SMP11NBC
SW01GAC	SIMILAR REPLACEMENT — SW01GBC
SW01NAC	SIMILAR REPLACEMENT — SW01NBC
SW02GAC	SIMILAR REPLACEMENT — SW02GBC
SW02NAC	SIMILAR REPLACEMENT — SW02NBC
SW05GAC	NOT RECOMMENDED FOR NEW DESIGNS
SW05GBC	NOT RECOMMENDED FOR NEW DESIGNS
SW05NBC	NOT RECOMMENDED FOR NEW DESIGNS
SW06GAC	SIMILAR REPLACEMENT — SW06GBC
SW06NAC	SIMILAR REPLACEMENT — SW06NBC
SW201GAC	SIMILAR REPLACEMENT — SW201GBC
SW201NAC	SIMILAR REPLACEMENT — SW201NBC
SW202GAC	SIMILAR REPLACEMENT — SW202GBC
SW202NAC	SIMILAR REPLACEMENT — SW202NBC
SW7510GAC	SIMILAR REPLACEMENT — SW7510GBC
SW7510NAC	SIMILAR REPLACEMENT — SW7510NBC
SW7511GAC	SIMILAR REPLACEMENT — SW7511GBC
SW7511NAC	SIMILAR REPLACEMENT — SW7511NBC

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PRODUCT ASSURANCE

Precision Monolithics Inc.

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Precision Monolithics Inc.

PRODUCT ASSURANCE

3

PRODUCT ASSURANCE PROGRAM

INTRODUCTION

PMI has long been recognized as a High Quality/Reliability supplier of Commercial, Industrial and Military/Aerospace Products. The PMI Product Assurance Department plays a vital role in controlling processes to ensure the manufacture of highly reliable, cost-effective product, and to make certain that all pertinent customer specifications and requirements are met.

ORGANIZATION

Product Assurance Department of PMI is composed of four functional departments: Process Quality Control, Quality Assurance, Reliability, and Program Management.

RESPONSIBILITIES

Process Control — The primary responsibility of the Process Control Department is to establish and maintain effective controls over process integrity by monitoring manufacturing processes and equipment operation; to provide real-time feedback of information concerning the status of these controls; and to initiate statistically valid techniques to further improve quality and reliability levels. These concepts are used extensively throughout all manufacturing processes.

Quality Assurance (Standard and Mil/Aero) — The primary responsibility of the Quality Assurance Department is to assure that the delivered product meets PMI or Customer Product Standards of reliability and quality. Process monitors and gate inspections are designed so that all devices are properly tested and required sample tests are performed prior to shipment. Inspection records and reports concerning monitor and inspection data keep all cognizant personnel fully informed about the status of the quality level of products going through final test operations.

Reliability — The Reliability Department assures a high and consistent reliability of PMI products. The Reliability Department establishes, defines, and maintains evaluation programs to determine process/product reliability. The Reliability Department will issue periodic reports on the results of all evaluation testing. Contact the nearest PMI Sales Office or the Literature

Department for the latest issue of the PMI Reliability Bulletin.

The Reliability Department also performs failure analyses as required.

Program Management — The primary responsibility of the Program Management Department is to ensure that the MIL-M-38510 JAN Program and other special customer program requirements are met. This is accomplished by monitoring the in-house procedures used to define each process step of a particular program. If necessary, baselining documentation is written detailing specific procedures and processing flows. A Configuration Control System consisting of maintenance of PMI standard baselining for each device type, as well as notification to customers of major process and product changes, are also responsibilities of this group.

Contact the nearest PMI Sales Office or the Literature Department for a copy of the comprehensive PMI Product Assurance Manual.

QUALITY LEVELS

PMI processes to stringent quality standards. Quality guarantees range from parts-per-million on Standard Product to imposed Quality Levels dictated by customer specification on custom orders.

Current information on Quality Levels is available upon request; contact the nearest PMI Sales Office or the Literature Department.

PROCESSING

The cornerstone of the manufacturing of PMI hermetic products is the strict adherence to all requirements of the latest revision of MIL-STD-883, Level B, for our "883" product line. PMI is also a leading producer of devices processed to Level S requirements — contact your PMI sales office to discuss your application.

The manufacture of plastic devices is inherently different from hermetic in the area of assembly. Automation of the assembly line has produced a tightly process-controlled product that requires few interim inspections from wafer fabrication to pre-mold visual. Plastic product may also be obtained with a burn-in (BI) option (see Section 2, Ordering Information for further details).



Precision Monolithics Inc.

PRODUCT ASSURANCE

DATA SHEET SPECIFICATIONS

PMI standard product is guaranteed to meet the published limits under the test conditions shown in the data sheet. Where practical, PMI performs 100% testing of the indicated parameters; however, following accepted industry practice, certain parameters may be guaranteed by sample testing or by using design and/or characterization data.

PMI provides separate data sheets for all "883" products in strict conformance with MIL-STD-883, Method 5005.8 and MIL-M-38510F, Appendix B. Interim Electrical Test Parameters (pre-burn-in), Final Electrical Test Parameters, Group A Test Parameters, and guidelines used for PDA calculations, are all detailed in tabular form on the "883" data sheets.

We recommend that the "883" data sheet be used as a baseline for new military or aerospace Source Control Drawings. Consult your sales representative to obtain these "883" data sheets.

TESTING

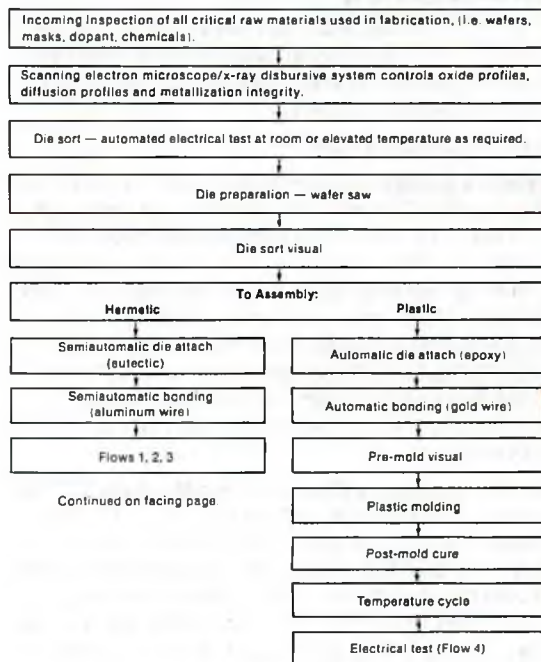
Testing of electrical parameters is generally performed using pulse testing techniques on automated test equipment. Unless otherwise specified, chip temperature remains close to the ambient temperature.

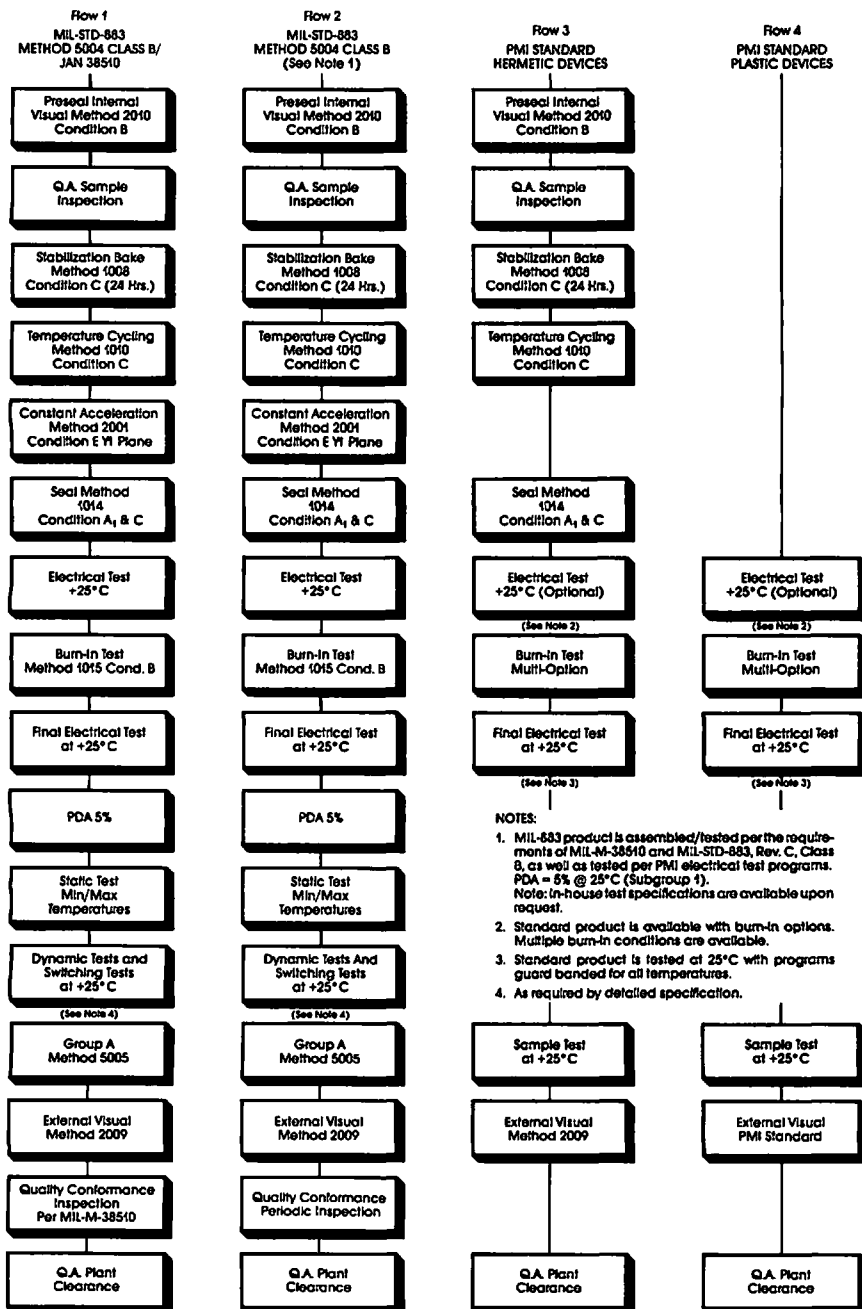
PROCESS CHANGE NOTIFICATION

PMI reviews all process, product, and package changes for possible impact on form, fit, or function. All major changes are submitted for a re-qualification, which may include electrical, mechanical, and/or thermal characterization. Where applicable, reliability re-qualification is performed.

Upon completion of this internal re-qualification, PMI informs all customers who have requested process change notification with a complete description of the change, along with applicable reliability or characterization data. Upon request, PMI will assist customers in their internal re-qualification effort.

STANDARD PROCESS FLOWS (JAN 38510, Class B, 883 Class B; PMI Industrial/Commercial) Die Fabrication





Country of Origin Assembly Codes: United States = S, Korea = K, Philippines = D, Puerto Rico = P

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DIRECT REPLACEMENT GUIDE

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AMD	PMI	ANALOG DEVICES	PMI	ANALOG DEVICES	PMI
Am1408L6	DAC1408A-6Q	AD542LH	OP41EJ	AD7524AD	PM7524FQ+
Am1408L7	DAC1408A-7Q	AD542SH	OP41BJ	AD7524AQ	PM7524FQ+
Am1408L8	DAC1408A-8Q	AD6012N	DAC312FR	AD7524BD	PM7524FQ
Am1408N6	DAC1408A-8P	AD611JH	OP15FJ	AD7524BQ	PM7524FQ
Am1408N7	DAC1408A-7P	AD611KH	OP15EJ	AD7524CD	PM7524EQ
Am1408N8	DAC1408A-8P	AD7224BQ	PM7224FX	AD7524CQ	PM7524EQ
Am1508L8	DAC1508A-8Q	AD7224CQ	PM7224EX	AD7524JN	PM7524HP+
Am6012ADC	DAC312ER	AD7224KN	PM7224HP	AD7524JP	PM7524HPC+
Am6012DC	DAC312FR	AD7224LN	PM7224GP	AD7524KN	PM7524HP
Am6012DM	DAC312BR	AD7224TD	PM7224BX	AD7524KP	PM7524HPC
Am6012PC	DAC312FR	AD7224UD	PM7224AX	AD7524LN	PM7524GP
		AD7226BCHIPS	PM7226GBC	AD7524SD	PM7524BQ+
		AD7226BQ	PM7226FR	AD7524SD/883	PM7524BQ/883+
		AD7226KN	PM7226HP	AD7524SQ/883	PM7524BQ/883+
		AD7226KP	PM7226HPC	AD7524TD	PM7524BQ
		AD7226TE/883	PM7226BRC/883	AD7524TD/883	PM7524BQ/883
		AD7226TQ	PM7226BR	AD7524TQ	PM7524BQ
		AD7226TQ/883	PM7226BR/883	AD7524TQ/883	PM7524BQ/883
		AD741CH	OP02DJ+	AD7524UD	PM7524AQ
		AD741CH	PM741CJ	AD7524UD/883	PM7524AQ/883
		AD741CN	OP02DP+	AD7524UQ	PM7524AQ
		AD741H	PM741J	AD7524UQ/883	PM7524AQ/883+
		AD741H	OP02BJ+	AD7528ACHIPS	PM7528GBC
		AD741JH	OP02J+	AD7528AQ	PM7528FR+
		AD741JN	OP02CP+	AD7528BQ	PM7528FR+
		AD741KH	OP02CJ+	AD7528CQ	PM7528ER
		AD741KN	OP02CP+	AD7528JN	PM7528HP+
		AD741LH	OP02EJ+	AD7528JP	PM7528HPC+
		AD741LN	OP02EP+	AD7528KN	PM7528HP
		AD741SH	OP02J+	AD7528KP	PM7528HPC
		AD7510DIJQ	SW7510EQ	AD7528LN	PM7528GP
		AD7510DIKQ	SW7510FQ	AD7528SD	PM7528BR+
		AD7510DISQ	SW7510AQ	AD7528SD/883	PM7528BR/883+
		AD7511DIJQ	SW7511EQ	AD7528SE/883	PM7528BRC/883+
		AD7511DIKQ	SW7511FQ	AD7528SQ	PM7528BR+
		AD7511DISQ	SW7511AQ	AD7528SQ/883	PM7528BR/883+
		AD7511DITQ	SW7511BQ	AD7528TD	PM7528BR
		AD7520JD	PM7533FQ+	AD7528TD/883	PM7528BR/883
		AD7520JN	PM7533HP+	AD7528TE/883	PM7528BRC/883
		AD7520KD	PM7533FQ	AD7528TQ	PM7528BR
		AD7520KN	PM7533HP	AD7528TQ/883	PM7528BR/883
		AD7520LD	PM7533EQ	AD7528UD	PM7528AR
		AD7520LN	PM7533GP	AD7528UD/883	PM7528AR/883
		AD7520SD	PM7533BQ+	AD7530JD	PM7533FQ+
		AD7520SD/883	PM7533BQ/883+	AD7530JN	PM7533HP+
		AD7520TD	PM7533BQ	AD7530KD	PM7533FQ
		AD7520TD/883	PM7533BQ/883	AD7530KN	PM7533HP
		AD7520UD	PM7533AQ	AD7530LD	PM7533EQ
		AD7520UD/883	PM7533AQ/883	AD7530LN	PM7533GP
		AD7521JD	PM7541FX+	AD7531JD	PM7541FX+

INDUSTRY CROSS REFERENCE

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

ANALOG DEVICES

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AD7521JN	PM7541HP+
AD7521KD	PM7541FX+
AD7521KN	PM7541HP+
AD7521LD	PM7541FX+
AD7521LN	PM7541HP+
AD7521SD	PM7541BX+
AD7521SD/883	PM7541BX/883+
AD7521TD	PM7541BX+
AD7521TD/883	PM7541BX/883+
AD7521UD	PM7541BX+
AD7521UD/883	PM7541BX/883+
AD7523JN	PM7524HP+
AD7523KN	PM7524HP+
AD7523LN	PM7524GP+
AD7524ACHIPS	PM7524GBC
AD7531JN	PM7541HP+
AD7531KD	PM7541FX+
AD7531KN	PM7541HP+
AD7531LD	PM7541FX+
AD7531LN	PM7541HP+
AD7533AD	PM7533FQ+
AD7533AQ	PM7533FQ+
AD7533BD	PM7533FQ
AD7533BQ	PM7533FQ
AD7533CD	PM7533EQ
AD7533CQ	PM7533EQ
AD7533JN	PM7533HP+
AD7533KN	PM7533HP
AD7533LN	PM7533GP
AD7533SD	PM7533BQ+
AD7533SD/883	PM7533BQ/883+
AD7533SQ	PM7533BQ+
AD7533SQ/883	PM7533BQ/883+
AD7533TD	PM7533BQ
AD7533TD/883	PM7533BQ/883
AD7533TQ	PM7533BQ
AD7533TQ/883	PM7533BQ/883
AD7533UD	PM7533AQ
AD7533UD/883	PM7533AQ/883
AD7533UQ	PM7533AQ
AD7533UQ/883	PM7533AQ/883
AD7541ACHIPS	PM7541AGBC+
AD7541AAQ	PM7541AFX+
AD7541ABQ	PM7541AEX+
AD7541AD	PM7541FX
AD7541AJN	PM7541AHP+
AD7541AKN	PM7541AGP+
AD7541ASD	PM7541ABX+
AD7541ASD/883	PM7541ABX/883+
AD7541ATD	PM7541AAX+

ANALOG DEVICES

ANALOG DEVICES	PMI
AD7541ATD/883	PM7541AAX/883+
AD7541BD	PM7541EX
AD7541JN	PM7541HP
AD7541KN	PM7541GP
AD7541SD	PM7541BX
AD7541SD/883	PM7541BX/883
AD7541TD	PM7541AX
AD7541TD/883	PM7541AX/883
AD7542AD	PM7542FQ+
AD7542BD	PM7542FQ+
AD7542GBD	PM7542EQ
AD7542GKN	PM7542GP
AD7542GTD	PM7542AQ
AD7542JN	PM7542HP+
AD7542KN	PM7542HP+
AD7542SD	PM7542BQ+
AD7542TD	PM7542BQ+
AD7543AD	PM7543FQ+
AD7543BD	PM7543FQ+
AD7543GBD	PM7543EQ
AD7543GKN	PM7543GP
AD7543GTD	PM7543AQ
AD7543JN	PM7543HP+
AD7543KN	PM7543HP+
AD7543SD	PM7543BQ+
AD7543TD	PM7543BQ+
AD7545ACHIPS	PM7545GBC
AD7545AQ	PM7545FR+
AD7545BQ	PM7545FR+
AD7545CQ	PM7545FR+
AD7545GCQ	PM7545ER
AD7545GLN	PM7545GP
AD7545GUD	PM7545AR
AD7545GUD/883	PM7545AR/883
AD7545GUQ	PM7545AR
AD7545GUQ/883	PM7545AR/883
AD7545JN	PM7545HP+
AD7545JP	PM7545HPC+
AD7545KN	PM7545HP+
AD7545KP	PM7545HPC+
AD7545LN	PM7545HP+
AD7545LP	PM7545HPC+
AD7545SD	PM7545BR+
AD7545SD/883	PM7545BR/883+
AD7545SE/883	PM7545BRC/883+
AD7545SQ	PM7545BR
AD7545SQ/883	PM7545BR/883
AD7545TD	PM7545BR+
AD7545TD/883	PM7545BR/883+
AD7545TE/883	PM7545BRC/883+

ANALOG DEVICES

ANALOG DEVICES	PMI
AD7545TQ	PM7545BR
AD7545TQ/883	PM7545BR/883
AD7545UD	PM7545BR+
AD7545UD/883	PM7545BR/883+
AD7545UE/883	PM7545BRC/883+
AD7545UQ	PM7545BR
AD7545UQ/883	PM7545BRC/883
AD7548AQ	PM7548FR+
AD7548BQ	PM7548ER+
AD7548JN	PM7548HP+
AD7548KN	PM7548GP+
AD7548SD	PM7548BR+
AD7548SD/883	PM7548BR/883+
AD7548TD	PM7548AR+
AD7548TD/883	PM7548AR/883+
AD7574AD	PM7574FX
AD7574AD	ADC908FX+
AD7574BD	PM7574EX
AD7574BD	ADC908EX+
AD7574JN	PM7574HP
AD7574JN	ADC908HP+
AD7574KN	PM7574GP
AD7574KN	ADC908GP+
AD7574SD	PM7574BX
AD7574SD	ADC908BX+
AD7574TD	PM7574AX
AD7574TD	ADC908AX+
AD7820BQ	PM0820FR
AD7820CQ	PM0820ER
AD7820KN	PM0820GP
AD7820LN	PM0820HP
AD7820TQ	PM0820BR
AD7820UQ	PM0820AR
ADDAC100JD	DAC100BCQ7
ADDAC100KD	DAC100ABQ7
ADDAC100LD	DAC100AAQ7
ADOP07AH	OP07AJ
ADOP07AH	OP77AJ+
ADOP07CH	OP07CJ
ADOP07CH	OP77FJ+
ADOP07CN	OP07CP
ADOP07CN	OP77GP+
ADOP07DH	OP07DJ
ADOP07DH	OP77FJ+
ADOP07DN	OP07DP
ADOP07DN	OP77GP+
ADOP07EH	OP07EJ
ADOP07EH	OP77FJ+
ADOP07EN	OP07EP
ADOP07EN	OP77FP+

+Direct pin-for-pin replacement with improved specifications.



Precision Monolithics Inc.

DIRECT REPLACEMENT GUIDE

ANALOG DEVICES		BURR-BROWN		FAIRCHILD		PMI	
ADOP07H	OP07J	OPA37FJ	OP37FJ	μA101HC	OP77FJ+		
ADOP07H	OP77BJ+	OPA37FZ	OP37FZ	μA101HM	OP77BJ+		
ADOP27AH	OP27AJ	OPA37GJ	OP37GJ	μA107HM	OP77BJ+		
ADOP27BH	OP27BJ	OPA37GP	OP37GP	μA107HM	OP07J+		
ADOP27CH	OP27CJ	OPA37GZ	OP37GZ	μA108AHM	PM108AJ/883C		
ADOP27EH	OP27EJ	OPA606KM	OP42FJ	μA108AHM	PM1008AJ+		
ADOP27FN	OP27EP	OPA608KP	OP42FZ	μA108HM	PM108J/883C		
ADOP27FH	OP27FJ	OPA606LM	OP42EJ	μA108HM	PM1008AJ+		
ADOP27FN	OP27FP	OPA806SM	OP42AJ	μA111HM	PM111J		
ADOP27GH	OP27GJ			μA111RM	PM111Z		
ADOP27GN	OP27GP			μA124	OP400+		
ADOP37AH	OP37AJ			μA124DM	OP421BY+		
ADOP37BH	OP37BJ	XR1458CN	OP14DZ+	μA139ADM	PM139AY		
ADOP37CH	OP37CJ	XR1458CP	OP14DP+	μA139DM	PM139Y		
ADOP37EH	OP37EJ	XR3403CN	OP421HY+	μA1458CHC	OP14CJ+		
ADOP37EN	OP37EP	XR3503M	OP421HY+	μA1458CRC	OP14CZ+		
ADOP37FJ	OP37FJ	XR4136CN	OP421CY+	μA1458CTC	OP14CP+		
ADOP37FN	OP37FP	XR4136CP	OP09FY+	μA1458HC	OP14EJ+		
ADOP37GH	OP37GJ	XR4136M	OP09FY	μA1458TC	OP14DP+		
ADOP37GN	OP37GP	XR4558CN	OP09AY+	μA148DM	PM148Y		
		XR4558CP	OP14DZ+	μA148DM	OP11AY+		
		XR4741CN	OP14DP+	μA201AHM	OP77FJ+		
		XR4741CP	OP11FY	μA207HM	OP77FJ+		
		XR4741CP	OP11GP	μA207HM	OP07J+		
		XR4741M	OP400GP+	μA208AHM	PM208AJ		
		XR4741M	OP11BY	μA208AHM	PM1008AJ+		
		XR-C277	OP400AY+	μA208HM	PM1008AJ+		
			RPT82FQ	μA224DC	OP400+		
				μA248DC	OP421FY+		
				μA248DC	PM248Y		
				μA248DC	OP11BY+		
				μA301ATO	OP77GP+		
				μA301HC	OP77FJ+		
				μA307HC	OP77FJ+		
				μA307HC	OP07DJ+		
				μA307TG	OP77GP+		
				μA307TG	OP07DP+		
				μA308AHM	PM308AJ		
				μA308AHM	PM1008GJ+		
				μA308ATC	PM308AP		
				μA308ATC	PM1008GP+		
				μA308HM	PM1008GJ+		
				μA308TC	PM1008GP+		
				μA311HC	PM211J+		
				μA311RC	PM211Z+		
				μA311TC	PM211Z+		
				μA324	OP400+		
				μA324DC	OP421HY+		
				μA3303PC	OP421GY+		
				μA3403DC	OP421OY+		
				μA3403PC	OP421HY+		
				μA348DC	OP11FY+		
				μA348PC	OP11FP+		
				μA4136DC	OP09FY		
				μA4136DM	OP09AY+		

BURR-BROWN		FAIRCHILD		PMI	
OPA11HT	OP02AJ	μA0801CDC	DAC08CQ	μA0801CDC	DAC08CQ
OPA121KM	OP41FJ+	μA0801CPC	DAC08CP	μA0801CPC	DAC08CP
OPA121KP	OP41GP+	μA0801DM	DAC08Q	μA0801DM	DAC08Q
OPA156AM	PM156AJ	μA0801EDC	DAC08EQ	μA0801EDC	DAC08EQ
OPA156AM	OP16BJ+	μA0801EPC	DAC08EP	μA0801EPC	DAC08EP
OPA21EZ	OP21EZ	μA0802ADC	DAC1408A-80	μA0802ADC	DAC1408A-80
OPA21GZ	OP21GZ	μA0802ADC	DAC08EQ+	μA0802ADC	DAC08EQ+
OPA27AJ	OP27AJ	μA0802APC	DAC1408A-8P	μA0802APC	DAC1408A-8P
OPA27AZ	OP27AZ	μA0802APC	DAC08EP+	μA0802APC	DAC08EP+
OPA27BJ	OP27BJ	μA0802BDC	DAC1408A-7O	μA0802BDC	DAC1408A-7O
OPA27BZ	OP27BZ	μA0802BDC	DAC08CQ+	μA0802BDC	DAC08CQ+
OPA27CJ	OP27CJ	μA0802BPC	DAC1408A-7P	μA0802BPC	DAC1408A-7P
OPA27CZ	OP27CZ	μA0802BPC	DAC08CP+	μA0802BPC	DAC08CP+
OPA27EJ	OP27EJ	μA0802CDC	DAC1408A-6Q	μA0802CDC	DAC1408A-6Q
OPA27EZ	OP27EZ	μA0802CDC	DAC08CQ+	μA0802CDC	DAC08CQ+
OPA27FJ	OP27FJ	μA0802ADC	DAC1408A-8P	μA0802ADC	DAC1408A-8P
OPA27FZ	OP27FZ	μA0802APC	DAC08CP+	μA0802APC	DAC08CP+
OPA27GJ	OP27GJ	μA0802APC	DAC1408A-8Q	μA0802APC	DAC1408A-8Q
OPA27GP	OP27GP	μA0802BDC	DAC08EQ+	μA0802BDC	DAC08EQ+
OPA27GZ	OP27GZ	μA0802BDC	OP77BJ+	μA0802BDC	OP77BJ+
OPA356AM	PM356AJ	μA0802CPC		μA0802CPC	
OPA356AM	OP18FJ+	μA0802CPC		μA0802CPC	
OPA37AJ	OP37AJ	μA0802DM		μA0802DM	
OPA37AZ	OP37AZ	μA101AHM		μA101AHM	
OPA37BJ	OP37BJ				
OPA37BZ	OP37BZ				
OPA37CJ	OP37CJ				
OPA37CZ	OP37CZ				
OPA37EJ	OP37EJ				
OPA37EZ	OP37EZ				

Direct pin for pin replacement with improved specifications.

INDUSTRY CROSS REFERENCE

4

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

FAIRCHILD

μ A4136PC
 μ A714EHC
 μ A714EHC
 μ A714HC
 μ A714HC
 μ A714HM
 μ A714HM
 μ A714LHC
 μ A714LHC
 μ A715
 μ A725AHM
 μ A725AHM
 μ A725HC
 μ A725HC
 μ A725HM
 μ A725HM
 μ A725TC
 μ A725TC
 μ A741AHM
 μ A741EHC
 μ A741HC
 μ A741HC
 μ A741HM
 μ A741HM
 μ A741RC
 μ A741TC
 μ A747ADM
 μ A747AHM
 μ A747CM
 μ A747DC
 μ A747DC
 μ A747DM
 μ A747DM
 μ A747EDC
 μ A747EHC
 μ A747HC
 μ A747HM
 μ A747IDC
 μ A747IDM
 μ A747IHC
 μ A747IHM
 μ A747PC
 μ A771ARC
 μ A771ARM
 μ A771ATC
 μ A771BRC
 μ A771BRM
 μ A771BTC
 μ A771LRC
 μ A771LTC

PMI

OP09FP
OP07EJ
OP77FJ+
OP07CJ
OP77FJ+
OP07J
OP77BJ+
OP07DJ+
OP77FJ+
OP44+
OP06AJ+
OP77BJ+
OP06GJ+
OP77FJ+
OP06BJ+
OP77BJ+
OP77GP+
OP06GZ+
OP02AJ+
OP02EJ+
PM741CJ
OP02CJ+
PM741J
OP02BJ+
OP02CZ+
OP02DP+
OP04Y+
OP04K/883C+
OP04BK/883C+
PM747CY
OP04DY+
PM747Y
OP04CY+
OP04CY+
OP04K/883C+
OP04BK/883C+
OP04BK/883C+
OP04CY
OP04AY
OP04K
OP04K
OP04DY
OP15FZ+
OP15BZ+
OP15FZ+
OP15GZ+
OP15BZ+
OP15GZ+
OP15GZ+

FAIRCHILD

μ A771RC
 μ A771TC
 μ A772ARC
 μ A772ARM
 μ A772ATC
 μ A772BRC
 μ A772BRM
 μ A772BTC
 μ A772RC
 μ A772TC
 μ A776HC
 μ A776HM
 μ A776TC
 μ A798

PMI

OP15GZ+
OP15GZ+
OP215FZ+
OP215BZ+
OP215FZ+
OP215FZ+
OP215BZ+
OP215FZ+
OP215GZ+
OP215GZ+
OP22EJ+
OP22AJ+
OP22HZ+
OP200FZ+

HARRIS

HA2-OP07AJ-2
HA2-OP07AJ-8
HA7-OP07AZ-2
HA7-OP07AZ-8
HA2-OP07CJ-5
HA3-OP07CP-5
HA7-OP07CZ-5
HA2-OP07EJ-5
HA3-OP07EP-5
HA7-OP07EZ-5
HA2-OP07J-2
HA2-OP07J-8
HA7-OP07Z-2
HA7-OP07Z-8
HA2-2600-2
HA7-2600-2
HA2-2600-8
HA7-2600-8
HA2-2602-2
HA7-2602-2
HA2-2602-8
HA7-2602-8
HA2-2605-5
HA3-2605-5
HA7-2605-5
HA2-2620-2
HA7-2620-2
HA2-2620-8
HA4-2620-8
HA7-2620-8
HA2-2622-2
HA7-2622-2
HA2-2622-8
HA7-2622-8
HA2-2625-5

PMI

OP07AJ
OP07AJ/883C
OP07AZ
OP07AZ/883C
OP07CJ
OP07CP
OP07CZ
OP07EJ
OP07EZ
OP07EZ
OP07J
OP07J/883C
OP07Z
OP07Z/883C
OP62AJ+
OP62AJ/883C+
OP62AZ/883C+
OP62AJ+
OP62AZ+
OP62AJ/883C+
OP62AZ/883C+
OP62FJ+
OP62GP+
OP62FZ+
OP64AJ+
OP64AZ+
OP64AJ/883C+
OP64ARC/883C+
OP64AZ/883C+
OP64AJ+
OP64AZ+
OP64AJ/883C+
OP64AZ/883C+
OP64FJ+

HARRIS

HA3-2625-5
HA7-2625-5
HA2-2650-2
HA7-2650-2
HA2-2650-8
HA7-2650-8
HA2-2650-8
HA2-2655-5
HA2-2655-5
HA7-2655-5
HA2-2720-2
HA7-2720-2
HA2-2720-8
HA7-2720-8
HA2-2725-5
HA7-2725-5
HA1-4600-2
HA1-4600-5
HA1-4600-8
HA1-4602-2
HA1-4602-8
HA1-4605-5
HA1-4741-2
HA1-4741-5
HA3-4741-5
HA1-4741-7
HA1-4741-8
HA7-5102-2
HA3-5102-5
HA7-5102-5
HA7-5102-8
HA1-5104-2
HA1-5104-5
HA3-5104-5
HA1-5104-8
HA2-5130-2
HA7-5130-2
HA2-5130-5
HA3-5130-5
HA7-5130-5
HA2-5130-8
HA7-5130-8
HA2-5135-2
HA7-5135-2
HA2-5135-5
HA3-5135-5
HA7-5135-5
HA2-5135-8
HA4-5135-8
HA7-5135-8
HA1-5190-2
HA1-5190-2
HA4-5190-8

PMI

OP64GP+
OP64FZ+
OP271AJ+
OP271AZ+
OP271AJ/883C+
OP271AZ/883C+
OP271FJ+
OP271FZ+
OP22BJ+
OP22BZ+
OP22BJ/883C+
OP22BZ/883C+
OP22HJ+
OP22HZ+
OP470AY
OP470FY
OP470AY/883C
OP470AY
OP470AY/883C
OP470FY
OP400AY+
OP400FY+
OP400GP+
OP400BIFY+
OP400AY/883C+
OP270AZ+
OP270GP+
OP270FZ+
OP270AZ/883C+
OP470AY+
OP470FY+
OP470GP+
OP470AY/883C+
OP77AJ+
OP77AZ+
OP77EJ+
OP77EP+
OP77EZ+
OP77AJ/883C+
OP77AZ/883C+
OP77BJ+
OP77BZ+
OP77FJ+
OP77FP+
OP77FZ+
OP77BJ/883C+
OP77BRC/883C+
OP77BRC/883C+
OP64AJ
OP64AJ/883C
OP64ARC/883C

+Direct pin-for-pin replacement with improved specifications.



Precision Monolithics Inc.

DIRECT REPLACEMENT GUIDE

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INDUSTRY CROSS REFERENCE

INTERSIL	PMI	INTERSIL	PMI	INTERSIL	PMI
AD7520JD	PM7533FQ+	AD7541JN	PM7541HP	OP07DJ	OP07DJ
AD7520JN	PM7533HP+	AD7541KN	PM7541GP	OP07DJ	OP77FJ+
AD7520KD	PM7533FQ	AD7541LN	PM7541GP	OP07DP	OP07DP
AD7520KN	PM7533HP	AD7541SD	PM7541BX	OP07DP	OP77GP+
AD7520LD	PM7533EQ	AD7541TD	PM7541AX	OP07EJ	OP07EJ
AD7520LN	PM7533GP	ICL8007ACTV	OP41EJ	OP07EJ	OP77FJ+
AD7520SD	PM7533BQ+	ICL8007AMTV	OP41AJ	OP07EP	OP07EP
AD7520TD	PM7533BQ	ICL8007CTY	OP41FJ	OP07EP	OP77FP+
AD7520UD	PM7533AQ	ICL8007MTY	OP41BJ	OP07EZ	OP07EZ
AD7521JD	PM7541FX+	ICL8008CPA	OP77GP+	OP07EZ	OP77FZ+
AD7521JN	PM7541HP+	ICL8008CTY	OP77FJ+	OP07J	OP07J
AD7521KD	PM7541FX+	ICL8008MTY	OP77BJ+	OP07J	OP77BJ+
AD7521KN	PM7541HP+	IH5108CPE	MUX08FP+	OP07Z	OP07Z
AD7521LD	PM7541FX+	IH5108IJE	MUX08FQ+	OP07Z	OP77BZ+
AD7521LN	PM7541HP+	IH5108MJE	MUX08BQ+		
AD7521SD	PM7541BX+	IH5208CPE	MUX24FP+		
AD7521TD	PM7541BX+	IH5208IJE	MUX24FQ+		
AD7521UD	PM7541BX+	IH6108CJE	MUX08EQ+		
AD7523AD	PM7524FQ+	IH6108CPE	MUX08EP+		
AD7523BD	PM7524FQ	IH6108MJE	MUX08AQ+		
AD7523CD	PM7524EQ	IH6116CJI	MUX16FT+		
AD7523JN	PM7524HP+	IH6116CPI	MUX16FT+		
AD7523KN	PM7524HP	IH6116MJI	MUX16BT+		
AD7523LN	PM7524GP	IH6208CJE	MUX24FQ+		
AD7523SD	PM7524BQ+	IH6208CPE	MUX24FP+		
AD7523TD	PM7524BQ	IH6216CJI	MUX28FT+		
AD7523UD	PM7524AQ	IH6216CPI	MUX28FT+		
AD7530JD	PM7533FQ+	LM108AH	OP97AJ+		
AD7530JN	PM7533HP+	LM108H	OP97AJ+		
AD7530KD	PM7533FQ	LM308AH	PM308AJ		
AD7530KN	PM7533HP	LM308AN	PM308AP		
AD7530LD	PM7533EQ	LM308H	OP97FJ+		
AD7530LN	PM7533GP	LM308N	OP97FP+		
AD7531JD	PM7541FX+	OP05AJ	OP05AJ		
AD7531JN	PM7541HP+	OP05CJ	OP05CJ		
AD7531KD	PM7541FX+	OP05CP	OP05CP		
AD7531KN	PM7541HP+	OP05EJ	OP05EJ		
AD7531LD	PM7541FX+	OP05EP	OP05EP		
AD7531LN	PM7541HP+	OP05J	OP05J		
AD7533AD	PM7533FQ+	OP05/D	OP05GBC		
AD7533BD	PM7533FQ	OP07AJ	OP07AJ		
AD7533CD	PM7533EQ	OP07AJ	OP77AJ+		
AD7533JN	PM7533HP+	OP07AZ	OP07AZ		
AD7533KN	PM7533HP	OP07AZ	OP77AZ+		
AD7533LN	PM7533GP	OP07CJ	OP07CJ		
AD7533SD	PM7533BQ+	OP07CJ	OP77FJ+		
AD7533TD	PM7533BQ	OP07CP	OP07CP		
AD7533UD	PM7533AQ	OP07CP	OP77GP+		
AD7541AD	PM7541FX	OP07CZ	OP07CZ		
AD7541BD	PM7541EX	OP07CZ	OP77FZ+		
				LINEAR TECHNOLOGY	PMI
				LT1001ACH	OP77EJ+
				LT1001ACJ8	OP77EZ+
				LT1001ACN8	OP77EP+
				LT1001AMH/883B	OP77AJ/883C+
				LT1001AMH	OP77AJ+
				LT1001AMJ8/883B	OP77AZ/883C+
				LT1001AMJ8	OP77AZ+
				LT1001CH	OP77FJ+
				LT1001CJ8	OP77GZ+
				LT1001CN8	OP77GP+
				LT1001MH/883B	OP77BJ/883C+
				LT1001MH	OP77BJ+
				LT1001MJ8/883B	OP77BZ/883C+
				LT1001MJ8	OP77BZ+
				LT1007ACH	OP27EJ
				LT1007ACJ8	OP27EZ
				LT1007ACN8	OP27EP
				LT1007AMH/883B	OP27AJ/883C
				LT1007AMH	OP27AJ
				LT1007AMJ8/883B	OP27AZ/883C
				LT1007AMJ8	OP27AZ
				LT1007CH	OP27FJ
				LT1007CJ8	OP27FZ
				LT1007CN8	OP27FP
				LT1007MH/883	OP27BJ/883C
				LT1007MH	OP27BJ
				LT1007MJ8/883	OP27BZ/883C
				LT1007MJ8	OP27BZ
				LT1008CH	PM1008GJ
				LT1008CN8	PM1008GP
				LT1008MH/883	PM1008AJ/883C
				LT1008MH	PM1008AJ
				LT1012CH	PM1012GJ
				LT1012CN8	PM1012GP
				LT1012MD/883B	PM1012AZ/883C

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

LINEAR TECHNOLOGY	PMI
LT1012MD	PM1012AZ
LT1012MH/883B	PM1012AJ/883C
LT1012MH	PM1012AJ
LT1013ACJ8	OP200EY+
LT1013AMJ8/883B	OP200AY/883C+
LT1013AMJ8	OP200AY+
LT1013CJ8	OP200FY+
LT1013CN8	OP200GP+
LT1013DN8	OP200GP+
LT1013MJ8/883B	OP200AY/883C+
LT1013MJ8	OP200AY+
LT1014ACJ	OP400EY+
LT1014AMJ/883B	OP400AY/883C+
LT1014AMJ	OP400AY+
LT1014CJ	OP400FY+
LT1014CN	OP400GP+
LT1014MJ/883B	OP400AY/883C+
LT1014MJ	OP400AY+
LT1023CH	OP42FJ+
LT1023CJ8	OP42FZ+
LT1023CN8	OP42FZ+
LT1023MH/883B	OP42AJ/883C+
LT1023MH	OP42AJ+
LT1023MJ8/883B	OP42AZ/883C+
LT1023MJ8	OP42AJ+
LT1037ACH	OP37EJ
LT1037ACJ8	OP37EZ
LT1037ACN8	OP37EP
LT1037AMH/883B	OP37AJ/883B
LT1037AMH	OP37AJ
LT1037AMJ8/883B	OP37AZ/883B
LT1037AMJ8	OP37AZ
LT1037CJ8	OP37FZ
LT1037CN8	OP37FP
LT1037MH/883B	OP37BJ/883B
LT1037MH	OP37BJ
LT1037MJ8/883B	OP37BZ/883C
LT1037MJ8	OP37BZ
OP05AH/883B	OP05AJ/883C
OP05AH	OP05AJ
OP05AJ8/883B	OP05AZ/883C
OP05AJ8	OP05AZ
OP05CH	OP05CJ
OP05CJ8	OP05CZ
OP05CN8	OP05CP
OP05EH	OP05EJ
OP05EJ8	OP05EZ
OP05EN8	OP05EP
OP05H/883B	OP05J/883C
OP05H	OP05J

LINEAR TECHNOLOGY	PMI
OP05J8/883B	OP05Z/883C
OP05J8	OP05Z
OP07AH/883B	OP07AJ/883C
OP07AH	OP07AJ
OP07AJ8/883B	OP07AZ/883C
OP07AJ8	OP07AZ
OP07CH	OP07CJ
OP07CJ8	OP07CZ
OP07CN8	OP07CP
OP07CH	OP07DJ
OP07DJ8	OP07CZ
OP07DN8	OP07DP
OP07EH	OP07EJ
OP07EJ8	OP07EZ
OP07EN8	OP07EP
OP07H/883B	OP07J/883C
OP07H	OP07J
OP07J8/883B	OP07Z/883C
OP07J8	OP07Z
OP15AH/883B	OP15AJ/883B
OP15AH	OP15AJ
OP15BH/883B	OP15BJ/883B
OP15BH	OP15BJ
OP15CH/883B	OP15BJ/883B
OP15CH	OP15BJ
OP15EH	OP15EJ
OP15FH	OP15FJ
OP15FN8	OP15FP
OP15GH	OP15GJ
OP15GN8	OP15GP
OP16AH/883B	OP16AJ/883B
OP16AH	OP16AJ
OP16BH/883B	OP16BJ/883B
OP16BH	OP16BJ
OP16CH/883B	OP16BJ/883B
OP16CH	OP16BJ
OP16EH	OP16EJ
OP16FH	OP16FJ
OP16FN8	OP16FP
OP16GH	OP16GJ
OP16GN8	OP16GP
OP27AH/883B	OP27AJ/883C
OP27AH	OP27AJ
OP27AJ8/883B	OP27AZ/883C
OP27AJ8	OP27AZ
OP27CH/883B	OP27CJ/883C
OP27CH	OP27CJ
OP27CJ8/883B	OP27CZ/883C
OP27CJ8	OP27CZ
OP27EH	OP27EJ

LINEAR TECHNOLOGY	PMI
OP27EJ8	OP27EZ
OP27EN8	OP27EP
OP27GH	OP27GJ
OP27GJ8	OP27GZ
OP27GN8	OP27GP
OP37AH/883B	OP37AJ/883C
OP37AH	OP37AJ
OP37AJ8/883B	OP37AZ/883C
OP37AJ8	OP37AZ
OP37CH/883B	OP37CJ/883C
OP37CH	OP37CJ
OP37CJ8/883B	OP37CZ/883C
OP37CJ8	OP37CZ
OP37EH	OP37EJ
OP37EJ8	OP37EZ
OP37EN8	OP37EP
OP37GH	OP37GJ
OP37GJ8	OP37GZ
OP37GN8	OP37GP
OP215AH/883B	OP215AJ/883C
OP215AH	OP215AJ
OP215AJ8/883B	OP215AZ/883C
OP215AJ8	OP215AZ
OP215CH/883B	OP215CJ/883C
OP215CH	OP215BJ
OP215CJ8/883B	OP215CZ/883C
OP215CJ8	OP215BZ
OP215EH	OP215EJ
OP215EJ8	OP215EZ
OP215EN8	OP215EZ
OP215GH	OP215GJ
OP215GJ8	OP215GZ
OP215GN8	OP215GZ
OP227AJ/883B	OP227AY/883C
OP227AJ	OP227AY
OP227CJ/883B	OP227CY/883C
OP227CJ	OP227AY
OP227EJ	OP227EY
OP227EN	OP227EY
OP227GJ	OP227GY
OP227GN	OP227GY
REF01AH/883B	REF01AJ/883C
REF01AH	REF01AJ
REF01AJ8/883B	REF01AZ/883C
REF01AJ8	REF01AZ
REF01CH	REF01CJ
REF01CJ8	REF01CZ
REF01CN8	REF01CP
REF01EH	REF01EJ
REF01EJ8	REF01EZ

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

LINEAR TECHNOLOGY

PMI	MAXIM
REF01EN8	AD7521UD
REF01H/883B	AD7523JN
REF01H	AD7523KN
REF01HH	AD7523LN
REF01HJ8	AD7524AC/D
REF01HN8	AD7524AD
REF01J8/883B	AD7524AQ
REF01J8	AD7524BD
REF02AH/883B	AD7524BQ
REF02AH	AD7524CD
REF02AJ8/883B	AD7524CQ
REF02AJ8	AD7524JN
REF02CH	AD7524KN
REF02CJ8	AD7524LN
REF02CN8	AD7528AQ
REF02DH	AD7528BQ
REF02DJ8	AD7528CQ
REF02DN8	AD7528JC/D
REF02EH	AD7528JN
REF02EJ8	AD7528KN
REF02EN8	AD7528LN
REF02H/883B	AD7528SQ
REF02H	AD7528TQ
REF02HH	AD7528UJ
REF02HJ8	AD7530JD
REF02HN8	AD7530JN
REF02J8/883B	AD7530KD
REF02J8	AD7530KN

MAXIM

PMI	MAXIM
PM7224FX	AD7224BQ
PM7224FX	AD7224CQ
PM7224HP	AD7224KN
PM7224HP	AD7224LN
PM7224BX	AD7224TD
PM7224BX	AD7224TQ
PM7224BX	AD7224UD
PM7224BX	AD7224UQ
PM7226FR	AD7226BQ
PM7226GBC	AD7226KC/D
PM7226HP	AD7226KN
PM7226BR	AD7226TQ
PM7521FX	AD7521JD
PM7541HP	AD7521JN
PM7541FX	AD7521KD
PM7541HP	AD7521KN
PM7541FX	AD7521LD
PM7541HP	AD7521LN
PM7541BX	AD7521SD
PM7541BX	AD7521TD

MAXIM

PMI	MAXIM
PM7541BX	AD7521UD
PM7524HP	AD7523JN
PM7524HP	AD7523KN
PM7523GP	AD7523LN
PM7524GBC	AD7524AC/D
PM7524FQ	AD7524AD
PM7524FQ	AD7524AQ
PM7524FQ	AD7524BD
PM7524FQ	AD7524BQ
PM7524EQ	AD7524CD
PM7524EQ	AD7524CQ
PM7524HP	AD7524JN
PM7524HP	AD7524KN
PM7524GP	AD7524LN
PM7528ER	AD7528AQ
PM7528ER	AD7528BQ
PM7528ER	AD7528CQ
PM7528GBC	AD7528JC/D
PM7528HP	AD7528JN
PM7528GP	AD7528KN
PM7528GP	AD7528LN
PM7528BR	AD7528SQ
PM7528AR	AD7528TQ
PM7528AR	AD7528UJ
PM7533FQ	AD7530JD
PM7533HP	AD7530JN
PM7533EQ	AD7530KD
PM7533GP	AD7530KN
PM7533GP	AD7530LN
PM7541FX	AD7531JD
PM7541HP	AD7531JN
PM7541FX	AD7531KN
PM7541HP	AD7531KN
PM7541EX	AD7531LD
PM7541GP	AD7531LN
PM7533FQ	AD7533AQ
PM7533FQ	AD7533BQ
PM7533EQ	AD7533CQ
PM7533HP	AD7533JN
PM7533HP	AD7533KN
PM7533GP	AD7533LN
PM7533BQ	AD7533SQ
PM7533BQ	AD7533TQ
PM7533AQ	AD7533UQ
PM7541AFX	AD7541AAQ
PM7541AEX	AD7541ABQ
PM7541AGBC	AD7541AJC/D
PM7541AHP	AD7541AJN
PM7541AGP	AD7541AKN

MAXIM

PMI	MAXIM
PM7541FX	AD7541AQ
PM7541ABX	AD7541ASQ
PM7541AAX	AD7541ATQ
PM7541EX	AD7541BQ
PM7541GBC	AD7541JC/D
PM7541HP	AD7541JN
PM7541GP	AD7541KN
PM7541BX	AD7541SQ
PM7541AX	AD7541TQ
PM7542FQ	AD7542AQ
PM7542EQ	AD7542BQ
PM7542GBC	AD7542JC/D
PM7542HP	AD7542JN
PM7542GP	AD7542KN
PM7542BQ	AD7542SQ
PM7542AQ	AD7542TQ
PM7543FQ	AD7543AQ
PM7543EQ	AD7543BQ
PM7543GBC	AD7543JC/D
PM7543HP	AD7543JN
PM7543GP	AD7543KN
PM7543BQ	AD7543SQ
PM7543AQ	AD7543TQ
PM7545FR	AD7545AQ
PM7545ER	AD7545BQ
PM7545GBC	AD7545JC/D
PM7545HP	AD7545JN
PM7545GP	AD7545KN
PM7545BR	AD7545SQ
PM7545AR	AD7545TQ
PM7645FR	AD7645AQ
PM7645ER	AD7645BQ
PM7645GBC	AD7645JC/D
PM7645HP	AD7645JN
PM7645GP	AD7645KN
PM7645BR	AD7645SQ
PM7645AR	AD7645TQ
DAC312ER	Am6012ADC
DAC312ER	Am6012APC
DAC312FR	Am6012DC
DAC312BR	Am8012DM
DAC312FR	Am8012PC
SW201BQ	DG201AAK
SW201FQ	DG201ABK
SW201GP	DG201ACJ
SW202BQ	DG202AAK
SW202FQ	DG202ABK
SW202GP	DG202ACJ
MUX08BQ	DG508AAK
MUX08FQ	DG508ABK

INDUSTRY CROSS REFERENCE

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+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

MAXIM	PMI	MAXIM	PMI	MICRO POWER	PMI
DG508ACJ	MUX08FP	REF02DZ	REF02DZ	MP308AP	OP97FP+
DG509AAK	MUX24BQ	REF02EJ	REF02EJ	MP355AJ	PM355AJ
DG509ABK	MUX24FQ	REF02EZ	REF02EZ	MP355AJ	OP15FJ+
DG509ACJ	MUX24FP	REF02HJ	REF02HJ	MP355AZ	PM355AZ
MAX400CPA	OP77EP+	REF02HP	REF02HP	MP355AZ	OP15FZ+
MAX400CTV	OP77EJ+	REF02HZ	REF02HZ	MP356AJ	PM356AJ
MAX400EJA	OP77EZ+	REF02J	REF02J	MP356AJ	OP16FJ+
MAX400MJA	OP77AZ+	REF02Z	REF02Z	MP356AZ	PM356AZ
OP07AJ	OP07AJ			MP356AZ	OP16FZ+
OP07AJ	OP77AJ+			MP357AJ	OP17AJ+
OP07AZ	OP07AZ				
OP07AZ	OP77AZ+			MP4136CY	OP09FY
OP07CJ	OP07CJ			MP4136Y	OP09AY+
OP07CJ	OP77FJ+			MP5520AD	DAC01Y/883C
OP07CP	OP07CP			MP5520BD	DAC01BY
OP07CP	OP77GP+			MP5520CD	DAC01CY
OP07CZ	OP07CZ			MP5520DD	DAC01DY
OP07CZ	OP77FZ+			MP5520FD	DAC01FY
OP07DJ	OP07DJ			MP5520HD	DAC01HY
OP07DJ	OP77FJ+			MP7510DIJD	SW7510FQ
OP07DP	OP07DP			MP7510DIJN	SW7510FQ
OP07DP	OP77GP+			MP7510DIKD	SW7510FQ
OP07EJ	OP07EJ			MP7510DIKN	SW7510FQ
OP07EJ	OP77FJ+			MP7510DISD	SW7510BQ
OP07EP	OP07EP			MP7510DITD	SW7510BQ
OP07EP	OP77FP+			MP7511DIJD	SW7511FQ
OP07EZ	OP07EZ			MP7511DIJN	SW7511FQ
OP07EZ	OP77FZ+			MP7511DIKD	SW7511FQ
OP07J	OP07J			MP7511DIKN	SW7511FQ
OP07J	OP77BJ+			MP7511DISD	SW7511BQ
OP07Z	OP07Z			MP7511DITD	SW7511BQ
OP07Z	OP77BZ+				
REF01AJ	REF01AJ			MP7524AD	PM7524FQ
REF01AZ	REF01AZ			MP7524BD	PM7524FQ
REF01CJ	REF01CJ			MP7524CD	PM7524EQ
REF01CP	REF01CP			MP7524JN	PM7524HP
REF01CZ	REF01CZ			MP7524KN	PM7524HP
REF01EJ	REF01EJ			MP7524LN	PM7524GP
REF01EZ	REF01EZ			MP7524SD	PM7524BQ
REF01HJ	REF01HJ			MP7524TD	PM7524BQ
REF01HP	REF01HP			MP7524UD	PM7524AQ
REF01HZ	REF01HZ			MP7528BD	PM7528FR
REF01J	REF01J			MP7528CD	PM7528ER
REF01Z	REF01Z			MP7528KN	PM7528HP
REF02AJ	REF02AJ			MP7528LN	PM7528GP
REF02AZ	REF02AZ			MP7528TD	PM7528BR
REF02CJ	REF02CJ			MP7528UD	PM7528AR
REF02CP	REF02CP			MP7531JD	PM7541AFX+
REF02CZ	REF02CZ			MP7531JN	PM7541AHP+
REF02DP	REF02DP			MP7531KD	PM7541AFX+
				MP7531KN	PM7541AHP+
				MP7531LD	PM7541AFX+
				MP7531LN	PM7541AHP+
				MP7533AD	PM7533FQ
				MP7533BD	PM7533FQ
				MP7533CD	PM7533EQ
				MP7533JN	PM7533HP

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

MICRO POWER

PMI

MP7533KN	PM7533HP
MP7533LN	PM7533GP
MP7533SD	PM7533BQ
MP7533TD	PM7533BQ
MP7533UD	PM7533AQ
MP7541AD	PM7541FX
MP7541BD	PM7541EX
MP7541JN	PM7541HP
MP7541KN	PM7541GP
MP7541SD	PM7541BX
MP7541TD	PM7541AX
MP7542AD	PM7542FQ
MP7542BD	PM7542FQ
MP7542JN	PM7542HP
MP7542KN	PM7542HP
MP7542SD	PM7542BQ
MP7542TD	PM7542BQ
MP7543AD	PM7543FQ
MP7543BD	PM7543FQ
MP7543JN	PM7543HP
MP7543KN	PM7543HP
MP7543SD	PM7543BQ
MP7543TD	PM7543BQ
MP7545AD	PM7545FR
MP7545BD	PM7545FR
MP7545CD	PM7545FR
MP7545JN	PM7545HP
MP7545KN	PM7545HP
MP7545LN	PM7545HP
MP7545SD	PM7545BR
MP7545TD	PM7545BR
MP7545UD	PM7545BR
MP7574AD	PM7574FX
MP7574AD	ADC908FX+
MP7574BD	PM7574EX
MP7574BD	ADC908EX+
MP7574JN	PM7574HP
MP7574JN	ADC908HP+
MP7574KN	PM7574GP
MP7574KN	ADC908GP+
MP7574SD	PM7574BX
MP7574SD	ADC908BX+
MP7574TD	PM7574AX
MP7574TD	ADC908AX+
MP7623AD	PM7541AFX
MP7623BD	PM7541AEX
MP7623JN	PM7541AHP
MP7623KN	PM7541AGP
MP7623SD	PM7541ABX
MP7623TD	PM7541AAAX

MICRO POWER

PMI

MP7628AD	DAC8408FT
MP7628BD	DAC8408ET
MP7628JN	DAC8408HP
MP7628KN	DAC8408GP
MP7628SD	DAC8408BT
MP7628TD	DAC8408AT
MP7645AD	PM7645FR
MP7645BD	PM7645FR
MP7645CD	PM7645ER
MP7648JN	PM7645HP
MP7645KN	PM7645HP
MP7645LN	PM7645GP
MP7645SD	PM7645BR
MP7645TD	PM7645BR
MP7645UD	PM7645AR
MPOP01CJ	OP01CJ
MPOP01CP	OP01CP
MPOP01CZ	OP01CZ
MPOP01GJ	OP01GJ
MPOP01HJ	OP01HJ
MPOP01HP	OP01HP
MPOP01HZ	OP01HZ
MPOP01J	OP01J
MPOP02AJ	OP02AJ
MPOP02AZ	OP02AZ
MPOP02BJ	OP02BJ
MPOP02BZ	OP02AZ
MPOP02CJ	OP02CJ
MPOP02CP	OP02CP
MPOP02CZ	OP02CZ
MPOP02DJ	OP02CJ
MPOP02DP	OP02DP
MPOP02DZ	OP02CZ
MPOP02EJ	OP02EJ
MPOP02EP	OP02EP
MPOP02EZ	OP02EZ
MPOP02J	OP02J
MPOP04AY	OP04AY
MPOP04CY	OP04CY
MPOP04DY	OP04DY
MPOP04EY	OP04EY
MPOP04Y	OP04Y
MPOP05AJ	OP05AJ
MPOP05BJ	OP05BJ
MPOP05CJ	OP05CJ
MPOP05CZ	OP05CZ
MPOP05DJ	OP05DJ
MPOP05EJ	OP05EJ
MPOP05EZ	OP05EZ
MPOP05J	OP05J

MICRO POWER

PMI

MPOP05Z	OP05Z
MPOP07AJ	OP07AJ
MPOP07AJ	OP77AJ+
MPOP07AZ	OP07AZ
MPOP07AZ	OP77AZ+
MPOP07CJ	OP07CJ
MPOP07CJ	OP77FJ+
MPOP07CP	OP07CP
MPOP07CP	OP77GP+
MPOP07CZ	OP07CZ
MPOP07CZ	OP77FZ+
MPOP07DJ	OP07DJ
MPOP07DJ	OP77FJ+
MPOP07DP	OP07DP
MPOP07DP	OP77GP+
MPOP07DZ	OP07DZ
MPOP07DZ	OP77FZ+
MPOP07EJ	OP07EJ
MPOP07EJ	OP77FJ+
MPOP07EP	OP07EP
MPOP07EP	OP77FP+
MPOP07EZ	OP07EZ
MPOP07EZ	OP77FZ+
MPOP07J	OP07J
MPOP07J	OP77BJ+
MPOP07Z	OP07Z
MPOP07Z	OP77BZ+
MPOP08AJ	OP08AJ
MPOP08AJ	OP08AZ
MPOP08EJ	OP08EJ
MPOP08EP	OP08EP
MPOP08EZ	OP08EZ
MPOP08GZ	OP08GZ
MPOP09AY	OP09AY
MPOP09EY	OP08EY
MPOP09FP	OP09FP
MPOP09FY	OP09FY
MPOP10AY	OP10AY
MPOP10CY	OP10CY
MPOP10EY	OP10EY
MPOP10Y	OP10Y
MPOP11AY	OP11AY
MPOP11BY	OP11BY
MPOP11EP	OP11EP
MPOP11EY	OP11EY
MPOP11FP	OP11FP
MPOP11FY	OP11FY
MPOP12AZ	OP12AZ
MPOP12BZ	OP12BZ
MPOP12CZ	OP12CZ
MPOP12EJ	OP12EJ
MPOP12EZ	OP12EZ
MPOP12FJ	OP12FJ
MPOP12FZ	OP12EZ
MPOP12GJ	OP12GJ

INDUSTRY CROSS REFERENCE

4

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

<u>MICRO POWER</u>	<u>PMI</u>	<u>MICRO POWER</u>	<u>PMI</u>	<u>MOTOROLA</u>	<u>PMI</u>
MPOP12GZ	OP12GZ	MPOP37GJ	OP37GJ	LF355BJ	PM355AZ
MPOP14AJ	OP14AJ	MPOP37GP	OP37GP	LF355BJ	OP15FZ+
MPOP14AZ	OP14AZ	MPOP37GZ	OP37GZ	LF355BN	PM355AZ
MPOP14CJ	OP14CJ	MPREF01AJ	REF01AJ	LF355BN	OP15FZ+
MPOP14CP	OP14CP	MPREF01AZ	REF01AZ	LF355H	PM355AJ
MPOP14CZ	OP14CZ	MPREF01CJ	REF01CJ	LF355H	OP15FJ+
MPOP14DP	OP14DP	MPREF01CP	REF01CP	LF355J	PM355AZ
MPOP14DZ	OP14DZ	MPREF01CZ	REF01CZ	LF355J	OP15FZ+
MPOP14EJ	OP14EJ	MPREF01EJ	REF01EJ	LF355N	PM355AZ
MPOP14EP	OP14EP	MPREF01EZ	REF01EZ	LF355N	OP15FZ+
MPOP14EZ	OP14EZ	MPREF01HJ	REF01HJ	LF356BH	PM356AJ
MPOP14J	OP14J	MPREF01HP	REF01HP	LF356BH	OP16FJ+
MPOP14Z	OP14Z	MPREF01HZ	REF01HZ	LF356BJ	PM356AZ
MPOP207AY	OP207AY	MPREF01J	REF01J	LF356BJ	OP16FZ+
MPOP207BY	OP207AY	MPREF01Z	REF01Z	LF356BN	PM356AZ
MPOP207EY	OP207EY	MPREF02AJ	REF02AJ	LF356BN	OP16FZ+
MPOP207FY	OP207FY	MPREF02AZ	REF02AZ	LF356H	PM356AJ
MPOP227AY	OP227AY	MPREF02CJ	REF02CJ	LF356H	OP16FJ+
MPOP227BY	OP227AY	MPREF02CP	REF02CP	LF356J	PM356AZ
MPOP227CY	OP227AY	MPREF02CZ	REF02CZ	LF356J	OP16FZ+
MPOP227EY	OP227EY	MPREF02DJ	REF02CJ	LF356N	PM356AZ
MPOP227FY	OP227FY	MPREF02DP	REF02DP	LF356N	OP16FZ+
MPOP227GY	OP227GY	MPREF02DZ	REF02CZ	LF357BH	PM357AJ
MPOP27AJ	OP27AJ	MPREF02EJ	REF02EJ	LF357BH	OP17FJ+
MPOP27AZ	OP27AZ	MPREF02EZ	REF02EZ	LF357BJ	PM357AZ
MPOP27BJ	OP27BJ	MPREF02HJ	REF02HJ	LF357BJ	OP17FZ+
MPOP27BZ	OP27BZ	MPREF02HP	REF02HP	LF357BN	PM357AZ
MPOP27CJ	OP27CJ	MPREF02HZ	REF02HZ	LF357BN	OP17FZ+
MPOP27CZ	OP27CZ	MPREF02J	REF02J	LF357H	PM357AJ
MPOP27EJ	OP27EJ	MPREF02Z	REF02Z	LF357H	OP17FJ+
MPOP27EP	OP27EP	MPREF05AJ/883	REF05AJ/883C	LF357J	PM357AZ
MPOP27EZ	OP27EZ	MPREF05BJ/883	REF05BJ/883C	LF357J	OP17FZ+
MPOP27FJ	OP27FJ	MPREF10AJ/883	REF10AJ/883C	LF357N	PM357AZ
MPOP27FP	OP27FP	MPREF10BJ/883	REF10BJ/883C	LF357N	OP17FZ+
MPOP27FZ	OP27FZ	MPT01AH	MAT01AH+	LM108AH	OP97AJ+
MPOP27GJ	OP27GJ	MPT01GH	MAT01GH+	LM108AH	PM108AJ
MPOP27GP	OP27GP	MPT02AH	MAT02AH+	LM108AJ	PM108AZ
MPOP27GZ	OP27GZ	MPT02BH	MAT02BH+	LM108AJ	OP97AZ+
MPOP37AJ	OP37AJ	MPT02EH	MAT02EH+	LM108AJ-8	PM108AZ
MPOP37AZ	OP37AZ	MPT02FH	MAT02FH+	LM108AJ-8	OP97AZ+
MPOP37BJ	OP37BJ			LM108H	PM108J
MPOP37BZ	OP37BZ			LM108H	OP97AJ+
MPOP37CJ	OP37CJ			LM108J	PM108AZ
MPOP37CZ	OP37CZ			LM108J	OP97AZ+
MPOP37EJ	OP37EJ			LM108J-8	PM108Z
MPOP37EP	OP37EP			LM108J-8	OP97AZ+
MPOP37EZ	OP37EZ			LM111H	PM111J
MPOP37FJ	OP37FJ			LM111J-8	PM111Z
MPOP37FP	OP37FP			LM139AJ	PM139AY
MPOP37FZ	OP37FZ			LM139J	PM139Y
		<u>MOTOROLA</u>	<u>PMI</u>		
		DAC08AQ	DAC08AQ		
		DAC08CP	DAC08CP		
		DAC08CQ	DAC08CQ		
		DAC08EP	DAC08EP		
		DAC08EQ	DAC08EQ		
		DAC08HP	DAC08HP		
		DAC08HQ	DAC08HQ		
		DAC08Q	DAC08Q		
		LF355BH	PM355AJ		
		LF355BH	OP15FJ+		

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

MOTOROLA

LM148J
LM208AH
LM208AJ
LM208AJ-8
LM208H

LM208J
LM208J-8
LM211H
LM211J-8
LM239AJ

LM239AN
LM239J
LM239N
LM248J
LM248N

LM2901N
LM308AH
LM308AJ
LM308AJ-8
LM308AN

LM308H
LM308J
LM308J-8
LM308N
LM311H

LM311J-8
LM311N
LM3302L
LM3302P
LM339AJ

LM339AN
LM339J
LM339N
LM348J
LM348N

MC1404AU10
MC1404AU5
MC1408L8
MC1408L7
MC1408L8

MC1408P6
MC1408P7
MC1408P8
MC1458CG
MC1458CP1

MC1458CU
MC1458G
MC1458NG
MC1458NP1
MC1458P1

PMI

OP11BY+
PM208AJ
PM208AZ
PM208AZ
PM208J

PM208Z
PM208Z
PM211J
PM211Z
PM139Y+

PM139Y+
PM139Y+
PM139Y+
OP11BY+
OP11BY+

CMP04FY+
PM308AJ
PM308AZ
PM308AZ
PM308AP

PM308J
PM308Z
PM308Z
PM308AP
PM211J+

PM211Z+
PM211Z+
CMP04FY+
CMP04FY+
PM339AY

PM339AY+
PM339AY+
PM339AY+
OP11FY+
OP11FP+

REF01HZ
REF02HZ
DAC1408A-8Q+
DAC1408A-7Q+
DAC1408A-8Q

DAC1408A-8P+
DAC1408A-7P+
DAC1408A-8P+
OP14DJ+
OP14DP+

OP14DZ+
OP14DJ+
OP14DZ+
OP14DP+
OP14DP+

MOTOROLA

MC1458U
MC1504AU10
MC1504AU5
MC1504U10
MC1504U5

MC1508L8
MC1558G
MC1558NG
MC1558NU
MC1558U

MC1709AG
MC1709AU
MC1709CG
MC1709CP1
MC1709CU

MC1709G
MC1741CG
MC1741CP1
MC1741CU
MC1741G

MC1741NC
MC1741NCG
MC1741NCP1
MC1741NCU
MC1741NU

MC1741SCG
MC1741SG
MC1741U
MC1747CG
MC1747CL

MC1747CP2
MC1747G
MC1747L
MC1776CG
MC1776CP1

MC1776CU
MC1776G
MC1776U
MC3303L
MC3303P

MC33078P
MC3358P1
MC3403L
MC3403P
MC3458G

MC3458P1
MC3458U
MC3503L
MC3558G
MC3558U

PMI

OP14DZ+
REF01Z+
REF02Z+
REF01Z+
REF02Z+

DAC1508A-8Q+
OP14BJ+
OP14BJ+
OP14BZ+
OP14BZ+

OP06CJ+
OP06CZ+
OP06GJ+
OP06GZ+
OP06GZ+

OP06GJ+
OP02DJ+
OP02DP+
OP02DZ+
OP02BJ+

OP02BJ+
OP02DJ+
OP02DP+
OP02DZ+
OP02BZ+

OP01CP+
OP01GJ+
OP02BZ+
OP04DJ+
OP04DZ+

OP04DP+
OP04BJ+
OP04BZ+
OP22HJ+
OP22HZ+

OP22HZ+
OP22BJ+
OP22BZ+
OP421GY+
OP421GY+

OP271GP+
OP221GZ+
OP421HY+
OP421HY+
OP221GJ+

OP221GZ+
OP221GZ+
OP421CY+
OP221CJ+
OP221CZ+

MOTOROLA

MC4741CL
MC4741CP
MC4741L
OP27AJ
OP27AZ

OP27BJ
OP27BZ
OP27CJ
OP27CZ
OP27EJ

OP27EP
OP27EZ
OP27FJ
OP27FP
OP27FZ

OP27GJ
OP27GP
OP27GZ
OP37AJ
OP37AZ

OP37BJ
OP37BZ
OP37CJ
OP37CZ
OP37EJ

OP37EP
OP37EZ
OP37FJ
OP37FP
OP37FZ

OP37GJ
OP37GP
OP37GZ

NATIONAL

AD7520JD
AD7520JN
AD7520KD
AD7520KN
AD7520LD

AD7520LN
AD7520SD
AD7520TD
AD7520UD
AD7521JD

AD7521JN
AD7521KD
AD7521KN
AD7521LD
AD7521LN

PMI

OP11GY+
OP11GP+
OP11CY+
OP27AJ
OP27AZ

OP27BJ
OP27BZ
OP27CJ
OP27CZ
OP27EJ

OP27EP
OP27EZ
OP27FJ
OP27FP
OP27FZ

OP27GJ
OP27GP
OP27GZ
OP37AJ
OP37AZ

OP37BJ
OP37BZ
OP37CJ
OP37CZ
OP37EJ

OP37EP
OP37EZ
OP37FJ
OP37FP
OP37FZ

OP37GJ
OP37GP
OP37GZ

PMI

PM7533FQ+
PM7533HP+
PM7533FQ
PM7533FP
PM7533EQ

PM7533GP
PM7533BQ+
PM7533BQ
PM7533AQ
PM7541FX+

PM7541HP+
PM7541FX+
PM7541HP+
PM7541FX+
PM7541HP+

INDUSTRY CROSS REFERENCE

4

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

NATIONAL	PMI	NATIONAL	PMI	NATIONAL	PMI
AD7521SD	PM7541BX+	LF357AH	PM357AJ	LM111J	PM111Y
AD7521TD	PM7541BX+	LF357H	PM357AJ+	LM111J-8	PM111Z
AD7521UD	PM7541BX+	LF357N	PM357AZ+	LM112H	OP12CJ+
AD7530JD	PM7533FQ+	LF411ACH	OP15EJ+	LM118H	OP42AJ+
AD7530JN	PM7533HP+	LF411ACN	OP15EZ+	LM118J	OP42AZ+
AD7530KD	PM7533FQ	LF411AMH	OP15AJ+	LM118J-8	OP42AZ+
AD7530KN	PM7533FP	LF411CH	OP15FJ+	LM119H	PM119K
AD7530LD	PM7533EQ	LF411CN	OP15FZ+	LM119J	PM119Y
AD7530LN	PM7533GP	LF411MH	OP15BJ+	LM124AJ	OP421BY+
AD7531JD	PM7541FX+	LF412ACH	OP215EJ+	LM124J	OP421BY+
AD7531JN	PM7541HP+	LF412ACN	OP215EZ+	LM139AJ	PM139AY
AD7531KD	PM7541FX+	LF412AMH	OP215AJ+	LM139J	PM139Y
AD7531KN	PM7541HP+	LF412CH	OP215FJ+	LM1458H	OP14DJ+
AD7531LD	PM7541FX+	LF412CN	OP215FZ+	LM1458J	OP14DZ+
AD7531LN	PM7541HP+	LF412MH	OP215BJ+	LM1458N	OP14DP+
ADC0820	PM0820	LF441ACH	OP43FJ+	LM148J	PM148Y+
DAC0800LCJ	DAC08EQ	LF441AMH	OP43AJ+	LM1558H	OP14BJ+
DAC0800LCN	DAC08FP	LF441CH	OP43FJ+	LM1558J	OP14BZ+
DAC0800LD	DAC08Q	LF441CN	OP43GP	LM158AH	OP221AJ+
DAC0801LCJ	DAC08CQ	LF11201D	SW201BQ+	LM158H	OP221CJ+
DAC0801LCN	DAC08CP	LF11202D	SW202BQ+	LM194H	MAT02AH+
DAC0802LCJ	DAC08HQ	LF11333D	SW06BQ+	LM207H	OP02J+
DAC0802LCN	DAC08HP	LF11508D	MUX08AQ	LM207J	OP02Z+
DAC0802LD	DAC08AQ	LF11509D	MUX24AQ	LM207J-14	OP02Z+
DAC0806LCJ	DAC1408A-6Q	LF13201D	SW201FQ+	LM208AH	PM208AJ
DAC0806LCN	DAC1408A-6P	LF13201N	SW201GP+	LM208AJ-8	PM208AZ
DAC0807LCJ	DAC1408A-7Q	LF13202D	SW202FQ+	LM208AN	PM208AZ+
DAC0807LCN	DAC1408A-7P	LF13202N	SW202GP+	LM208H	PM208J
DAC0808LCJ	DAC1408A-8Q	LF13333D	SW06FQ+	LM208J-8	PM208Z
DAC0808LCN	DAC1408A-8P	LF13333N	SW06GP+	LM210H	OP15CJ+
DAC0808LD	DAC1508A-8Q	LF13508D	MUX08EQ	LM210J	OP15CZ+
LF155AH	PM155AJ	LF13508N	MUX08EP	LM211H	PM211J
LF155H	PM155J	LF13509D	MUX24EQ	LM211J	PM211Y
LF156AH	PM156AJ	LF13509N	MUX24EP	LM212H	OP12CJ+
LF156H	PM156J	LH0044ACH	OP77EJ+	LM218H	OP42FJ+
LF157AH	PM157AJ	LH0044AH	OP77AJ+	LM218J	OP42FZ+
LF157H	PM157J	LH0044BH	OP77EJ+	LM218J-8	OP42FZ+
LF255H	PM155J+	LH0044CH	OP77FJ+	LM219H	PM219K
LF256H	PM156J+	LH0044H	OP77AJ+	LM219J	PM219Y
LF257H	PM157J+	LH740ACH	OP43FJ+	LM224AJ	OP421FY+
LF351H	OP15GJ+	LH740AH	OP43BJ+	LM224J	OP421FY+
LF351N	OP15GZ+	LM107H	OP02J+	LM239AJ	PM139AY+
LF353H	OP215FJ	LM107J	OP02Z+	LM239J	PM139Y+
LF353N	OP215FZ	LM107J-14	OP02Z+	LM248J	PM248Y+
LF355AH	PM355AJ	LM108AH	PM108AJ	LM258AH	OP221FJ+
LF355H	PM355AJ+	LM108AJ-8	PM108AZ	LM258H	OP221GJ+
LF355N	PM355AZ+	LM108H	PM108J	LM2901J	PM139Y+
LF356AH	PM356AJ	LM108J-8	PM108Z	LM2901N	PM339AY+
LF356H	PM356AJ+	LM110H	OP15CJ+	LM2902J	OP421GY+
LF356N	PM356AZ+	LM111H	PM111J	LM2902N	OP421GY+

+Direct pin-for-pin replacement with improved specifications.



Precision Monolithics Inc.

DIRECT REPLACEMENT GUIDE

NATIONAL

LM2904N
LM307H
LM307J
LM307J-14
LM307N
LM308AH
LM308AH-1
LM308AH-2
LM308AJ-8
LM308AN
LM308H
LM308J-8
LM308N
LM310H
LM310J
LM310J
LM310J-8
LM310N
LM311H
LM311J
LM311J-8
LM311N
LM311N-14
LM312H
LM318H
LM318J
LM318JN
LM318J-8
LM319H
LM319J
LM324AJ
LM324AN
LM324J
LM324N
LM339AJ
LM339AN
LM339J
LM339N
LM348J
LM348N
LM358AH
LM358AN
LM358H
LM358N
LM394BH
LM394CH
LM394H
LM709CH
LM709CN
LM709CN-8

PMI

OP221GZ+
OP02DJ+
OP02DZ+
OP02DZ+
OP02DP+
PM308AJ
PM1012GJ+
OP97EJ+
PM308AZ
PM308AP
PM308H
PM308J
PM308Z
PM308AP
OP15GJ+
OP15CZ+
OP15GZ+
OP15GZ+
OP15GZ+
PM211J+
PM211Y+
PM211Z+
PM211Z+
PM211Y+
OP12GJ+
OP42FJ+
OP42FZ+
OP42FZ+
OP42FZ+
OP42FZ+
PM219K+
PM319Y
OP421HY+
OP421HY+
OP421HY+
OP421HY+
PM339AY
PM339AY+
PM339AY+
PM339AY+
PM248Y+
PM248Y+
OP221FJ+
OP221FZ+
OP221GJ+
OP221GZ+
MAT02FH+
MAT02FH+
MAT02FH+
OP06GJ+
OP08GZ+
OP06GZ+

NATIONAL

LM709H
LM725AH
LM725CH
LM725CN
LM725H
LM741AH
LM741CH
LM741CJ
LM741CN
LM741EH
LM741EN
LM741H
LM747AH
LM747AJ
LM747CH
LM747CJ
LM747CN
LM747EH
LM747EJ
LM747EN
LM747H
LM747J
LM748CH
LM748CJ
LM748CN
LM748H
LM748J
LM3302J
LM3302N
LM4250CH
LM4250CJ
LM4250CN
LM4250H
LM4250J

NEC

μPC1458C
μPC301AC
μPC311C
μPC318C
μPC319C
μPC324C
μPC339C
μPC3403C
μPC356C
μPC356C
μPC357C
μPC358C
μPC4071C
μPC4072C
μPC4081C

PMI

OP06CJ+
OP06BJ+
OP06GZ+
OP06GZ+
OP06BJ+
OP77FJ+
PM741CJ
OP77GZ+
OP77GP+
OP77FJ+
OP77GP+
PM741J
OP04K+
OP04Y+
OP04DK+
OP04DY+
OP04DP+
OP04CK+
OP04CY+
OP04CP+
OP04K+
OP04Y+
PM1008GJ+
PM1008GZ+
PM1008GP+
PM1008AJ+
PM1008AZ+
PM139Y+
PM339AY+
OP22HJ+
OP22HZ+
OP22HZ+
OP22BJ+
OP22BZ+
PMI
OP14DP+
OP77GP+
PM211Z
OP42FZ+
PM219Y
OP421HY+
PM139Y
OP421HY+
PM356AZ
OP16GZ+
OP17GZ+
OP221GZ+
OP15GZ
OP215GZ
OP15GZ

NEC

μPC4082C
μPC4250C
μPC4557C
μPC4558C
μPC4559C
μPC4560C
μPC4574C
μPC4741C
μPC4741C
μPC6012C
μPC624C
μPC624D
μPC741C
μPC811C
μPC812C
μPC813C

RCA

CA101
CA124E
CA139AF
CA139F
CA1458E
CA1458T
CA1558E
CA1558T
CA158
CA158
CA158AE
CA158AT
CA201
CA224E
CA239AF
CA239F
CA258
CA258
CA258AE
CA258AT
CA2904E
CA301
CA301A
CA307E
CA307T
CA311E
CA311T
CA3140AE
CA3140AT
CA3140E
CA3140T
CA3160AT
CA3160T
CA3193AE
CA3193AT

PMI

OP215GZ
OP22HZ+
OP270+
OP270+
OP270+
OP270+
OP270+
OP471FY
OP11GP+
OP400FY+
DAC312FR
DAC08EP
DAC08EQ
OP02DP+
OP15FZ
OP215FZ
OP16FZ
PMI
OP77+
OP421CY+
PM139AY
PM139Y
OP14DP+
OP14CJ+
OP14Z+
OP14J+
OP221AZ+
OP221CJ+
OP221AZ+
OP221CJ+
OP77+
OP421GY+
PM139AY
PM139Y
OP221GZ+
OP221GJ+
OP221GZ+
OP221GJ+
OP221GZ+
OP77+
OP77+
OP77GP+
OP77FJ+
PM211Y
PM211J
OP41GP+
OP41BJ+
OP41GP+
OP41FJ+
OP41BJ+
OP41FJ+
OP77FZ+
OP77FJ+

INDUSTRY CROSS REFERENCE

4

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

<u>RCA</u>	<u>PMI</u>	<u>RAYTHEON</u>	<u>PMI</u>	<u>RAYTHEON</u>	<u>PMI</u>
CA3193E	OP77GP+	HA1-4741-2	OP11BY+	OP07AT	OP77AJ+
CA3193T	OP77FJ+	HA1-4741-2	OP400AY+	OP07AT/883B	OP07AJ/883C
CA3240AE	OP215BZ+	HA1-4741-5	OP11GP+	OP07AT/883B	OP77AJ/883C+
CA3240AE1	OP215BY+	HA1-4741-5	OP400FY+	OP07CDE	OP07EZ
CA3240E	OP215CZ+	HA1-4741-8	OP11BY/883C+	OP07CDE	OP77FZ+
CA3240E1	OP215CY+	HA1-4741-8	OP400AY/883C+	OP07CNB	OP07CP
CA324E	OP421HY+	HA3-4741-5	OP11FY+	OP07CNB	OP77GP+
CA339AF	PM139AY	HA3-4741-5	OP400FY+	OP07CT	OP07CJ
CA339F	PM139Y	LM101ADE	OP77BZ+	OP07CT	OP77FJ+
CA3493AE	OP77BZ+	LM101ADE/883B	OP77BZ/883C+	OP07DDE	OP07CZ
CA3493AT	OP77BJ+	LM101AH	OP77BJ+	OP07DDE	OP77FZ+
CA3493E	OP77GP+	LM101AH/883B	OP77BJ/883C+	OP07DE	OP07Z
CA3493T	OP77FJ+	LM124	OP400+	OP07DE	OP77BZ+
CA358	OP221GZ+	LM139AJ	CMP04BY+	OP07DE/883B	OP07Z/883C
CA358	OP221GJ+	LM139AJ	PM139AY	OP07DE/883B	OP77BZ/883C+
CA358AE	OP221GZ+	LM139AJ/883B	PM139Y/883C	OP07DNB	OP07DP
CA358AT	OP221GJ+	LM139J	PM139Y	OP07DNB	OP77GP+
CA741CE	PM741CY	LM139J/883B	PM139Y/883C	OP07DT	OP07DJ
CA741CE	OP77GZ+	LM148J	OP400AY+	OP07DT	OP77FJ+
CA741CT	PM741CJ	LM148J/883B	OP400AY/883C+	OP07EDE	OP07EZ
CA741CT	OP77FJ+	LM201ADE	OP77FZ+	OP07EDE	OP77FZ+
CA741E	PM741Y	LM201AH	OP77FJ+	OP07ENB	OP07EP
CA741E	OP77BZ+	LM248J	OP400FY+	OP07ENB	OP77FP+
CA741T	PM741J	LM248N	OP400GP+	OP07ET	OP07EJ
CA741T	OP77BJ+	LM2901N	CMP04FP+	OP07ET	OP77FJ+
CA747CE	OP04DY+	LM301ADE	OP77FZ+	OP07T	OP07J
CA747E	OP04Y+	LM301AH	OP77FJ+	OP07T	OP77BJ+
CA748CE	OP08GZ+	LM301AN	OP77GP+	OP07T/883B	OP07J/883C
CA748CT	OP08EJ+	LM339N	CMP04FP+	OP07T/883B	OP77BJ/883C+
CA748E	OP08AZ+	LM348J	OP400FY+	OP27ADE	OP27AZ
CA748T	OP08AJ+	LM348N	OP400GP+	OP27ADE/883B	OP27AZ/883C
LM311E	PM211Y	OP05ADE	OP05AZ	OP27AT	OP27AJ
LM311T	PM211J	OP05ADE/883B	OP05AZ/883C	OP27AT/883B	OP27AJ/883C
LM324E	OP421HY+	OP05AT	OP05AJ	OP27BDE	OP27BZ
		OP05AT/883B	OP05AJ/883C	OP27BDE/883B	OP27BZ/883C
		OP05CDE	OP05CZ	OP27BT	OP27BJ
RAYTHEON	PMI	OP05CNB	OP05CP	OP27BT/883B	OP27BJ/883C
DAC08ADM	DAC08AQ	OP05CT	OP05CJ	OP27CDE	OP27CZ
DAC08ADM/883B	DAC08AQ/883C	OP05DE	OP05Z	OP27CDE/883B	OP27CZ/883C
DAC08CDC	DAC08CQ	OP05DE/883B	OP05Z/883C	OP27CT	OP27CJ
DAC08DM	DAC08Q	OP05EDE	OP05EZ	OP27CT/883B	OP27CJ/883C
DAC08EDC	DAC08EQ	OP05ENB	OP05EP	OP27EDE	OP27EZ
DAC08HDC	DAC08HQ	OP05ET	OP05EJ	OP27ENB	OP27EP
DAC10BDM	DAC10BX	OP05T	OP05J	OP27ET	OP27EJ
DAC10BDM/883B	DAC10BX/883C	OP05T/883B	OP05J/883C	OP27FDE	OP27FZ
DAC10CDM	DAC10CX	OP07ADE	OP07AZ	OP27FNB	OP27FP
DAC10CDM/883B	DAC10BX/883C	OP07ADE	OP77AZ+	OP27FT	OP27FJ
DAC10FDC	DAC10FX	OP07ADE/883B	OP07AZ/883C	OP27GDE	OP27GZ
DAC10GDC	DAC10GX	OP07ADE/883B	OP77AZ/883C+	OP27GNB	OP27GP
DAC6012ADC	DAC312ER	OP07AT	OP07AJ	OP27GT	OP27GJ
DAC6012DC	DAC312FR				
DAC6012DM/883B	DAC312BR/883C				

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

RAYTHEON

OP37ADE
OP37ADE/883B
OP37AT
OP37AT/883B
OP37BDE
OP37BDE/883B
OP37BT
OP37BT/883B
OP37CDE
OP37CDE/883B
OP37CT
OP37CT/883B
OP37EDE
OP37ENB
OP37ET
OP37FDE
OP37FNB
OP37FT
OP37GDE
OP37GNB
OP37GT
RC1458DE
RC1458H
RC1458NB
RC1458T
RC2041
RC3302DB
RC4136DB
RC4136DC
RC4156DB
RC4156DC
RC4556
RC4558
RC4559
RC4805DE
RC4805EDE
RC4805ET
RC4805T
RC714CDE
RC714CDE
RC714CH
RC714CH
RC714EDE
RC714EDE
RC714EH
RC714EH
RC714LDE
RC714LDE
RC714LH
RC714LH

PMI

OP37AZ
OP37AZ/883C
OP37AJ
OP37AJ/883C
OP37BZ
OP37BZ/883C
OP37BJ
OP37BJ/883C
OP37CZ
OP37CZ/883C
OP37CJ
OP37CJ/883C
OP37EZ
OP37EP
OP37EJ
OP37FZ
OP37FP
OP37FJ
OP37GZ
OP37GP
OP37GJ
OP14CZ+
OP14CJ+
OP14DP+
OP14CJ+
OP270+
CMP04FP+
OP09FP+
OP09FY+
OP470FY+
OP470FY+
OP270+
OP270+
OP270+
CMP05GZ
CMP05FZ
CMP05FJ
CMP05GJ
OP07CZ
OP77FZ+
OP07CJ
OP77FJ+
OP07EZ
OP77FZ+
OP07EJ
OP77FJ+
OP07CZ+
OP77FZ+
OP07DJ+
OP77FJ+

RAYTHEON

RC725T
RC725T
RC741H
RC741H
RC741T
RC741T
RC747DB
RC747DB
RC747DC
RC747DC
REF01ADE/883B
REF01AT/883B
REF01CDE
REF01CT
REF01DDE
REF01DE/883B
REF01DT
REF01EDE
REF01ET
REF01HDE
REF01HT
REF01T/883B
REF02ADE/883B
REF02AT/883B
REF02CDE
REF02CT
REF02DDE
REF02DE/883B
REF02DT
REF02EDE
REF02ET
REF02HDE
REF02HT
REF02T/883B
REF03CNB
REF03NB
RM1558DE
RM1558DE/883B
RM1558T
RM1558T/883B
RM4136DC
RM4136DC/883B
RM4156DC
RM4156DC/883B
RM714DE
RM714DE
RM714DE/883B
RM714DE/883B
RM714H
RM714H

PMI

OP06GJ+
OP77FJ+
PM741CJ
OP77FJ+
PM741CJ
OP77FJ+
PM747CY
OP04CY+
PM747CY
OP04DY+
REF01AZ/883C
REF01AJ/883C
REF01CJ
REF01CJ
REF01CZ+
REF01Z/883C
REF01CJ
REF01EZ
REF01EJ
REF01HZ
REF01HJ
REF01J/883C
REF02AZ/883C
REF02AJ/883C
REF02CZ
REF02CJ
REF02CZ
REF02Z/883C
REF02DJ
REF02EZ
REF02EJ
REF02HZ
REF02HJ
REF02J/883C
REF03GP+
REF03GP+
OP14Z+
OP14Z/883C+
OP14J+
OP14J/883C+
OP09AY+
OP09AY/883C+
OP470AY+
OP470AY/883C+
OP07Z/883C
OP77BZ+
OP07Z/883C
OP77BZ/883C+
OP07J
OP77BJ+

RAYTHEON

RM714H/883B
RM714H/883B
RM725T
RM741T
RM741T
RM747DC
RM747DC
RM747DC/883B

PMI

OP07J/883C
OP77BJ/883C+
OP06CJ+
PM741J
OP77BJ+
PM747Y
OP04Y+
OP04Y/883C+

SIGNETICS

Am6012F
DAC08AF
DAC08CF
DAC08CN
DAC08EF
DAC08EN
DAC08F
DAC08HF
DAC08HN
LM111FE
LM119F
LM139AF
LM139AF
LM139F
LM139F
LM211FE
LM219F
LM239
LM239AF
LM339
LM339AN
MC1408-7F
MC1408-7N
MC1458H
MC1458N
MC1508-8F
MC1558H
MC1558N
MC3303F
MC3403F
MC3503F
NE4558FE
NE4558N
NE530FE
NE530H
NE531FE
NE531H
NE538FE
NE538H
NE5512FE

PMI

DAC312FR
DAC08AQ
DAC08CQ
DAC08CP
DAC08EQ
DAC08EP
DAC08Q
DAC08HQ
DAC08HP
PM111Z
PM119Y
PM139AY
CMP04BY+
PM139Y
CMP04BY+
PM211Z
PM219Y
CMP04FY+
CMP04FY+
CMP04FP+
CMP04FP+
DAC1408A-7Q
DAC1408A-7P
OP14CJ+
OP14DP+
DAC1508A-8Q
OP14J+
OP14Z+
OP14Z+
OP421HY+
OP421HY+
OP421CY+
OP14DZ+
OP14DP+
OP42FZ+
OP42FJ+
OP42FZ+
OP42FJ+
OP42FJ+
OP270+

INDUSTRY CROSS REFERENCE

4

+Direct pin-for-pin replacement with improved specifications.



DIRECT REPLACEMENT GUIDE

Precision Monolithics Inc.

SIGNETICS

NE5514F	OP470FY+
NE5514N	OP470FY+
NE5532	OP270
NE5532A	OP270
NE5534	OP27GZ+
NE5534	OP27GP+
NE5534AFE	OP27GZ+
NE5534AN	OP27GP+
SA1458N	OP14Z+
SA4558FE	OP14CZ+
SA4558N	OP14CZ+
SA741CN	OP02DZ+
SE4558FE	OP14Z+
SE530FE	OP42AZ+
SE530H	OP42AJ+
SE531FE	OP42AZ+
SE531H	OP42AJ+
SE538FE	OP42AZ+
SE538H	OP42AJ+
SE5512FE	OP270+
SE5514F	OP470AY+
SE5514N	OP470AY+
SE5534	OP27CZ+
SE5534AFE	OP27CZ+
μA741CFE	OP02DP+
μA741CN	OP02DP+
μA741FE	OP02BZ+
μA741N	OP02BZ+
μA747CF	PM747CY
μA747CF	OP04DY+
μA747F	PM747Y
μA747F	OP04Y+

SILICONIX

DG200AAA	SW05BK
DG200AAK	SW05BY
DG200ABA	SW05FK
DG200ABK	SW05FY
DG200ACJ	SW05GP
DG200ACK	SW05FY
DG201AAK	SW201BQ
DG201ABK	SW201FQ
DG201ACJ	SW201GP
DG201ACK	SW201FQ
DG202AK	SW202BQ
DG202BK	SW202FQ
DG202CJ	SW202GP
DG202CK	SW202FQ
DG506AAK	MUX16AT

PMI

OP470FY+
OP470FY+
OP270
OP270
OP27GZ+
OP27GP+
OP27GZ+
OP27GP+
OP14Z+
OP14CZ+
OP14CZ+
OP02DZ+
OP14Z+
OP42AZ+
OP42AJ+
OP42AZ+
OP42AJ+
OP42AZ+
OP42AJ+
OP270+
OP470AY+
OP470AY+
OP27CZ+
OP27CZ+
OP02DP+
OP02DP+
OP02BZ+
OP02BZ+
PM747CY
OP04DY+
PM747Y
OP04Y+

PMI

SW05BK
SW05BY
SW05FK
SW05FY
SW05GP
SW05FY
SW201BQ
SW201FQ
SW201GP
SW201FQ
SW202BQ
SW202FQ
SW202GP
SW202FQ
MUX16AT

SILICONIX

DG506ABK
DG506ACK
DG507AAK
DG507ABK
DG507ACK
DG508AAK
DG508ABK
DG508ACJ
DG508ACK
DG509AAK
DG509ABK
DG509ACJ
DG509ACK

TELEDYNE

TSC9495CJ
TSC9495CJ
TSC9496CJ
TSC9496CJ

TI

LM101AJG
LM107JG
LM108JG
LM108JG
LM124J
LM139AFH
LM139AJ
LM139J
LM148J
LM148J
LM201AJG
LM207JG
LM208JG
LM224J
LM301AP
LM307P
LM308P
LM324N
LM3302J
MC1458JG
MC1558JG
MC3303J
MC3403J
MC3503J
OP07CJG

PMI

MUX16ET
MUX16FT
MUX28AT
MUX28ET
MUX28FT
MUX08AQ
MUX08EQ
MUX08FP
MUX08FQ
MUX24AQ
MUX24EQ
MUX24FP
MUX24FQ

PMI

REF02CP
REF02HP+
REF01CP
REF01HP+

PMI

OP77BZ+
OP77BZ+
PM108Z
OP97AZ+
OP400AY+
PM139ARC/883C
PM139AY
PM139Y
PM148Y
OP400AY+
OP77FZ+
OP77FZ+
OP97FZ+
OP400FY+
OP77GP+
OP77GP+
OP97FP+
OP400GP+
CMP04FY+
OP14DZ+
OP14BZ+
OP421GY+
OP421HY+
OP421CY+
OP07CZ

TI

OP07CJG
OP07CP
OP07CP
OP07DP
OP07DP
OP07EJG
OP07EJG
OP07EP
OP07EP
OP12AJG
OP12AJG
OP12BJG
OP12BJG
OP12CJG
OP12CJG
OP12EJG
OP97EJG
OP12FJG
OP12FJG
OP12GJG
OP12GJG
OP227EJ
OP227FJ
OP227GJ
RC4136J
RC4136N
RC4558JG
RC4559
RM4136J
RM4558JG
RV4136J
RV4558JG
TL136CJ
TLC7524CN
TLC7528IN
μA714CJG
μA714EJG
μA714LJG
μA741CJG
μA741MJG

PMI

OP77FZ+
OP07CP
OP77GP+
OP07DP
OP77GP+
OP07EZ
OP77FZ+
OP07EP
OP77FP+
OP12AZ
OP97AZ+
OP12BJG
OP97AZ+
OP12CZ
OP97AZ+
OP12EZ
OP97FZ+
OP12EZ
OP97FZ+
OP12GZ
OP97FZ+
OP227EY
OP227FY
OP227GY
OP09FY+
OP09FP+
OP270+
OP270+
OP09AY+
OP270+
OP09AY+
OP270+
OP470FY+
PM7524HP
PM7528FR
OP07CZ+
OP07EZ+
OP07CZ+
OP77FZ+
OP77BZ+

-Direct pin-for-pin replacement with improved specifications.



FUNCTIONAL REPLACEMENT GUIDE

Precision Monolithics Inc.

These devices are functionally similar, but may have some electrical and/or pin-out differences.

<u>ANALOG DEVICES</u>	<u>PMI</u>	<u>BURR-BROWN</u>	<u>PMI</u>	<u>HARRIS</u>	<u>PMI</u>
AD1403	REF43	OPA103BM	OP41AJ	HA2-2502-2	OP42AJ
AD1403A	REF43	OPA103CM	OP41AJ	HA7-2502-8	OP42AZ/883C
AD509JH	OP44FJ	OPA103DM	OP41AJ	HA2-2502-8	OP42AJ/883C
AD509KH	OP44EJ	OPA104	OP80	HA3-2505-5	OP42GP
AD509SH	OP44AJ	OPA111AM	OP41EJ	HA2-2505-5	OP42FJ
AD515	OP80	OPA111BM	OP41EJ	HA7-2505-5	OP42FZ
AD521	AMP01	OPA111SM	OP41AJ	HA7-2510-2	OP42AZ
AD522	AMP01	OPA128	OP80	HA2-2510-2	OP42AJ
AD544JH	OP43FJ	OPA211	OP215AJ	HA7-2510-8	OP42AZ/883C
AD544KH	OP43FJ	REF10JM	REF01EJ	HA2-2510-8	OP42AJ/883C
AD544LH	OP43EJ	REF10KM	REF01EJ	HA4-2510-8	OP42ARC/883C
AD544SH	OP43AJ	REF10RM	REF10AJ	HA2-2512-2	OP42AJ
AD545JH	OP41FJ	REF10SM	REF10AJ	HA7-2512-2	OP42AZ
AD545KH	OP41FJ	SHC298AM	SMP10	HA2-2512-8	OP42AJ/883C
AD545LH	OP41EJ	SHC85	SMP10	HA7-2512-8	OP42AZ/883C
AD547JH	OP41FJ			HA3-2515-5	OP42GP
AD547SH	OP41AJ			HA2-2515-5	OP42FJ
AD580	REF43	<u>EXAR</u>	<u>PMI</u>	HA7-2515-5	OP42FZ
AD581	REF01	XR082CN	OP215GZ	HA7-2520-2	OP44AZ
AD582	SMP10	XR082CP	OP215GZ	HA2-2520-2	OP44AJ
AD583	SMP10	XR082M	OP215BZ	HA2-2520-8	OP44AJ/883C
AD625	AMP01	XR082N	OP215BZ	HA7-2520-8	OP44AZ/883C
AD642	OP215	XR082P	OP215BZ	HA4-2520-8	OP44ARC/883C
AD644JH	OP215FJ	XR4212CN	OP470FY	HA2-2522-2	OP44AJ
AD644KH	OP215EJ	XR4212CP	OP470FY	HA7-2522-2	OP44AZ
AD644SH	OP215AJ	XR4212M	OP470AY	HA7-2522-8	OP44AZ/883C
AD711	OP15	XR4560	OP271	HA2-2522-8	OP44AJ/883C
AD712	OP16	XR5532	OP270	HA2-2525-5	OP44FJ
AD7225	DAC8408	XR5532A	OP270	HA3-2525-5	OP44GP
AD7501	MUX08	XR5533	OP215	HA7-2525-5	OP44FZ
AD7502	MUX24	XR5533A	OP215	HA1-2541-5	OP65EZ
AD7503	MUX08	XR5534	OP27	HA4-4741-8	OP400ARC/883C
AD7506	MUX16	XR5534A	OP27	HA1-4900-2	CMP04AY
AD7507	MUX28			HA1-4900-8	CMP04AY/883C
AD7537	DAC8248	<u>FAIRCHILD</u>	<u>PMI</u>	HA1-4902-2	CMP04AY
AD7547	DAC8212	μ A198	SMP11	HA1-4902-8	CMP04AY/883C
		μ A398	SMP11	HA1-4905-5	CMP04FY
		μ A710H	CMP05J	HA4-5102-8	OP270ARC/883C
		μ A734	CMP01	HA4-5104-8	OP470ARC/883C
		μ A798TC	OP220GZ	HA-5127	OP27
				HA1-5134A-2	OP400AY
				HA1-5134A-5	OP400EY
				HA1-5134-2	OP400AY
				HA1-5134-5	OP400FY
				HA-5137	OP37
				HA2-5141A-2	OP20CJ
				HA7-5141A-2	OP20CZ
				HA3-5141A-5	OP20HP
				HA7-5141A-5	OP20HZ
				HA2-5141A-5	OP20HJ
<u>BURR-BROWN</u>	<u>PMI</u>	<u>HARRIS</u>	<u>PMI</u>		
AD515	OP80	HA2-2500-2	OP42AJ		
BB4085	PKD01	HA7-2500-2	OP42AZ		
INA101	AMP01	HA2-2500-8	OP42AJ/883C		
INA104	AMP01	HA7-2500-8	OP42AZ/883C		
INA110	AMP05	HA7-2502-2	OP42AZ		
OPA101AM	OP42FJ				
OPA101BM	OP42EJ				
OPA102AM	OP44FJ				
OPA102BM	OP44EJ				
OPA103AM	OP41AJ				

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INDUSTRY CROSS REFERENCE



These devices are functionally similar, but may have some electrical and/or pin-out differences.

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These devices are functionally similar, but may have some electrical and/or pin-out differences.

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FUNCTIONAL REPLACEMENT GUIDE

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These devices are functionally similar, but may have some electrical and/or pin-out differences.

SIGNETICS

LF198	SMP10
LF298	SMP10
LF398	SMP10
LM124F	OP421BY
LM158FE	OP221AZ
LM158H	OP221CJ
LM224F	OP421FY
LM224N	OP421GY
LM258FE	OP221GZ
LM258H	OP221GJ
LM324F	OP421HY
LM324N	OP421HY
MC3410	DAC10
NE532FE	OP221GZ
NE532H	OP221GJ
NE5535	OP271
SE532FE	OP221AZ
SE532H	OP221CJ
SE5535	OP271

SILICONIX

DG211CJ	SW01FQ
DG212CJ	SW02FQ
DG5045	SW7510

TELEDYNE

TSC05/2.5V	REF43
TSC441	SW01
TSC442	SW02
TSC443	SW06
TSC4201	SW01
TSC4202	SW02
TSC4203	SW06

TI

LM158JG	OP221AJ
NE5532	OP271
NE5532A	OP271
NE5534	OP37
NE5534A	OP37
SE5534	OP37
SE5534A	OP37
TL022CJG	OP220GZ
TL022CP	OP220GZ
TL044CJ	OP420HY

TI

TL044MJ	OP420CY
TL071CJG	OP15GZ
TL071MJG	OP15BZ
TL072CJG	OP215GZ
TL072MJG	OP215BZ
TL081CJG	OP15GZ
TL081MJG	OP15BZ
TL082CJG	OP215GZ
TL082MJG	OP215BZ
TL087CJG	OP15EZ
TL088CJG	OP15FZ
TL088MJG	OP15BZ
TL288CJG	OP215FZ
TL288MJG	OP215BZ
TL321	OP20
TL322	OP220
TL510	CMP05
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TLC272CJG	OP290FZ
TLC274CJG	OP490FY

PMI

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Operational Amplifier5-164



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Low-Bias-Current, High-Stability
JFET Operational Amplifier 5-176 | *OP-90
Precision Low-Voltage Micropower
Operational Amplifier 5-252 |
| *OP-42
High-Speed, Fast-Settling Precision
Operational Amplifier 5-187 | *OP-97
Low-Power, High-Precision
Operational Amplifier 5-263 |
| *OP-43
Low-Bias-Current, Fast JFET
Operational Amplifier 5-199 | *OP-200
Dual Low-Offset, Low-Power
Operational Amplifier 5-273 |
| *OP-44
High-Speed, Precision
Operational Amplifier 5-212 | OP-207
Dual Ultra-Low V_{OS} Matched
Operational Amplifier 5-283 |
| OP-50
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Operational Amplifier 5-221 | OP-215
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Operational Amplifier 5-289 |
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Dual Micropower
Operational Amplifier 5-296 |
| *OP-65
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Dual High-Speed Current-Feedback
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*Indicates new product or product whose data sheet has been finalized since the 1986 data book.



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*Indicates new product or product whose data sheet has been finalized since the 1986 data book.



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JM38510/10106

JAN Dual Low-Input-Current

Operational Amplifier 5-451

JM38510/11004

JAN Quad 741-Type

Operational Amplifier 5-454

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INTRODUCTION

Precision Monolithics pioneered in the development of low-offset, high-gain operational amplifiers for use in precision applications. PMI's proprietary bipolar process with nitride passivation offers low noise, enhanced long term reliability and improved radiation resistance. In addition to standard NPN and PNP devices, PMI processing capabilities include high speed PNP, JFET, and super-beta transistors as well as laser-trimmed thin film resistors. PMI invented the "zener-zapping" technique to trim offset errors at the wafer level. This error correction method was designed to provide stable offset reduction and high reliability for maximum in-circuit cost/performance value. A low noise, low drift process combined with zener-zap trimming enables PMI to produce the industry's most innovative operational amplifier circuit designs. Included in this large selection are amplifiers representing the state-of-the-art in precision performance devices combining extremely high speed with excellent DC performance, as well as devices providing high precision at extremely low supply currents. Numerous amplifiers are also offered in space saving dual and quad versions where the use of standard pin-outs allows easy upgrading of existing designs without circuit or PC board modification.

The table below summarizes PMI's operational amplifier families. All devices feature low input offset voltage, low drift, and high open-loop gain.

Operational Amplifiers

- General Purpose Bipolar

SINGLE

OP-02	Improved General Purpose
OP-01	High Speed Inverting

DUAL

OP-04/14	Matched, 8-Pin
----------	----------------

QUAD

OP-09/11	High Gain
PM148	High Gain

- General Purpose JFET

SINGLE

PM-155/156/157	
JM-38510/11401-6	JAN versions

- Precision High Speed Improved JFET

SINGLE

OP-15/16/17	Low V_{OS} , Fast
OP-41	Low I_B , High Stability
OP-42	High Speed
OP-43	Low I_B , Medium Speed
OP-44	Very High Speed

DUAL

OP-215	Dual OP-15
--------	------------

- Wide Bandwidth, High Speed

SINGLE

OP-42	High Speed
OP-44	Very High Speed
OP-62	High Bandwidth, Precision
OP-63	High Speed, High Bandwidth
OP-64	Very High Speed, High Bandwidth
OP-65	SuperFast, Very High Bandwidth

DUAL

OP-260	SuperFast, Very High Bandwidth
--------	--------------------------------

- High Accuracy Bipolar

SINGLE

OP-05	Low V_{OS} , High Gain
OP-06	Low V_{OS} , High Gain
OP-08	Low V_{OS} , Low Noise
OP-12	Low V_{OS} , Low Noise
OP-50	Low V_{OS} , High Output Current

- Precision Bipolar

SINGLE

OP-07	High Gain, Low Noise
OP-77	High Gain, Low Noise
OP-97	High Gain, Low Noise
OP-27	Very Low Noise
OP-37 (Fast)	Very Low Noise
PM-1008	Low V_{OS}/I_B , High Gain
PM-1012	Low V_{OS}/I_B , High Gain

DUAL

OP-10	Low Offset
OP-207	Low Offset
OP-200	Dual OP-07/OP-77
OP-227	Low V_{OS} , Low Noise
OP-270	Low V_{OS} , Low Noise
OP-271	High Speed OP-270

- Precision Bipolar

QUAD	
OP-400	Quad OP-07/OP-77
OP-470	Low V_{OS} , Low Noise
OP-471 (Fast)	Low V_{OS} , Low Noise

- Low Power, Low Input Bias Current

SINGLE

PM-108/208/308	Industry STD
OP-08	Improved 108
OP-12	Compensated OP-08
PM-1008	Low I_B over Temp
PM-1012	Low I_B over Temp
OP-21	Low Power, Fast
OP-80	CMOS, Ultra Low I_B
OP-97	Precision, Low I_B Over Temp.

DUAL

OP-221	Dual OP-21
PM-2108	Dual 108

QUAD

OP-421	Quad OP-21
--------	------------

- Micropower, Single Supply Bipolar

SINGLE

OP-20	Precision, Very Low I_{SY}
OP-90	Precision, Very Low I_{SY}
OP-22	Programmable
OP-32	Programmable

DUAL

OP-220	Precision, Very Low I_{SY}
OP-290	Precision, Very Low I_{SY}

QUAD

OP-420	Very Low I_{SY}
OP-490	Very Low I_{SY}

DEFINITIONS

Average Bias Current Drift (TCI_B) — The ratio of change in input bias current to a change in temperature.

Average Offset Current Drift (TCI_{OS}) — The ratio of change in input offset current to a change in temperature.

Average Offset Voltage Drift (TCV_{OS}) — The ratio of change in input offset voltage to a change in temperature.

Average Offset Voltage Drift With External

Trimming (TCV_{OSN}) — The ratio of the change in input offset voltage to a change in temperature with the input offset voltage trimmed to zero at room temperature.

Common-Mode Input Resistance (R_{inCM})

— The ratio of input voltage range to the change in input bias current over this range.

Common-Mode Rejection Ratio (CMRR)

— The ratio of the common-mode voltage range (CMVR) to the peak-to-peak change in equivalent input offset voltage (CME) over this range. CMRR is specified for a specific CMVR. $CMRR = 20 \log_{10} (CMVR/CME)$

Gain-Bandwidth Product (GBW)

— The frequency at which the open-loop gain equals unity.

Input Bias Current (I_B) — The average of the currents into the two input terminals when the output is at zero volts with no load. I_B is measured at $V_{CM} = 0$.

Input Noise Current (I_{np-p}) — The peak-to-peak noise current within a specified frequency band.

Input Noise Current Density (i_n) — The rms noise current in a 1Hz band centered on a specified frequency.

Input Noise Voltage (e_{np-p}) — The peak-to-peak noise voltage within a specified frequency band.

Input Noise Voltage Density (e_n) — The rms noise voltage in a 1Hz band centered on a specified frequency.

Input Offset Current (I_{OS}) — The difference between the currents into the two input terminals when the output is at zero volts with no load.

Input Offset Voltage (V_{OS}) — The voltage which must be applied between the input terminals to obtain zero output voltage with no load.

Input Resistance-Differential Mode (R_{IN}) — The ratio of small-signal change in input voltage to a change in input current at either input terminal with the other grounded.



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Input Voltage Range (IVR) — The range of input voltage for which the device will operate as a linear amplifier.

Large-Signal Voltage Gain (A_{VO}) — The ratio of change in output voltage (over a specified range) to a change in input voltage.

Open-Loop Output Resistance (R_O) — The small-signal driving-point resistance of the output terminal with respect to ground at a specified quiescent DC output voltage and current.

Output Voltage Swing (V_O) — The peak output voltage that can be obtained without clipping into a specified load resistance.

Power Dissipation (P_d) — The total power dissipated in the amplifier with the output at zero volts with no load.

Power Supply Rejection Ratio (PSRR) — The inverse ratio of change in input offset voltage to a change in power supply voltage. PSRR can be specified in dB or $\mu V/V$.

Slew Rate (SR) — The ratio of a change in output voltage to the minimum time required to effect this change under large-signal drive conditions. Slew rate may be specified separately for positive and negative-going changes.

Supply Current (I_{SY}) — The current required from the power supply to operate the amplifier with no load and the output at zero volts.

Unity-Gain Closed-Loop Bandwidth (BW)

— The frequency at which the magnitude of the small-signal voltage gain of the amplifier, operated closed-loop as a unity-gain follower, is 3dB below unity.

MATCHING PARAMETER DEFINITIONS

Input Offset Voltage Match (ΔV_{OS}) — The difference between the offset voltages of side A and side B ($V_{OSA} - V_{OSB}$). If $V_{OSA} = V_{OSB}$, the net differential offset voltage at the output of the amplifier pair equals zero.

Input Offset Voltage Tracking ($TC\Delta V_{OS}$)

— The ratio of change in ΔV_{OS} to a change in temperature.

Average Noninverting Bias Current (I_{B+}) — The average of the side A and side B noninverting input bias currents:

$$\frac{I_{BA+} + I_{BB+}}{2}$$

Noninverting Input Offset Current (I_{OS+}) — The difference between the noninverting input bias currents of side A and side B; ($I_{BA+} - I_{BB+}$).

Inverting Input Offset Current (I_{OS-}) — The difference between the inverting input bias currents of side A and side B; ($I_{BA-} - I_{BB-}$).

Average Drift Of Noninverting Bias Current (TCI_{B+}) — The ratio of change in noninverting bias current to a change in temperature.

Average Drift of Noninverting Offset Current (TCI_{OS+}) — The ratio of change in noninverting offset current to a change in temperature.

Common-Mode Rejection-Ratio Match ($\Delta CMRR$) — The difference between the common-mode rejection ratios (expressed in volt/volt of side A and side B. $\Delta CMRR$ in dB = $20 \log_{10} (\Delta CMRR$ in volt/volt).

Power Supply Rejection-Ratio Match ($\Delta PSRR$) — The difference between the power supply rejection ratios (expressed in volt/volt) of side A and side B. $\Delta PSRR$ in dB = $20 \log_{10} (\Delta PSRR$ in volt/volt).

Channel Separation — The ratio of change in offset voltage of one channel to a change in output voltage in the second channel.

SELECTION PRINCIPLES

Selecting an operational amplifier can be a frustrating experience. The choice of circuit configuration, and of associated component values, interrelates to the choice of op amp for a given application. Op amps are specified as open-loop devices, but in a circuit application they generally have feedback applied. The designer must predict the closed-loop circuit performance as determined by his choice of op amp and choice of circuit configuration (and component tolerances). Detailed literature is available on circuit configurations to accomplish



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particular analog circuit functions using op amps. This Selection Guide gives recommended guidelines and a design strategy for selecting op amps to best meet your needs.

The first design steps are to:

1. Completely define the design objectives.

Input Signal — Determine the signal level, frequency content, and impedance of the input.

Accuracy Required — For linear amplification, this consists of limits for offset, gain error, and nonlinearity. Establish your bandwidth and slew rate needs. Distortion is often critical for audio use and fast settling may be essential in a data-conversion application.

Output Load — Op amps are sometimes called upon to drive long cables, storage capacitors, transformers, or other semiconductors. High-speed circuits generally require low-impedance feedback elements and the load is usually low impedance; therefore, relatively high output current drive is needed for high-speed circuits.

Environmental Conditions — Temperature range and power supply characteristics are very important factors. Power supply drain is often critical in battery-powered equipment, process control systems, and satellites. In addition, op-amp package type is generally dictated by environmental and cost factors. Another factor to consider is the *electrical environment*. Minimize accuracy degradation from unavoidable ground noise and power supply fluctuations by choosing an op amp with high CMRR and PSRR.

2. Use the published op-amp specifications and characterization graphs.

PMI provides comprehensive specification tables with well-defined test conditions for operation at 25°C and over specific temperature ranges. The "Typical Performance Curves" show the characteristic response of an op amp to variations in frequency, temperature, supply voltage, or load impedance. Since op amps often perform much better than indicated by their min/max specification limits, the designer may be tempted to ask for special selection to tighter

limits. Although sometimes necessary, special selection tends to be costly. A better strategy is to select a standard op amp that meets the application need on a worst-case basis. Careful initial selection of a high-performance standard op amp will provide predictable circuit performance on a continuing basis.

Selection Process

Operational amplifiers can be divided into four basic functional categories:

Category*	Primary Characteristics
General Purpose	"741" types.
High Accuracy	Low input offsets ($V_{OS} < 1\text{mV}$), high DC gain, high CMRR, and low noise.
High Speed	Optimized for high slew rate, high gain-bandwidth, and fast settling time.
Low Power, Wide Supply Range	Low supply drain ($I_{SY} < 1\text{mA}$), wide input and output voltage range. Includes micropower ($I_{SY} < 100\mu\text{A}$) units for battery operation.

* In many cases, dual and quad versions are available in the various categories.

There can be overlap between some categories, while others are mutually exclusive. For example, the PMI OP-97 covers both "High Accuracy" and "Low Power". However, "High Speed" and "Low Power" tend to be mutually exclusive; it is difficult to simultaneously optimize both speed and power.

Economics is another important dimension of the selection process. The "General Purpose" category is generally lowest in cost, but a "High Accuracy" op amp with low input-offset-voltage may be more cost effective if it eliminates the need for external trimming components. The PMI high-accuracy OP-77 is often used in place of general-purpose 741-types because of its low input-offset-voltage and high gain.

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AC Considerations

Consideration of AC requirements for an application is a good starting point in the op amp selection process. If high frequency ($GBW > 10\text{MHz}$, $SR > 10\text{V}/\mu\text{s}$) is the primary concern, then the choice quickly narrows down to the "High Speed" category.

Two factors will generally dictate the op amp choice:

1. The loop gain (excess of open-loop gain over closed-loop gain) must be sufficient at the highest frequency of interest. For example, if 1.0% accuracy at 10kHz is required when operating at closed-loop gain of 10, then the op amp must have an open-loop gain of at least 1000 at 10kHz ($10/1000 = 1\%$). When operating at high closed-loop gains, uncompensated op amps generally offer the advantage of better gain bandwidth product without a price/performance penalty.

2. Slew rate must be high enough to follow the fastest signal input without causing distortion or other anomalies. Slew-rate symmetry, linearity, and overload recovery should be considered. The detrimental effects of slew-rate limiting can be subtle; it is best to avoid trouble by choosing an op amp with at least a 20% safety margin in minimum slew-rate.

High speed implies a need for high output current. Applications such as audio amplifiers, active filters, DAC-output amplifiers, and fast integrators often require high output currents for driving feedback capacitors or low-impedance networks. Driving such capacitive loads as long cables or storage capacitors at high frequency requires high output currents.

OP-42, OP-44 have high slew rates and good settling times, OP-62, OP-63, OP-64, and OP-65 add high bandwidth to high slew rate.

DC Considerations

If the application requires a high closed-loop gain, choose a "High Accuracy" op amp. These op amps feature:

Low Input Offsets	
Low Input Offset Voltage	$V_{OS} \leq 1\text{mV}$, $TCV_{OS} \leq 2\mu\text{V}/^\circ\text{C}$
Low Input Bias Current	
— Bipolar Input Stage	$I_B \leq 100\text{nA}$ ($I_B \leq 10\text{nA}$ is desirable)
— JFET Input Stage	$I_B \leq 200\text{pA}$
— CMOS Input Stage	$I_B \leq 2\text{pA}$
High Open-Loop DC Gain	$A_{VOL} \geq 1,000,000$
High Common-Mode Rejection	$CMR \geq 100\text{dB}$
Low Input Noise at 100Hz	$e_n \leq 15\text{nV}/\sqrt{\text{Hz}}$

A leading op amp in the High-Accuracy category is the PMI OP-77 with these key specifications:

$$\begin{aligned}V_{OS} &\leq 25\mu\text{V} \\I_B &\leq \pm 2\text{nA}, I_{OS} \leq 2\text{nA} \\A_{VOL} &\geq 5,000,000 \\CMRR &\geq 114\text{dB} \\e_n &\leq 11\text{nV}/\sqrt{\text{Hz}} \text{ at } 1000\text{Hz}\end{aligned}$$

The OP-77 performs very well even at high closed-loop gains. For example, consider a noninverting configuration with a closed-loop gain of 100. Assume a signal source with a range of $\pm 0.1\text{V}$ and source impedance of $10\text{k}\Omega$. If the feedback resistances are chosen to be relatively low, then the maximum offset caused by input bias current will be 4.4nA ($I_B + I_{OS}/2 = 4.4\text{nA}$) multiplied by the $10\text{k}\Omega$ source resistance, or $44\mu\text{V}$. Total input offset, even without external offset nulling, will be less than $119\mu\text{V}$ (approximately 0.12% of full-scale). The effect of CMRR is negligible in this example; the $\pm 0.1\text{V}$ input



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divided by 110dB of common-mode rejection is only $0.3\mu\text{V}$ referred-to-input. Gain error factor is $1/(1 + A_{VCL}/A_{VOL})$, which is a gain error of approximately A_{VCL}/A_{VOL} . The DC gain error at A_{VCL} of 100 will be less than $100/5,000,000$, a 0.002%-of-full-scale gain error. The worst-case sum of offset and gain errors for this example is only 0.12% of full-scale, and is achieved without any external trimming of offset or gain.

Selection of a specific op-amp type within the High-Accuracy category is generally determined by impedance levels of the input signal and feedback elements. High impedances ($R_S > 10\text{k}\Omega$) imply a need for an op amp with low input bias currents. This need for low bias current can be met through use of CMOS or FET-input op amps, or by using bipolar-input op amps specifically designed for low input-bias-current.

The OP-41/43 JFET-input op amps have less than $\pm 5\text{pA}$ of input bias current, and the OP-15/16/17 JFET-input op amps have bias currents specified to within $\pm 50\text{pA}$. At high temperature, however, the input bias current for JFET-input op amps rises to a level which is typically 3 orders of magnitude higher than the room-temperature value. CMOS input types such as OP-80 have the lowest values of I_B .

The OP-07, OP-50, and OP-77 are bipolar op amps which have input bias cancellation circuitry that significantly reduces input-bias-current, and maintain low input-bias-current levels over temperature. For example, the OP-07/77 op amps have bias-current limits set at $\pm 4\text{nA}$ over the full Military temperature range. The OP-97 has a superbeta input stage which also provides very good high-temperature high-impedance operation ($I_B \leq 250\text{pA}$ at 125°C).

The OP-22/32 programmable micropower op amps have PNP input stages which also have very low input bias current over temperature. Their input-bias-current remains below 5nA over the full Military temperature range.

1. Design with low impedances — Using low impedances minimizes the effect of current noise flowing through the source impedance, reduces resistor thermal noise, and reduces stray pick-up of RF noise.

2. Restrict the system bandwidth — Noise outside the frequency range of interest can usually be attenuated by filtering. Block high-frequency power-supply noise from the signal path by use of decoupling capacitors at the op-amp supply inputs.

3. Select a low-noise op amp — Some op amps, such as the bipolar-input OP-27, are designed for minimum noise. The input stage current is set to a relatively high value which reduces input noise ($5.5\text{nV}/\sqrt{\text{Hz}}$ max at 10Hz). Output swing is increased to $\pm 10\text{V}$ into 600Ω to allow the use of low-impedance, low-noise feedback elements.

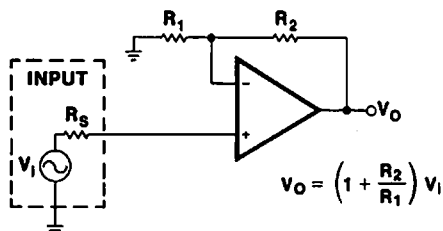
Power Supply Considerations

The op-amp power-supply requirements are the next factors to consider. If the circuit is to be operated from a battery, such as in portable instruments, missiles, or spacecraft, then narrow the selection to the "Low-Power, Wide Supply Range" category. Low-power op amps are designed for minimum quiescent supply current. Speed is traded off for lower power consumption and output drive is generally reduced. The input and output stages are designed for linear operation over a wide voltage range which is very helpful for single-power-supply operation. The PMI line of low-power, wide-supply-range op amps all feature high open-loop gain, low input offsets, and high CMRR. They can provide high accuracy even at high closed-loop gain.

The low-power family includes *programmable* micropower op amps that offer the designer another dimension in circuit design. The quiescent supply current is set by an external resistor which allows the circuit designer to trade off quiescent supply current against speed. Since the quiescent current directly controls slew rate and gain-bandwidth product, these programmable op amps are easily frequency-compensated in such circuits as active filters, oscillators, or multi-stage instrumentation amplifiers.

DC ERROR CALCULATIONS FOR STANDARD CONFIGURATIONS

NONINVERTING CONFIGURATION



$$\text{Output Offset} = \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \left(\frac{R_1 R_2}{R_1 + R_2} - R_S \right) I_B + \left(\frac{R_1 R_2}{R_1 + R_2} + R_S \right) \frac{I_{OS}}{2} \right]$$

Special Cases:

$$\text{Max Output Offset} = \left(1 + \frac{R_2}{R_1}\right) (V_{OS} + R_S I_{OS}) \text{ if } R_S = \frac{R_1 R_2}{R_1 + R_2}$$

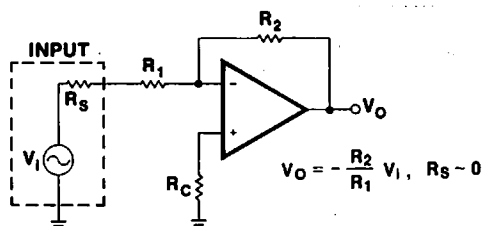
$$\sim \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \left| \frac{R_1 R_2}{R_1 + R_2} - R_S \right| I_B \right] \text{ if } I_{OS} \ll I_B$$

$$\sim \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + R_S \left(I_B + \frac{I_{OS}}{2} \right) \right] \text{ if } R_S \gg \frac{R_1 R_2}{R_1 + R_2}$$

Note: I_B is the average of the input bias currents and I_{OS} is the difference.

$$\text{Gain Error} \sim \left(1 + \frac{R_2}{R_1}\right) \frac{1}{A_{VO}} + \frac{1}{CMRR}, \text{ where } A_{VO} = \text{Open-Loop Gain and } A_{VO} \gg \left(1 + \frac{R_2}{R_1}\right)$$

INVERTING CONFIGURATION



$$\text{Output Offset} = \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \left(\frac{R_1 R_2}{R_1 + R_2} - R_C \right) I_B + \left(\frac{R_1 R_2}{R_1 + R_2} + R_C \right) \frac{I_{OS}}{2} \right] \text{ if } R_S \sim 0$$

Special Cases:

$$\begin{aligned} \text{Max Output Offset} &= \left(1 + \frac{R_2}{R_1}\right) (V_{OS} + R_C I_{OS}) \text{ if } R_C = \frac{R_1 R_2}{R_1 + R_2} \\ &\sim \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \left| \frac{R_1 R_2}{R_1 + R_2} - R_C \right| I_B \right] \text{ if } I_{OS} \ll I_B \\ &\sim \left(1 + \frac{R_2}{R_1}\right) \left[V_{OS} + \frac{R_1 R_2}{R_1 + R_2} \left(I_B + \frac{I_{OS}}{2} \right) \right] \text{ if } R_C = 0 \end{aligned}$$

Note: I_B is the average of the input bias currents and I_{OS} is the difference.

$$\text{Gain Error} \sim \left(1 + \frac{R_2}{R_1}\right) \frac{1}{A_{VO}} + \frac{R_S}{R_1} \frac{R_2}{R_1}, \text{ where } A_{VO} = \text{Open-Loop Gain and } R_S \ll R_1$$



OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

OPERATIONAL AMPLIFIER SELECTION GUIDE Low Offset Voltage Operational Amplifiers

Product	V _{os} μV	I _b nA	I _{os} nA	CMR dB	PSRR μV/V	A _{vo} V/mV	SR V/μs	GBW MHz
OP07	25	2	2	110	10	300	0.1	0.6
OP27	25	40	35	114	10	1000	1.7	8
OP37	25	40	35	114	10	1000	11	63
OP50	25	5	1	126	0.5	10000	2.5	15
OP77	25	2	1.5	120	3	5000	0.1	0.6
OP97	25	0.1	0.1	114	2	300	0.1	0.6
PM1012	35	0.1	0.1	114	2	300	0.1	0.6
OP270	50	10	10	110	1.8	1000	1.4	6
OP200	75	2	1	120	1.8	5000	0.1	0.5
OP227	80	40	35	114	10	1000	1.7	8
OP207	100	3	2.8	106	20	200	—	0.6
OP21	100	100	4	100	6	1000	—	0.6
PM1008	120	0.1	0.1	114	2	200	0.1	0.9
OP05	150	2	2	114	10	300	0.1	0.6
OP08	150	2	0.2	104	7	80	—	—
OP12	150	2	0.2	104	7	80	—	0.8
OP220	150	20	1.5	95	10	1000	—	0.2
OP221	150	80	3	95	10	1500	0.2	0.6
OP290	150	15	3	100	5.6	700	0.005	0.02
OP400	150	3	1	120	1.8	5000	0.1	0.5
OP90	150	15	3	100	5.6	700	0.005	0.02
OP06	200	70	2	114	2	1000	—	—
OP62	200	300	100	110	5.6	350	15	50
OP20	250	25	1.5	100	6	1000	—	0.1
OP41	250	0.005	0.001	100	25	1000	1	0.5
OP43	250	0.005	0.001	100	25	1000	5	2.5



OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

Low Offset Voltage Operational Amplifiers

Product	I_{SV} mA	$e_n@10\text{Hz}$ nV/ $\sqrt{\text{Hz}}$	$e_n@1\text{kHz}$ nV/ $\sqrt{\text{Hz}}$	I_{OUT} mA	# of Amps	Notes
OP07	4	10.3	9.6	10.5	1	1
OP27	4.7	3.5	3	16.7	1	1
OP37	4.7	3.5	3	16.7	1	1,4
OP50	3.3	5.5	4.5	60	1	2,4,6
OP77	2	10.3	9.6	12	1	1
OP97	0.6	17	14	5	1	1,9
PM1012	0.6	17	14	5	1	1
OP270	2.5	2.6	2.0	6	2	1,9
OP200	0.725	22	11	5.5	2	1
OP227	4.7	3.5	3	16.7	2	2
OP207	4	10.3	9.6	10	2	2
OP21	0.23	—	—	1.4	1	1
PM1008	0.6	17	14	5	1	1,6
OP05	4	10.3	9.6	10.5	1	1
OP08	0.6	22	20	5	1	1,6
OP12	0.6	22	20	5	1	1
OP220	0.09	—	—	0.56	2	1,7
OP221	0.4	—	—	1.4	2	1
OP290	0.02	60	60	5.5	2	2,7,9
OP400	0.725	22	11	5.5	4	2
OP90	0.02	60	60	5.5	1	1,7
OP06	4	9	7	11	1	1,6
OP62	7	—	2.5	20	1	1,9
OP20	0.055	—	—	0.56	1	1,7
OP41	1	—	32	12	1	1
OP43	1	—	32	12	1	1

NOTES:

1. 8 pin package
2. 14 pin package
3. 16 pin package
4. $Av_{CL} \geq 5$
5. $Av_{CL} \geq 10$
6. Externally compensated
7. Single-supply capable
8. Programmable supply current
9. Preliminary specifications
10. $Av_{CL} \geq 3$

OPERATIONAL AMPLIFIERS

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OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

Low Bias Current Operational Amplifiers

Product	V _{os} μV	I _b nA	I _{os} nA	CMR dB	PSRR μV/V	A _{vo} V/mV	SR V/μs	GBW MHz
OP80	1000	0.00006	—	72	700	100	0.2	0.3
OP41	500	0.005	0.001	100	25	1000	1	0.5
OP43	250	0.005	0.001	100	25	1000	5	2.5
OP15	500	0.05	0.01	86	51	100	10	6
OP16	500	0.05	0.01	86	51	100	18	8
OP17	500	0.05	0.01	86	51	100	45	30
PM155A	2000	0.05	0.01	85	57	50	3	2.5
PM156A	2000	0.05	0.01	85	57	50	10	4.5
PM157A	2000	0.05	0.01	85	57	50	40	20
OP215	1000	0.1	0.05	86	51	150	10	5.7
OP97	25	0.1	0.1	114	2	300	0.1	0.6
PM1008	120	0.1	0.1	114	2	200	0.1	0.9
PM1012	35	0.1	0.1	114	2	300	0.1	0.6
OP42	750	0.2	0.04	88	40	500	50	10
OP44	750	0.2	0.04	86	40	500	100	23

Low-Noise Operational Amplifiers

Product	V _{os} μV	I _b nA	I _{os} nA	CMR dB	PSRR μV/V	A _{vo} V/mV	SR V/μs	GBW MHz
OP270	50	10	10	110	1.8	1000	1.4	6
OP27	25	40	35	114	10	1000	1.7	8
OP227	80	40	35	114	10	1000	1.7	8
OP37	25	40	35	114	10	1000	11	63
OP62	200	300	100	110	5.6	350	15	50
OP470	400	25	10	110	1.8	1000	1.4	6
OP50	25	5	1	126	0.5	10000	2.5	15
OP271	300	10	10	110	5.6	1000	6.5	6.5
OP471	800	25	10	105	5.6	500	6.5	6.5
OP64	750	300	100	110	10	100	200	200
OP63	750	300	100	110	10	100	50	50



OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

Low Bias Current Operational Amplifiers

Product	I_{SY} mA	$e_n@10\text{Hz}$ nV/ $\sqrt{\text{Hz}}$	$e_n@1\text{kHz}$ nV/ $\sqrt{\text{Hz}}$	I_{OUT} mA	# of Amplis	Notes
OP80	0.2	—	70	10	1	1,9
OP41	1	—	32	12	1	1
OP43	1	—	32	12	1	1,4
OP15	4	—	15	5.5	1	1
OP16	7	—	15	5.5	1	1
OP17	7	—	15	5.5	1	1,4
PM155A	4	—	20	5	1	1
PM156A	7	—	12	5	1	1
PM157A	7	—	12	5	1	1,4
OP215	4.25	—	15	5.5	2	1,2
OP97	0.6	17	14	5	1	1,9
PM1008	0.6	17	14	5	1	1,6
PM1012	0.6	17	14	5	1	1
OP42	6	38	13	20	1	1
OP44	7	38	13	20	1	1,10

Low-Noise Operational Amplifiers

Product	I_{SY} mA	$e_n@10\text{Hz}$ nV/ $\sqrt{\text{Hz}}$	$e_n@1\text{kHz}$ nV/ $\sqrt{\text{Hz}}$	I_{OUT} mA	# of Amplis	Notes
OP270	2.5	2.6	2.0	6	2	1,9
OP27	4.7	3.5	3	16.7	1	1
OP227	4.7	3.5	3	16.7	2	2
OP37	4.7	3.5	3	16.7	1	1,4
OP62	7	—	2.5	20	1	1,9
OP470	2.75	3.8	3.2	6	4	2
OP50	3.3	5.5	4.5	60	1	2,4,6
OP271	2.5	9	6.5	6	2	1,9
OP471	2.75	9	6.5	6	4	2
OP64	7	—	7	20	1	1,4,9
OP63	7	—	7	20	1	1,9

NOTES:

1. 8 pin package
2. 14 pin package
3. 16 pin package
4. $A_{VCL} \geq 5$
5. $A_{VCL} \geq 10$
6. Externally compensated
7. Single-supply capable
8. Programmable supply current
9. Preliminary specifications
10. $A_{VCL} \geq 3$

OPERATIONAL AMPLIFIERS

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OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

Wideband Operational Amplifiers

Product	V _{OS} μV	I _b nA	I _{OS} nA	CMR dB	PSRR μV/V	A _{VO} V/mV	SR V/μs	GBW MHz
OP260	8000	400	—	50	1000	25	200	500
OP06	200	70	2	114	2	1000	—	—
OP64	750	300	100	110	10	100	200	200
OP65	2000	2500	2000	85	32	100	200	150
OP37	25	40	35	114	10	1000	11	63
OP63	750	300	100	110	10	100	50	50
OP62	200	300	100	110	5.6	350	15	50
OP17	500	0.05	0.01	86	51	100	45	30
OP44	750	0.2	0.04	86	40	500	100	23
PM157A	2000	0.05	0.01	85	57	50	40	20
OP50	25	5	1	126	0.5	10000	2.5	15
OP42	750	0.2	0.04	88	40	500	50	10
OP32	300	—	—	100	6	1000	—	—
OP16	500	0.05	0.01	86	51	100	18	8
OP227	80	40	35	114	10	1000	1.7	8
OP27	25	40	35	114	10	1000	1.7	8
OP271	300	10	10	110	5.6	1000	6.5	6.5
OP471	800	25	10	105	5.6	500	6.5	6.5
OP15	500	0.05	0.01	86	51	100	10	6
OP270	50	10	10	110	1.8	1000	1.4	6
OP470	400	25	10	110	1.8	1000	1.4	6

Low Power Operational Amplifiers

Product	V _{OS} μV	I _b nA	I _{OS} nA	CMR dB	PSRR μV/V	A _{VO} V/mV	SR V/μs	GBW MHz
OP22	300	—	—	100	6	1000	—	—
OP32	300	—	—	100	6	1000	—	—
OP290	150	15	3	100	5.6	700	0.005	0.02
OP490	500	15	3	100	5.6	700	0.005	0.02
OP90	150	15	3	100	5.6	700	0.005	0.02
OP20	250	25	1.5	100	6	1000	—	0.1
OP220	150	20	1.5	95	10	1000	—	0.2
OP420	2500	20	1.5	83	30	600	—	0.15
OP80	1000	0.00006	—	72	700	100	0.2	0.3
OP21	100	100	4	100	6	1000	—	0.6
OP221	150	80	3	95	10	1500	0.2	0.6
OP421	2500	50	5	83	30	200	0.25	1.9
OP08	150	2	0.2	104	7	80	—	—
OP12	150	2	0.2	104	7	80	—	0.8
OP97	25	0.1	0.1	114	2	300	0.1	0.6
PM1008	120	0.1	0.1	114	2	200	0.1	0.6
PM1012	35	0.1	0.1	114	2	300	0.1	0.6
PM108	500	2	0.2	96	15	80	—	—
PM2108	500	2	0.2	96	15	80	—	—
OP200	75	2	1	120	1.8	5000	0.1	0.5
OP400	150	3	1	120	1.8	5000	0.1	0.5
OP41	250	0.005	0.001	100	25	1000	1	0.5
OP43	250	0.005	0.001	100	25	1000	5	2.5



OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

Wideband Operational Amplifiers

Product	I_{SV} mA	$e_n@10\text{Hz}$ nV/ $\sqrt{\text{Hz}}$	$e_n@1\text{kHz}$ nV/ $\sqrt{\text{Hz}}$	I_{OUT} mA	# of Ampl	Notes
OP260	5.5	—	7	20	2	1,9
OP06	4	9	7	11	1	1,6
OP64	7	—	7	20	1	1,4,9
OP65	25	—	—	50	1	1,9
OP37	4.7	3.5	3	16.7	1	1,4
OP63	7	—	7	20	1	1,9
OP62	7	—	2.5	20	1	1,9
OP17	7	—	15	5.5	1	1,4
OP44	7	38	13	20	1	1,10
PM157A	7	—	12	5	1	1,4
OP50	3.3	5.5	4.5	60	1	2,4,6
OP42	6	38	13	20	1	1
OP32	—	—	—	—	1	1,5,8
OP16	7	—	15	5.5	1	1
OP227	4.7	3.5	3	16.7	2	2
OP27	4.7	3.5	3	16.7	1	1
OP271	2.5	9	6.5	6	2	1,9
OP471	2.75	9	6.5	6	4	2
OP15	4	—	15	5.5	1	1
OP270	2.5	2.6	2.0	6	2	1,9
OP470	2.75	3.8	3.2	6	4	2

Low Power Operational Amplifiers

Product	I_{SV} mA	$e_n@10\text{Hz}$ nV/ $\sqrt{\text{Hz}}$	$e_n@1\text{kHz}$ nV/ $\sqrt{\text{Hz}}$	I_{OUT} mA	# of Ampl	Notes
OP22	—	—	—	—	1	1,8
OP32	—	—	—	—	1	1,5,8
OP290	0.02	60	60	5.5	2	1,7,9
OP490	0.02	60	60	5	4	2,7
OP90	0.02	60	60	5.5	1	1,7
OP20	0.055	—	—	0.56	1	1,7
OP220	0.09	—	—	0.56	2	1,7
OP420	0.09	—	—	0.56	4	2,7
OP80	0.2	—	70	10	1	1,7,9
OP21	0.23	—	—	1.4	1	1
OP221	0.4	—	—	1.4	2	1
OP421	0.45	20	15	1.4	4	2
OP08	0.6	22	20	5	1	1,6
OP12	0.6	22	20	5	1	1
OP97	0.6	17	14	5	1	1,9
PM1008	0.6	17	14	5	1	1,6
PM1012	0.6	17	14	5	1	1
PM108	0.6	—	—	1.3	1	1,6
PM2108	0.6	—	—	1.3	2	3,6
OP200	0.725	22	11	5.5	2	1
OP400	0.725	22	11	5.5	4	2
OP41	1	—	32	12	1	1
OP43	1	—	32	12	1	1

OPERATIONAL AMPLIFIERS

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OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

High Slew-Rate Operational Amplifiers

Product	V _{OS} μV	I _b nA	I _{OS} nA	CMR dB	PSRR μV/V	A _{VO} V/mV	SR V/μs	GBW MHz
OP260	8000	400	—	50	1000	25	200	500
OP65	2000	2500	2000	85	32	100	200	150
OP64	750	300	100	110	10	100	200	200
OP44	750	0.2	0.04	86	40	500	100	23
OP06	200	70	2	114	2	1000	—	—
OP42	750	0.2	0.04	88	40	500	50	10
OP63	750	300	100	110	10	100	50	50
OP17	500	0.05	0.01	86	51	100	45	30
PM157A	2000	0.05	0.01	85	57	50	40	20
OP16	500	0.05	0.01	86	51	100	18	8
OP62	200	300	100	110	5.6	350	15	50
OP01	700	30	2	85	60	50	12	2.5
OP37	25	40	35	114	10	1000	11	63
OP15	500	0.05	0.01	86	51	100	10	6
OP215	1000	0.1	0.05	86	51	150	10	5.7
PM156A	2000	0.05	0.01	85	57	50	10	4.5
OP271	300	10	10	110	5.6	1000	6.5	6.5
OP471	800	25	10	105	5.6	500	6.5	6.5
OP43	250	0.005	0.001	100	25	1000	5	2.5

8-Pin Dual Operational Amplifiers

Product	V _{OS} μV	I _b nA	I _{OS} nA	CMR dB	PSRR μV/V	A _{VO} V/mV	SR V/μs	GBW MHz
OP270	50	10	10	110	1.8	1000	1.4	6
OP200	75	2	1	120	1.8	5000	0.1	0.5
OP220	150	20	1.5	95	10	1000	—	0.2
OP221	150	80	3	95	10	1500	0.2	0.6
OP290	150	15	3	100	5.6	700	0.005	0.02
OP271	300	10	10	110	5.6	1000	6.5	6.5
OP14	750	50	5	85	60	100	0.25	1.3
OP215	1000	0.1	0.05	86	51	150	10	5.7
OP260	8000	400	—	50	1000	25	200	500



OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

High Slew-Rate Operational Amplifiers

Product	I _{SY} mA	e _n @10Hz nV/√Hz	e _n @1kHz nV/√Hz	I _{OUT} mA	# of Ampl	Notes
OP260	5.5	—	7	20	2	1,9
OP65	25	—	—	50	1	1,9
OP64	7	—	7	20	1	1,4,9
OP44	7	38	13	20	1	1,10
OP06	4	9	7	11	1	1,6
OP42	6	38	13	20	1	1
OP63	7	—	7	20	1	1,9
OP17	7	—	15	5.5	1	1,4
PM157A	7	—	12	5	1	1,4
OP16	7	—	15	5.5	1	1
OP62	7	—	2.5	20	1	1,9
OP01	3	—	—	6	1	1
OP37	4.7	3.5	3	16.7	1	1,4
OP15	4	—	15	5.5	1	1
OP215	4.25	—	15	5.5	2	1,2
PM156A	7	—	12	5	1	1
OP271	2.5	9	6.5	6	2	1,9
OP471	2.75	9	6.5	6	4	2
OP43	1	—	32	12	1	1,4

8-Pin Dual Operational Amplifiers

Product	I _{SY} mA	e _n @10Hz nV/√Hz	e _n @1kHz nV/√Hz	I _{OUT} mA	# of Ampl	Notes
OP270	2.5	2.6	2.0	6	2	1,9
OP200	0.725	22	11	5.5	2	1
OP220	0.09	—	—	0.56	2	1,7
OP221	0.4	—	—	1.4	2	1
OP290	0.02	60	60	5.5	2	1,7,9
OP271	2.5	9	6.5	6	2	1,9
OP14	3	25	21	6	2	1
OP215	4.25	—	15	5.5	2	1,2
OP260	5.5	—	7	20	2	1,9

NOTES:

1. 8 pin package
2. 14 pin package
3. 16 pin package
4. A_{VCL} ≥ 5
5. A_{VCL} ≥ 10
6. Externally compensated
7. Single-supply capable
8. Programmable supply current
9. Preliminary specifications
10. A_{VCL} ≥ 3

OPERATIONAL AMPLIFIERS

5



OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

14-Pin Quad Operational Amplifiers

Product	V _{OS} μV	I _b nA	I _{OS} nA	CMR dB	PSRR μV/V	A _{VO} V/mV	SR V/μs	GBW MHz
OP400	150	3	1	120	1.8	5000	0.1	0.5
OP470	400	25	10	110	1.8	1000	1.4	6
OP09	500	300	20	100	32	100	0.7	3
OP11	500	300	20	100	32	100	0.7	3
OP490	500	15	3	100	5.6	700	0.005	0.02
OP471	800	25	10	105	5.6	500	6.5	6.5
OP420	2500	20	1.5	83	30	600	—	0.15
OP421	2500	50	5	83	30	200	0.25	1.9

14 & 16 Pin Dual Operational Amplifiers

Product	V _{OS} μV	I _b nA	I _{OS} nA	CMR dB	PSRR μV/V	A _{VO} V/mV	SR V/μs	GBW MHz
OP227	80	40	35	114	10	1000	1.7	8
OP207	100	3	2.8	106	20	200	—	0.6
OP10	500	3	2.8	110	10	200	—	0.6
PM2108	500	2	0.2	96	15	80	—	—
OP04	750	50	5	85	60	100	0.25	1.3
OP215	1000	0.1	0.05	86	51	150	10	5.7
PM747	5000	500	200	70	150	50	—	—



OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

14-Pin Quad Operational Amplifiers

Product	I_{SY} mA	$e_n@10\text{Hz}$ nV/ $\sqrt{\text{Hz}}$	$e_n@1\text{kHz}$ nV/ $\sqrt{\text{Hz}}$	I_{OUT} mA	# of Ampl	Notes
OP400	0.725	22	11	5.5	4	2
OP470	2.75	3.8	3.2	6	4	2
OP09	1.5	18	12	5.5	4	2
OP11	1.5	18	12	5.5	4	2
OP490	0.02	60	60	5	4	2,7
OP471	2.75	9	6.5	6	4	2
OP420	0.09	—	—	0.56	4	2,7
OP421	0.45	20	15	1.4	4	2

5

14 & 16 Pin Dual Operational Amplifiers

Product	I_{SY} mA	$e_n@10\text{Hz}$ nV/ $\sqrt{\text{Hz}}$	$e_n@1\text{kHz}$ nV/ $\sqrt{\text{Hz}}$	I_{OUT} mA	# of Ampl	Notes
OP227	4.7	3.5	3	16.7	2	2
OP207	4	10.3	9.6	10	2	2
OP10	4	10.3	9.6	10.5	2	2
PM2108	0.6	—	—	1.3	2	6,8
OP04	3	25	21	6	2	2
OP215	4.25	—	15	5.5	2	1,2
PM747	2.8	—	—	5	2	2

NOTES:

1. 8 pin package
2. 14 pin package
3. 16 pin package
4. $A_{VCL} \geq 5$
5. $A_{VCL} \geq 10$
6. Externally compensated
7. Single-supply capable
8. Programmable supply current
9. Preliminary specifications
10. $A_{VCL} \geq 3$

OPERATIONAL AMPLIFIERS



OP-01

INVERTING HIGH-SPEED OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Fast Settling Time $1\mu\text{s}$ to 0.1% Max
- High Slew Rate $12\text{V}/\mu\text{s}$ Min
- Power Bandwidth 150kHz Min
- Low Power Consumption 80mW Max
- Excellent DC Specifications
- Internally Compensated
- Ideal DAC Output Amplifier
- MIL-STD-883 Processing Available
- Fits Standard 741 Sockets
- Low Cost

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	
0.7	OP01J*	—	—	MIL
0.7	OP01HJ	OP01HZ	OP01HP	COM
5.0	OP01GJ	—	—	MIL
5.0	OP01CJ	OP01CZ	OP01CP	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

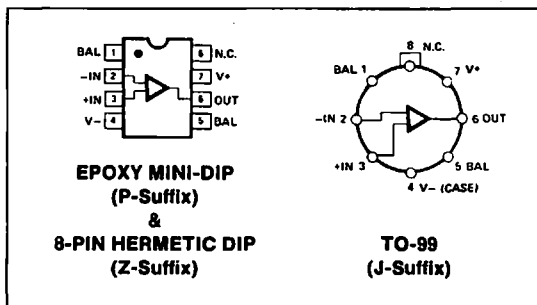
GENERAL DESCRIPTION

The OP-01 series of monolithic inverting high-speed operational amplifiers combines high slew rate, fast settling time

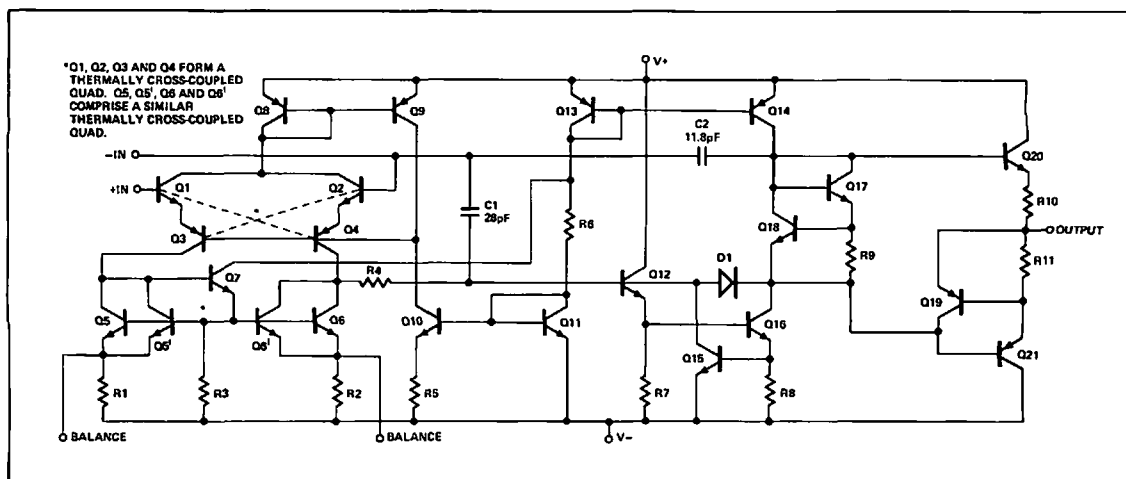
and excellent DC input characteristics. An internal feed-forward frequency compensation network provides simplicity of application — no external capacitors are required for stable, high-speed performance. The fast output response is achieved without sacrifice of input bias current or power consumption. A 250kHz typical power bandwidth is attained with a small-signal bandwidth of only 2.5MHz, thus board layout is non-critical. The OP-01 is completely protected at both input and output, fits standard 741 sockets, and is offset nulled with a $10\text{k}\Omega$ potentiometer.

The fast output response combined with excellent settling time makes the OP-01 ideal for use as a D/A converter output amplifier.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Total Supply Voltage, OP-01, OP-01H, OP-01N, OP-01NT, OP-01G, OP-01GT	±22V
OP-01G, OP-01C, OP-01GR	±20V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 3)	±15V
Short-Circuit Duration	Indefinite
Operating Temperature Range	
OP-01, OP-01G	-55°C to +125°C
OP-01H, OP-01C	0°C to +70°C
DICE Junction Temperature (T_j)	-65°C to +150°C
Storage Temperature Range	
J and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C

Lead Temperature (Soldering, 60 sec) 300°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TQ-89 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	35°C	5.6mW/°C

- Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

- For supply voltages less than ±15V, the maximum input voltage is the supply voltage.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-01 OP-01H			OP-01G OP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.7	—	2.0	5.0	mV
Input Offset Current	I_{OS}		—	0.5	2.0	—	2.0	20	nA
Input Bias Current	I_B		—	18	30	—	25	100	nA
Input Voltage Range	IVR		±12	±13	—	±12	±13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	100	150	$\mu V/V$
Output Voltage Swing	V_O	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	±12.5 ±12.0	±13.5 ±13.0	—	±12.5 ±12.0	±13.5 ±13.0	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	75	—	V/mV
Power Consumption	P_d	$V_{OUT} = 0$	—	50	90	—	50	90	mW
Settling Time to 0.1% (Summing Node Error)	t_s	$A_V = -1$ (Notes 1, 2) $V_{IN} = 5V$	—	0.7	1.0	—	0.7	1.0	μs
Slew Rate (Notes 2, 3)	SR	$A_V = -1$ $R_S = 3k$ to $5k\Omega$	12	18	—	12	18	—	V/ μs
Large-Signal Bandwidth (Notes 3, 4)			150	250	—	150	250	—	kHz
Small-Signal Bandwidth (Notes 3, 4)			1.5	2.5	—	1.5	2.5	—	MHz
Risetime	t_r	$A_V = -1$ $V_{IN} = 50mV$	—	150	—	—	150	—	ns
Overshoot	OS		—	2	—	—	2	—	%

NOTES:

- $R_L = 25k\Omega$; $C_L = 50pF$. See Settling Time Test Circuit.
- Sample tested.
- See applications information.
- Guaranteed by design.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-01, OP-01G and $0^\circ C \leq T_A \leq +70^\circ C$ for OP-01H, OP-01C, unless otherwise noted.

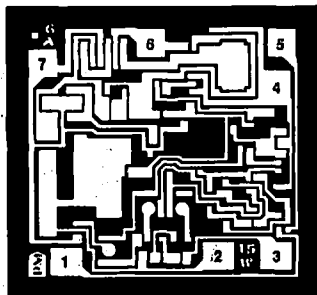
PARAMETER	SYMBOL	CONDITIONS	OP-01 OP-01H			OP-01G OP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.0	—	3.0	6.0	mV
Input Offset Current	I_{OS}		—	1	4	—	4	40	nA
Input Bias Current	I_B		—	30	50	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	110	—	80	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	30	60	—	15	50	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	± 12.5 ± 12.0	± 13.5 ± 13.0	—	± 12.5 ± 12.0	± 13.5 ± 13.0	—	V
Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S \leq 5k\Omega$	—	2	8	—	5	20	$\mu V/^\circ C$

NOTE:

1. Sample tested.



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)

DIE SIZE 0.047 × 0.043 inch, 2021 sq. mils
(1.19 × 1.09 mm, 1.30 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. NULL
6. OUTPUT
7. V₊

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-01N, OP-01G and OP-01GR devices; $T_A = 125^\circ C$ for OP-01NT and OP-01GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-01NT LIMIT	OP-01N LIMIT	OP-01GT LIMIT	OP-01G LIMIT	OP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	1.0	0.7	3.0	2.0	5.0	mV MAX
Input Offset Current	I_{OS}		4	2	10	5	20	nA MAX
Input Bias Current	I_B		50	30	100	50	100	nA MAX
Input Voltage Range	IVR		± 10	± 12	± 10	± 12	± 12	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	85	80	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	60	100	100	150	$\mu V/V$ MAX
Output Voltage Swing	V_{OM}	$R_L \geq 5k\Omega$ $R_L \geq 2k\Omega$	± 12.5 ± 12.0	± 12.5 ± 12.0	± 12.5 ± 12.0	± 12.5 ± 12.0	± 12.5 ± 12.0	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	30	50	25	50	25	V/mV MIN
Power Consumption	P_d	$V_{OUT} = 0$	—	90	—	90	90	mW MAX

NOTES:

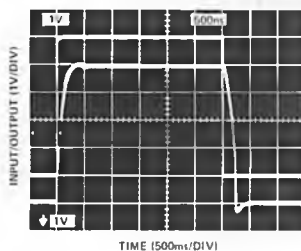
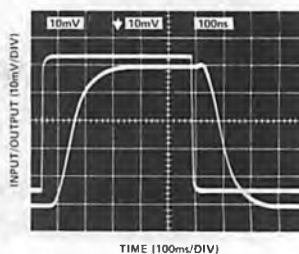
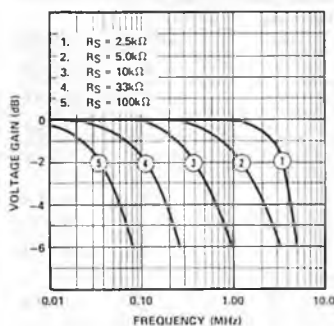
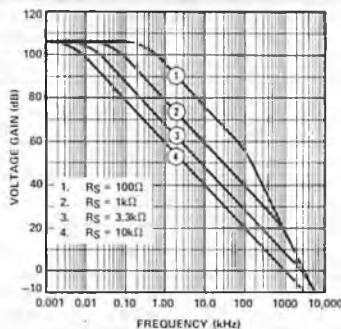
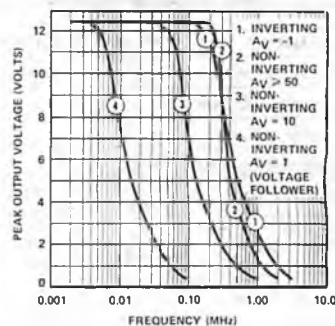
For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ALL GRADES TYPICAL	UNITS
Slew Rate	SR	$A_{VCL} = -1$, $R_S = 3k\Omega$ to $5k\Omega$	18	V/ μs
Settling Time to 0.1% (Summing Node Error)	t_s	$V_{IN} = 5V$ $A_V = -1$ $R_L = 2k\Omega$ (See Settling Time Test Circuit) $C_L = 50pF$	1.0	μs
Large-Signal Bandwidth			250	kHz
Small-Signal Bandwidth			2.5	MHz
Risetime	t_r	$V_{IN} = 50mV$ $A_V = -1$	150	ns

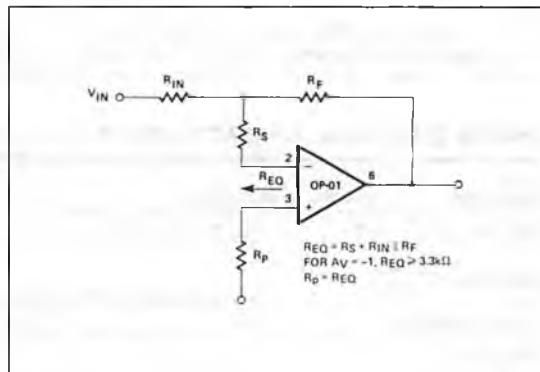
TYPICAL PERFORMANCE CHARACTERISTICS

LARGE-SIGNAL
PULSE RESPONSE
 $V_S = \pm 15V, A_V = -1, R_L = 2k\Omega, C_L = 50pF$
SMALL-SIGNAL
PULSE RESPONSE
 $V_S = \pm 15V, A_V = -1, R_L = 2k\Omega, C_L = 50pF$
UNITY-GAIN BANDWIDTH
vs SOURCE RESISTANCEOPEN-LOOP GAIN
vs FREQUENCYLARGE-SIGNAL OUTPUT
SWING vs FREQUENCY

APPLICATIONS INFORMATION

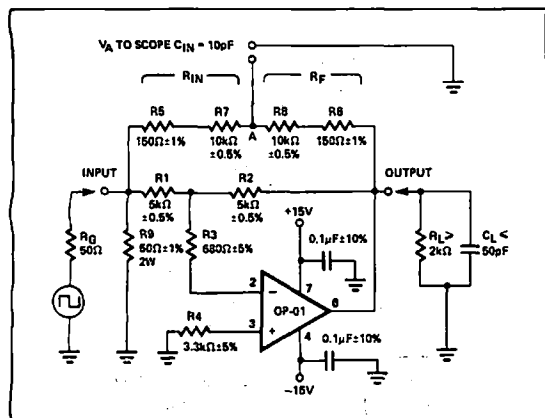
The OP-01 incorporates an internal feed-forward compensation network to provide fast slewing and settling times in all inverting and moderate-to-high-gain noninverting applications. Unity-gain bandwidth is a function of the total equivalent source resistance seen by the inverting terminal. Proper choice of this resistance will allow the user to maximize bandwidth while assuring proper stability. The equivalent-inverting-terminal-resistance is defined as $R_{IN} \parallel R_F$, and it must be greater than $3.3k\Omega$ to assure stability in all closed-loop gain configurations including unity gain. Should $R_{IN} \parallel R_F \leq 3.3k\Omega$, a resistor (R_S) may be placed between the inverting input and the sum node to provide the required resistance. (See Fast Inverting Amplifier Diagram.) Lower values of total equivalent resistance may be used to improve bandwidth in higher closed-loop gain configurations, as indicated by the Open-Loop Gain vs. Frequency plot.

FAST INVERTING AMPLIFIER

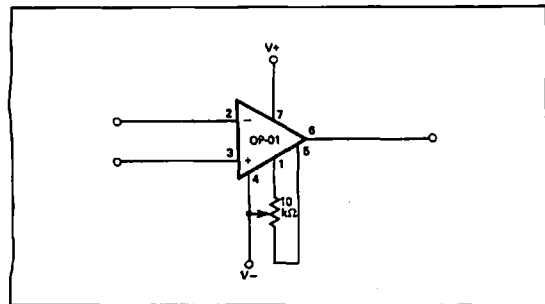


SETTLING-TIME TEST CIRCUIT

Settling time may be measured using the circuit shown below. This circuit incorporates the "false sum node" technique to produce accurate, repeatable results. For a 5V input step, 0.1% settling will be achieved when the false sum node settles to within $\pm 2.5\text{mV}$ of its final value. The oscilloscope used for observation of the false sum node should have wide bandwidth, fast overload recovery time, and be used with a low capacity probe ($\leq 10\text{pF}$, including strays). A Tektronix 7504 scope with a 7A11 probe or equivalent is suggested. The pulse generator should have a 50Ω output impedance and be capable of a 5V rise time in $\leq 20\text{ns}$ with ringing less than 2.5mV after $0.5\mu\text{s}$. Measurements to 0.1% require R_{IN} to equal R_F within 0.01%; R_5 and R_6 are used as trimming resistors to achieve this matching.

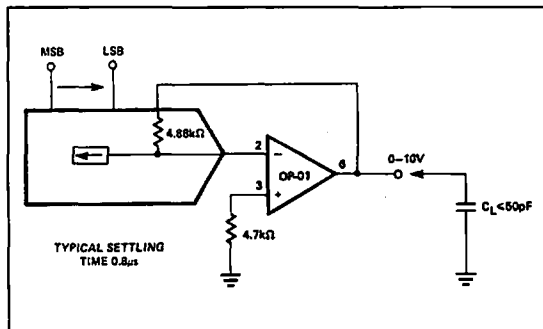


OFFSET NULLING CIRCUIT

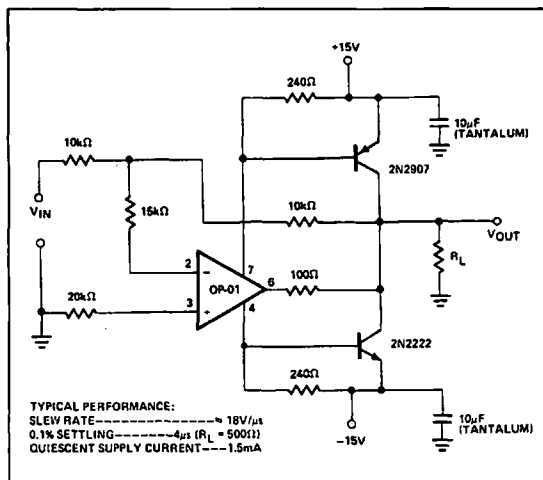


TYPICAL APPLICATIONS

FAST VOLTAGE-OUTPUT D/A CONVERTER



PRECISION POWER-BOOSTER CIRCUIT





OP-02

GENERAL-PURPOSE OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Excellent DC Specifications
- Low Noise $0.65\mu\text{V}_{\text{p-p}}$ Typ
- Low Drift (TCV_{OS}) $8\mu\text{V}/^\circ\text{C}$ Max
- Silicon-Nitride Passivation
- 125°C Tested Dice Available
- "Premium" 741 Replacement

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	
0.5	OP02AJ*	OP02AZ*	—	MIL
0.5	OP02EJ	OP02EZ	OP02EP	COM
2.0	OP02J*	OP02Z*	—	MIL
2.0	OP02CJ	OP02CZ	OP02CP	COM
5.0	OP02BJ*	—	—	MIL
5.0	—	—	OP02DP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1888 Data Book, Section 2.

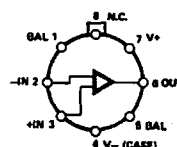
GENERAL DESCRIPTION

This high-performance general-purpose operational amplifier provides significant improvements over industry-standard and "premium" 741 types while maintaining pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS} , I_{OS} , I_{B} , CMRR, PSRR, and A_{VO} are

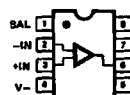
guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise." A thermally-symmetrical input-stage design provides low input offset voltage drift and insensitivity to output load conditions.

The OP-02 is a direct replacement for the 741. It is ideal for upgrading existing designs where accuracy improvements are required and for eliminating special low-drift or low-noise selected types.

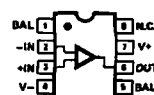
PIN CONNECTIONS



TO-99
(J-Suffix)

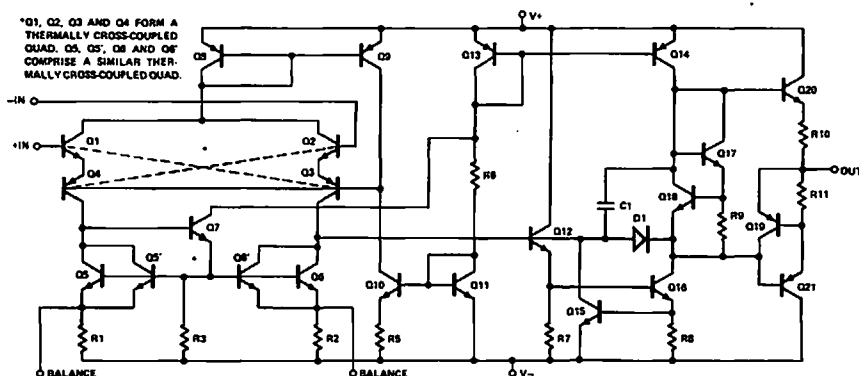


8-PIN HERMETIC DIP
(Z-Suffix)



EPOXY MINI-DIP
(P-Suffix)

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	±22V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
OP-02A, OP-02, OP-02B	-55°C to +125°C
OP-02E, OP-02C, OP-02D	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T _j)	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	38°C	5.6mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02A OP-02E			OP-02 OP-02C			OP-02B OP-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	R _S ≤ 20kΩ	—	0.3	0.5	—	1	2	—	3	5	mV
Input Offset Current	I _{OS}		—	0.5	2	—	1	5	—	5	25	nA
Input Bias Current	I _B		—	18	30	—	20	50	—	30	100	nA
Input Resistance-Differential-Mode	R _{IN}	(Note 2)	3.4	5.7	—	2.0	5.2	—	1	3.5	—	MΩ
Input Voltage Range	IVR		±10	±13	—	±10	±13	—	±10	±13	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±10V R _S ≤ 20kΩ	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ±5 to ±20V R _S ≤ 20kΩ	—	10	60	—	30	100	—	100	150	μV/V
Output Voltage Swing	V _O	R _L ≥ 2kΩ	±12	±13	—	±12	±13	—	±12	±13	—	V
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2kΩ V _O = ±10V	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption	P _d	V _O = 0V	—	40	70	—	50	90	—	50	90	mW
Input Noise Voltage	e _{np-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV _{p-p}
Input Noise Voltage Density	e _n	f _O = 10Hz	—	25	—	—	25	—	—	25	—	nV/√Hz
		f _O = 100Hz	—	22	—	—	22	—	—	22	—	
		f _O = 1000Hz	—	21	—	—	21	—	—	21	—	
Input Noise Current	I _{np-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA _{p-p}
Input Noise Current Density	I _n	f _O = 10Hz	—	1.4	—	—	1.4	—	—	1.4	—	pA/√Hz
		f _O = 100Hz	—	0.7	—	—	0.7	—	—	0.7	—	
		f _O = 1000Hz	—	0.4	—	—	0.4	—	—	0.4	—	
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/μs
Large-Signal Bandwidth		V _O = 20V _{p-p} (Notes 1, 4)	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth	BW	A _{VCL} = +1 (Note 3)	1	1.3	—	1	1.3	—	1	1.3	—	MHz
Risetime	t _r	A _{VCL} = +1 V _{IN} = 50mV (Note 1)	—	200	350	—	200	350	—	200	350	ns
Overshoot	OS	(Note 1)	—	5	10	—	5	10	—	5	10	%

NOTES:

1. Sample tested.
2. Guaranteed by input bias current.
3. Guaranteed by maximum risetime.
4. Guaranteed by minimum slew rate.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02A			OP-02			OP-02B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.5	1	—	1.4	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1	5	—	2	10	—	5	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	75	—	15	150	—	30	300	$pA/^\circ C$
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	95	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	25	60	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 10	± 13	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

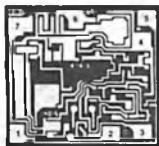
PARAMETER	SYMBOL	CONDITIONS	OP-02E			OP-02C			OP-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.7	4	—	1.4	10	—	5	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	$pA/^\circ C$
Input Bias Current	I_B		—	22	50	—	25	100	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	90	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 10	± 13	—	V

NOTE:

1. Sample tested.



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.047 × 0.043 inch, 2021 sq. mils
(1.19 × 1.09 mm, 1.30 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. NULL
6. OUTPUT
7. V₊

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-02N, OP-02G and OP-02GR devices; $T_A = 125^\circ C$ for OP-02NT and OP-02GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-02NT LIMIT	OP-02N LIMIT	OP-02GT LIMIT	OP-02G LIMIT	OP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	1	0.5	3	2	5	mV MAX
Input Offset Current	I_{OS}		5	3	6	5	25	nA MAX
Input Bias Current	I_B		50	30	60	50	200	nA MAX
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	85	80	80	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	60	100	100	150	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12	±12	±12	±12	±12	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	25	50	25	V/mV MIN
Power Consumption	P_d	$V_O = 0V$	—	90	—	90	90	mW MAX

NOTE:

For 25°C characteristics of NT and GT devices, see N and G characteristics, respectively.

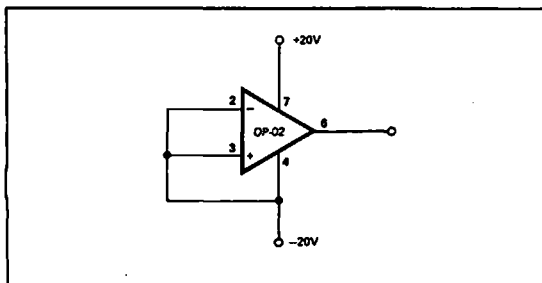
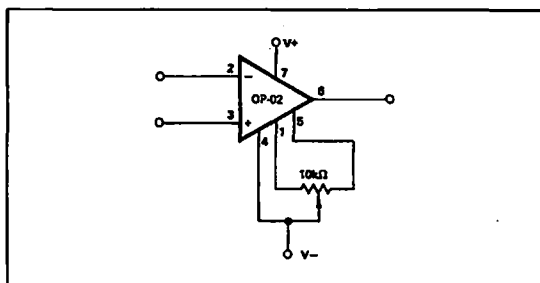
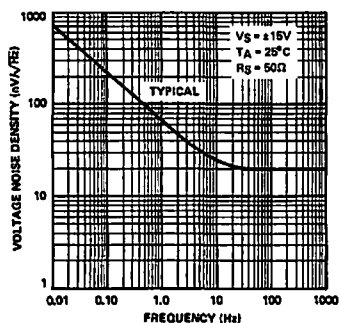
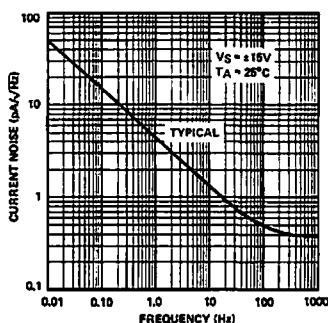
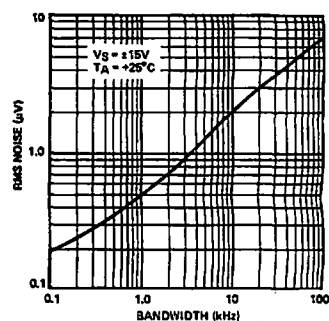
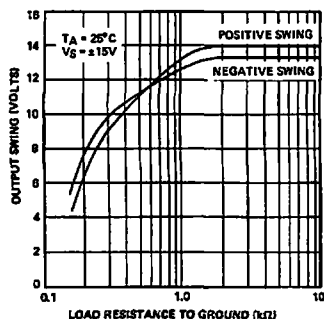
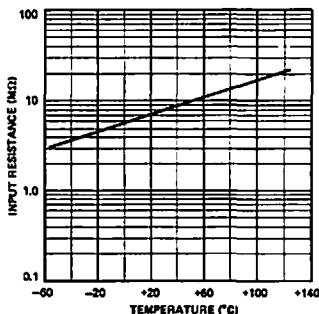
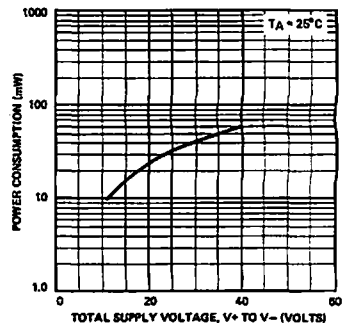
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

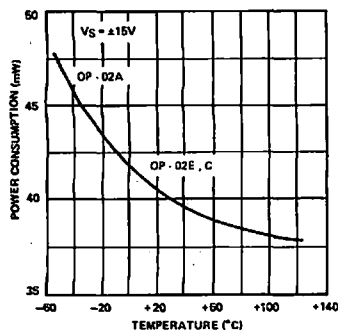
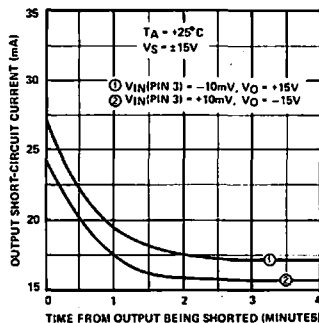
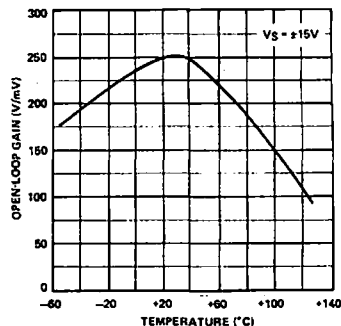
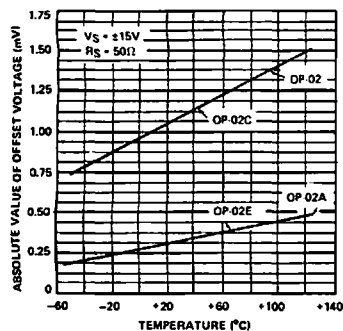
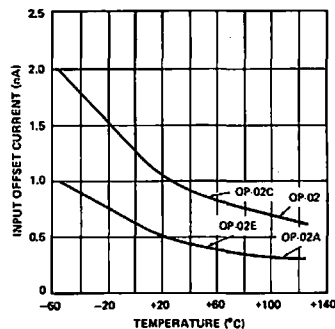
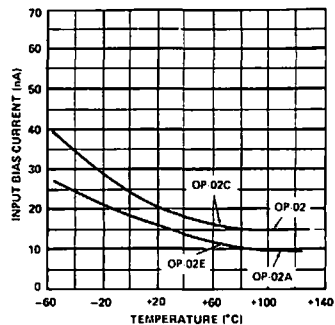
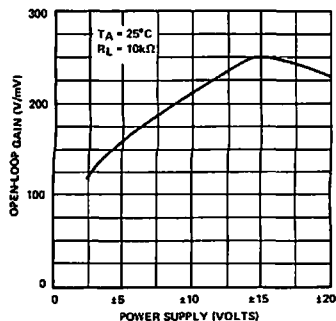
PARAMETER	SYMBOL	CONDITIONS	OP-02NT OP-02N TYPICAL	OP-02GT OP-02G TYPICAL	OP-02GR TYPICAL	UNITS
Input Resistance Differential-Mode	R_{IN}		5.7	5.2	3.5	M Ω
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	0.65	0.65	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	25	25	25	nV/ $\sqrt{Hz}$
		$f_O = 100Hz$	22	22	22	
		$f_O = 1000Hz$	21	21	21	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	12.8	12.8	12.8	pA _{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	1.4	1.4	1.4	pA/ $\sqrt{Hz}$
		$f_O = 100Hz$	0.7	0.7	0.7	
		$f_O = 1000Hz$	0.4	0.4	0.4	
Slew Rate	SR		0.5	0.5	0.5	V/ μs
Large-Signal Bandwidth		$V_O = 20V_{p-p}$	8	8	8	kHz
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	1.3	1.3	1.3	MHz
Risetime	t_r	$A_V = +1$ $V_{IN} = 50mV$	200	200	200	ns
Overshoot	OS		15	15	15	%
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 500\Omega$ (Note 1)	2	4	8	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		7.5	15	30	pA/ $^\circ C$

NOTE:

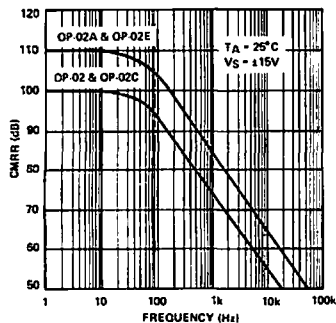
1. Sample tested.

BURN-IN CIRCUIT

OFFSET NULLING CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS
**INPUT SPOT NOISE
VOLTAGE vs FREQUENCY**

**INPUT SPOT NOISE
CURRENT vs FREQUENCY**

**INPUT WIDEBAND NOISE vs
BANDWIDTH (0.1Hz TO
FREQUENCY INDICATED)**

**OUTPUT VOLTAGE vs
LOAD RESISTANCE**

**DIFFERENTIAL
INPUT RESISTANCE
vs TEMPERATURE**

**POWER CONSUMPTION
vs POWER SUPPLY**


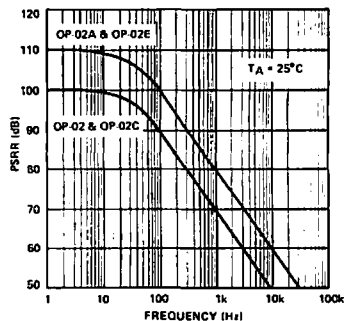
TYPICAL PERFORMANCE CHARACTERISTICS

 POWER CONSUMPTION
vs TEMPERATURE

 OUTPUT SHORT-CIRCUIT
CURRENT vs TIME

 OPEN-LOOP GAIN
vs TEMPERATURE

 UNTRIMMED OFFSET VOLTAGE
vs TEMPERATURE

 INPUT OFFSET CURRENT
vs TEMPERATURE

 INPUT BIAS CURRENT
vs TEMPERATURE

 OPEN-LOOP GAIN vs
POWER SUPPLY VOLTAGE


CMRR vs FREQUENCY

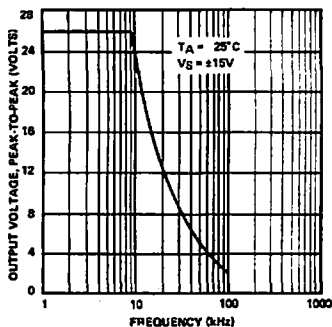


PSRR vs FREQUENCY

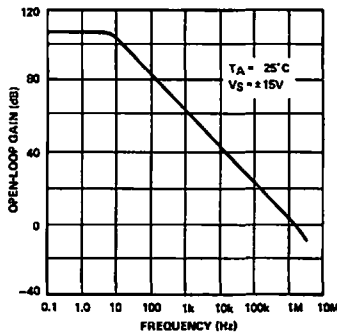


TYPICAL PERFORMANCE CHARACTERISTICS

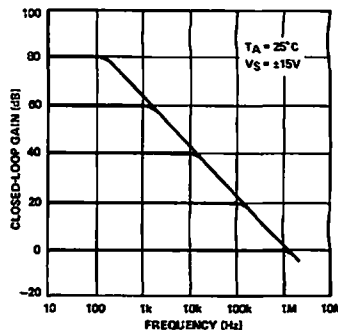
MAXIMUM UNDISTORTED
OUTPUT vs FREQUENCY



OPEN-LOOP
FREQUENCY RESPONSE

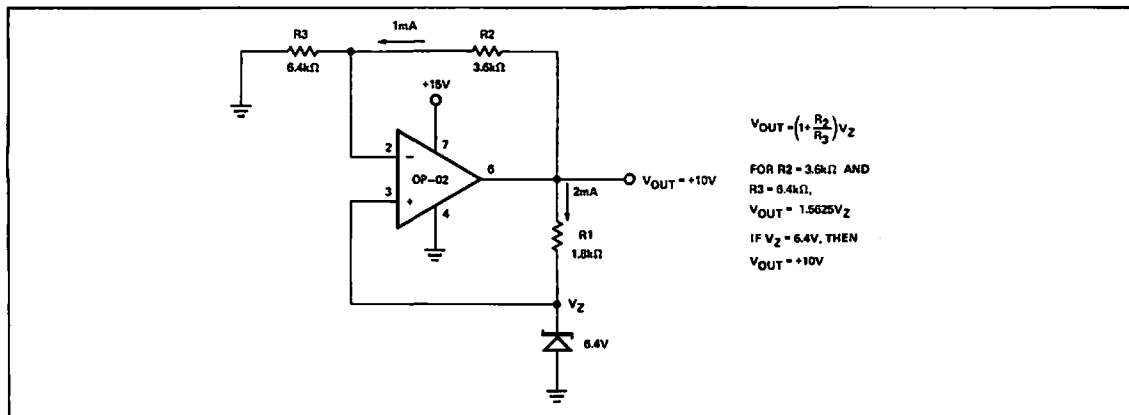


CLOSED-LOOP RESPONSE
FOR VARIOUS GAIN
CONFIGURATIONS

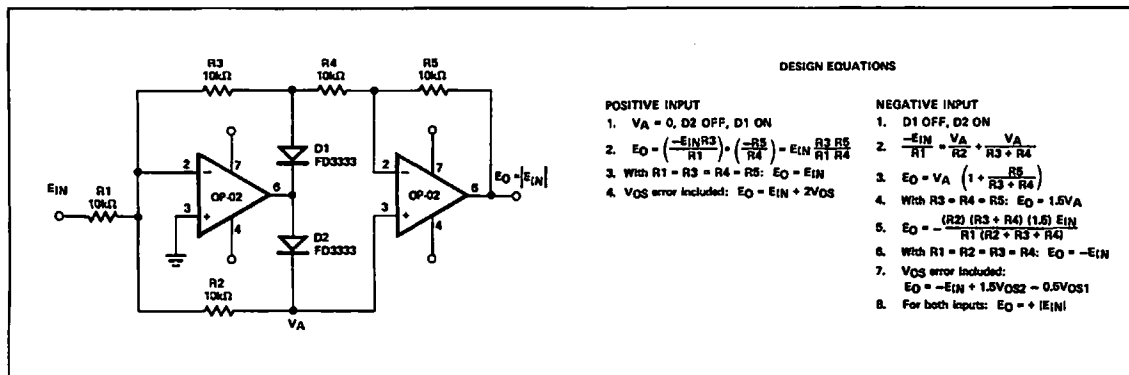


TYPICAL APPLICATIONS

HIGH-STABILITY VOLTAGE REFERENCE

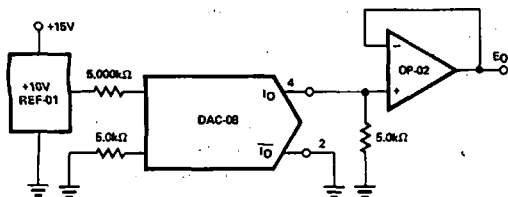


ABSOLUTE VALUE CIRCUIT



TYPICAL APPLICATIONS

DAC-08 OUTPUT AMPLIFIER



FOR COMPLEMENTARY OUTPUT (OPERATION AS A NEGATIVE LOGIC DAC) CONNECT NON-INVERTING INPUT OF OP-AMP TO $\overline{I_O}$ (PIN 2), CONNECT I_O (PIN 4) TO GROUND.

INPUT/OUTPUT TABLE

	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	E_O
FULL-SCALE -1 LSB	1	1	1	1	1	1	1	1	1.992	-9.960
FULL-SCALE -2 LSB	1	1	1	1	1	1	1	0	1.984	-9.920
HALF-SCALE +LSB	1	0	0	0	0	0	0	1	1.008	-5.040
HALF-SCALE	1	0	0	0	0	0	0	0	1.000	-5.000
HALF-SCALE -LSB	0	1	1	1	1	1	1	1	0.992	-4.960
ZERO-SCALE +LSB	0	0	0	0	0	0	0	1	0.0008	-0.040
ZERO-SCALE	0	0	0	0	0	0	0	0	0.000	0.000



OP-04/OP-14

DUAL MATCHED HIGH-PERFORMANCE OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

FEATURES

- Excellent DC Input Specifications
- Matched V_{OS} and CMRR
- OP-14 Fits Standard 1458/1558 Sockets
- Internally Compensated
- Low Noise
- Low Drift
- Low Cost
- $0^{\circ}\text{C}/+70^{\circ}\text{C}$ and $-55^{\circ}\text{C}/+125^{\circ}\text{C}$ Models
- Silicon-Nitride Passivation
- Models with MIL-STD-883 Class B Processing Available From Stock

ORDERING INFORMATION†

PACKAGE						
T _A = 25°C	HERMETIC		PLASTIC		OPERATING TEMPERATURE RANGE	
	TO-99	TO-100	DIP			DIP
			8-PIN	14-PIN		
V _{OS} (mV)	8-PIN	10-PIN	8-PIN	14-PIN	8-PIN	
0.75	OP14AJ*	OP04AK*	OP14AZ*	OP04AY*	—	MIL
0.75	OP14EJ	—	OP14EZ	OP04EY	OP14EP	COM
2.0	OP14J*	OP04K*	OP14Z*	OP04Y*	—	MIL
2.0	OP14CJ	OP04CK	OP14CZ	OP04CY	OP14CP	COM
5.0	—	OP04BK	—	—	—	MIL
5.0	OP14DJ	—	OP14DZ	OP04DY	OP14DP	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

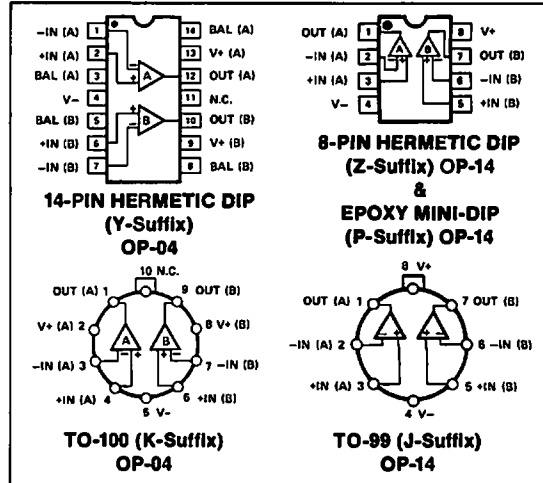
†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

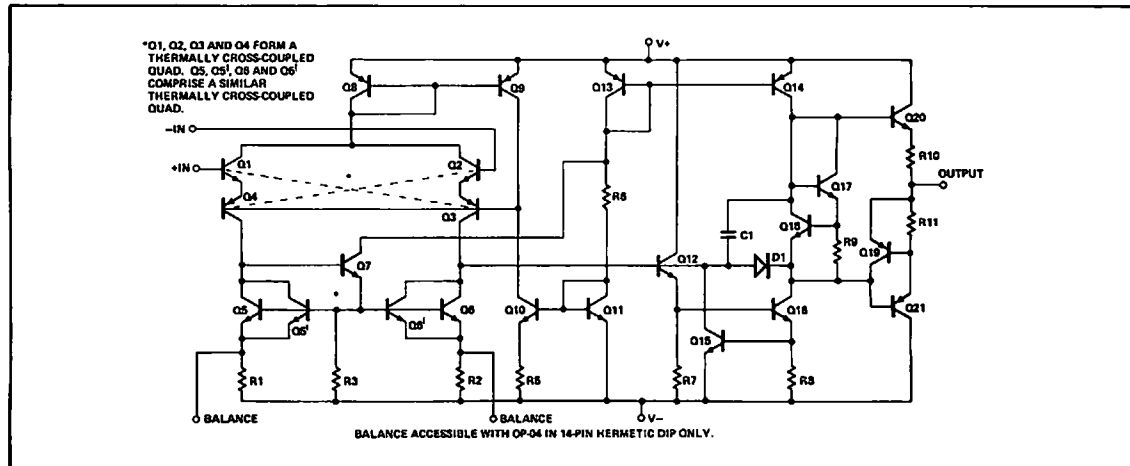
The OP-04/OP-14 series of dual general-purpose operational amplifiers provides significant improvements over industry-standard 747 and 1458/1558 (OP-14) types while maintaining

pin-for-pin compatibility, ease of application, and low cost. Key specifications, such as V_{OS} , I_{OS} , I_B , CMRR, PSRR and A_{VO} , are guaranteed over the full operating temperature range. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise". A thermally-symmetrical input stage design provides low TCV_{OS} , TCI_{OS} , and insensitivity to output load conditions. This series is ideal for upgrading existing designs where accuracy improvements are desired. For more stringent requirements, refer to the OP-207, OP-220, or OP-221 dual-matched operational amplifier data sheets.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (Each Amplifier)



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	$\pm 22\text{V}$
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	$\pm 30\text{V}$
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, K, Y, and Z Packages	-65°C to $+150^{\circ}\text{C}$
P Package	-65°C to $+125^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	
A, Plain, B-Suffix	-55°C to $+125^{\circ}\text{C}$
E, C, D-Suffix	0°C to $+70^{\circ}\text{C}$
DICE Junction Temperature (T_J)	-65°C to $+150^{\circ}\text{C}$

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y) OP-04	100°C	$10.0\text{mW}/^{\circ}\text{C}$
TO-100 (K) OP-04	80°C	$7.1\text{mW}/^{\circ}\text{C}$
TO-99 (J) OP-14	80°C	$7.1\text{mW}/^{\circ}\text{C}$
8-Pin Hermetic DIP (Z) OP-14	75°C	$6.7\text{mW}/^{\circ}\text{C}$
8-Pin Plastic DIP (P) OP-14	38°C	$5.6\text{mW}/^{\circ}\text{C}$

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

MATCHING CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A OP-04E OP-14A OP-14E			OP-04 OP-04C OP-14 OP-14C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20\text{k}\Omega$	—	0.3	1	—	1	2	mV
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10\text{V}$, $R_S \leq 100\Omega$	94	106	—	94	106	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15\text{V}$, $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for OP-04A, OP-14A, OP-04 and OP-14, $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for OP-04E, OP-14E, OP-04C and OP-14C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A OP-04E OP-14A OP-14E			OP-04 OP-04C OP-14 OP-14C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20\text{k}\Omega$	—	0.5	1.5	—	1.5	3	mV
Common-Mode Rejection Ratio Match	ΔCMRR	$V_{CM} = \pm 10\text{V}$, $R_S \leq 100\Omega$	90	100	—	90	100	—	dB

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A			OP-04/OP-14			OP-04B/OP-14B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20\text{k}\Omega$	—	0.3	0.75	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	5	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	50	—	20	75	—	30	100	nA
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	2.0	7.5	—	1.35	7	—	1	5	—	M Ω
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10\text{V}$ $R_S \leq 20\text{k}\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5\text{V}$ to $\pm 20\text{V}$ $R_S \leq 20\text{k}\Omega$	—	10	60	—	30	100	—	100	150	$\mu\text{V/V}$
Output Voltage Swing	V_O	$R_L \geq 2\text{k}\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A			OP-04/OP-14			OP-04B/OP-14B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	200	—	V/mV
Power Consumption (Note 2)	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	e_{n-p-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	25	—	—	25	—	—	25	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	22	—	—	22	—	—	22	—	
		$f_O = 1000Hz$	—	21	—	—	21	—	—	21	—	
Input Noise Current	i_{n-p-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/ μs
Large-Signal Bandwidth (Notes 1, 5)		$V_O = 20V_{p-p}$	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1.0$	1.0	1.3	—	1.0	1.3	—	1.0	1.3	—	MHz
Risetime (Note 1)	t_r	$A_V = +1$, $V_{IN} = 50mV_{p-p}$ $R_L = 2k\Omega$, $C_L = 50pF$	—	260	350	—	260	350	—	260	350	ns
Overshoot (Note 1)	OS	$A_V = +1$, $V_{IN} = 50mV_{p-p}$ $R_L = 2k\Omega$, $C_L = 50pF$	—	5	10	—	5	10	—	5	10	%

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04A/OP-14A			OP-04/OP-14			OP-04B/OP-14B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1	10	—	2	10	—	10	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	$pA/^\circ C$
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	25	60	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 10	± 13	—	V

NOTES:

1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by input bias current.
4. Guaranteed by maximum risetime.
5. Guaranteed by minimum slew rate.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04E/OP-14E			OP-04C/OP-14C			OP-04D/OP-14D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.3	0.75	—	1	2	—	3	5	mV
Input Offset Current	I_{OS}		—	0.5	5	—	1	5	—	5	25	nA
Input Bias Current	I_B		—	18	50	—	20	75	—	30	100	nA
Input Resistance — Differential-Mode	R_{iN}	(Note 3)	2.0	7.5	—	1.35	7	—	1	5	—	M Ω
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	100	—	80	95	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	250	—	50	200	—	25	150	—	V/mV
Power Consumption (Note 2)	P_d	$V_O = 0V$	—	50	90	—	50	90	—	50	90	mW
Input Noise Voltage	e_{n-p-p}	0.1Hz to 10Hz	—	0.65	—	—	0.65	—	—	0.65	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	25	—	—	25	—	—	25	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	22	—	—	22	—	—	22	—	
		$f_O = 1000Hz$	—	21	—	—	21	—	—	21	—	
Input Noise Current	i_{n-p-p}	0.1Hz to 10Hz	—	12.8	—	—	12.8	—	—	12.8	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.4	—	—	1.4	—	—	1.4	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1000Hz$	—	0.4	—	—	0.4	—	—	0.4	—	
Channel Separation	CS		100	—	—	100	—	—	80	—	—	dB
Slew Rate (Note 1)	SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/ μs
Large-Signal Bandwidth (Notes 1, 5)		$V_O = 20V_{p-p}$	4	8	—	4	8	—	4	8	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1$	0.8	1.3	—	0.8	1.3	—	0.8	1.3	—	MHz
Risetime (Note 1)	t_r	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	260	350	—	260	350	—	260	350	ns
Overshoot (Note 1)	OS	$A_V = +1$, $V_{IN} = 50mV$ $R_L = 2k\Omega$, $C_L = 50pF$	—	5	10	—	5	10	—	5	10	%

NOTES:

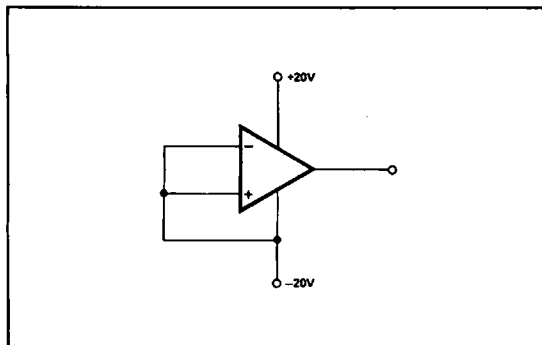
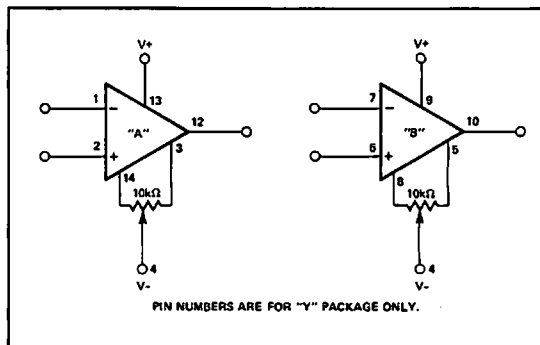
1. Sample tested.
2. Power dissipation per amplifier.
3. Guaranteed by input bias current.
4. Guaranteed by maximum risetime.
5. Guaranteed by minimum slew rate.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04E/OP-14E			OP-04C/OP-14C			OP-04D/OP-14D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	0.4	1.5	—	1.2	3	—	3	6	mV
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$R_S = 50\Omega$	—	2	8	—	4	10	—	8	20	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1	10	—	2	10	—	10	50	nA
Average Input Offset Current Drift (Note 1)	TCI_{OS}		—	7.5	120	—	15	250	—	70	500	$pA/^\circ C$
Input Bias Current	I_B		—	30	60	—	40	100	—	50	200	nA
Input Voltage Range	IVR		± 10	± 13	—	± 10	± 13	—	± 10	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	80	100	—	80	85	—	70	85	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	—	10	60	—	30	100	—	100	150	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	—	25	60	—	15	25	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 10	± 13	—	V

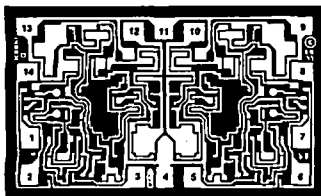
NOTES:

1. Sample tested.

BURN-IN CIRCUIT (1/2 of OP-04, OP-14)

OFFSET ADJUST CIRCUIT




DICE CHARACTERISTICS



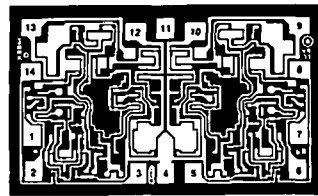
OP-14

DIE SIZE 0.080 × 0.050 inch, 4000 sq. mils
(2.03 × 1.27 mm, 2.58 sq. mm)

For additional DICE ordering information,
refer to 1988 Data Book, Section 2.

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V-
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUTPUT (B)
11. V+
12. OUTPUT (A)
13. V+
14. BALANCE (A)

NOTE: 9, 11 and 13 are internally connected.



OP-04

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V-
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+ (B)
10. OUTPUT (B)
11. NO CONNECTIONS
12. OUTPUT (A)
13. V+ (A)
14. BALANCE (A)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-04N OP-14N LIMIT	OP-04G OP-14G LIMIT	OP-14GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	0.75	2	6	mV MAX
Input Offset Voltage Match	ΔV_{OS}	$R_S \leq 20k\Omega$	1	2	—	mV MAX
Input Offset Current	I_{OS}		5	5	200	nA MAX
Input Bias Current	I_B		50	75	500	nA MAX
Input Voltage Range	IVR		± 10	± 10	± 10	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$ $R_S \leq 20k\Omega$	85	80	70	dB MIN
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$ $R_S \leq 100\Omega$	94	94	—	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$ $R_S \leq 20k\Omega$	60	100	150	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	± 12 ± 12	± 12 ± 12	± 12 ± 10	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	100	50	25	V/mV MIN
Power Consumption (Both Amplifiers)	P_d	$V_{OUT} = 0$	170	170	180	mW MAX
Channel Separation	CS		100	100	—	dB MIN

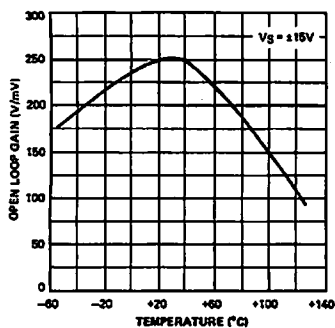
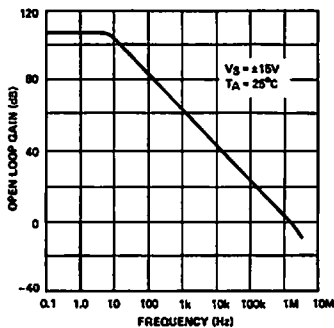
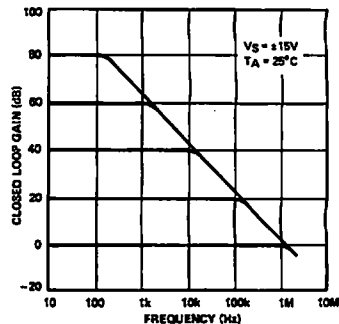
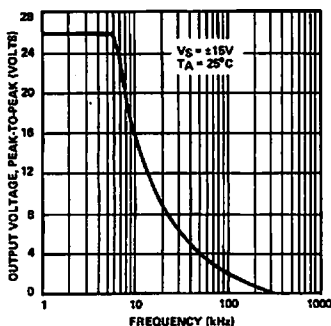
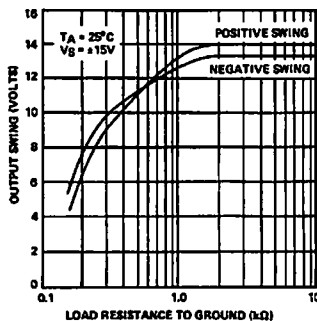
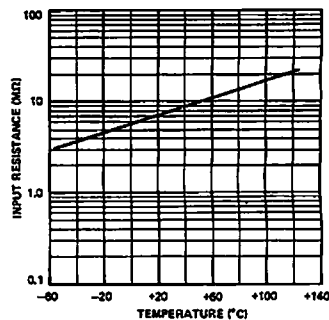
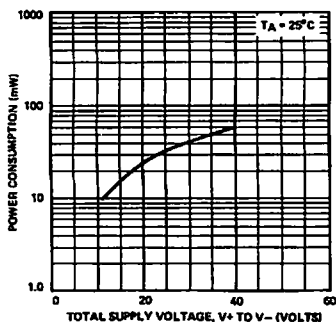
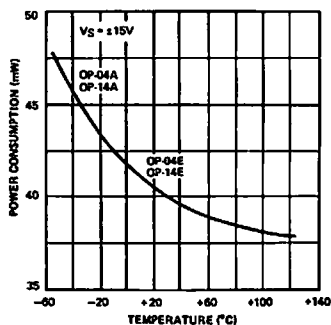
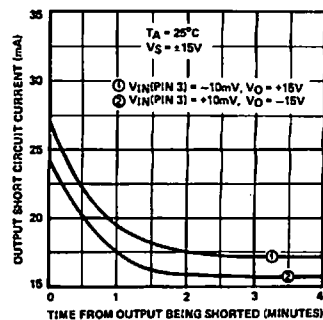
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

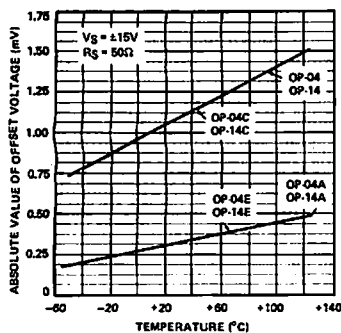
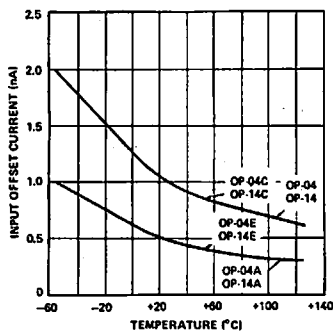
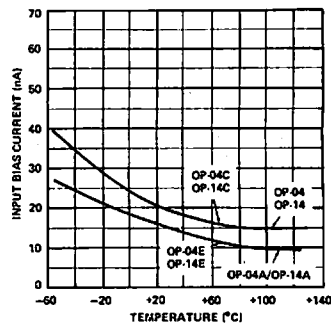
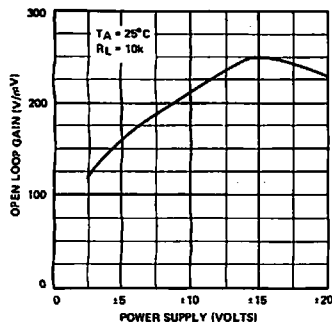
PARAMETER	SYMBOL	CONDITIONS	OP-04N OP-14N TYPICAL	OP-04G OP-14G TYPICAL	OP-14GR TYPICAL	UNITS
Risetime	t_r	$A_V = +1$ $V_{IN} = 50mV$ $R_L = 2k\Omega$ $C_L = 50pF$	200	200	200	ns
Overshoot	OS	$A_V = +1$ $V_{IN} = 50mV$ $R_L = 2k\Omega$ $C_L = 50pF$	5	5	5	%
Slew Rate	SR	$R_L = 2k\Omega$ $C_L = 100pF$	0.25	0.25	—	V/ μs

TYPICAL PERFORMANCE CHARACTERISTICS (Each Amplifier)

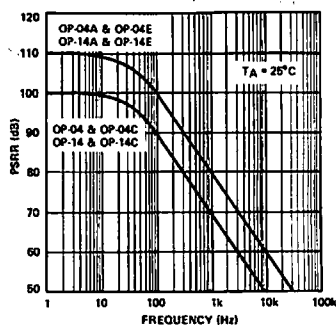
 OPEN-LOOP GAIN
vs TEMPERATURE

 OPEN-LOOP
FREQUENCY RESPONSE

 CLOSED-LOOP RESPONSE
FOR VARIOUS
GAIN CONFIGURATIONS

 MAXIMUM UNDISTORTED
OUTPUT vs FREQUENCY

 OUTPUT VOLTAGE vs
LOAD RESISTANCE

 INPUT RESISTANCE
vs TEMPERATURE

 POWER CONSUMPTION
vs POWER SUPPLY
 POWER CONSUMPTION
vs TEMPERATURE

 OUTPUT SHORT-CIRCUIT
CURRENT vs TIME




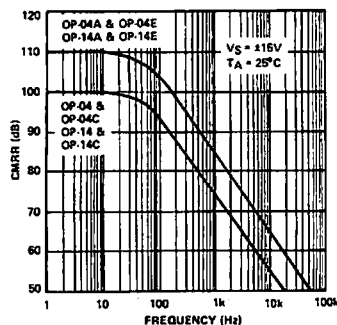
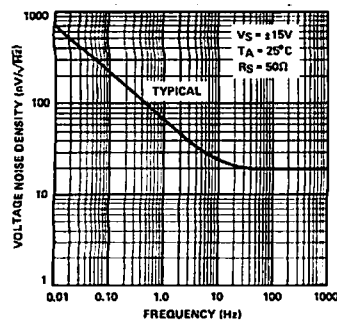
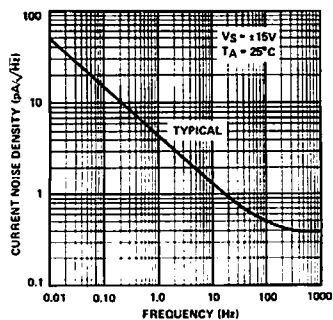
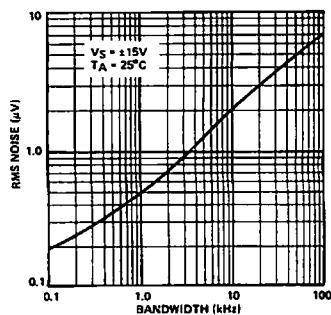
TYPICAL PERFORMANCE CHARACTERISTICS (Each Amplifier)

UNTRIMMED OFFSET VOLTAGE
vs TEMPERATUREINPUT OFFSET CURRENT
vs TEMPERATUREINPUT BIAS CURRENT
vs TEMPERATUREOPEN-LOOP GAIN vs
POWER SUPPLY VOLTAGE

PSRR vs FREQUENCY



CMRR vs FREQUENCY

INPUT SPOT NOISE
VOLTAGE vs FREQUENCYINPUT SPOT NOISE
CURRENT vs FREQUENCYINPUT WIDEBAND NOISE vs
BANDWIDTH (0.1Hz TO
FREQUENCY INDICATED)



OP-05

INSTRUMENTATION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Noise $0.6\mu V_{p-p}$ Max, 0.1 to 10Hz
- Low Drift vs. Temperature $0.5\mu V/^{\circ}C$ Max
- Low Drift vs. Time $0.2\mu V/\text{Month}$ Typ
- Low Bias Current 2.0nA Max
- High CMRR 114dB Min
- High PSRR 100dB Min
- High Gain 300,000 Min
- High R_{IN} Differential $30M\Omega$ Min
- High R_{IN} CM $200G\Omega$ Typ
- Internally Compensated Stable to 500pF Load
- Fits 725, 108A and 741 Sockets
- $125^{\circ}C$ Temperature Tested Dice

ORDERING INFORMATION†

$T_A = 25^{\circ}C$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC	PLASTIC		
	TO-99 8-PIN	DIP 8-PIN	DIP 8-PIN	
0.15	OP05AJ*	OP05AZ*	—	MIL
0.5	OP05J*	OP05Z*	—	MIL
0.5	OP05EJ	OP05EZ	OP05EP	COM
1.3	OP05CJ	OP05CZ	OP05CP	COM

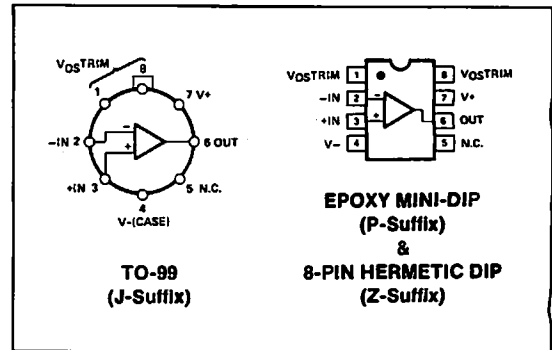
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

applications with the simplicity of use of a fully-protected, internally-compensated op amp. The OP-05 has low input offset voltage and bias current combined with very high levels of gain, input impedance, CMRR, and PSRR.

The OP-05 is a direct replacement in 725, 108A, and unnull 741 sockets allowing instant system performance improvement without redesign. The OP-05 is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high-gain active filters, buffers, integrators, and sample-and-hold amplifiers. For dual-matched versions, refer to the OP-207 and OP-10 data sheets.

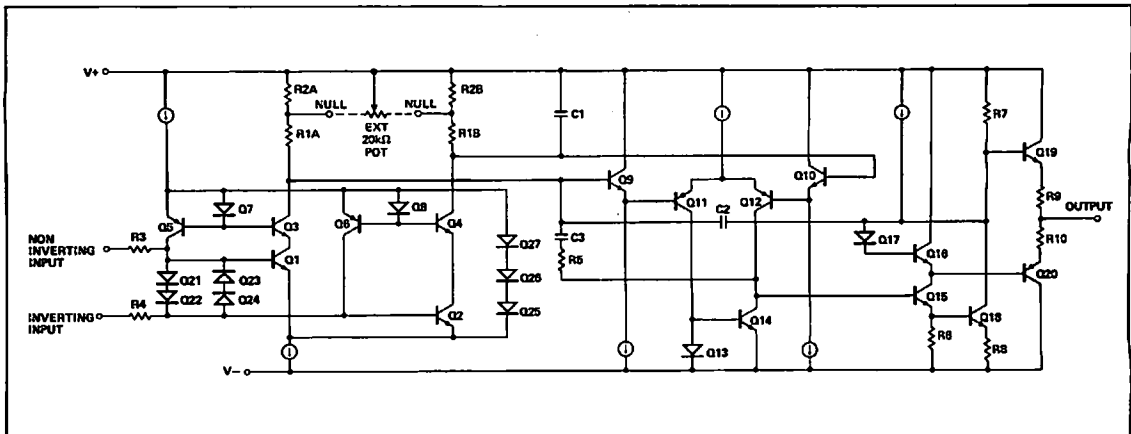
PIN CONNECTIONS



GENERAL DESCRIPTION

The OP-05 series of monolithic instrumentation operational amplifiers combine excellent performance in low-signal-level

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 3)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Operating Temperature Range	
OP-05A, OP-05	-55°C to +125°C
OP-05E, OP-05C	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

3. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)	—	0.2	1.0	—	0.2	1.0	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	0.7	2.0	—	1.0	2.8	nA
Input Bias Current	I_B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage (Note 2)	e_{n-p-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.6	11.0	
Input Noise Current (Note 2)	I_{n-p-p}	0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density (Note 2)	I_n	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	30	60	—	20	60	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	G Ω
Input Voltage Range	IVR		±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	114	126	—	114	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	300	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)	150	500	—	150	500	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	
		$R_L \geq 1k\Omega$	±10.5	±12.0	—	±10.5	±12.0	—	
Slew Rate (Note 2)	SR	$R_L \geq 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/ μs
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load	—	90	120	—	90	120	mW
		$V_S = \pm 3V$, No load	—	4	6	—	4	6	
Offset Adjustment Range		$R_P = 20k\Omega$	—	4	—	—	4	—	mV

NOTES:1. Long-term input offset voltage stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30operating days are typically $2.5\mu V$. Refer to typical performance curve.

2. Sample tested.

3. Guaranteed by design.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.10	0.24	—	0.3	0.7	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.3	0.9	—	0.7	2.0	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.5	—	0.3	1.0	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1.0	4.0	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1	± 4	—	± 2	± 6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	110	123	—	110	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 12.0	± 12.6	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.3	1.3	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Notes 1, 2)	—	0.3	1.5	—	0.4	2.0	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	± 1.2	± 4.0	—	± 1.8	± 7.0	nA
Input Noise Voltage (Note 2)	e_{n-p-p}	0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density (Note 2)	e_n	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.5	20.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	10.0	13.0	—	10.2	13.5	
		$f_O = 1000\text{Hz}$	—	9.8	11.0	—	9.8	11.5	
Input Noise Current (Note 2)	i_{n-p-p}	0.1Hz to 10Hz	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density (Note 2)	i_n	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.35	0.90	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	0.14	0.23	—	0.15	0.27	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	180	—	—	120	—	G Ω
Input Voltage Range	IVR		± 13.5	± 14.0	—	± 13.0	± 14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	110	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$	150	500	—	100	400	—	
		$V_S = \pm 3V$ (Note 3)	—	—	—	—	—	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0	—	± 12.0	± 13.0	—	V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 11.5	± 12.8	—	
		$R_L \geq 1k\Omega$	± 10.5	± 12.0	—	—	± 12.0	—	
Slew Rate (Note 2)	SR	$R_L \geq 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/ μs
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No load	—	90	120	—	95	150	mW
		$V_S = \pm 3V$, No load	—	4	8	—	4	8	
Offset Adjustment Range		$R_P = 20k\Omega$	—	4	—	—	4	—	mV

NOTE: See notes on previous page.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

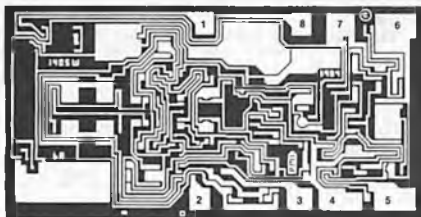
PARAMETER	SYMBOL	CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.25	0.8	—	0.35	1.8	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	1.3	4.5	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.8	—	0.4	1.5	
Input Offset Current	I_{OS}		—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1.5	± 5.5	—	± 2.2	± 9.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	107	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	180	450	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 11.0	± 12.8	—	V

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$. Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.101 × 0.052 inch, 5300 sq. mils
(2.57 × 1.32 mm, 3.34 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. NO CONNECTION
6. OUTPUT
7. V₊
8. BALANCE

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-05N, OP-05G and OP-05GR devices; $T_A = 125^\circ C$ for OP-05NT and OP-05GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05NT LIMIT	OP-05N LIMIT	OP-05GT LIMIT	OP-05G LIMIT	OP-05GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.25	0.15	0.7	0.5	1.3	mV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.7	3.8	6.0	nA MAX
Input Bias Current	I_B		±4	±2	±6	±4	±7	nA MAX
Input Resistance Differential Mode	R_{IN}	(Note 2)	—	20	—	15	8	MΩ MIN
Input Voltage Range	IVR		±13.0	±13.5	±13.0	±13.5	±13.0	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ at $+25^\circ C$ $V_{CM} = \pm 13.0$ at $+125^\circ C$	110	114	110	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	20	30	μV/V MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$	—	±12.5	—	±12.5	±12.0	V MIN
		$R_L = 2k\Omega$	±12.0	±12.0	±12.0	±12.0	±11.5	
		$R_L = 1k\Omega$	—	±10.5	—	±10.5	—	
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	200	200	150	200	120	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

NOTES:

1. For $25^\circ C$ characteristics of NT & GT devices see N & G characteristics respectively.
2. Guaranteed by design.

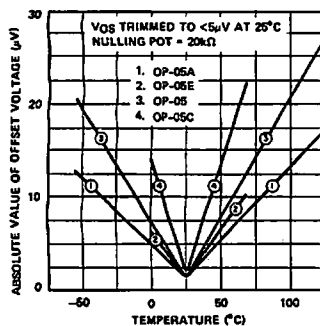
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

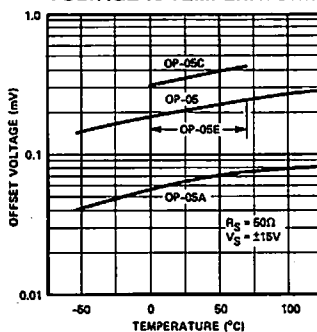
PARAMETER	SYMBOL	CONDITIONS	OP-05NT TYPICAL	OP-05N TYPICAL	OP-05GT TYPICAL	OP-05G TYPICAL	OP-05GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.3	0.7	0.7	1.2	μV/°C
Nullified Input Offset Voltage Drift	TCV_{OSn}	$R_S \leq 50\Omega$, $R_p = 20k\Omega$	0.2	0.2	0.3	0.3	0.4	μV/°C
Average Input Offset Current Drift	TCI_{OS}		5	5	8	8	12	pA/°C
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

TYPICAL PERFORMANCE CHARACTERISTICS

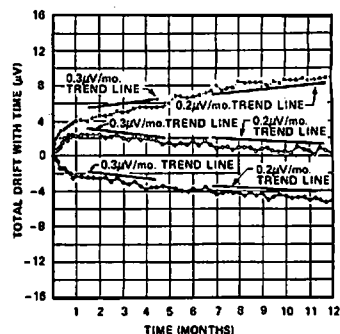
TRIMMED OFFSET VOLTAGE vs TEMPERATURE



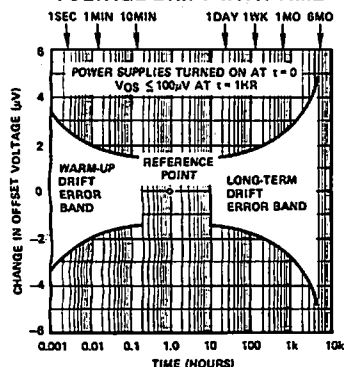
UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE



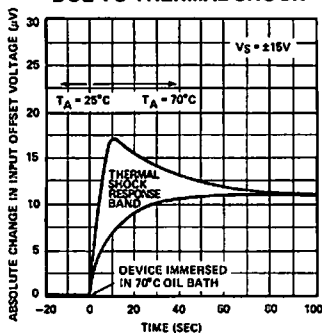
TYPICAL OFFSET VOLTAGE STABILITY vs TIME



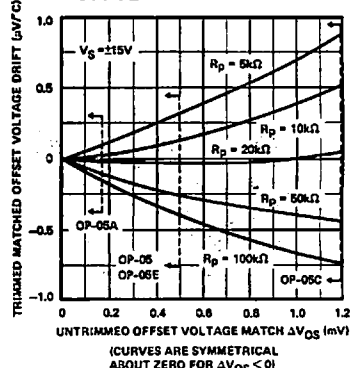
OFFSET VOLTAGE DRIFT WITH TIME



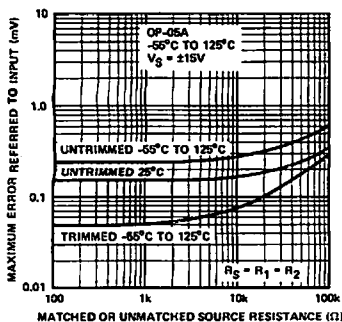
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



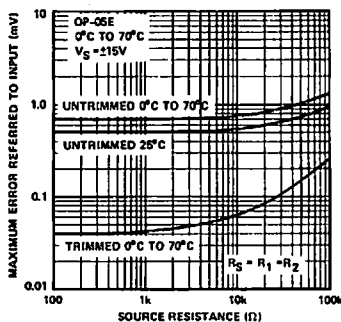
TRIMMED OFFSET VOLTAGE DRIFT



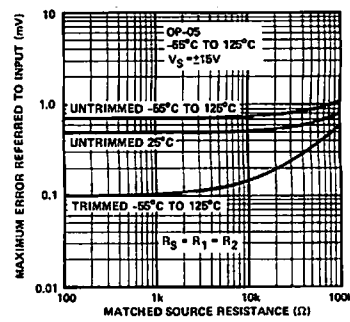
MAXIMUM ERROR vs SOURCE RESISTANCE



MAXIMUM ERROR vs SOURCE RESISTANCE



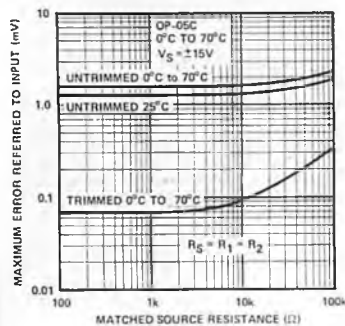
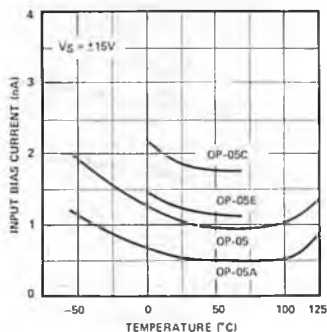
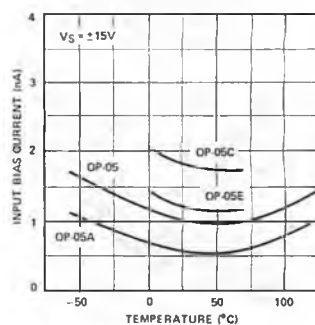
MAXIMUM ERROR vs SOURCE RESISTANCE



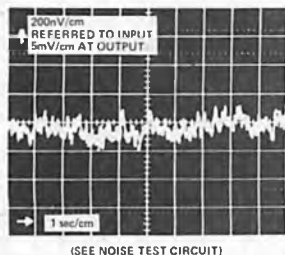
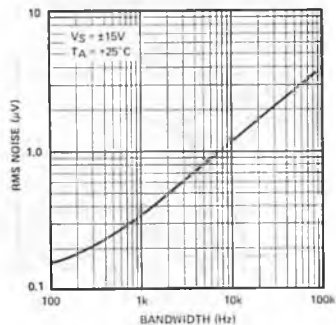
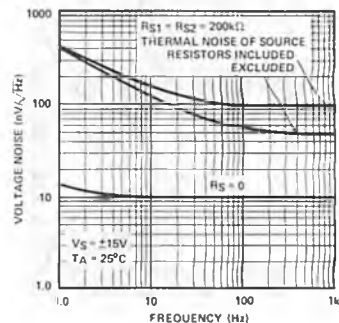
OPERATIONAL AMPLIFIERS

5

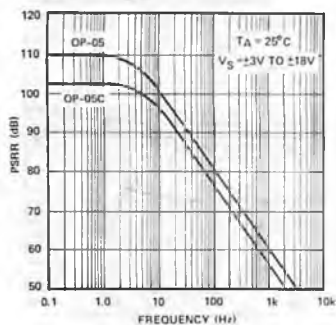
TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM ERROR
vs SOURCE RESISTANCEINPUT BIAS CURRENT
vs TEMPERATUREINPUT OFFSET CURRENT
vs TEMPERATURE

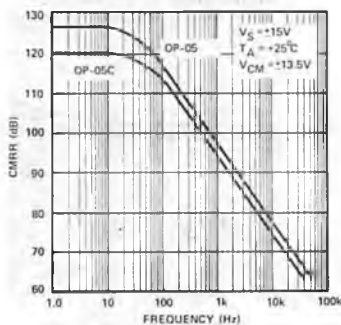
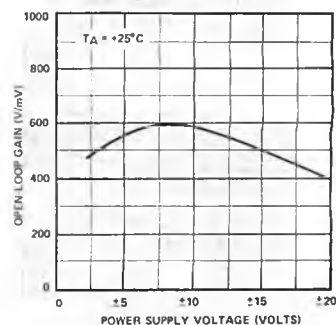
OP-05 LOW FREQUENCY NOISE

INPUT WIDEBAND NOISE
vs BANDWIDTH (0.1Hz
TO FREQUENCY INDICATED)VOLTAGE NOISE DENSITY
vs FREQUENCY

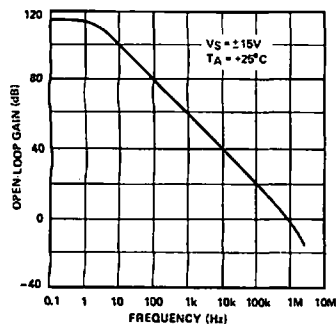
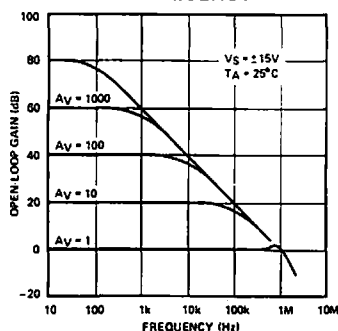
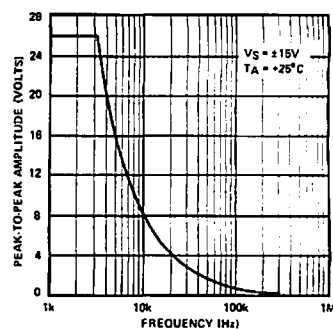
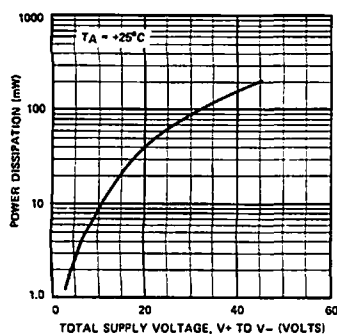
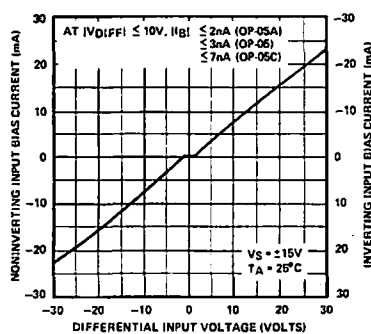
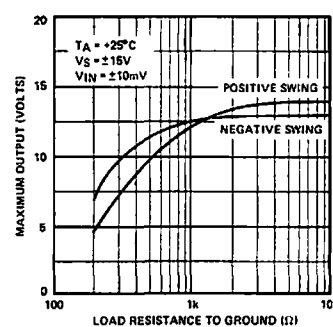
PSRR vs FREQUENCY



CMRR vs FREQUENCY

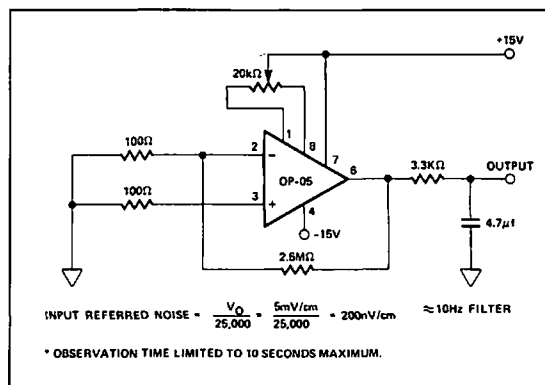
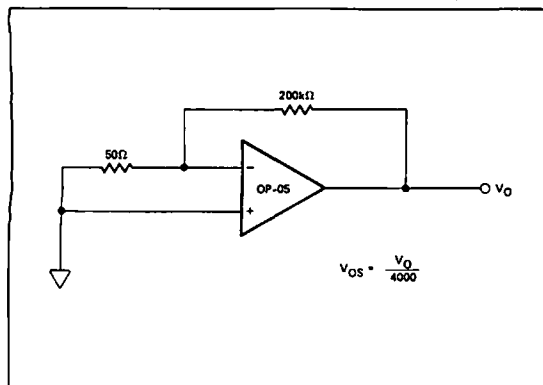
OPEN-LOOP GAIN vs
POWER SUPPLY VOLTAGE

TYPICAL PERFORMANCE CHARACTERISTICS

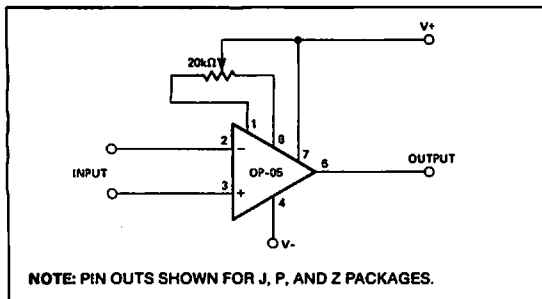
 OPEN-LOOP GAIN
vs FREQUENCY

 CLOSED-LOOP GAIN
vs FREQUENCY

 MAXIMUM OUTPUT SWING
vs FREQUENCY

 POWER CONSUMPTION
vs POWER SUPPLY

 INPUT BIAS CURRENT vs
DIFFERENTIAL INPUT VOLTAGE

 MAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCE


OPERATIONAL AMPLIFIERS

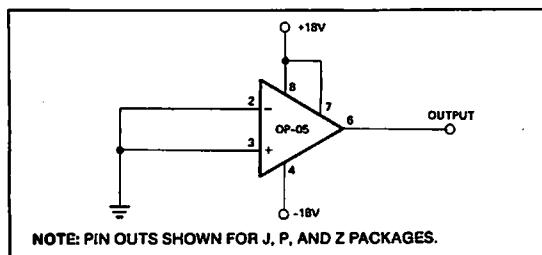
TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT*



OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



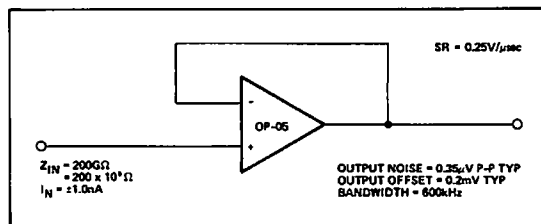
APPLICATIONS INFORMATION

OP-05 series devices may be fitted directly to 725 and 108/108A Series sockets with or without removal of external compensation components. Additionally, the OP-05 may be fitted to unnullled 741 series sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-05 operation. The OP-05 provides stable operation with load capacitance of up to 500pF and $\pm 10V$ swings; larger capacitances should be decoupled with a 50Ω resistor.

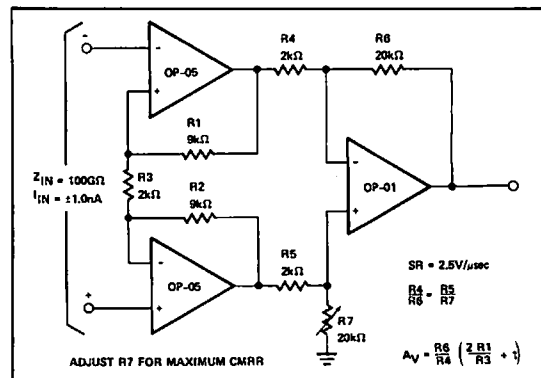
Offset stability can be degraded by stray thermoelectric voltages arising from dissimilar metals at the contacts to the input terminals. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

TYPICAL APPLICATIONS

STABLE, HIGH-IMPEDANCE BUFFER



HIGH IMPEDANCE, HIGH COMMON-MODE REJECTION INSTRUMENTATION AMPLIFIER



Precision Monolithics Inc.

FEATURES

- **Very High Voltage Gain** 1,000V/mV Min
- **Low Offset Voltage and Offset Current**
- **Low Drift vs. Temperature**
(TCV_{OS}) 0.8μV/°C Max
- **Low Input Voltage and Current Noise**
- **Low Offset Voltage Drift with Time**
- **High Common-Mode Rejection** 120dB Typ
- **High Power Supply Rejection** 2μV/V Max
- **Wide Supply Range** ±3.0V to ±22V
- **MIL-STD-883 Processing Available**
- **Slew Rate to** 100V/μs

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	
0.2	—	OP06EZ	COM
0.2	OP06AJ*	—	MIL
0.5	OP06FJ	OP06FZ	COM
0.5	OP06BJ*	—	MIL
1.3	OP06GJ	OP06GZ	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

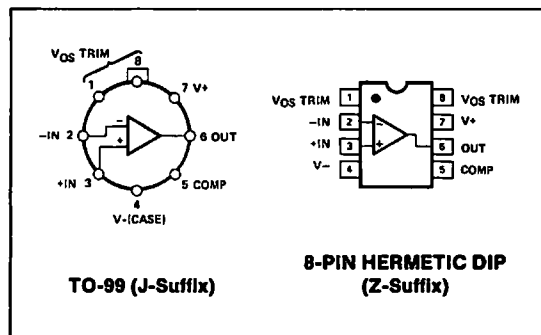
GENERAL DESCRIPTION

The OP-06 monolithic instrumentation operational amplifier is designed for accurate high-gain amplification of low level signals. High common-mode rejection reduces signal degradation when large common-mode voltages are present.

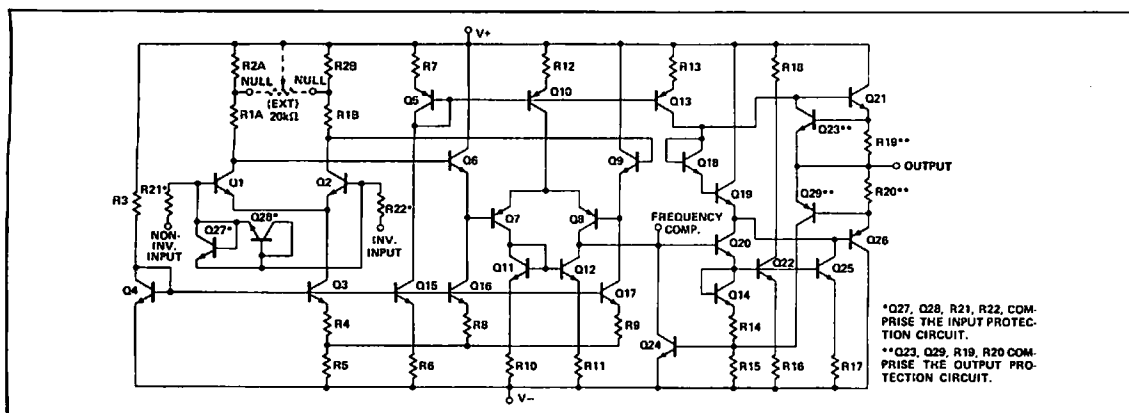
Superior DC input characteristics include very low offset voltage and current, extremely high open-loop gain, low 1/f and wideband noise, and low "popcorn" noise. Low offset voltage drift is improved by a nulling technique that optimizes TCV_{OS} performance when V_{OS} is nulled to zero. Very high common-mode and power supply rejection enable accurate performance in noisy environments.

Flexible external compensation provides wide-bandwidth and high slew rate operation in high closed-loop gain applications. Excellent long-term stability, and compatibility with MIL-STD-883 processing, make the OP-06 an excellent choice for high-reliability applications. For example, process control and aerospace applications; including strain gauge and thermocouple amplifiers, low-noise audio amplifiers, and instrumentation amplifiers. The OP-06 is a direct replacement for all 725 types providing superior DC and noise performance plus the unique feature of complete input differential voltage and output short-circuit protection.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



*Q27, Q28, R21, R22, COMPRISE THE INPUT PROTECTION CIRCUIT.
**Q23, Q29, R19, R20 COMPRISE THE OUTPUT PROTECTION CIRCUIT.

**ABSOLUTE MAXIMUM RATINGS** (Note 3)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-06A, OP-06B	-55°C to +125°C
OP-06E, OP-06F, OP-06G	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

3. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-06A/E			OP-06B/F			OP-06G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	0.06	0.2	—	0.2	0.5	—	0.4	1.3	mV
Input Offset Current	I_{OS}		—	0.3	2.0	—	0.75	5.0	—	2	13	nA
Input Bias Current	I_B		—	30	70	—	30	80	—	40	110	nA
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 1)	—	9.0	15.0	—	9.0	15.0	—	9.0	15.0	nV/ $\sqrt{Hz}$
		$f_O = 100Hz$ (Note 1)	—	8.0	9.0	—	8.0	9.0	—	8.0	9.0	
		$f_O = 1000Hz$ (Note 1)	—	7.0	7.5	—	7.0	7.5	—	7.0	7.5	
Input Noise Current Density	i_n	$f_O = 10Hz$ (Note 1)	—	0.5	1.2	—	0.5	1.2	—	0.6	1.4	pA/ $\sqrt{Hz}$
		$f_O = 100Hz$ (Note 1)	—	0.25	0.6	—	0.25	0.6	—	0.3	0.7	
		$f_O = 1000Hz$ (Note 1)	—	0.15	0.25	—	0.15	0.25	—	0.2	0.3	
Input Resistance	R_{IN}	(Note 3)	0.8	1.8	—	0.7	1.8	—	0.5	1.5	—	M Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	1,000	3,000	—	1,000	3,000	—	500	3,000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	±12.0	±13.0	—	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	—	±12.0	±12.8	—	±11.5	±12.8	—	
		$R_L \geq 1k\Omega$	±11.0	±12.5	—	±11.0	±12.5	—	—	±12.0	—	
Input Voltage Range	IVR		±13.5	±14.0	—	±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \leq 20k\Omega$	114	120	—	114	120	—	110	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	—	0.5	2.0	—	1.0	5.0	—	2.0	10	$\mu V/V$
Power Consumption	P_d		—	90	120	—	90	120	—	110	150	mW
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 500\Omega$, (Note 3)	100	600	—	100	600	—	60	600	—	V/mV
		$V_O = \pm 0.5V$										
		$V_S = \pm 3V$										
Power Consumption	P_d	$V_S = \pm 3V$	—	4	6	—	4	6	—	4	8	mW

NOTES:

- Sample tested.
- Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Both sides of the contacts should be kept at approximately the same temperature. All temperature gradients should be minimized.
- Guaranteed by design.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08A			OP-08B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	0.08	0.28	—	0.3	0.7	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{OS}	$R_S = 50\Omega$ (Notes 1, 2)	—	0.3	0.8	—	0.7	2.0	$\mu V/^\circ C$
Average Input Offset Voltage Drift (With external trim)	TCV_{OSn}	$R_S = 50\Omega$ (Notes 2, 3) $R_P = 20k\Omega$	—	0.2	0.6	—	0.28	1.0	$\mu V/^\circ C$
Input Offset Current	I_{OS}	T_A MAX T_A MIN	—	0.25 0.8	1.0 4.0	—	0.6 2.0	4.0 18.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	3	20	—	8	90	$pA/^\circ C$
Input Bias Current	I_B	T_A MAX T_A MIN	—	22 40	60 120	—	25 45	70 180	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \leq 20k\Omega$	109	112	—	109	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	—	1	5	—	2	8	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$; $R_L \geq 2k\Omega$ T_A MAX T_A MIN	1,000 700	3,500 2,000	—	1,000 700	3,500 1,800	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 12.0	± 12.6	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08E			OP-08F			OP-08G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Without external trim)	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	0.08	0.28	—	0.25	0.6	—	0.5	1.6	mV
Average Input Offset Voltage Drift (Without external trim)	TCV_{OS}	$R_S = 50\Omega$ (Notes 1, 2)	—	0.3	0.8	—	0.7	2.0	—	1.4	4.5	$\mu V/^\circ C$
Average Input Offset Voltage Drift (With external trim)	TCV_{OSn}	$R_S = 50\Omega$ (Notes 2, 3) $R_P = 20k\Omega$	—	0.2	0.6	—	0.28	1.0	—	0.5	1.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}	T_A MAX T_A MIN	—	0.25 0.8	1.0 4.0	—	0.65 2.0	5.0 18.0	—	2.0 3.0	15 25	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	3	20	—	8	90	—	14	150	$pA/^\circ C$
Input Bias Current	I_B	T_A MAX T_A MIN	—	22 40	60 120	—	30 45	80 180	—	35 45	110 180	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ $R_S \leq 20k\Omega$	109	112	—	109	112	—	95	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	—	1.0	5.0	—	1.8	7.0	—	3.0	15	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$; $R_L \geq 2k\Omega$ T_A MAX T_A MIN	1,000 800	3,500 2,000	—	1,000 800	3,500 1,800	—	400 300	3,200 1,700	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 12.0	± 12.6	—	± 11.0	± 12.6	—	V

NOTES:

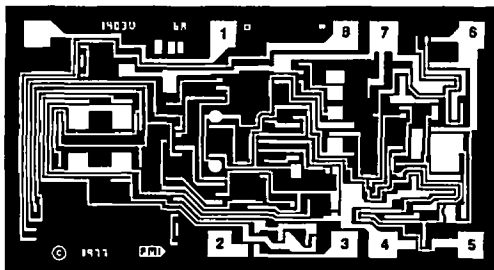
1. Sample tested.
2. Thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Both sides of the

contacts should be kept at approximately the same temperature. All temperature gradients should be minimized.

3. Guaranteed by input bias current.



DICE CHARACTERISTICS



DIE SIZE 0.095 × 0.051 inch, 4845 sq. mils
(2.41 × 1.30 mm, 3.13 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. COMPENSATION
6. OUTPUT
7. V₊
8. NULL

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-06N, OP-06G and OP-06GR devices; $T_A = 125^\circ C$ for OP-06NT and OP-06GT devices, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	OP-06NT LIMIT	OP-06N LIMIT	OP-06GT LIMIT	OP-06G LIMIT	OP-06GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	0.3	0.2	0.7	0.5	1.3	mV MAX
Input Offset Current	I_{OS}		1	2	4	5	13	nA MAX
Input Bias Current	I_B		60	70	70	80	110	nA MAX
Input Resistance Differential Mode	R_{IN}	(Note 1)	—	0.8	—	0.7	0.5	MΩ MIN
Input Voltage Range	IVR		±13.0	±13.5	±13.0	±13.5	±13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5$ $R_S \leq 20k\Omega$	108	114	108	114	110	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$ $R_S \leq 20k\Omega$	6	2	8	5	10	μV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	—	±12.5	—	±12.5	±12.0	V MIN
		$R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.0 —	±12.0 ±11.0	±12.0 —	±12.0 ±11.0	±11.5 —	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	1000	1000	800	1000	500	V/mV MIN
Differential Input Voltage			±30	±30	±30	±30	±30	V MAX
Power Consumption ($V_{OUT} = 0V$)	P_d		—	120	—	120	150	mW MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

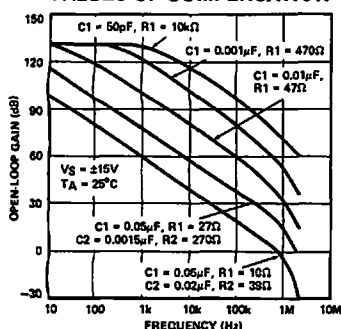
PARAMETER	SYMBOL	CONDITIONS	OP-06NT TYPICAL	OP-06N TYPICAL	OP-06GT TYPICAL	OP-06G TYPICAL	OP-06GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 50\Omega$	0.3	0.3	0.7	0.7	1.4	μV/°C
Nullified Input Offset Voltage Drift	TCV_{OSn}	$R_S \leq 50k\Omega$ $R_P = 20k\Omega$	0.2	0.2	0.28	0.28	0.5	μV/°C
Average Input Offset Current Drift	TCI_{OS}		3	3	8	8	14	pA/°C

NOTES:

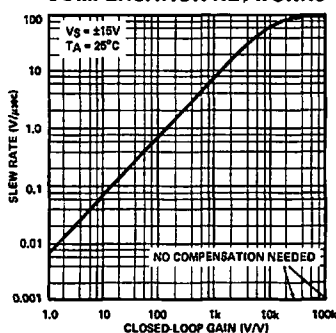
1. Guaranteed by input bias current.
2. For $+25^\circ C$ specifications of OP-06NT and OP-06GT, see OP-06N and OP-06G respectively.

TYPICAL PERFORMANCE CHARACTERISTICS

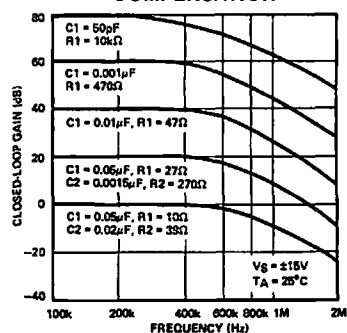
OPEN-LOOP RESPONSE FOR VALUES OF COMPENSATION



SLEW RATE USING RECOMMENDED COMPENSATION NETWORKS



CLOSED-LOOP FREQUENCY RESPONSE FOR VALUES OF COMPENSATION

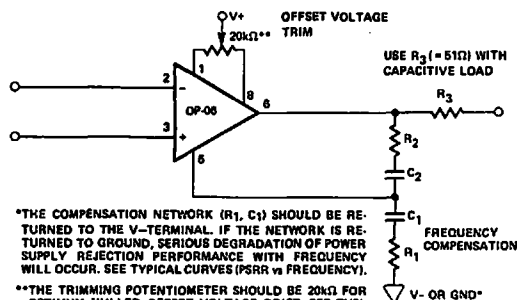


FREQUENCY COMPENSATION

COMPENSATION VALUES

Avcl	R ₁ (Ω)	C ₁ (μF)	R ₂ (Ω)	C ₂ (μF)
10000	10k	50pF	—	—
1000	470	0.001	—	—
100	47	0.01	—	—
10	27	0.05	270	0.0015
1	10	0.05	39	0.02

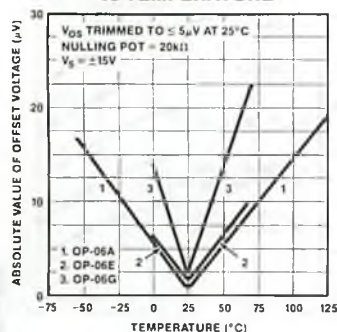
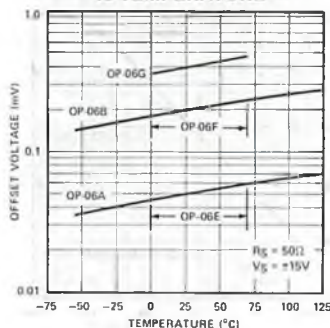
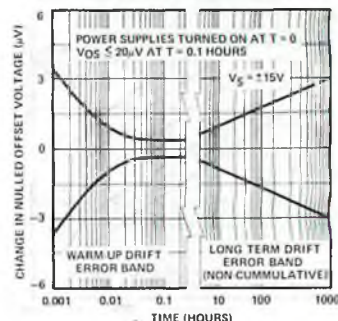
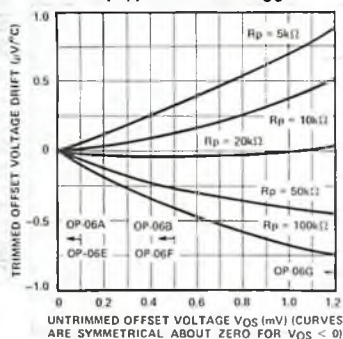
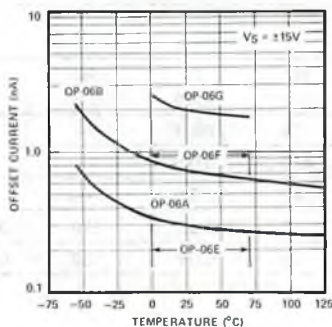
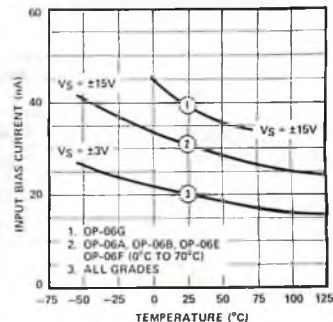
COMPENSATION CIRCUIT (J or Z PACKAGE)



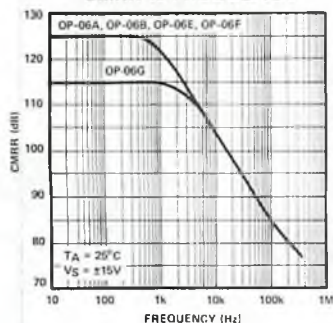
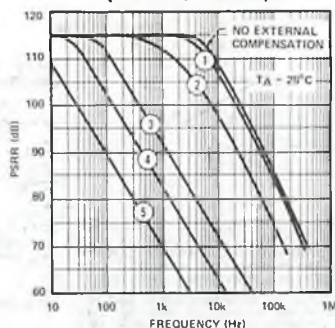
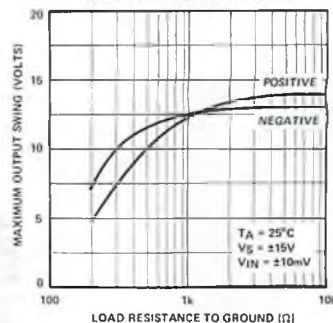
*THE COMPENSATION NETWORK (R₁, C₁) SHOULD BE RETURNED TO THE V-TERMINAL. IF THE NETWORK IS RETURNED TO GROUND, SERIOUS DEGRADATION OF POWER SUPPLY REJECTION PERFORMANCE WITH FREQUENCY WILL OCCUR. SEE TYPICAL CURVES (PSRR vs FREQUENCY).

**THE TRIMMING POTENTIOMETER SHOULD BE 20kΩ FOR OPTIMUM NULLED OFFSET VOLTAGE DRIFT. SEE TYPICAL CURVES (TRIMMED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POTENTIOMETER).

TYPICAL PERFORMANCE CHARACTERISTICS

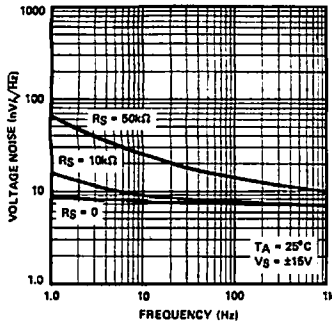
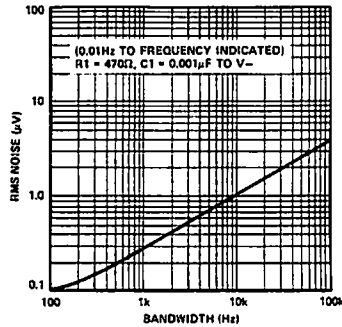
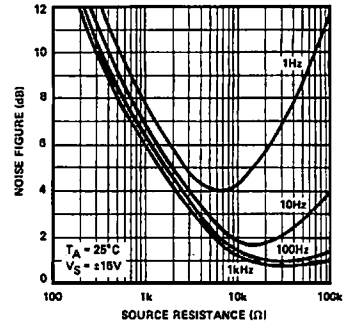
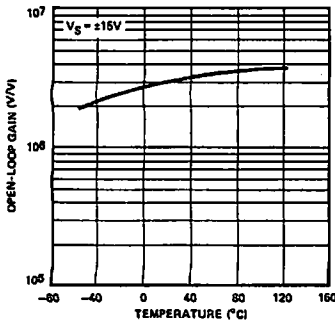
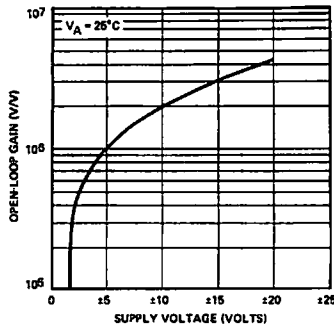
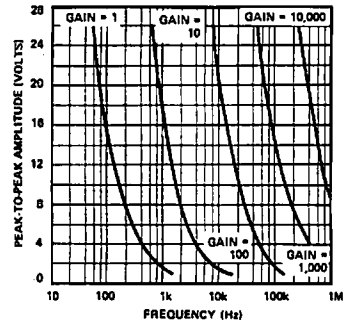
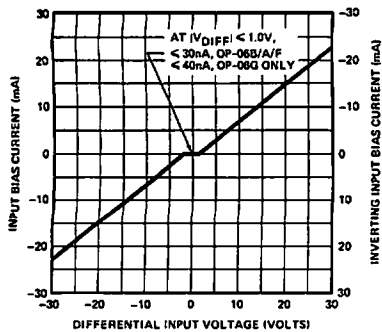
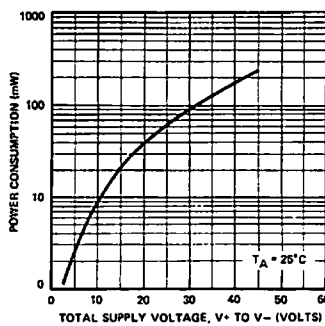
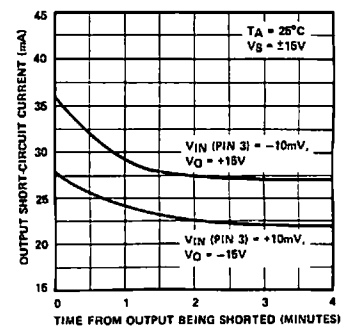
TRIMMED OFFSET VOLTAGE
vs TEMPERATUREOFFSET VOLTAGE
vs TEMPERATUREOFFSET VOLTAGE DRIFT
WITH TIMETRIMMED OFFSET VOLTAGE
DRIFT AS A FUNCTION OF
TRIMMING POTENTIOMETER
(R_P) SIZE AND V_{OS} OFFSET CURRENT
vs TEMPERATUREINPUT BIAS CURRENT
vs TEMPERATURE

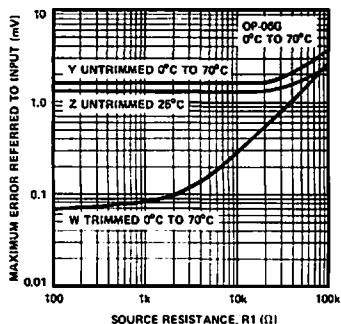
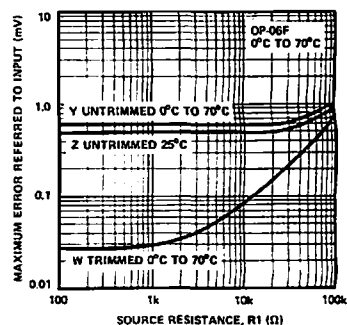
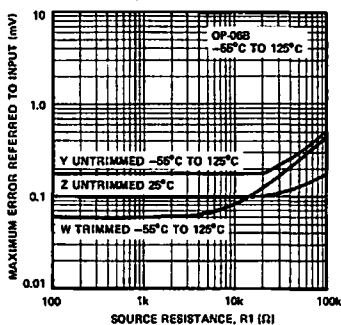
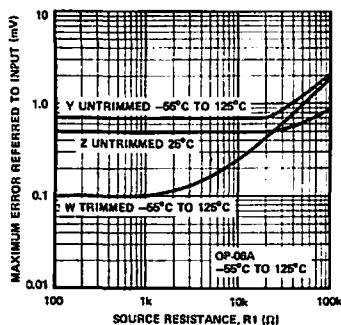
CMRR vs FREQUENCY

PSRR vs FREQUENCY
(OP-06B, OP-06E)MAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCE

1. C1 = 0.001μF, R1 = 470Ω; FROM PIN 5 TO V-
2. C1 = 0.1μF, R1 = 5Ω; TO V-
3. C1 = 0.001μF, R1 = 470Ω; FROM PIN 5 TO GND
4. C1 = 0.05μF, R1 = 10Ω, C2 = 0.02μF, R2 = 39Ω; TO V-
5. C1 = 0.05μF, R1 = 10Ω, C2 = 0.02μF, R2 = 39Ω; TO GND

TYPICAL PERFORMANCE CHARACTERISTICS

 VOLTAGE NOISE DENSITY
vs FREQUENCY

 INPUT WIDEBAND NOISE
vs BANDWIDTH

 NOISE FIGURE vs
SOURCE RESISTANCE

 OPEN-LOOP GAIN vs
TEMPERATURE

 OPEN-LOOP GAIN vs
SUPPLY VOLTAGE

 MAXIMUM OUTPUT SWING
vs FREQUENCY

 INPUT BIAS CURRENT vs
DIFFERENTIAL
INPUT VOLTAGE

 POWER CONSUMPTION vs
SUPPLY VOLTAGE

 OUTPUT SHORT-CIRCUIT
CURRENT


GUARANTEED PERFORMANCE CHARACTERISTICS


These graphs depict maximum error referred to the input as a function of source resistance (R_1). Curves W are shown with V_{OS} trimmed at $+25^\circ\text{C}$ and include errors due to V_{OS} and I_{OS} over the indicated temperature range. Curves Y and Z plot maximum errors with V_{OS} not trimmed.

FEATURES

- Low V_{OS} $25\mu V$ Max
- Low V_{OS} Drift $0.6\mu V/^{\circ}C$ Max
- Ultra-Stable vs Time $1.0\mu V$ /Month Max
- Low Noise $0.6\mu V_{p-p}$ Max
- Wide Input Voltage Range $\pm 14V$
- Wide Supply Voltage Range $\pm 3V$ to $\pm 18V$
- Fits 725, 108A/308A, 741, AD510 Sockets
- $125^{\circ}C$ Temperature-Tested Dice

ORDERING INFORMATION†

$T_A = 25^{\circ}C$ ΔV_{OS} MAX (μV)	PACKAGE				OPERATING TEMPERATURE RANGE
	TO-99	CERDIP	PLASTIC	LCC	
25	OP07AJ*	OP07AZ*	—	—	MIL
75	OP07EJ	OP07EZ	OP07EP	—	COM
75	OP07J*	OP07Z*	—	OP07RC/883	MIL
150	OP07CJ	OP07CZ	OP07CP	—	COM
150	—	—	OP07CS††	—	COM
150	OP07DJ	—	OP07DP	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

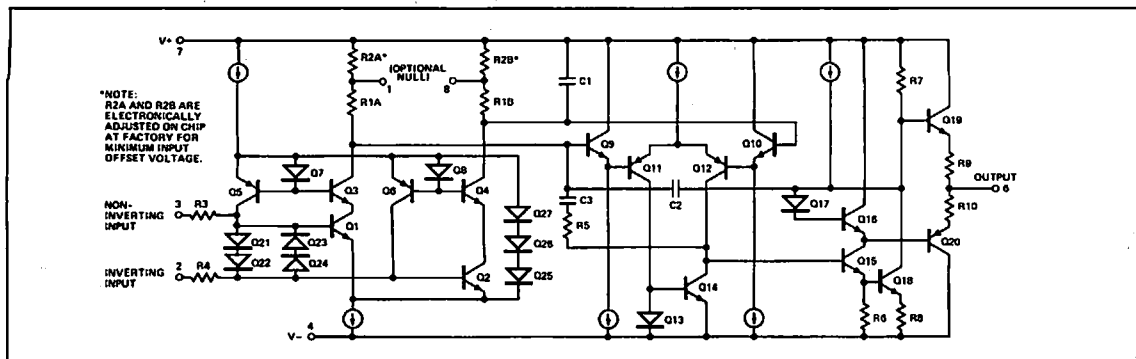
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-07 has very low input offset voltage ($25\mu V$ max for OP-07A) which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current ($\pm 2nA$ for OP-07A) and high open-loop gain ($300V/mV$ for OP-07A). The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain instrumentation applications.

The wide input voltage range of $\pm 13V$ minimum combined with high CMRR of 110dB (OP-07A) and high input impedance provides high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

SIMPLIFIED SCHEMATIC

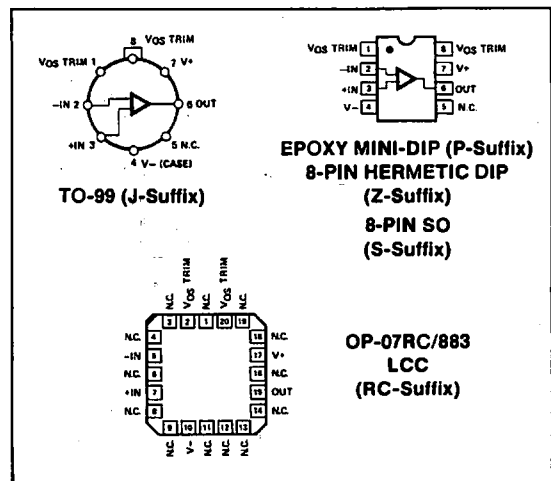


Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP-07, even at high gain, combined with the freedom from external nulling have made the OP-07 a new industry standard for instrumentation and military applications.

The OP-07 is available in five standard performance grades. The OP-07A and the OP-07 are specified for operation over the full military range of $-55^{\circ}C$ to $+125^{\circ}C$; the OP-07 E, C, and D are specified for operation over the $0^{\circ}C$ to $+70^{\circ}C$ range.

The OP-07 is available in hermetically-sealed TO-99 metal can or ceramic 8-pin Mini-DIP, and in epoxy 8-pin Mini-DIP. It is a direct replacement for 725, 108A, and OP-05 amplifiers; 741-types may be directly replaced by removing the 741's nulling potentiometer. The OP-207, a dual OP-07, is available for applications requiring close matching of two OP-07 amplifiers. For improved specifications, see the OP-77.

PIN CONNECTIONS



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, RC and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Operating Temperature Range	
OP-07A, OP-07, OP-07RC	-55°C to +125°C
OP-07E, OP-07C, OP-07D	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature (T _J)	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
LCC (RC)	72°C	7.8mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	(Note 1)	—	10	25	—	30	75	μV
Long-Term Input Offset Voltage Stability	ΔV _{OS} /Time	(Note 2)	—	0.2	1.0	—	0.2	1.0	μV/Mo
Input Offset Current	I _{OS}		—	0.3	2.0	—	0.4	2.8	nA
Input Bias Current	I _B		—	±0.7	±2.0	—	±1.0	±3.0	nA
Input Noise Voltage	e _{np-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.35	0.6	μV _{p-p}
Input Noise Voltage Density	e _n	f _O = 10Hz (Note 3)	—	10.3	18.0	—	10.3	18.0	nV/√Hz
		f _O = 100Hz (Note 3)	—	10.0	13.0	—	10.0	13.0	
		f _O = 1000Hz (Note 3)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i _{np-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	14	30	pA _{p-p}
Input Noise Current Density	i _n	f _O = 10Hz (Note 3)	—	0.32	0.80	—	0.32	0.80	pA/√Hz
		f _O = 100Hz (Note 3)	—	0.14	0.23	—	0.14	0.23	
		f _O = 1000Hz (Note 3)	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R _{IN}	(Note 4)	30	80	—	20	60	—	MΩ
Input Resistance — Common-Mode	R _{INCM}		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±13V	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ±3V to ±18V	—	4	10	—	4	10	μV/V
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2kΩ, V _O = ±10V	300	500	—	200	500	—	V/mV
		R _L ≥ 500Ω, V _O = ±0.5V, V _S = ±3V (Note 4)	150	400	—	150	400	—	
Output Voltage Swing	V _O	R _L ≥ 10kΩ	±12.5	±13.0	—	±12.5	±13.0	—	V
		R _L ≥ 2kΩ	±12.0	±12.8	—	±12.0	±12.8	—	
		R _L ≥ 1kΩ	±10.5	±12.0	—	±10.5	±12.0	—	
Slew Rate	SR	R _L ≥ 2kΩ (Note 3)	0.1	0.3	—	0.1	0.3	—	V/μs
Closed-Loop Bandwidth	BW	A _{VCL} = +1 (Note 3)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R _O	V _O = 0, I _O = 0	—	60	—	—	60	—	Ω
Power Consumption	P _d	V _S = ±15V, No Load	—	75	120	—	75	120	mW
		V _S = ±3V, No Load	—	4	6	—	4	6	
Offset Adjustment Range		R _P = 20kΩ	—	±4	—	—	±4	—	mV

NOTES:1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation.Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV — refer to typical performance curves. Parameter is sample tested.

3. Sample tested.

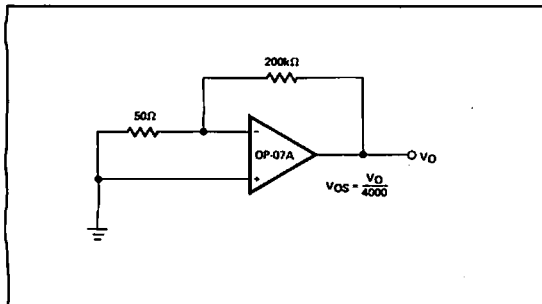
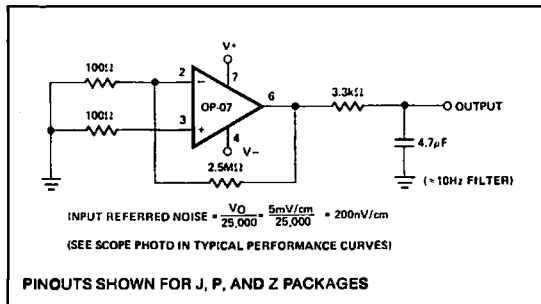
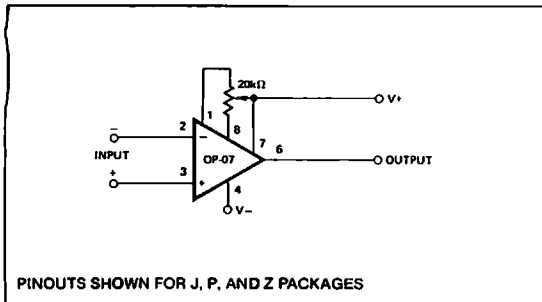
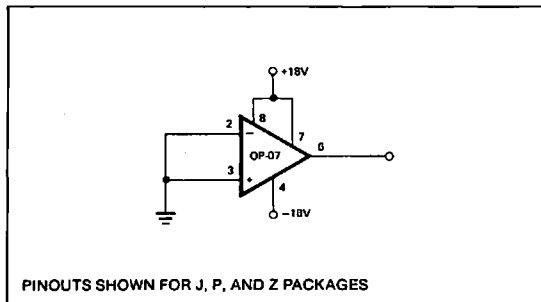
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07A			OP-07			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	25	60	—	60	200	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	0.2	0.6	—	0.3	1.3	$\mu V/^\circ C$
	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.3	1.3	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.8	4	—	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	5	25	—	8	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1	± 4	—	± 2	± 6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	13	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13	± 13.5	—	± 13	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 12.6	—	± 12	± 12.6	—	V

NOTES:

1. OP-07A grade V_{OS} is measured approximately one minute after application of power. For all other grades V_{OS} is measured approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.

TYPICAL OFFSET VOLTAGE TEST CIRCUIT

TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT

OPTIONAL OFFSET NULLING CIRCUIT

BURN-IN CIRCUIT


**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	30	75	—	60	150	—	60	150	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 2)	—	0.3	1.5	—	0.4	2.0	—	0.5	3.0	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	0.5	3.8	—	0.8	6.0	—	0.8	6.0	nA
Input Bias Current	I_B		—	± 1.2	± 4.0	—	± 1.8	± 7.0	—	± 2.0	± 12	nA
Input Noise Voltage	e_{n-p-p}	0.1Hz to 10Hz (Note 3)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 3)	—	10.0	13.0	—	10.2	13.5	—	10.3	13.5	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{n-p-p}	0.1Hz to 10Hz (Note 3)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 3)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 4)	15	50	—	8	33	—	7	31	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	180	—	—	120	—	—	120	—	G Ω
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	94	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	120	400	—	V/mV
		$R_L \geq 500\Omega$	—	—	—	—	—	—	—	—	—	
		$V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 4)	150	400	—	100	400	—	—	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0	—	± 12.0	± 13.0	—	± 12.0	± 13.0	—	V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 11.5	± 12.8	—	± 11.5	± 12.8	—	
		$R_L \geq 1k\Omega$	± 10.5	± 12.0	—	—	± 12.0	—	—	± 12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 3)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 5)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	75	120	—	80	150	—	80	150	mW
		$V_S = \pm 3V$, No Load	—	4	6	—	4	8	—	4	8	
Offset Adjustment Range		$R_P = 20k\Omega$	—	± 4	—	—	± 4	—	—	± 4	—	mV

NOTES:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves. Parameter is sample tested.
3. Sample tested.
4. Guaranteed by design.
5. Guaranteed but not tested.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

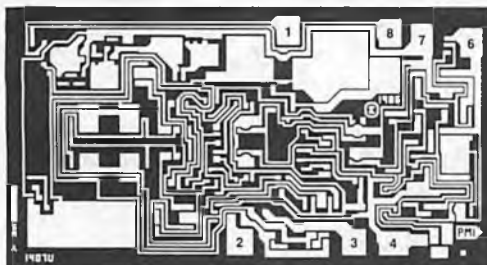
PARAMETER	SYMBOL	CONDITIONS	OP-07E			OP-07C			OP-07D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	45	130	—	85	250	—	85	250	μV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 3)	—	0.3	1.3	—	0.5	1.8	—	0.7	2.5	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.3	—	0.4	1.8	—	0.7	2.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.9	5.3	—	1.6	8.0	—	1.6	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	35	—	12	50	—	12	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1.5	± 5.5	—	± 2.2	± 9.0	—	± 3.0	± 14	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	35	—	18	50	—	18	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	94	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	180	450	—	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 12.6	—	± 11	± 12.6	—	± 11	± 12.6	—	V

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. Sample tested.
3. Guaranteed by design.



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.100 × 0.055 inch, 5500 sq. mils
(2.54 × 1.40 mm, 3.56 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
6. OUTPUT
7. V₊
8. BALANCE

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-07N, OP-07G and OP-07GR devices; $T_A = 125^\circ C$ for OP-07NT and OP-07GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-07NT LIMIT	OP-07N LIMIT	OP-07GT LIMIT	OP-07G LIMIT	OP-07GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		140	40	210	80	150	μV MAX
Input Offset Current	I_{OS}		4.0	2.0	5.6	2.8	6.0	nA MAX
Input Bias Current	I_B		± 4	± 2	± 6	± 3	± 7	nA MAX
Input Resistance Differential-Mode	R_{IN}	(Note 2)	—	20	—	20	8	M Ω MIN
Input Voltage Range	IVR		± 13	± 13	± 13	± 13	± 13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	110	100	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	10	30	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$	—	± 12.5	—	± 12.0	± 12.0	V MIN
		$R_L = 2k\Omega$	± 12.0	± 12.0	± 12.0	± 11.5	± 11.5	
		$R_L = 1k\Omega$	—	± 10.5	—	± 10.5	—	
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	200	200	150	120	120	V/mV MIN
Differential Input Voltage			± 30	± 30	± 30	± 30	± 30	V MAX
Power Consumption	P_d	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

NOTES:

1. For $25^\circ C$ characteristics of OP-07NT and OP-07GT, see OP-07N and OP-07G characteristics, respectively.
2. Guaranteed by design.

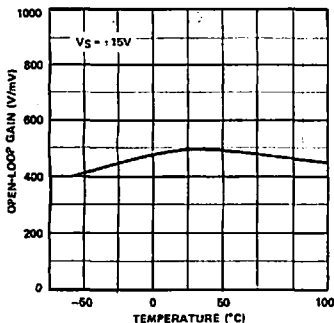
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

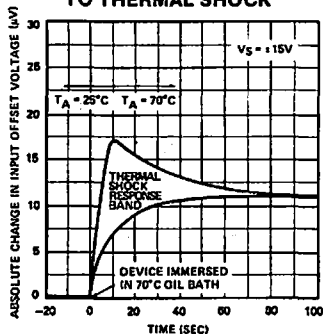
PARAMETER	SYMBOL	CONDITIONS	OP-07NT TYPICAL	OP-07N TYPICAL	OP-07GT TYPICAL	OP-07G TYPICAL	OP-07GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	0.2	0.2	0.3	0.3	0.7	$\mu V/^\circ C$
Nullled Input Offset Voltage Drift	TCV_{OSn}	$R_S = 50\Omega$, $R_P = 20k\Omega$	0.2	0.2	0.3	0.3	0.7	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		5	5	8	8	12	pA/°C
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

TYPICAL PERFORMANCE CHARACTERISTICS

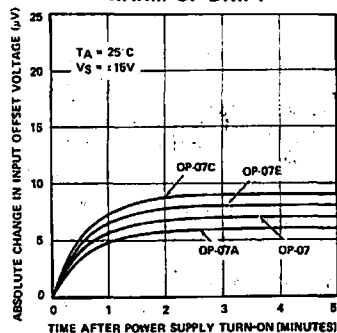
OPEN-LOOP GAIN vs TEMPERATURE



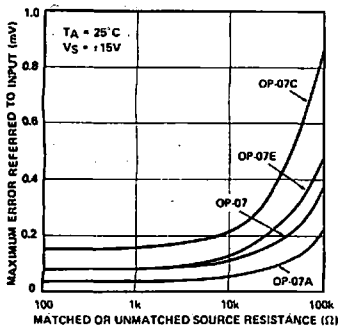
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



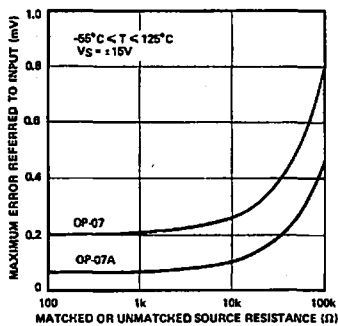
WARM-UP DRIFT



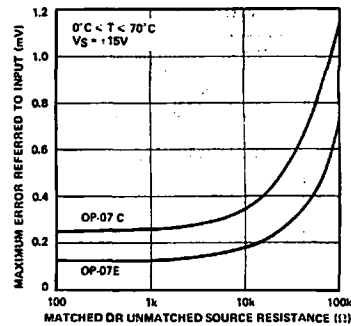
MAXIMUM ERROR vs SOURCE RESISTANCE



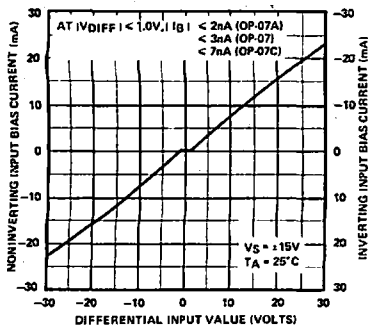
MAXIMUM ERROR vs SOURCE RESISTANCE



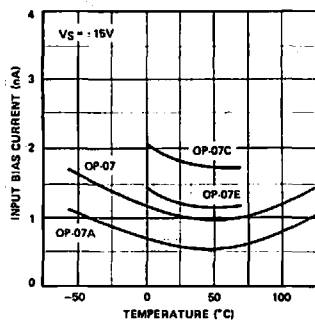
MAXIMUM ERROR vs SOURCE RESISTANCE



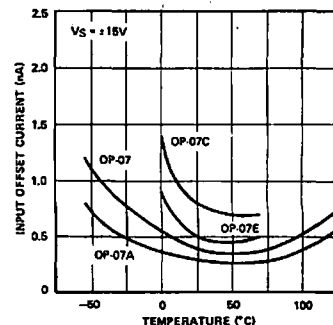
INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

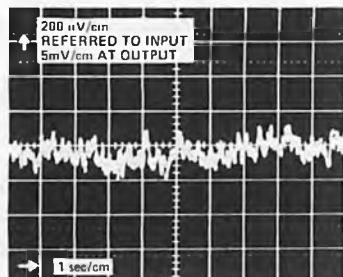
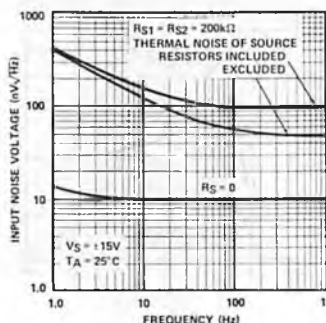
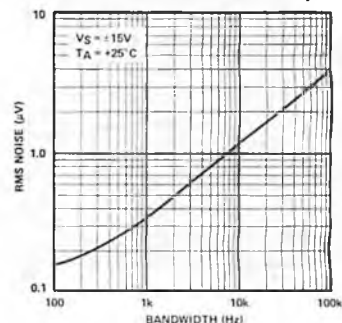


INPUT OFFSET CURRENT vs TEMPERATURE

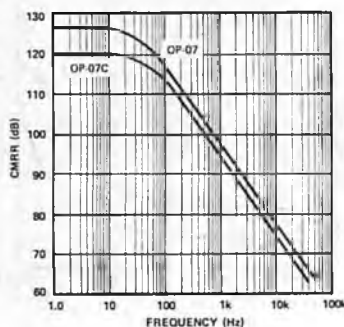


TYPICAL PERFORMANCE CHARACTERISTICS

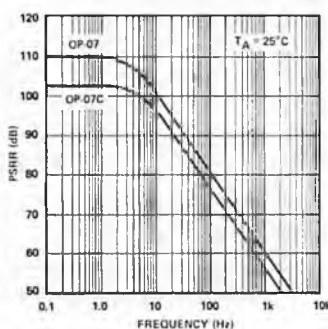
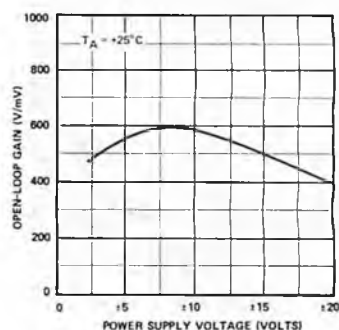
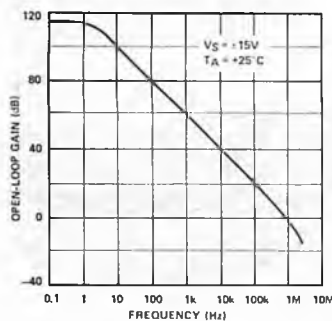
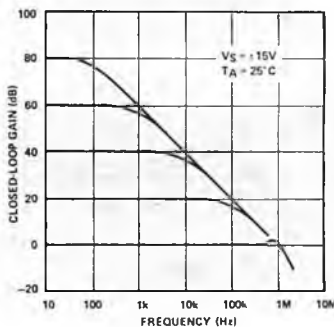
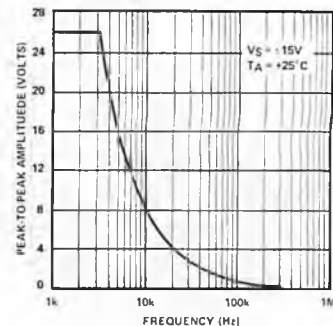
OP-07 LOW FREQUENCY NOISE

TOTAL INPUT NOISE VOLTAGE
vs FREQUENCYINPUT WIDEBAND NOISE vs
BANDWIDTH (0.1Hz TO
FREQUENCY INDICATED)

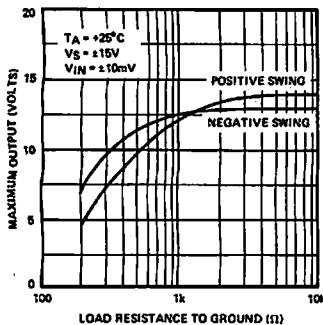
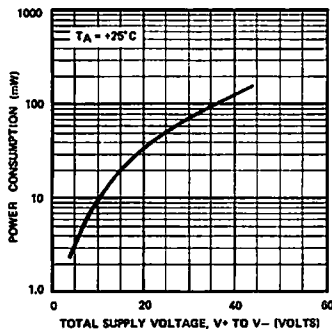
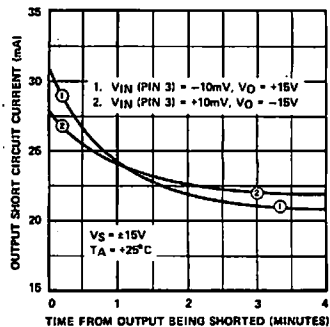
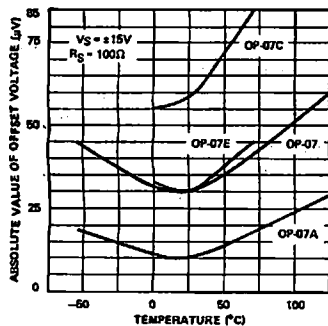
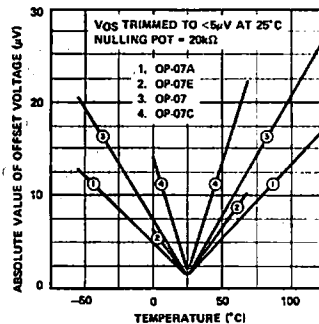
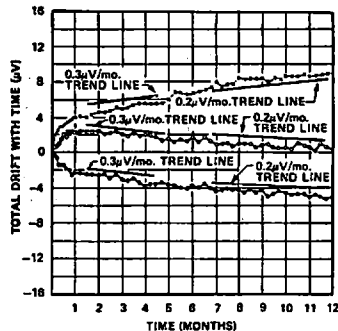
CMRR vs FREQUENCY



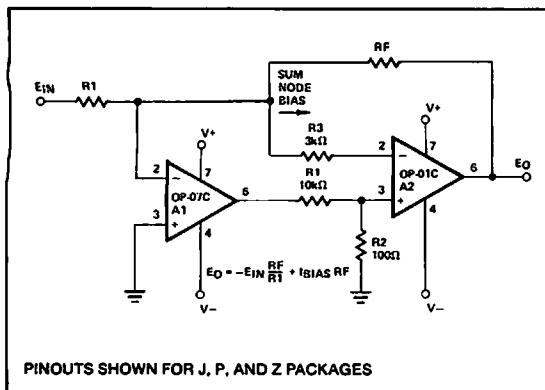
PSRR vs FREQUENCY

OPEN-LOOP GAIN vs
POWER SUPPLY VOLTAGEOPEN-LOOP
FREQUENCY RESPONSECLOSED-LOOP RESPONSE
FOR VARIOUS
GAIN CONFIGURATIONSMAXIMUM OUTPUT SWING
vs FREQUENCY

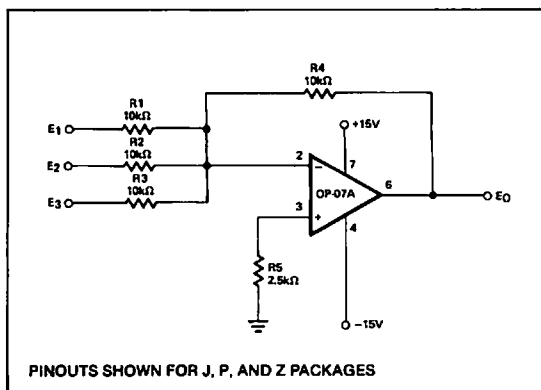
TYPICAL PERFORMANCE CHARACTERISTICS

 MAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCE

 POWER CONSUMPTION
vs POWER SUPPLY

 OUTPUT SHORT-CIRCUIT
CURRENT vs TIME

 UNTRIMMED OFFSET VOLTAGE
vs TEMPERATURE

 TRIMMED OFFSET VOLTAGE
vs TEMPERATURE

 OFFSET VOLTAGE STABILITY
vs TIME


TYPICAL APPLICATIONS

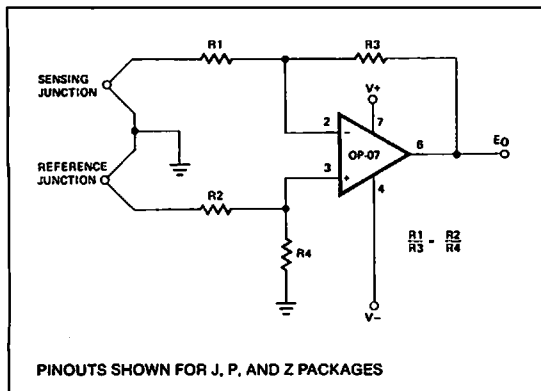
 HIGH SPEED, LOW V_{OS} COMPOSITE AMPLIFIER


ADJUSTMENT-FREE PRECISION SUMMING AMPLIFIER



TYPICAL APPLICATIONS

HIGH-STABILITY THERMOCOUPLE AMPLIFIER

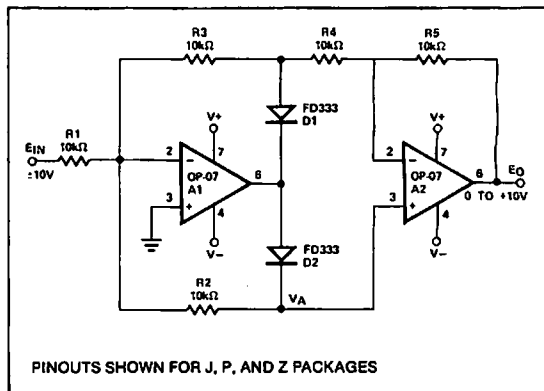


APPLICATIONS INFORMATION

OP-07 series units may be substituted directly into 725, 108A/308A* and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-07 may be used in unnullified 741-type sockets. However, if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. OP-07 offset voltage may be nulled to zero through use of a potentiometer (see offset nulling circuit diagram).

*TO-99 Package only

PRECISION ABSOLUTE-VALUE CIRCUIT



The OP-07 provides stable operation with load capacitance of up to 500pF and $\pm 10V$ swings; larger capacitances should be decoupled with a 50 Ω decoupling resistor.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can degrade drift performance. Therefore, best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the package temperature.

Precision Monolithics Inc.

FEATURES

- Low Offset Voltage 150 μ V Max
- Low Offset Voltage Drift 2.5 μ V/ $^{\circ}$ C Max
- Five Times PM108A Output Current 5mA Min
- Low Offset Current 200pA Max
- Low Bias Current 2nA Max
- Low Power Consumption 18mW Max @ $\pm$ 15V
- High Common-Mode Input Range $\pm$ 13.5V Min
- MIL-STD-883 Class B Processing Available
- Silicon-Nitride Passivation
- 125 $^{\circ}$ C Temperature-Tested Dice

ORDERING INFORMATION†

T _A = 25 $^{\circ}$ C V _{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	DIP 8-PIN	PLASTIC DIP 8-PIN	
0.15	OP08AJ*	OP08AZ*	—	MIL
0.15	OP08EJ	OP08EZ	OP08EP	COM
1.0	—	OP08CZ/883	—	MIL
1.0	—	OP08GZ	—	COM

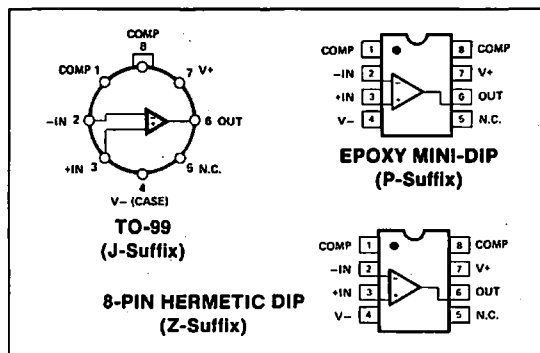
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

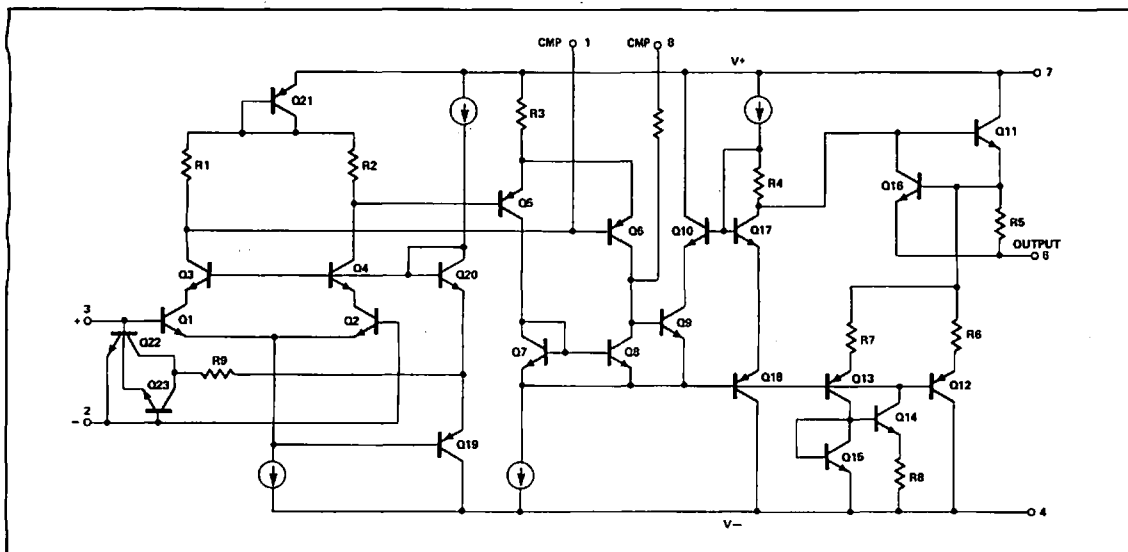
GENERAL DESCRIPTION

The PMI OP-08 is an improved version of the popular LM108A low-power op amp. Excellent performance is achieved by applying PMI's ion-implanted super-beta process and on-chip-zener-zap trimming. The OP-08 has a three-times lower offset voltage and a two-times lower offset voltage drift. Worst-case input offset voltage over -55° C to $+125^{\circ}$ C for the OP-08 is only 350 μ V. In addition, the OP-08 has five times the output current capability of the 108A. For an op amp with identical specifications plus internal frequency compensation, see the OP-12 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 4)

Supply Voltage	
OP-08A, OP-08E (All DICE except GR)	$\pm 20\text{V}$
OP-08C, OP-08G (GR DICE Only)	$\pm 18\text{V}$
Internal Power Dissipation (Note 1)	
500mW	
Differential Input Current (Note 2)	
$\pm 10\text{mA}$	
Input Voltage (Note 3)	
$\pm 15\text{V}$	
Output Short-Circuit Duration	
Indefinite	
Operating Temperature Range	
OP-08A, OP-08C	-55°C to $+125^{\circ}\text{C}$
OP-08E, OP-08G	0°C to $+70^{\circ}\text{C}$
Storage Temperature Range (J, Z)	
-65°C to $+150^{\circ}\text{C}$	
Storage Temperature Range (P)	
-65°C to $+125^{\circ}\text{C}$	
Lead Temperature Range (Soldering, 60 sec)	
300°C	
DICE Junction Temperature (T_J)	
-65°C to $+150^{\circ}\text{C}$	

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	$7.1\text{mW}/^{\circ}\text{C}$
8-Pin Plastic DIP (P)	36°C	$5.6\text{mW}/^{\circ}\text{C}$
8-Pin Hermetic DIP (Z)	75°C	$6.7\text{mW}/^{\circ}\text{C}$

NOTES:

- See table for maximum ambient temperature rating and derating factor.
- The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs without some limiting resistance.
- For supply voltages less than $\pm 15\text{V}$, the absolute maximum input voltage is equal to the supply voltage.
- Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $T_A = +25^{\circ}\text{C}$, $V_S = \pm 20\text{V}$ for A and E Grades, $V_S = \pm 15\text{V}$ for C and G Grades, unless otherwise noted. Compensation capacitor = 30pF.

PARAMETER	SYMBOL	CONDITIONS	OP-08A/E			OP-08C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.25	1.0	mV
Input Offset Current	I_{OS}		—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I_B		—	0.80	2.0	—	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	22	—	—	22	—	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	21	—	—	21	—	
		$f_O = 1000\text{Hz}$	—	20	—	—	20	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	0.15	—	—	0.15	—	$\text{pA}/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	0.14	—	—	0.14	—	
		$f_O = 1000\text{Hz}$	—	0.13	—	—	0.13	—	
Input Resistance — Differential Mode	R_{IN}	(Note 1)	26	70	—	10	50	—	M Ω
Input Voltage Range	IVR	$V_S = \pm 15\text{V}$	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5\text{V}$	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	—	1	7	—	2	63	$\mu\text{V}/\text{V}$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10\text{k}\Omega$, $V_O = \pm 10\text{V}$	80	300	—	40	250	—	V/mV
		$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$, $V_S = \pm 15\text{V}$	50	150	—	—	100	—	
Output Voltage Swing	V_O	$R_L \geq 10\text{k}\Omega$, $V_S = \pm 15\text{V}$	± 13	± 14	—	± 13	± 14	—	V
		$R_L \geq 2\text{k}\Omega$, $V_S = \pm 15\text{V}$	± 10	± 12	—	± 10	± 12	—	
Slew Rate	SR	$R_L \geq 2\text{k}\Omega$	—	0.12	—	—	0.12	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.8	—	—	0.8	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	200	—	—	200	—	Ω
Power Consumption	P_d	$V_S = \pm 15\text{V}$	—	9	18	—	12	24	mW
		$V_S = \pm 5\text{V}$	—	3	6	—	4	8	

NOTE:

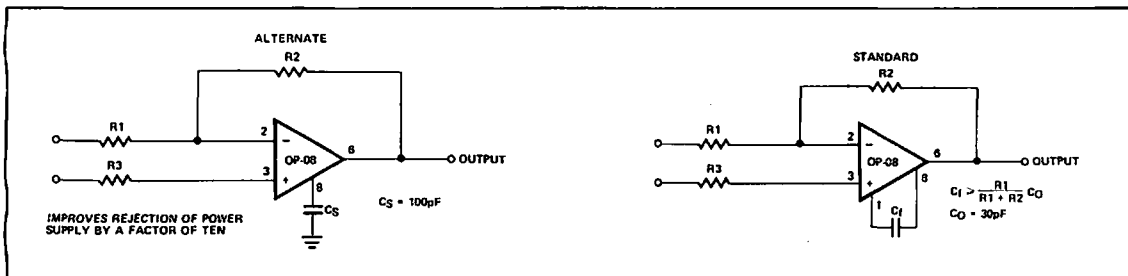
- Guaranteed by input bias current.



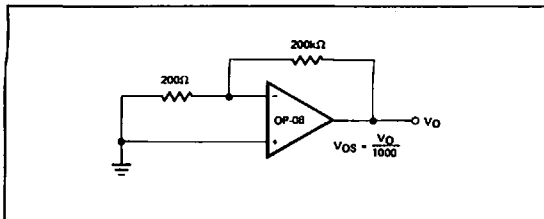
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for C Grade and $V_S = \pm 20V$ for A Grade, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08A			OP-08C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.12	0.35	—	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.5	10	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.12	0.40	—	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	1.0	5.0	$pA/^\circ C$
Input Bias Current	I_B		—	1.2	3.0	—	1.8	10	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	100	110	—	80	106	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	4	10	—	5	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 5k\Omega$, $V_O = \pm 10V$, $V_S = \pm 15V$	40	120	—	15	80	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	V
		$R_L \geq 5k\Omega$, $V_S = \pm 15V$	± 10	± 12	—	± 10	± 12	—	
Power Consumption	P_d	$V_S = \pm 15V$	—	9	18	—	15	24	mW

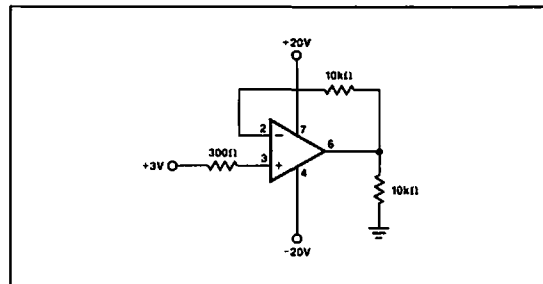
COMPENSATION CIRCUITS



OFFSET VOLTAGE TEST CIRCUIT



BURN-IN CIRCUIT



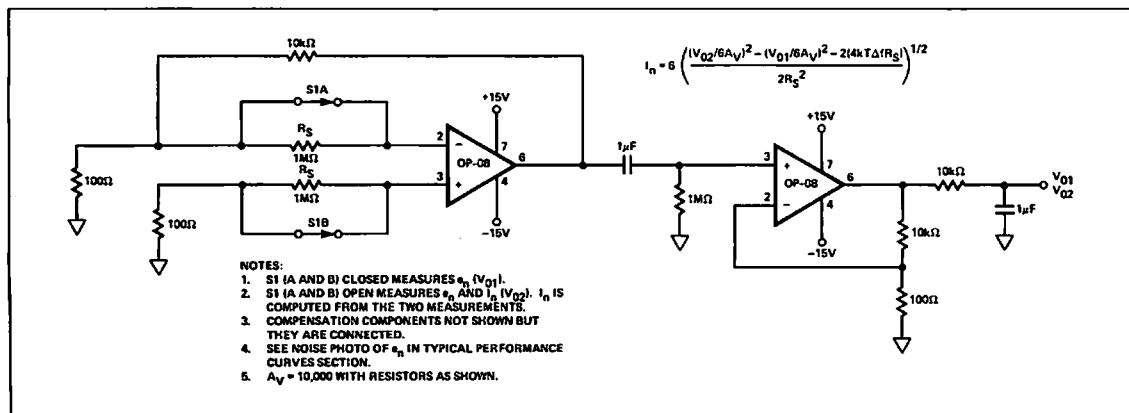
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for G Grade and $V_S = \pm 20V$ for E Grade, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08E			OP-08G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.10	0.25	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.50	2.5	—	1.5	10	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.12	6.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	0.50	2.5	—	2.0	50	$pA/^\circ C$
Input Bias Current	I_B		—	1.0	2.6	—	1.4	6.5	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	2	10	—	3	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	100	—	—	80	—	V/mV
		$R_L \geq 10k\Omega$, $V_O = \pm 10V$, $V_S = \pm 15V$	60	200	—	25	150	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	V
		$R_L \geq 2k\Omega$, $V_S = \pm 15V$	± 10	± 12	—	± 10	± 12	—	
Power Consumption	P_d	$V_S = \pm 15V$	—	9	18	—	15	24	mW

NOTE:

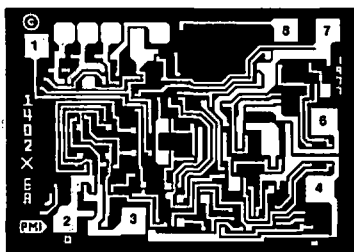
1. Sample tested.

LOW-FREQUENCY NOISE TEST CIRCUIT (0.1 to 10Hz)





DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.059 × 0.043 inch, 2537 sq. mils
(1.50 × 1.09 mm, 1.64 sq. mm)

1. COMPENSATION
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
6. OUTPUT
7. V₊
8. COMPENSATION

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 20V$ and $T_A = 25^\circ C$ for OP-08N and OP-08G devices; $V_S = \pm 20V$ and $T_A = 125^\circ C$ for OP-08NT and OP-08GT devices; $V_S = \pm 15V$ and $T_A = 25^\circ C$ for OP-08GR devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08NT LIMIT	OP-08N LIMIT	OP-08GT LIMIT	OP-08G LIMIT	OP-08GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.35	0.15	0.6	0.3	1.0	mV MAX
Input Offset Current	I_{OS}		0.4	0.2	0.4	0.2	0.5	nA MAX
Input Bias Current	I_B		3	2	4	2	5	nA MAX
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13.5	± 13.5	± 13.5	± 13.5	± 13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$ $V_S = \pm 15V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	$\mu V/V$ MAX
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L \geq 10k\Omega$	± 13	± 13	± 13	± 13	± 13	V MIN
		$R_L \geq 2k\Omega$	—	± 10	—	± 10	± 10	
		$R_L \geq 5k\Omega$	± 10	—	± 10	—	—	
Large-Signal Voltage Gain ($V_O = \pm 10V$)	A_{VO}	$R_L \geq 10k\Omega$	—	80	—	80	40	V/mV MIN
		$R_L \geq 2k\Omega$, $V_S = \pm 15V$	—	50	—	50	—	
		$R_L \geq 5k\Omega$, $V_S = \pm 15V$	40	—	40	—	—	
Input Resistance	R_{IN}	(Note 2)	—	25	—	25	10	M Ω MIN
Supply Current	I_{SV}	$I_{OUT} = 0$, $V_S = \pm 15V$ $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

NOTES:

1. For 25°C characteristics of NT & GT devices, see N & G characteristics, respectively.
2. Guaranteed by input bias current.

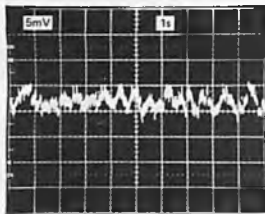
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

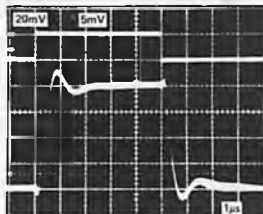
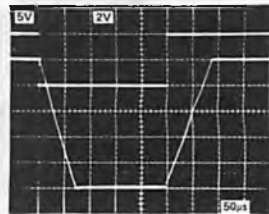
PARAMETER	SYMBOL	CONDITIONS	OP-08NT TYPICAL	OP-08N TYPICAL	OP-08GT TYPICAL	OP-08G TYPICAL	OP-08GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		0.5	0.5	1.0	1.0	1.5	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	0.5	0.5	1.0	pA/°C

TYPICAL PERFORMANCE CHARACTERISTICS

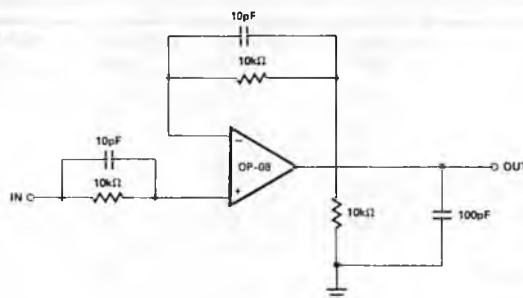
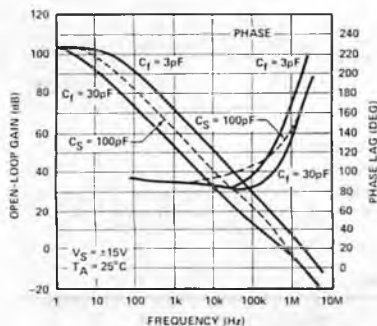
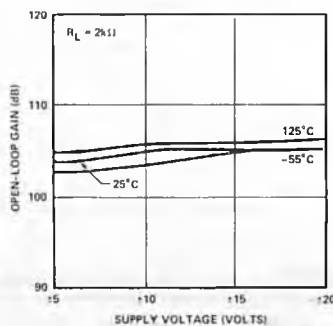
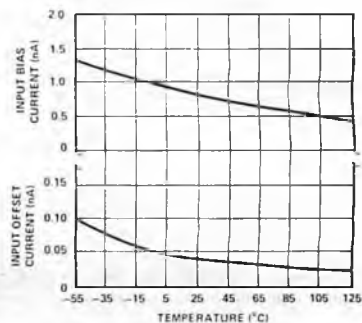
LOW FREQUENCY NOISE



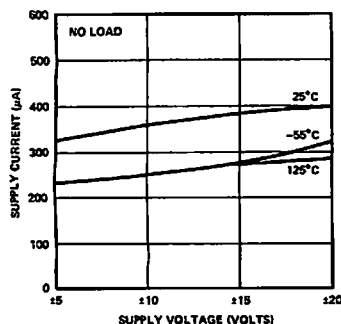
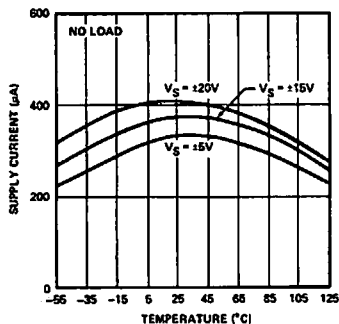
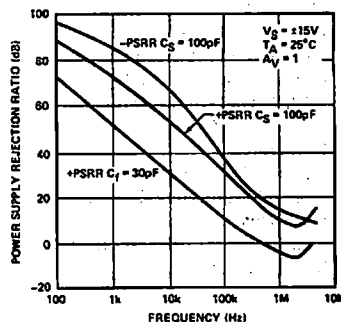
$R_L = 0.8M\Omega$ $f = 0.1Hz$ TO $10Hz$
 $5mV/DIV$ AT READOUT
 $0.5V/DIV$ REFERRED TO INPUT

SMALL-SIGNAL
TRANSIENT RESPONSE

LARGE-SIGNAL
TRANSIENT RESPONSE


TRANSIENT RESPONSE TEST CIRCUIT


OPEN-LOOP GAIN AND PHASE
vs FREQUENCY

OPEN-LOOP GAIN
vs SUPPLY VOLTAGE

INPUT BIAS CURRENT
AND INPUT OFFSET CURRENT
vs TEMPERATURE


TYPICAL PERFORMANCE CHARACTERISTICS

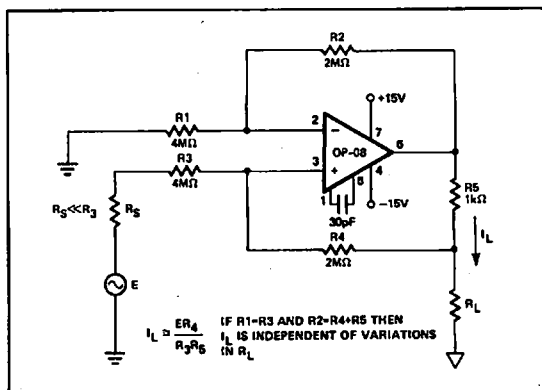
SUPPLY CURRENT
vs SUPPLY VOLTAGESUPPLY CURRENT
vs TEMPERATUREPOWER SUPPLY
REJECTION RATIO (PSRR)
vs FREQUENCY

APPLICATIONS INFORMATION

The OP-08 series has very low input offset and bias currents; the user is cautioned that printed circuit board leakage currents can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is needed to take full advantage of the OP-08 performance. Board leakage is minimized by encircling the input pins with a guard ring maintained at the same potential as the inputs. This guard ring should be driven by a low impedance source, such as an amplifier's output or ground.

TYPICAL APPLICATION

BILATERAL CURRENT SOURCE





OP-09/OP-11

QUAD MATCHED
741-TYPE OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

FEATURES

- Guaranteed V_{OS} 500 μ V Max
- Guaranteed Matched CMRR 84dB Min
- Guaranteed Matched V_{OS} 750 μ V Max
- RC/RM4136 Direct Replacement (OP-09)
- LM148/LM348 Direct Replacement (OP-11)
- Low Noise
- Silicon-Nitride Passivation
- Internal Frequency Compensation
- Low Crossover Distortion
- Continuous Short-Circuit Protection
- Low Input Bias Current

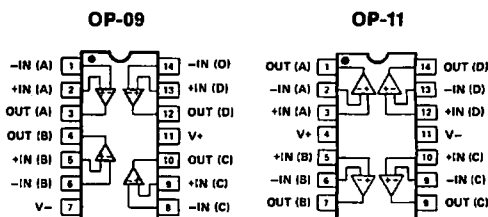
ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC DIP 14-PIN	EPOXY DIP 14-PIN	LCC	
0.5	OP-09AY* OP-11AY*	—	OP11ARC/883	MIL
0.5	OP-09EY OP-11EY	OP-11EP	—	COM
2.5	OP-11BY*	—	—	MIL
2.5	OP-09FY OP-11FY	OP-09FP OP-11FP	—	COM
5.0	OP-11CY/883	—	—	MIL
5.0	—	OP-11GP	—	COM

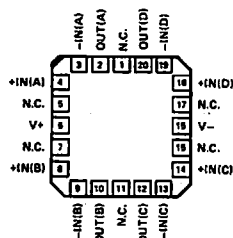
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

PIN CONNECTIONS

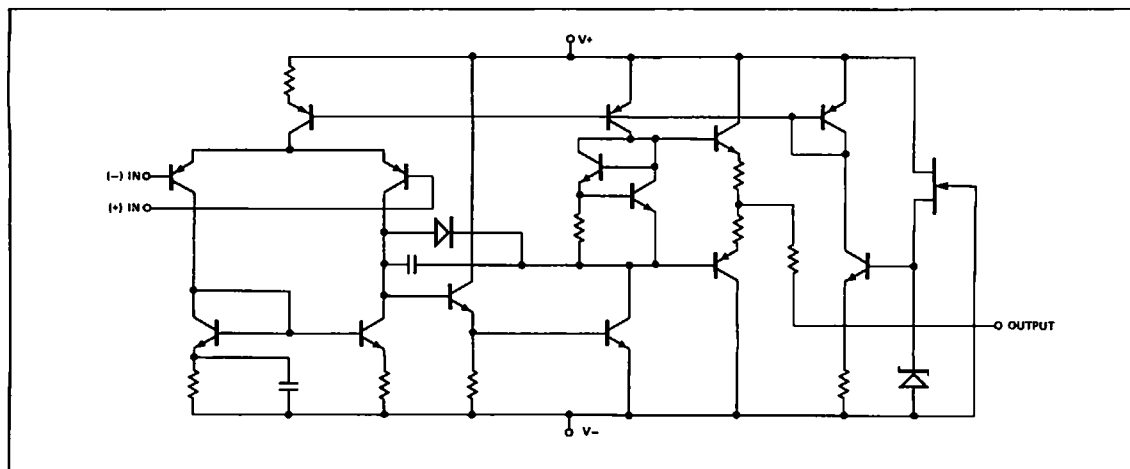


14-PIN HERMETIC DIP (Y-Suffix)
EPOXY DIP (P-Suffix)



OP-11ARC/883
LCC
(RC-Suffix)

SIMPLIFIED SCHEMATIC (One of Four Amplifiers is Shown)



GENERAL DESCRIPTION

The OP-09 and OP-11 provide four matched 741-type operational amplifiers in a single 14-pin DIP package. The OP-11 is pin compatible with the LM148, LM348, RM4156, and HA4741 amplifiers. The OP-09 is pin compatible with the RM4136 and RC4136. The amplifiers are matched for common-mode rejection ratio and offset voltage which is very important in designing instrumentation amplifiers. In addition, the amplifier is designed to have equal positive-going and negative-going slew rates. This is an important consideration for good audio system performance.

Each of the four amplifiers has the proven OP-02 advantages of low noise, low drift, and excellent long-term stability. Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process reduces "popcorn noise", provides high reliability, and assures long-term stability of parameters.

The OP-09 and OP-11 are ideal for use in designs requiring minimum space and cost while maintaining OP-02-type performance.

OP-09's and OP-11's with processing per the requirements of MIL-STD-883 are available. For dual-741-type versions, see the OP-04/14 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±22V
OP-09GR and OP-11GR (Only)	±18V
Internal Power Dissipation (Note 1)	
RC, Y-Package	800mW
P-Package	500mW

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, $R_S \leq 100\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.5	0.75	—	0.8	2.0	mV
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 12V$ $V_{CM} = \pm 12V$	—	1	20	—	1	20	$\mu V/V$ dB
			94	120	—	94	120	—	

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-09A, OP-09B, OP-11A and OP-11B, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-09E, OP-09F, OP-11E and OP-11F, $R_S \leq 100\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A, OP-09E OP-11A, OP-11E			OP-09B, OP-09F OP-11B, OP-11F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.6	1.0	—	1.0	2.5	mV
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 12V$ $V_{CM} = \pm 12V$	—	3.2	20	—	3.2	20	$\mu V/V$ dB
			94	110	—	94	110	—	

Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous (One Amplifier Only)

Storage Temperature Range

RC, Y-Package	−65°C to +150°C
P-Package	−65°C to +125°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_J)	−65°C to +150°C

Operating Temperature Range

OP-09A, OP-09B	−55°C to +125°C
OP-09E, OP-09F	0°C to +70°C
OP-11A, OP-11B,	
OP-11C, OP-11ARC	−55°C to +125°C
OP-11E, OP-11F, OP-11G	0°C to +70°C

NOTES:

- See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	70°C	10.0mW/°C
14-Pin Plastic DIP (P)	42°C	6mW/°C
LCC (RC)	70°C	7.8mW/°C

- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

**ELECTRICAL CHARACTERISTICS** (Each Amplifier) at $V_S = \pm 15V$ $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A/E OP-11A/E			OP-09B/F OP-11B/F			OP-11C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.3	0.5	—	0.6	2.5	—	1.2	5.0	mV
Input Offset Current	I_{OS}		—	5.5	20	—	25	50	—	75	200	nA
Input Bias Current	I_B		—	180	300	—	300	500	—	300	500	nA
Input Resistance Differential Mode	R_{IN}	(Note 3)	0.17	0.29	—	0.1	0.17	—	0.1	0.17	—	M Ω
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	$\mu V/V$
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11	± 13	—	± 11	± 13	—	± 11	± 13	—	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	100	650	—	100	650	—	50	500	—	V/mV
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	105	180	—	123	180	—	210	340	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.7	—	—	0.7	—	—	0.7	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	18	—	—	18	—	—	18	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	14	—	—	14	—	—	14	—	
		$f_O = 1000Hz$	—	12	—	—	12	—	—	12	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	17	—	—	17	—	—	17	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$	—	1.8	—	—	1.8	—	—	1.8	—	$pA/\sqrt{Hz}$
		$f_O = 100Hz$	—	1.5	—	—	1.5	—	—	1.5	—	
		$f_O = 1000Hz$	—	1.2	—	—	1.2	—	—	1.2	—	
Channel Separation	CS		100	130	—	100	130	—	—	130	—	dB
Slew Rate (Note 2)	SR		0.7	1.0	—	0.7	1.0	—	0.7	1.0	—	V/ μs
Large-Signal Bandwidth (Note 2)		$V_O = 20V_{p-p}$	11	16	—	11	16	—	11	16	—	kHz
Closed-Loop Bandwidth (Note 4)	BW	$A_{VCL} = +1.0$	2.4	3.0	—	2.4	3.0	—	2.4	3.0	—	MHz
Risetime (Note 2)	t_r	$A_V = +1$, $V_{IN} = 50mV$	—	110	145	—	110	145	—	110	145	ns
Overshoot (Note 2)	OS		—	15	25	—	15	25	—	15	25	%

NOTES:

1. Total dissipation for all four amplifiers in package.
2. Sample tested.
3. Guaranteed by input bias current.
4. Guaranteed by risetime.

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09A OP-11A			OP-09B OP-11B			OP-11C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.4	1.0	—	1.0	3.5	—	1.5	6.0	mV
Average Input Offset Voltage Drift (Note 3)	TCV_{OS}	$R_S \leq 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	20	40	—	40	80	—	250	300	nA
Average Input Offset Current Drift (Note 3)	TCI_{OS}		—	0.1	0.3	—	0.3	0.6	—	0.3	0.6	$nA/^\circ C$
Input Bias Current	I_B		—	200	375	—	400	650	—	400	800	nA
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11	± 13	—	± 11	± 13	—	± 11	± 13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

ELECTRICAL CHARACTERISTICS (Each Amplifier) at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09E OP-11E			OP-09F OP-11F			OP-11G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.4	0.8	—	0.8	3.0	—	1.5	6.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 10k\Omega$	—	2.0	10	—	4.0	15	—	4.0	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	14	30	—	40	60	—	250	300	nA
Average Input Offset Current Drift (Note 3)	TCI_{OS}		—	0.1	0.3	—	0.3	0.6	—	0.3	0.6	$nA/^\circ C$
Input Bias Current	I_B		—	200	350	—	400	550	—	400	800	nA
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$, $R_S \leq 10k\Omega$	100	120	—	100	120	—	70	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$, $R_S \leq 10k\Omega$	—	4	32	—	4	32	—	10	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	250	—	50	250	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11	± 13	—	± 11	± 13	—	± 11	± 13	—	V
Power Consumption (Note 1)	P_d	$V_O = 0V$	—	115	200	—	115	200	—	250	400	mW

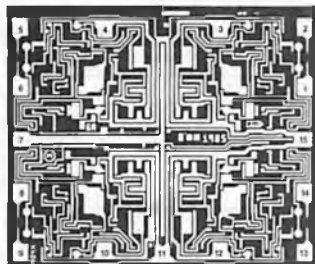
NOTES:

1. Total dissipation for all four amplifiers in package.
2. Sample tested.
3. Guaranteed but not tested.



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)

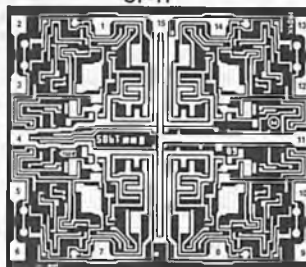
OP-09



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. OUTPUT (A)
4. OUTPUT (B)
5. NONINVERTING INPUT (B)
6. INVERTING INPUT (B)
7. V -
8. INVERTING INPUT (C)
9. NONINVERTING INPUT (C)
10. OUTPUT (C)
11. V -
12. OUTPUT (D)
13. NONINVERTING INPUT (D)
14. INVERTING INPUT (D)
15. V -

DIE SIZE 0.086 × 0.072 inch, 6192 sq. mils
(2.18 × 1.83 mm, 3.99 sq. mm)

OP-11



1. OUTPUT (A)
2. INVERTING INPUT (A)
3. NONINVERTING INPUT (A)
4. V -
5. NONINVERTING INPUT (B)
6. INVERTING INPUT (B)
7. OUTPUT (B)
8. OUTPUT (C)
9. INVERTING INPUT (C)
10. NONINVERTING INPUT (C)
11. V -
12. NONINVERTING INPUT (D)
13. INVERTING INPUT (D)
14. OUTPUT (D)
15. V -

DIE SIZE 0.086 × 0.072 inch, 6192 sq. mils
(2.18 × 1.83 mm, 3.99 sq. mm)

NOTE:

Either or both V+ pads may be used without any change in performance.

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-09/11N, OP-09/11G and OP-09/11GR devices; $T_A = 125^\circ C$ for OP-09/11NT and OP-09/11GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09NT OP-11NT LIMIT	OP-09N OP-11N LIMIT	OP-09GT OP-11GT LIMIT	OP-11G LIMIT	OP-09GR OP-11GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	1.0	0.5	3.5	2.5	5.0	mV MAX
Input Offset Current	I_{OS}		20	20	50	50	200	nA MAX
Input Bias Current	I_B		300	300	500	500	500	nA MAX
Input Voltage Range	IVR		± 12	± 12	± 12	± 12	± 12	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$ $R_S \leq 10k\Omega$	100	100	100	100	70	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$ $R_S \leq 10k\Omega$	32	32	32	32	100	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $R_L = 2k\Omega$	± 11 ± 11	± 12 ± 11	± 11 ± 11	± 12 ± 11	± 11 ± 11	V MIN
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	100	50	100	50	V/mV MIN
Power Consumption (Four Amplifiers)	P_d	$V_{OUT} = 0$ No Load	200	180	200	180	340	mW MAX

NOTES:

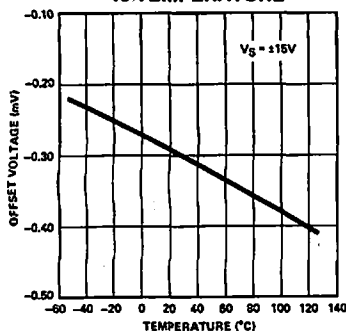
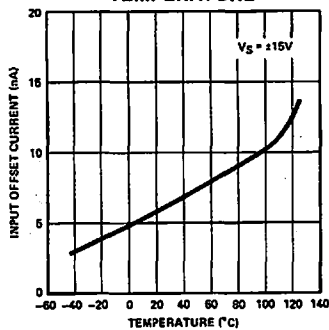
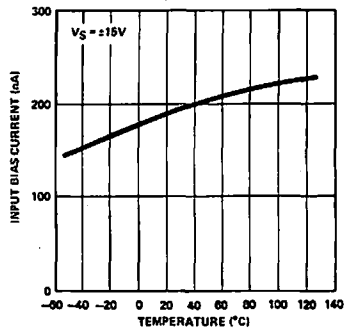
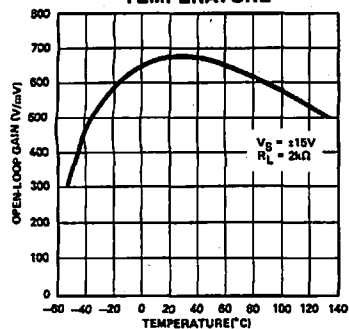
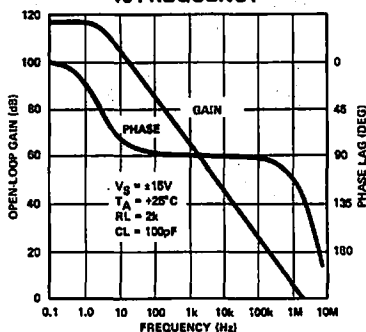
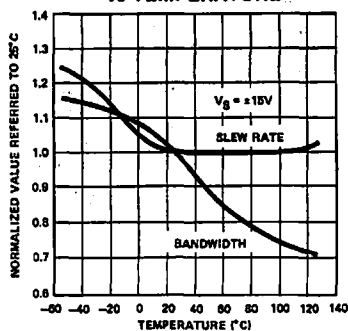
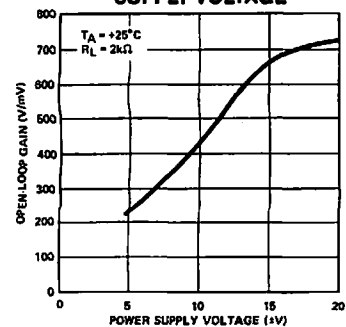
For 25°C characteristics of NT & GT devices, see N & G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

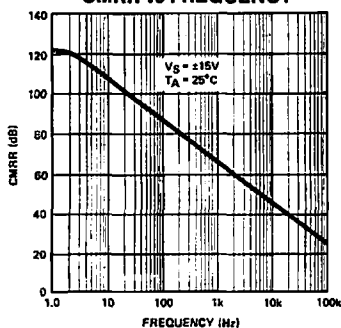
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-09NT OP-11NT TYPICAL	OP-09N OP-11N TYPICAL	OP-09GT OP-11GT TYPICAL	OP-11G TYPICAL	OP-09GR OP-11GR TYPICAL	UNITS
Slew Rate	SR	$A_V = 1$ $R_L \geq 2k\Omega$	1	1	1	1	1	V/ μs
Unity Gain Bandwidth	GBW		2	2	2	2	2	MHz
Channel Separation	CS	$A_V = 100$ $f = 10kHz$ $R_S = 1k\Omega$	130	130	130	130	130	dB

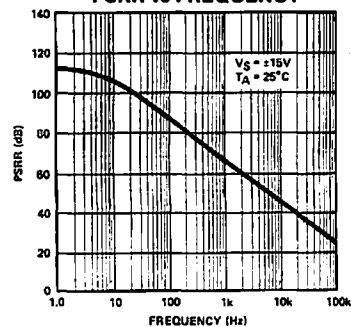
TYPICAL PERFORMANCE CHARACTERISTICS

 INPUT OFFSET VOLTAGE
vs TEMPERATURE

 OFFSET CURRENT vs
TEMPERATURE

 BIAS CURRENT vs
TEMPERATURE

 OPEN-LOOP GAIN vs
TEMPERATURE

 OPEN-LOOP GAIN AND PHASE
vs FREQUENCY

 NORMALIZED SLEW RATE
AND BANDWIDTH
vs TEMPERATURE

 OPEN-LOOP GAIN vs
SUPPLY VOLTAGE


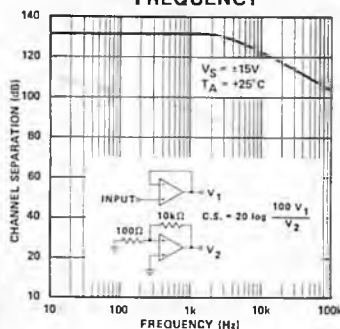
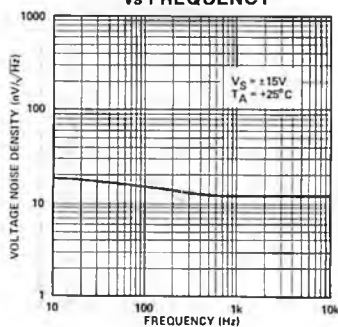
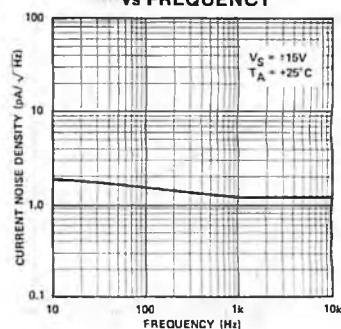
CMRR vs FREQUENCY



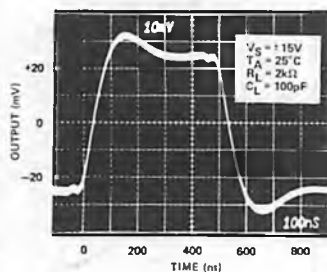
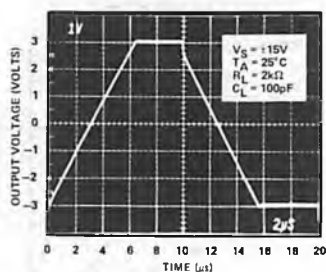
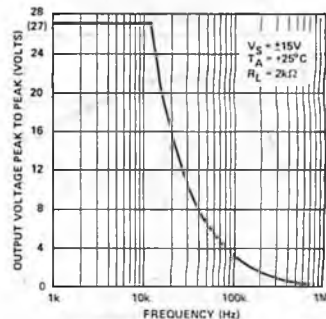
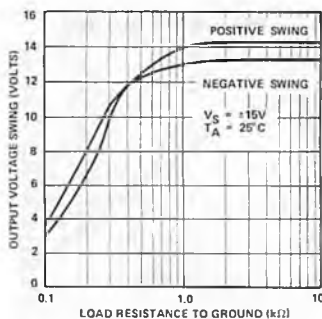
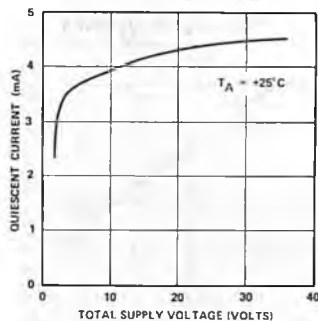
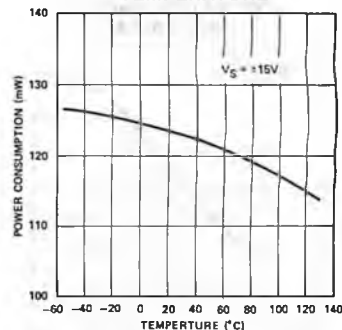
PSRR vs FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS

CHANNEL SEPARATION vs
FREQUENCYNOISE VOLTAGE DENSITY
vs FREQUENCYNOISE CURRENT DENSITY
vs FREQUENCY

TRANSIENT RESPONSE

VOLTAGE FOLLOWER
PULSE RESPONSEMAXIMUM OUTPUT SWING
vs FREQUENCYOUTPUT VOLTAGE vs
LOAD RESISTANCEQUIESCENT CURRENT vs
SUPPLY VOLTAGEPOWER CONSUMPTION vs
TEMPERATURE

FEATURES

- **Extremely Tight Matching**
- **Excellent Individual Amplifier Parameters**
- **Offset Voltage Match** 0.18mV Max
- **Offset Voltage Match vs Temp.** 0.8 μ V/ $^{\circ}$ C Max
- **Common-Mode Rejection Match** 114dB Min
- **Power Supply Rejection Match** 100dB Min
- **Bias Current Match** 3.0nA Max
- **Low Noise** 0.6 μ V_{p-p} Max
- **Low Bias Current** 3.0nA Max
- **High Common-Mode Input Impedance** 200G Ω Typ
- **Excellent Channel Separation** 128dB Min

ORDERING INFORMATION†

T _A = 25 $^{\circ}$ C V _{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
0.5	OP10AY*	MIL
0.5	OP10EY	COM
0.5	OP10Y*	MIL
0.5	OP10CY	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

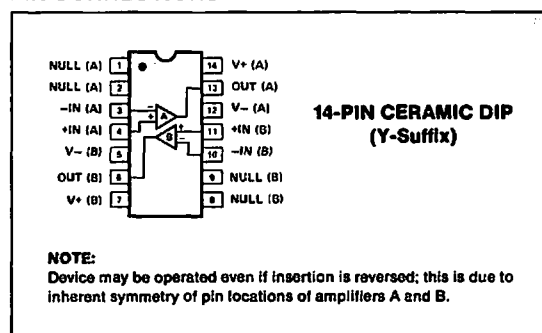
The OP-10 series of dual-matched instrumentation operational amplifiers consists of two independent monolithic high-performance operational amplifiers in a single 14-pin dual-in-line package. Tight matching of critical parameters

is provided between channels of the dual operational amplifier.

The excellent specifications of the individual amplifiers and tight matching over temperature enable construction of high-performance instrumentation amplifiers. The designer can achieve the guaranteed specifications because the common package eliminates temperature differentials which occur in designs using separately housed amplifiers.

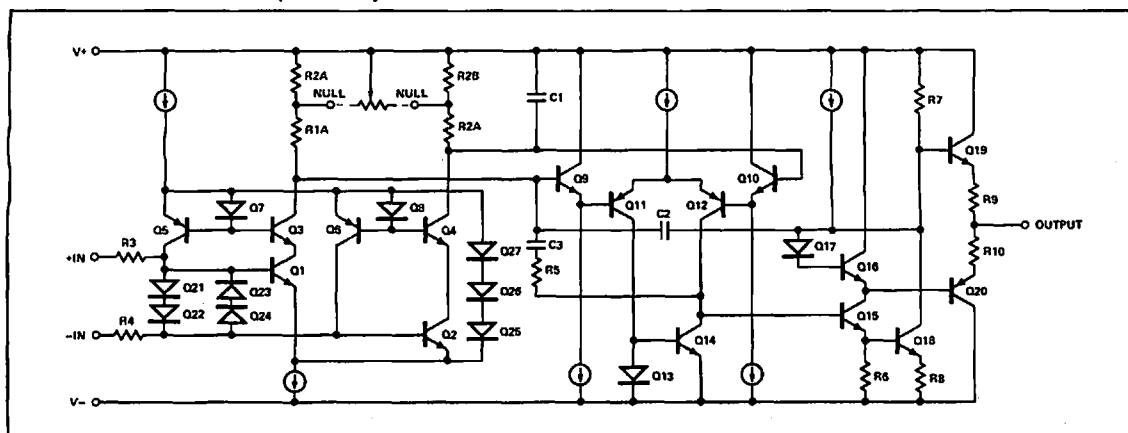
Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode and power-supply rejection ratios. The individual amplifiers feature extremely low offset voltage, offset voltage drift, low noise voltage, low bias current, internal compensation and input/output protection.

PIN CONNECTIONS



OPERATIONAL AMPLIFIERS

SIMPLIFIED SCHEMATIC (1/2 OP-10)



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	$\pm 22V$
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	$\pm 30V$
Input Voltage (Note 2)	$\pm 22V$
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature Range	
OP-10A, OP-10	$-55^{\circ}C$ to $+125^{\circ}C$
OP-10E, OP-10C	$0^{\circ}C$ to $+70^{\circ}C$

DICE Junction Temperature (T_J) $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temperature Range (Soldering, 60 sec) $300^{\circ}C$

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
Dual-In-Line (Y)	$106^{\circ}C$	$11.3mW/^{\circ}C$

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. For supply voltages less than $\pm 22V$, the absolute maximum input voltage is equal to the supply voltage.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Notes 1, 2)	—	0.25	1.0	—	0.25	1.0	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	1.0	2.8	—	1.0	2.8	nA
Input Bias Current	I_B		—	± 1	± 3	—	± 1	± 3	nA
Input Noise Voltage	e_{np-p}	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{\text{Hz}}$
		(Note 2) $f_O = 100\text{Hz}$	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{np-p}	(Note 2) 0.1Hz to 10Hz	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.32	0.80	$pA/\sqrt{\text{Hz}}$
		(Note 2) $f_O = 100\text{Hz}$	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	20	60	—	20	60	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	G Ω
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	10	—	4	10	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	200	500	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 3)	150	500	—	150	500	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0	—	± 12.5	± 13.0	—	V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 12.0	± 12.8	—	
		$R_L \geq 1k\Omega$	± 10.5	± 12.0	—	± 10.5	± 12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	Each Amplifier	—	90	120	—	90	120	mW
		$V_S = \pm 3V$	—	4	6	—	4	6	
Offset Adjustment Range		$R_P = 20k\Omega$	—	± 4	—	—	± 4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.3	0.7	—	0.3	0.7	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	0.7	2.0	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.0	—	0.3	1.0	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1.8	5.6	—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	50	—	8	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 2	± 6	—	± 2	± 6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	50	—	13	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	400	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 12.0	± 12.6	—	V

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	ΔV_{OS}		—	0.07	0.18	—	0.12	0.5	mV
Average Noninverting Bias Current	I_{B+}		—	± 1.0	± 3.0	—	± 1.3	± 4.5	nA
Noninverting Offset Current	I_{OS+}		—	0.8	2.8	—	1.1	4.5	nA
Inverting Offset Current	I_{OS-}		—	0.8	2.8	—	1.1	4.5	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	114	123	—	106	120	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	3	10	—	4	20	$\mu V/V$
Channel Separation	CS	(Note 2)	126	140	—	126	140	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.1	0.3	—	0.2	0.9	mV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 2)	—	0.45	1.3	—	0.9	2.5	$\mu V/^\circ C$
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 3) Channel A only	—	0.3	0.8	—	0.4	1.2	$\mu V/^\circ C$

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

**MATCHING CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Average Noninverting Bias Current	I_{B+}		—	± 2.0	± 6.0	—	± 2.4	± 8.0	nA
Average Drift of Noninverting Bias Current	TCI_{B+}	(Note 2)	—	10	40	—	15	—	pA/ $^\circ C$
Noninverting Offset Current	I_{OS+}		—	2.0	6.5	—	2.4	9.0	nA
Average Drift of Noninverting Offset Current	TCI_{OS+}	(Note 2)	—	12	50	—	18	—	pA/ $^\circ C$
Inverting Offset Current	I_{OS-}		—	2.0	6.5	—	2.4	9.0	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	108	120	—	103	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	6	20	—	7	32	$\mu V/V$

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.2	0.5	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Notes 1, 2)	—	0.3	1.5	—	0.5	—	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	I_B		—	± 1.2	± 4.0	—	± 1.8	± 7.0	nA
Input Noise Voltage	e_{n-p-p}	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.5	20.0	$nV/\sqrt{\text{Hz}}$
		(Note 2) $f_O = 100\text{Hz}$	—	10.0	13.0	—	10.2	13.5	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.8	11.5	
Input Noise Current	i_{n-p-p}	(Note 2) 0.1Hz to 10Hz	—	14	30	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.35	0.90	$pA/\sqrt{\text{Hz}}$
		(Note 2) $f_O = 100\text{Hz}$	—	0.14	0.23	—	0.15	0.27	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	15	50	—	8	33	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	160	—	—	120	—	G Ω
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	10	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	120	400	—	V/mV
		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$ (Note 3)	150	500	—	100	400	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0	—	± 12.0	± 13.0	—	V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 11.5	± 12.8	—	
		$R_L \geq 1k\Omega$	± 10.5	± 12.0	—	—	± 12.0	—	

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Stewing Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0, I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	Each Amplifier	—	90	120	—	95	150	mW
		$V_S = \pm 3V$	—	4	6	—	4	8	
Offset Adjustment Range		$R_P = 20k\Omega$	—	± 4	—	—	± 4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	(Note 2)	—	0.7	2.0	—	1.2	4.5	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.0	—	0.4	1.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	8	50	—	12	50	$pA/^\circ C$
Input Bias Current	I_B		—	± 1.5	± 5.5	—	± 2.2	± 8.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	13	50	—	18	50	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega, V_O = \pm 10V$	100	400	—	100	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.6	—	± 11.0	± 12.6	—	V

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$ — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

**MATCHING CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.12	0.5	—	0.3	—	mV
Average Noninverting Bias Current	I_{B+}		—	± 1.3	± 4.5	—	± 2.0	—	nA
Noninverting Offset Current	I_{OS+}		—	1.1	4.5	—	1.8	—	nA
Inverting Offset Current	I_{OS-}		—	1.1	4.5	—	1.8	—	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	106	120	—	—	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	5	—	$\mu V/V$
Channel Separation	CS	(Note 1)	126	140	—	120	137	—	dB

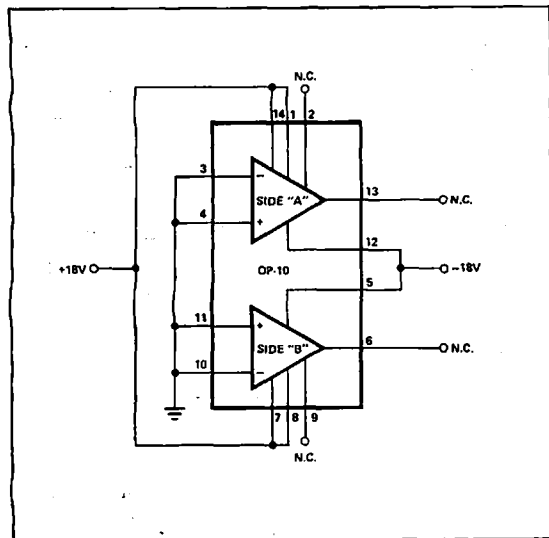
MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	0.18	0.7	—	0.4	—	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.9	2.3	—	1.3	—	$\mu V/^\circ C$
With External Trim	$TC\Delta V_{OSn}$	$R_L = 20k\Omega$ Channel A Only (Note 2)	—	0.3	0.9	—	0.6	—	$\mu V/^\circ C$
Average Noninverting Bias Current	I_{B+}		—	± 2.0	± 6.0	—	± 2.8	—	nA
Average Drift of Noninverting Bias Current	TCI_{B+}	(Note 1)	—	12	40	—	18	—	$pA/^\circ C$
Noninverting Offset Current	I_{B+}		—	2.0	6.0	—	2.8	—	nA
Average Drift of Noninverting Offset Current	TCI_{OS+}	(Note 1)	—	15	50	—	20	—	$pA/^\circ C$
Input Offset Current	I_{OS-}		—	2.0	6.0	—	2.8	—	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	103	117	—	—	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	6	32	—	8	—	$\mu V/V$

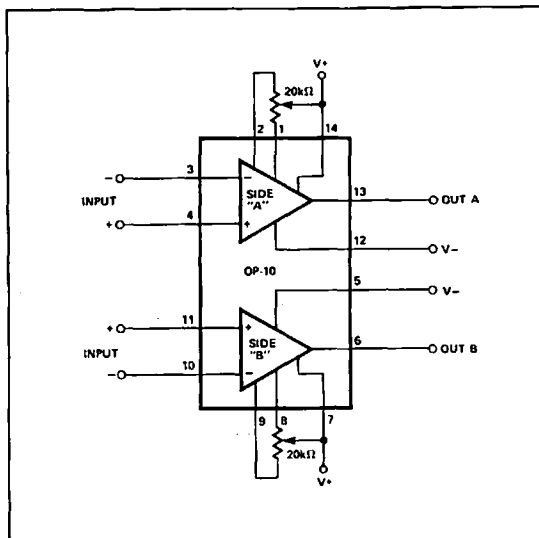
NOTES:

1. Sample tested.
2. Guaranteed by design.

BURN-IN CIRCUIT

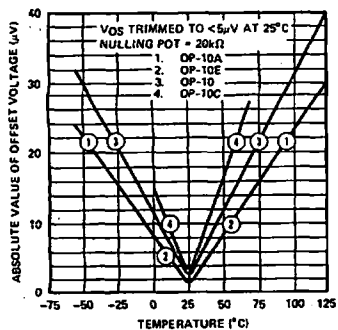


OFFSET NULLING CIRCUIT

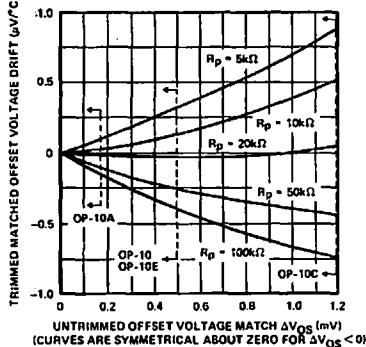


TYPICAL PERFORMANCE CHARACTERISTICS

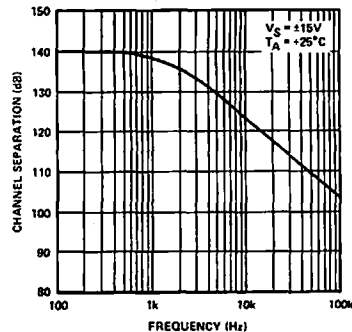
MATCHING CHARACTERISTICS TRIMMED OFFSET VOLTAGE MATCH vs TEMPERATURE



MATCHING CHARACTERISTICS TRIMMED MATCHED OFFSET VOLTAGE DRIFT AS A FUNCTION OF TRIMMING POT (R_P) SIZE AND ΔV_{OS}

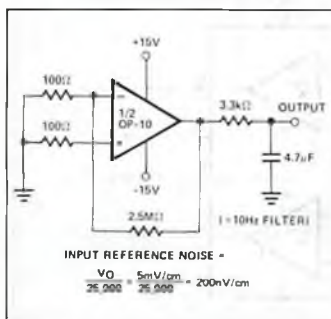
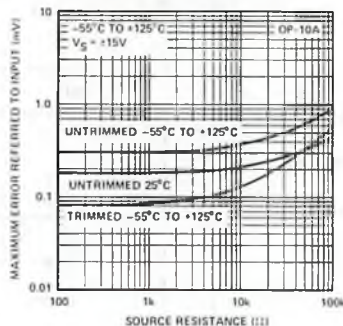
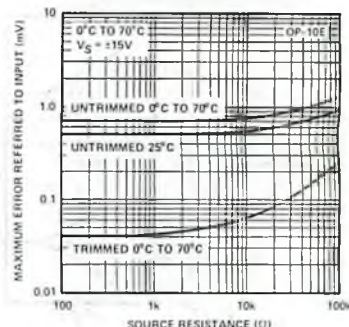


MATCHING CHARACTERISTICS CHANNEL SEPARATION vs FREQUENCY

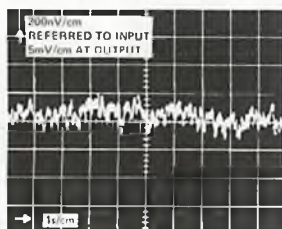
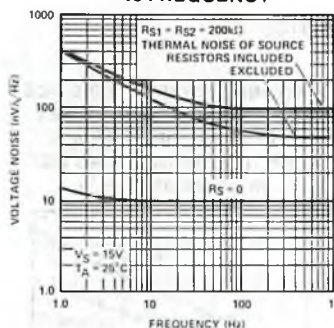
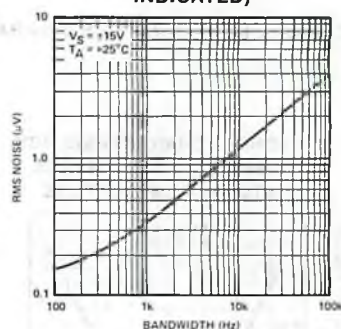
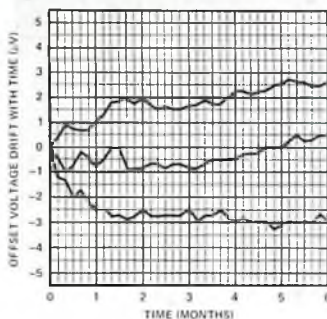
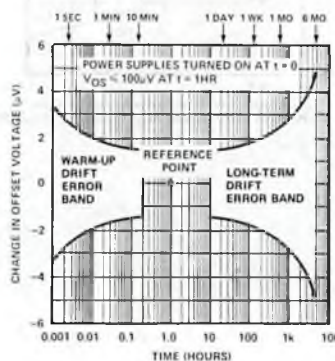
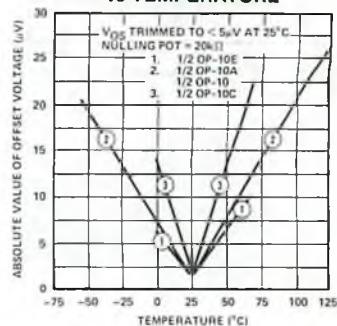


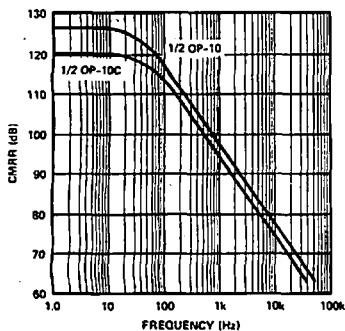
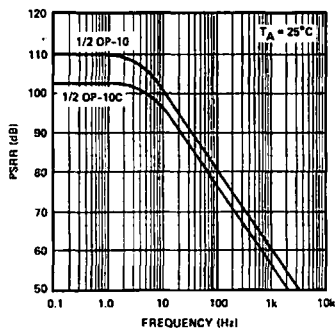
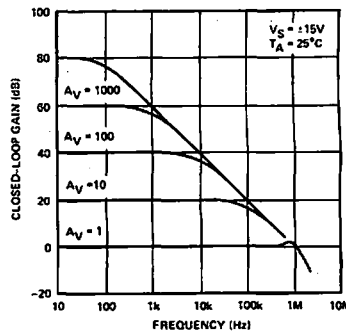
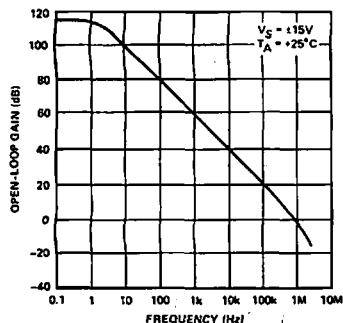
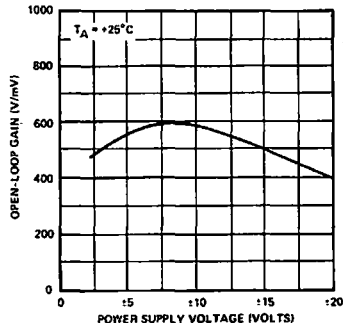
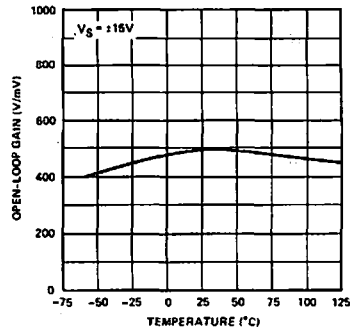
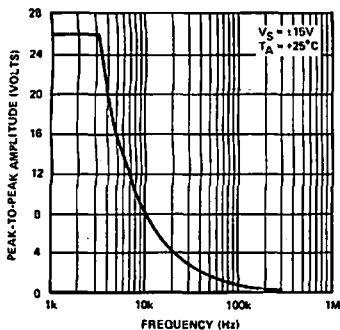
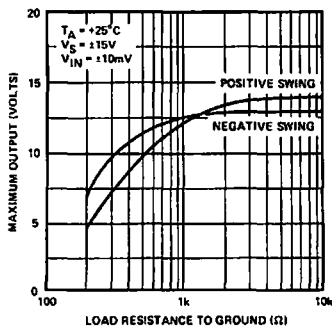
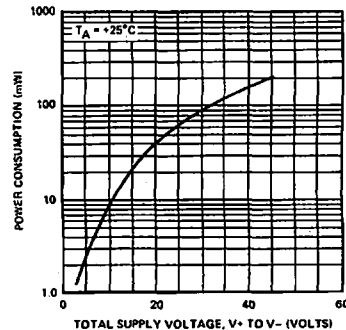
TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT


 MATCHING CHARACTERISTIC
MAXIMUM INPUT ERROR vs
SOURCE RESISTANCE

 MATCHING CHARACTERISTIC
MAXIMUM INPUT ERROR vs
SOURCE RESISTANCE


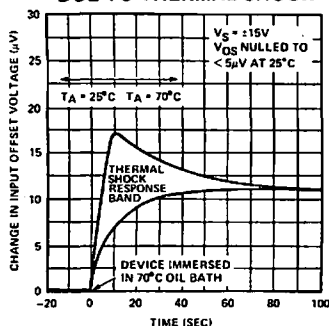
OP-10 LOW FREQUENCY NOISE


 VOLTAGE NOISE DENSITY
vs FREQUENCY

 INPUT WIDEBAND NOISE
vs BANDWIDTH
(0.1Hz TO FREQUENCY
INDICATED)

 TYPICAL OFFSET VOLTAGE
STABILITY vs TIME

 OFFSET VOLTAGE DRIFT
WITH TIME

 TRIMMED OFFSET VOLTAGE
vs TEMPERATURE


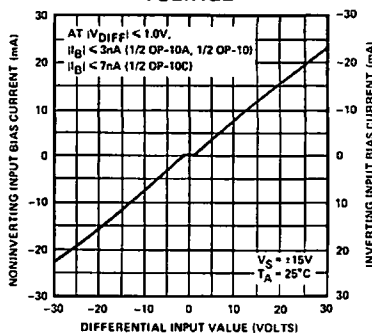
TYPICAL PERFORMANCE CHARACTERISTICS
CMRR vs FREQUENCY

PSRR vs FREQUENCY

CLOSED-LOOP GAIN vs FREQUENCY

OPEN-LOOP GAIN vs FREQUENCY

OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE

OPEN-LOOP GAIN vs TEMPERATURE

MAXIMUM OUTPUT SWING vs FREQUENCY

MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

POWER CONSUMPTION vs POWER SUPPLY


TYPICAL PERFORMANCE CHARACTERISTICS

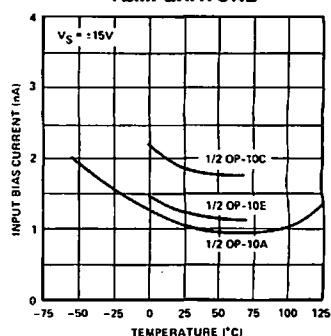
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE



APPLICATIONS INFORMATION

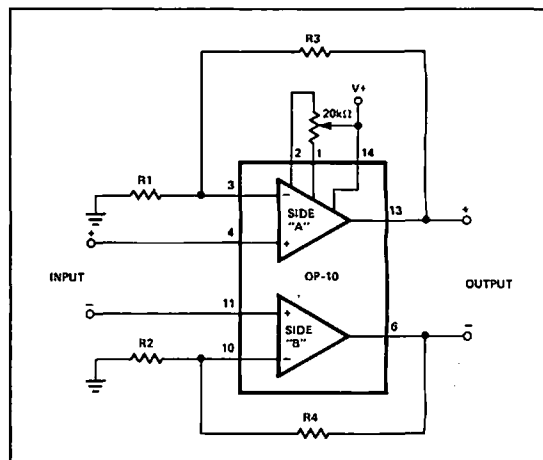
ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide a powerful tool for the solution of some difficult circuit design problems. Circuits include true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references and many other demanding applications. These designs all require good matching between two operational amplifiers.

The adjacent circuit, a differential-in, differential-out amplifier, shows how errors can be reduced. Assuming the resistors used are matched, the gain of each side will be identical; if the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the difference between the amplifiers' offset voltages. This error-cancellation principle holds for a number of input-referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made very high; this is especially important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than errors due to noise or drift with temperature.

For example, consider the case of two op amps, each with 80dB ($100\mu\text{V/V}$) CMRR. If the CMRR of one device is $+100\mu\text{V/V}$ while CMRR of the other is $-100\mu\text{V/V}$, then the net

CMRR will be $200\mu\text{V/V}$, a 6dB degradation. The matching of CMRR increases the effective CMRR when used as an instrumentation input stage.



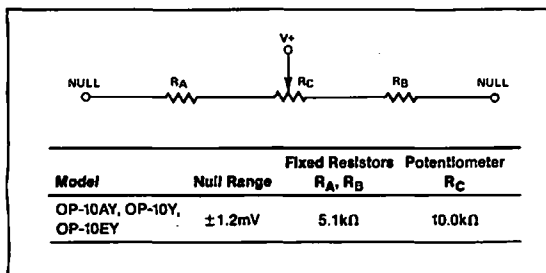
POWER SUPPLIES

The V_+ supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The V_- supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Offset trimming terminals are provided for each amplifier of the OP-10. Guaranteed performance over temperature is obtained by trimming only one side (side A) to match the offset of the other; a net differential offset of zero results. This procedure is used during factory testing of the devices; however, essentially the same results may be obtained by trimming side B to match side A, or by nulling each side individually.

The OP-10 provides lowest drift when trimmed with a 20k Ω potentiometer; this value provides about ± 4 mV of adjustment range which should be more than adequate for most applications. Where finer trimming resolution is desired, or where unwanted changes in potentiometer position with time and temperature could create unacceptable offsets, the adjustment sensitivity may be reduced by using the circuit shown below.



INSTRUMENTATION AMPLIFIERS USING OP-10

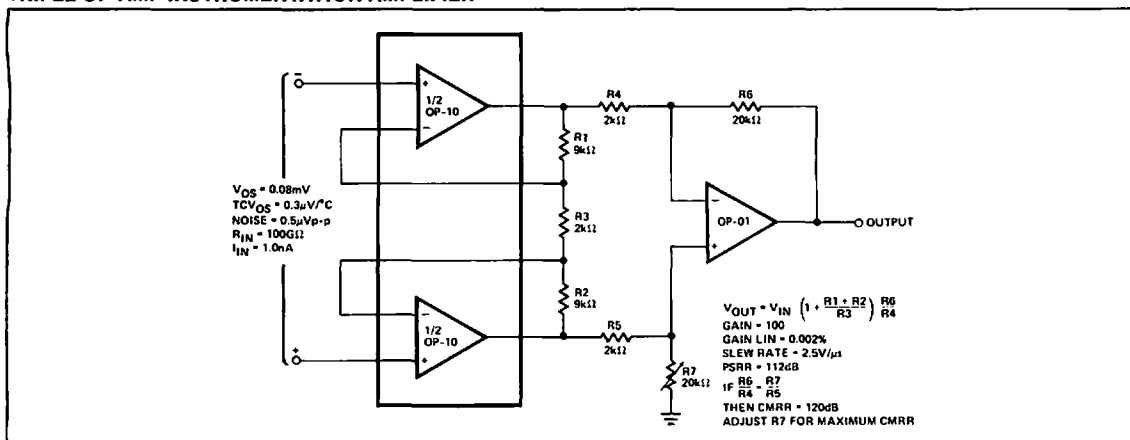
Instrumentation amplifiers with excellent performance can be easily built using the OP-10. Typical performance for a two and three-amplifier design are given in the table. The three-amplifier design, while more complex, has the advantages of simple gain adjustment by trimming a single resistor (R_3) and

wide common-mode voltage capability at any gain, plus improved gain linearity. Slew rate, small-signal bandwidth, and full power bandwidth are also superior. Speed will be improved by using an OP-01 for the output stage.

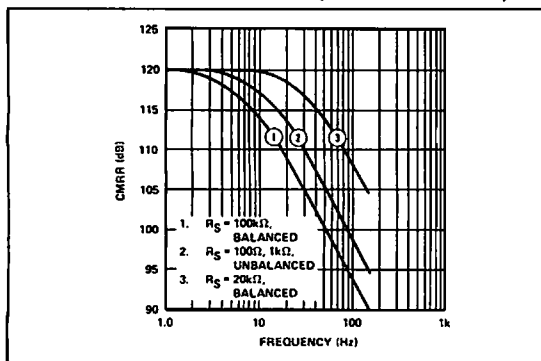
TYPICAL PERFORMANCE OF INSTRUMENTATION AMPLIFIERS GAIN = 100

PARAMETER	2 OP AMP DESIGN	3 OP AMP DESIGN
Gain Nonlinearity	0.004%	0.001% (OP-05) 0.002% (OP-01)
Initial Input Offset Voltage	70 μ V	75 μ V
vs. Temperature (amplifier A nulled with 20k pot)	0.3 μ V/ $^{\circ}$ C	0.3 μ V/ $^{\circ}$ C
vs. Time	3.5 μ V/month	3.5 μ V/month
Input Bias Current	± 1 nA	± 1 nA
vs. Temperature	10pA/ $^{\circ}$ C	10pA/ $^{\circ}$ C
Input Offset Current	0.8nA	0.8nA
vs. Temperature	12pA/ $^{\circ}$ C	12pA/ $^{\circ}$ C
Input Impedance Differential	80G Ω	100G Ω
Common-Mode	100G Ω	100G Ω
Input Noise Voltage (0.1 to 10Hz)	0.5 μ V _{p-p}	0.5 μ V _{p-p}
Input Noise Current (0.1 to 10Hz)	14pA _{p-p}	14pA _{p-p}
Common-Mode Rejection	120dB	120dB
Power Supply Rejection	112dB	112dB
Frequency Response		
Small-Signal (-3dB)	6.0Hz	26kHz (OP-05) 85kHz (OP-01)
Full Power	2.5Hz	4.3kHz (OP-05) 43kHz (OP-01)
Slew Rate	0.17V/ μ s	0.17V/ μ s (OP-05) 4.0V/ μ s (OP-01)

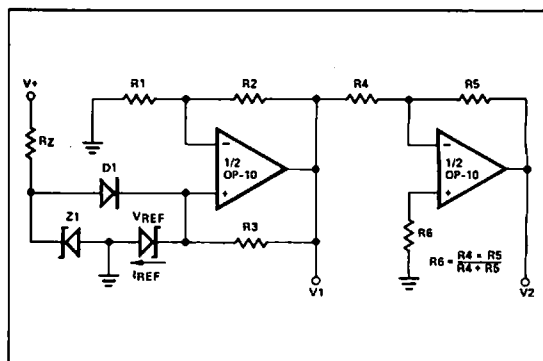
TRIPLE OP-AMP INSTRUMENTATION AMPLIFIER



CMRR vs FREQUENCY INSTRUMENTATION AMPLIFIER (3 OP-AMP DESIGN)



PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10



PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10

Precision dual tracking voltage references using a single reference source are easily constructed using OP-10. These references exhibit low noise, excellent stability vs. temperature and time, and have excellent power supply rejection.

In the circuit shown, R_3 should be adjusted to set I_{REF} to operate V_{REF} at its minimum temperature coefficient current. Proper circuit start-up is assured by R_Z , Z_1 , and D_1 .

$$V_{Z1} \leq V_{REF} + 2V$$

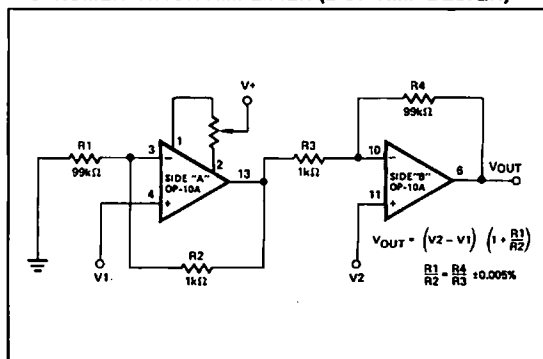
$$V1 = V_{REF} \left(1 + \frac{R2}{R1} \right)$$

$$I_{REF} = (V1 - V_{REF}) / R3$$

$$V2 = V1 \left(\frac{-R5}{R4} \right)$$

Output Impedance ($\Delta I_L: 1.0mA-5.0mA$) $0.25 \times 10^{-3}\Omega$

INSTRUMENTATION AMPLIFIER (2 OP-AMP DESIGN)





OP-12

PRECISION LOW-INPUT-CURRENT OPERATIONAL AMPLIFIER (INTERNALLY COMPENSATED)

Precision Monolithics Inc.

FEATURES

- Low Offset Voltage 150 μ V Max
- Low Offset Voltage Drift 2.5 μ V/ $^{\circ}$ C Max
- Load Current Capability 5mA Min
- Internal Frequency Compensation
- 125 $^{\circ}$ C Temperature Tested Die
- Low Offset Current 200pA Max
- Low Bias Current 2.0nA Max
- Low Power Consumption 18mW Max @ $\pm$ 15V
- High Common-Mode Input Range $\pm$ 13V Min
- MIL-STD-883 Class B Processing Available
- Silicon-Nitride Passivation

ORDERING INFORMATION†

T _A = 25 $^{\circ}$ C V _{OS} MAX (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	
0.15	—	OP12AZ*	MIL
0.15	OP12EJ	OP12EZ	COM
0.30	OP12BJ	OP12BZ*	MIL
0.30	OP12FJ	OP12FZ	COM
1.0	—	OP12CZ	MIL
1.0	OP12GJ	OP12GZ	COM

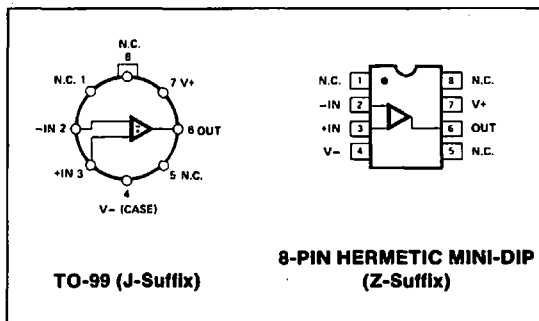
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

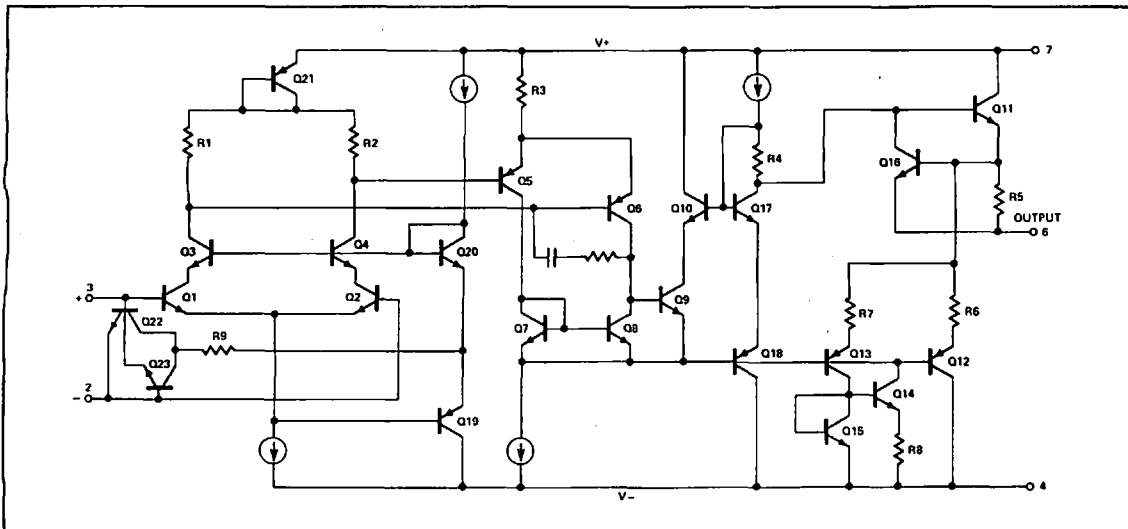
GENERAL DESCRIPTION

The PMI OP-12 is an improved version of the popular LM108A low-power op amp. The OP-12 is internally compensated and its chip dimensions are only 42 X 58 mils. Offset voltage is lower; the total worst-case input offset voltage over -55 $^{\circ}$ C to +125 $^{\circ}$ C for the OP-12A is only 350 μ V. In addition, the OP-12 drives a 2k Ω load which is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super-beta process and on-chip zener-zap trimming capabilities. The internal compensation makes this op amp ideal for hybrid assembly applications.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



OPERATIONAL AMPLIFIERS

5

**ABSOLUTE MAXIMUM RATINGS** (Note 4)**Supply Voltage**

OP-12A, OP-12B,

OP-12E, OP-12F, All DICE except GR $\pm 20\text{V}$ OP-12C, OP-12G, GR DICE Only $\pm 15\text{V}$ **Operating Temperature Range**OP-12A, OP-12B, OP-12C -55°C to $+125^\circ\text{C}$ OP-12E, OP-12F, OP-12G 0°C to $+70^\circ\text{C}$ **Storage Temperature Range** -65°C to $+150^\circ\text{C}$ **Lead Temperature Range (Soldering, 60 sec)** 300°C **Internal Power Dissipation (Note 1)** 500mW **Differential Input Current (Note 2)** $\pm 10\text{mA}$ **Input Voltage (Note 3)** $\pm 15\text{V}$ **Output Short-Circuit Duration** Indefinite**DICE Junction Temperature (T_J)** -65°C to $+150^\circ\text{C}$ **NOTES:**

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	$7.1\text{mW}/^\circ\text{C}$
8-Pin Hermetic DIP (Z)	75°C	$6.7\text{mW}/^\circ\text{C}$

2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.3. For supply voltages less than $\pm 15\text{V}$, the absolute maximum input voltage is equal to the supply voltage.

4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 20\text{V}$ and $T_A = 25^\circ\text{C}$ for A, B, E and F grades, $V_S = \pm 15\text{V}$, and $T_A = 25^\circ\text{C}$ for C and G grades, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12A/E			OP-12B/F			OP-12C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.18	0.30	—	0.25	1.0	mV
Input Offset Current	I_{OS}		—	0.05	0.20	—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I_B		—	0.8	2.0	—	0.8	2.0	—	1.0	5.0	nA
Input Resistance — Differential-Mode	R_{IN}	(Note 1)	26	70	—	26	70	—	10	50	—	M Ω
Input Voltage Range	IVR	$V_S = \pm 15\text{V}$	± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13\text{V}$	104	120	—	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5\text{V}$ to $\pm 15\text{V}$	—	1	7	—	1	7	—	4	63	$\mu\text{V}/\text{V}$
Output Voltage Swing	V_O	$R_L \geq 10\text{k}\Omega$, $V_S = \pm 15\text{V}$	± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
		$R_L \geq 2\text{k}\Omega$, $V_S = \pm 15\text{V}$	± 10	± 12	—	± 10	± 12	—	± 10	± 12	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10\text{k}\Omega$	80	300	—	80	300	—	40	250	—	V/mV
		$V_O = \pm 10\text{V}$										
		$R_L \geq 2\text{k}\Omega$	50	150	—	50	150	—	—	100	—	
Power Consumption	P_d	$V_S = \pm 15\text{V}$, No Load	—	9	18	—	9	18	—	12	24	mW
		$V_S = \pm 5\text{V}$, No Load	—	3	6	—	3	6	—	4	8	
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	—	0.9	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	22	—	—	22	—	—	22	—	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	21	—	—	21	—	—	21	—	
		$f_O = 1000\text{Hz}$	—	20	—	—	20	—	—	20	—	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	—	3	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	0.15	—	—	0.15	—	—	0.15	—	$\text{pA}/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	0.14	—	—	0.14	—	—	0.14	—	
		$f_O = 1000\text{Hz}$	—	0.13	—	—	0.13	—	—	0.13	—	
Slew Rate	SR	$R_L \geq 2\text{k}\Omega$	—	0.12	—	—	0.12	—	—	0.12	—	$\text{V}/\mu\text{s}$
Closed-Loop Bandwidth	BW	$A_{VOL} = +1$	—	0.80	—	—	0.80	—	—	0.80	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	200	—	—	200	—	—	200	—	Ω

NOTE:

1. Guaranteed by input bias current.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, for C grade, $V_S = \pm 20V$ for A and B grades, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12A			OP-12B			OP-12C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.12	0.35	—	0.28	0.60	—	0.40	2.0	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.12	0.40	—	0.12	0.40	—	0.18	1.0	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	0.50	2.5	—	1.0	5.0	$pA/^\circ C$
Input Bias Current	I_B		—	1.2	3.0	—	1.2	3.0	—	1.8	10	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$	—	4	10	—	4	10	—	6	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 5k\Omega$ $V_O = \pm 10V$	40	120	—	40	120	—	15	80	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$ $R_L \geq 5k\Omega$, $V_S = \pm 15V$	± 13 ± 10	± 14 ± 13	—	± 13 ± 10	± 14 ± 13	—	± 13 ± 10	± 14 ± 12	—	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	9	18	—	9	18	—	15	24	mW

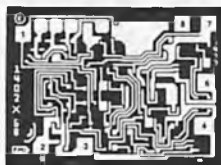
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for G grade, $V_S = \pm 20V$ for E and F grades, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12E			OP-12F			OP-12G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.10	0.26	—	0.23	0.45	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.11	0.60	—	0.12	0.70	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	1.0	5.0	—	1.0	5.0	$pA/^\circ C$
Input Bias Current	I_B		—	1.0	2.6	—	1.2	5.2	—	1.4	6.5	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5$ to $\pm 15V$	—	4	10	—	4	10	—	6	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$ $V_O = \pm 10V$	60	200	—	60	200	—	25	150	—	V/mV
		$R_L \geq 2k\Omega$ $V_O = \pm 10V$	25	100	—	25	100	—	—	80	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$ $V_S = \pm 15V$	± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
		$R_L \geq 5k\Omega$ $V_S = \pm 15V$	± 10	± 12	—	± 10	± 12	—	± 10	± 12	—	
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	9	18	—	9	18	—	15	24	mW

For typical performance characteristics, see OP-08 data sheet. Assume $C_C = 30pF$.



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.059 × 0.043 inch, 2537 sq. mils
(1.50 × 1.09 mm, 1.64 sq. mm)

1. NO CONNECTION
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
6. OUTPUT
7. V₊
8. NO CONNECTION

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-12N, OP-12G and OP-12GR devices; $T_A = 125^\circ C$ for OP-12NT and OP-12GT devices, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	OP-12NT LIMIT	OP-12N LIMIT	OP-12GT LIMIT	OP-12G LIMIT	OP-12GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.35	0.15	0.6	0.3	1	mV MAX
Input Offset Current	I_{OS}		0.4	0.2	0.4	0.2	0.5	nA MAX
Input Bias Current	I_B		3	2	3	2	5	nA MAX
Input Voltage Range	IVR		± 13	± 13	± 13	± 13	± 13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 13	± 13	± 13	± 13	± 13	V MIN
		$R_L \geq 2k\Omega$	—	± 10	—	± 10	± 10	
		$R_L \geq 5k\Omega$	± 10	—	± 10	—	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_O = \pm 10V$	80	80	80	80	40	V/mV MIN
		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	—	50	—	50	—	
		$R_L \geq 5k\Omega$, $V_O = \pm 10V$	40	—	40	—	—	
Input Resistance	R_{IN}	(Note 1)	26	26	26	26	10	MΩ MIN
Supply Current	I_{SY}	$I_{OUT} = 0$ $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

NOTES:

1. Guaranteed by design.

2. For 25°C specifications of OP-12NT and OP-12GT, see OP-12N and OP-12G, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12NT TYPICAL	OP-12N TYPICAL	OP-12GT TYPICAL	OP-12G TYPICAL	OP-12GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		0.5	0.5	1.0	1.0	1.5	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	1.0	1.0	1.0	pA/°C

Precision Monolithics Inc.

FEATURES (All Devices)

- Significant Performance Advantages over LF155, 156 and 157 Devices.
- Low Input Offset Voltage 500 μ V Max
- Low Input Offset Voltage Drift 2.0 μ V/ $^{\circ}$ C
- Minimum Slew Rate Guaranteed on All Models
- Temperature-Compensated Input Bias Currents
- Guaranteed Input Bias Current @ 125 $^{\circ}$ C
- Bias Current Specified WARMED UP Over Temperature
- Internal Compensation
- Low Input Noise Current 0.01pA/ $\sqrt{\text{Hz}}$
- High Common-Mode Rejection Ratio 100dB
- Models With MIL-STD-883 Processing Available
- 125 $^{\circ}$ C Temperature Tested DICE

OP-15

- 156 Speed With 155 Dissipation (80mW Typ)
- Wide Bandwidth 6MHz
- High Slew Rate 13V/ μ s
- Fast Settling to $\pm 0.1\%$ 1200ns

OP-16

- Higher Slew Rate 25V/ μ s
- Faster Settling to $\pm 0.1\%$ 900ns
- Wider Bandwidth 8MHz

OP-17

- Highest Slew Rate 60V/ μ s
- Fastest Settling to $\pm 0.1\%$ 600ns
- Highest Gain Bandwidth Product ($A_{VCL} = 5 \text{ Min}$) 30MHz

GENERAL DESCRIPTION

The PMI JFET-input series of devices offer clear advantages over industry-generic devices and are superior in both cost and performance to many dielectrically-isolated and hybrid

op amps. All devices offer offset voltages as low as 0.5mV with TCV_{OS} guaranteed to 5 μ V/ $^{\circ}$ C. A unique input bias cancellation circuit reduces the I_B by a factor of 10 over conventional designs. In addition, PMI specifies I_B and I_{OS} with the devices warmed up and operating at 25 $^{\circ}$ C ambient.

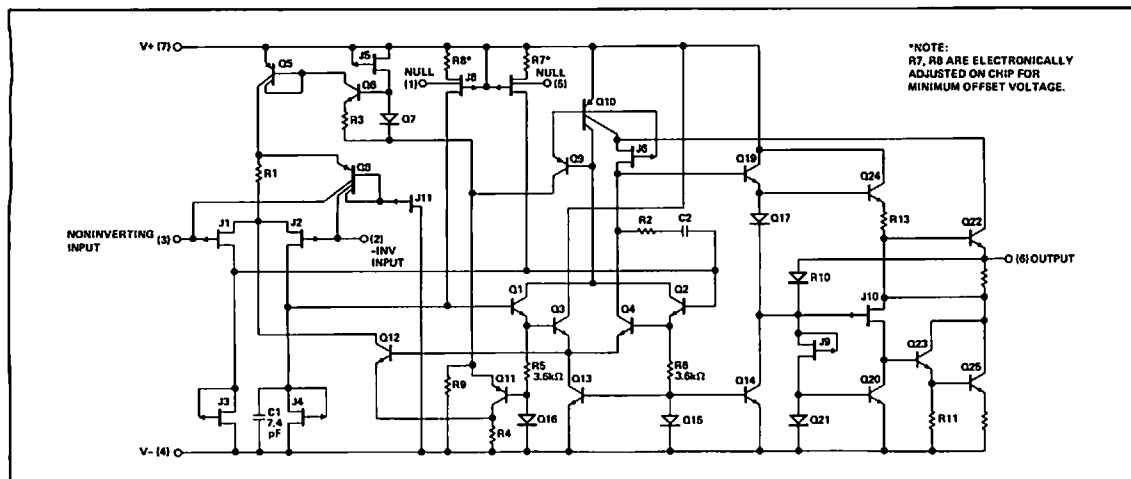
These devices were designed to provide real precision performance along with high speed. Although they can be nulled, the design objective was to provide low offset-voltage without nulling. Systems generally become more cost effective as the number of trim circuits is decreased. PMI achieves this performance by use of an improved Bipolar compatible JFET process coupled with on-chip, zener-zap offset trimming.

The OP-15 provides an excellent combination of high speed and low input offset voltage. In addition, the OP-15 offers the speed of the 156A op amp with the power dissipation of a 155A. The combination of a low input offset voltage of 500 μ V, slew rate of 13V/ μ s, and settling time of 1200ns to 0.1% makes the OP-15 an op amp of both precision and speed. The additional features of low supply current coupled with an input bias current of 9nA at 125 $^{\circ}$ C ambient (not junction) temperature makes the OP-15 ideal for a wide range of applications.

The OP-16 features a slew rate of 25V/ μ s and a settling time of 900ns to 0.1% which represents a significant improvement in speed over the 156. Also, the OP-16 has all the DC features of the OP-15.

The OP-17 has a slew rate of 60V/ μ s and is the best choice for applications requiring high closed-loop gain with high speed. See the OP-42 data sheet for unity gain applications and the OP-215 data sheet for a dual configuration of the OP-15.

SIMPLIFIED SCHEMATIC





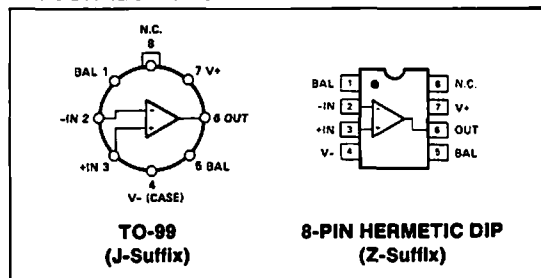
ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	8-PIN HERMETIC DIP	
0.5	OP15AJ* OP16AJ* OP17AJ*	OP15AZ* — OP17AZ*	MIL
0.5	OP15EJ OP16EJ OP17EJ	OP15EZ OP16EZ OP17EZ	COM
1.0	OP15BJ* OP16BJ* OP17BJ*	OP15BZ OP16BZ/883 OP17BZ*	MIL
1.0	OP15FJ OP16FJ OP17FJ	OP15FZ OP16FZ OP17FZ	COM
3.0	— OP17CJ	OP16CZ/883 —	MIL
3.0	OP15GJ OP16GJ OP17GJ	OP15GZ OP16GZ OP17GZ	COM

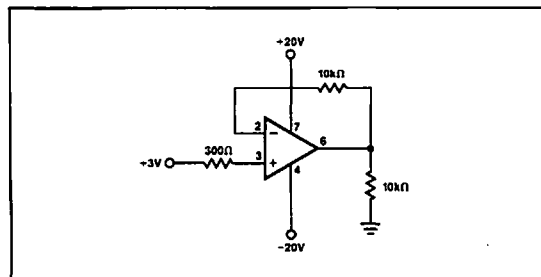
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

PIN CONNECTIONS



BURN-IN CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage

All Devices Except C, G (Packaged) & GR Grades . . . ±22V

C, G (Packaged) & GR Grades ±18V

Internal Power Dissipation (Note 1) 500mW

Operating Temperature

A, B, & C Grades -55°C to +125°C

E, F & G Grades 0°C to +70°C

Maximum Junction Temperature +150°C

DICE Junction Temperature (T_j) -65°C to +150°C

Differential Input Voltage

All Devices Except C, G (Packaged) & GR Grades . . . ±40V

C, G (Packaged) & GR Grades ±30V

Input Voltage (Note 3)

All Devices Except C, G (Packaged) & GR Grades . . . ±20V

C, G (Packaged) & GR Grades ±16V

Input Voltage

OP-15A, OP-15B, OP-15E, OP-15F ±20V

OP-15G ±16V

OP-16A, OP-16B, OP-16E, OP-16F ±20V

OP-16C, OP-16G ±16V

OP-17A, OP-17B, OP-17E, OP-17F ±20V

OP-17C, OP-17G ±16V

Output Short-Circuit Duration Indefinite

Storage Temperature Range -65°C to +150°C

Lead Temperature Range (Soldering, 60 sec) +300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
Hermetic 8-Pin Dip (Z)	75°C	6.7mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power-supply voltage.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-15A/E OP-16A/E OP-17A/E			OP-15B/F OP-16B/F OP-17B/F			OP-15G OP-16C/G OP-17C/G			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$		—	0.2	0.5	—	0.4	1.0	—	0.5	3.0	mV
Input Offset Current	I_{OS}	$T_J = 25^\circ C$ (Note 1)	OP-15	—	3	10	—	6	20	—	12	50	pA
		Device Operating		—	5	22	—	10	40	—	20	100	
		$T_J = 25^\circ C$ (Note 1)	OP-16/OP-17	—	3	10	—	6	20	—	12	50	
		Device Operating		—	5	25	—	10	50	—	20	125	
Input Bias Current	I_B	$T_J = 25^\circ C$ (Note 1)	OP-15	—	± 15	± 50	—	± 30	± 100	—	± 60	± 200	pA
		Device Operating		—	± 18	± 110	—	± 40	± 200	—	± 80	± 400	
		$T_J = 25^\circ C$ (Note 1)	OP-16/OP-17	—	± 15	± 50	—	± 30	± 100	—	± 60	± 200	
		Device Operating		—	± 20	± 130	—	± 40	± 250	—	± 80	± 500	
Input Resistance	R_{IN}			—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$		100	240	—	75	220	—	50	200	—	V/mV
Output Voltage Swing	V_O	$R_L = 10k\Omega$		± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
		$R_L = 2k\Omega$		± 11	± 12.7	—	± 11	± 12.7	—	± 11	± 12.7	—	
Supply Current	I_{SY}		OP-15	—	2.7	4.0	—	2.7	4.0	—	2.8	5.0	mA
			OP-16/OP-17	—	4.6	7.0	—	4.6	7.0	—	4.8	8.0	
Slew Rate	SR	$A_{VCL} = +1$ (Note 3)	OP-15	10	13	—	7.5	11	—	5	9	—	V/ μs
			OP-16	18	25	—	12	21	—	9	17	—	
		$A_{VCL} = +5$ (Note 3)	OP-17	45	60	—	35	50	—	25	40	—	
Gain Bandwidth Product	GBW	(Note 3)	OP-15	4.0	6.0	—	3.5	5.7	—	3.0	5.4	—	MHz
			OP-16	6.0	8.0	—	5.5	7.6	—	5.0	7.2	—	
			OP-17	20	30	—	15	28	—	11	26	—	
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	OP-15	—	14	—	—	13	—	—	12	—	MHz
			OP-16	—	19	—	—	18	—	—	17	—	
		$A_{VCL} = +5$	OP-17	—	11	—	—	10	—	—	9	—	
Settling Time	t_s	to 0.01%	OP-15	—	4.5	—	—	4.5	—	—	4.7	—	μs
		to 0.05% (Note 2)		—	1.5	—	—	1.5	—	—	1.6	—	
		to 0.10%		—	1.2	—	—	1.2	—	—	1.3	—	
		to 0.01%	OP-16	—	3.8	—	—	3.8	—	—	4.0	—	
		to 0.05% (Note 2)		—	1.2	—	—	1.2	—	—	1.3	—	
		to 0.10%		—	0.9	—	—	0.9	—	—	1.0	—	
		to 0.01%	OP-17	—	1.5	—	—	1.5	—	—	1.6	—	
		to 0.05% (Note 4)		—	0.7	—	—	0.7	—	—	0.8	—	
		to 0.10%		—	0.6	—	—	0.6	—	—	0.7	—	
Input Voltage Range	IVR			± 10.5	—	—	± 10.5	—	—	± 10.3	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.5V$		86	100	—	86	100	—	—	—	—	dB
		$V_{CM} = \pm 10.3V$		—	—	—	—	—	—	82	96	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$		—	10	51	—	10	51	—	—	—	$\mu V/V$
		$V_S = \pm 10V$ to $\pm 15V$		—	—	—	—	—	—	—	10	60	
Input Noise Voltage Density	e_n	$f_O = 100Hz$		—	20	—	—	20	—	—	20	—	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$		—	15	—	—	15	—	—	15	—	
Input Noise Current Density	i_n	$f_O = 100Hz$		—	0.01	—	—	0.01	—	—	0.01	—	$pA/\sqrt{Hz}$
		$f_O = 1000Hz$		—	0.01	—	—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}			—	3	—	—	3	—	—	3	—	pF

NOTES:

- Input bias current is specified for two different conditions. The $T_J = 25^\circ C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at $25^\circ C$ ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_J and I_B vs T_A . PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Settling time is defined here for a unity gain inverter connection using $2k\Omega$ resistors. It is the time required for the error voltage (the voltage at the

inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.

- Sample tested.
- Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15A OP-16A OP-17A			OP-15B OP-16B OP-17B			OP-16C OP-17C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.4	0.9	—	0.7	2.0	—	0.9	4.5	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	(Note 2)	—	2	5	—	3	10	—	4	15	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	2	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = 125^\circ C$ $T_A = 125^\circ C$ Device Operating	—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	nA
		OP-15	—	0.8	7.0	—	1.2	11	—	1.5	17	
		$T_J = 125^\circ C$ $T_A = 125^\circ C$ Device Operating	—	0.6	4.0	—	0.8	6.0	—	1.0	9.0	
		OP-16/OP-17	—	1.0	8.5	—	1.3	14.5	—	1.7	22	
Input Bias Current (Note 1)	I_B	$T_J = 125^\circ C$ $T_A = 125^\circ C$ Device Operating	—	± 1.2	± 5.0	—	± 1.5	± 7.5	—	± 1.8	± 10	nA
		OP-15	—	± 1.7	± 9.0	—	± 2.2	± 14	—	± 2.7	± 19	
		$T_J = 125^\circ C$ $T_A = 125^\circ C$ Device Operating	—	± 1.2	± 5.0	—	± 1.5	± 7.5	—	± 1.8	± 10	
		OP-16/OP-17	—	± 2.0	± 11	—	± 2.5	± 18	—	± 3.0	± 25	
Input Voltage Range	IVR		± 10.4	—	—	± 10.4	—	—	± 10.25	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$	85	97	—	85	97	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$	—	—	—	—	—	—	80	93	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	15	57	—	15	57	—	—	—	$\mu V/V$
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	23	100	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	35	120	—	30	110	—	25	100	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

NOTES:

- Input bias current is specified for two different conditions. The $T_J = 25^\circ C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at $25^\circ C$ ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_J and I_B vs T_A . PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Sample tested.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15E OP-16E OP-17E			OP-15F OP-16F OP-17F			OP-15G OP-16G OP-17G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.3	0.75	—	0.55	1.5	—	0.7	3.8	mV
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}		—	2	5	—	3	10	—	4	15	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	2	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = 70^\circ C$	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	nA
		$T_A = 70^\circ C$	—	0.06	0.55	—	0.08	0.80	—	0.10	1.2	
		Device Operating	—	0.04	0.30	—	0.06	0.45	—	0.08	0.65	
		Device Operating	—	0.07	0.70	—	0.10	1.1	—	0.15	1.7	
Input Bias Current (Note 1)	I_B	$T_J = 70^\circ C$	—	± 0.10	± 0.40	—	± 0.12	± 0.60	—	± 0.14	± 0.80	nA
		$T_A = 70^\circ C$	—	± 0.13	± 0.75	—	± 0.16	± 1.1	—	± 0.19	± 1.5	
		Device Operating	—	± 0.10	± 0.40	—	± 0.12	± 0.60	—	± 0.14	± 0.80	
		Device Operating	—	± 0.15	± 0.80	—	± 0.20	± 1.4	—	± 0.25	± 2.0	
Input Voltage Range	IVR		± 10.4	—	—	± 10.4	—	—	± 10.25	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10.4V$	85	98	—	85	98	—	—	—	—	dB
		$V_{CM} = \pm 10.25V$	—	—	—	—	—	—	80	84	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	13	57	—	13	57	—	—	—	$\mu V/V$
		$V_S = \pm 10V$ to $\pm 15V$	—	—	—	—	—	—	—	20	100	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	65	200	—	50	180	—	35	160	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

NOTES:

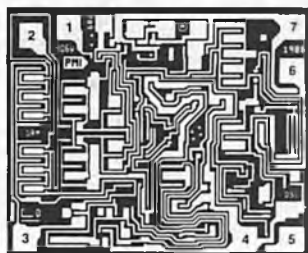
- Input bias current is specified for two different conditions. The $T_J = 25^\circ C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at $25^\circ C$ ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs T_J and I_B vs T_A . PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Sample tested.

5

OPERATIONAL AMPLIFIERS

DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)

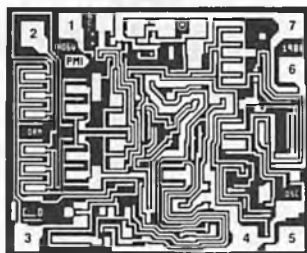
OP-15



DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils
(1.73 × 1.42mm, 2.46 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. BALANCE
6. OUTPUT
7. V₊

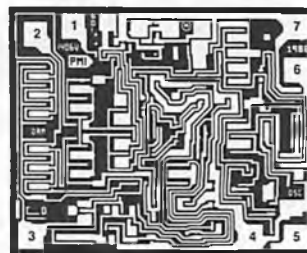
OP-16



DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils
(1.73 × 1.42mm, 2.46 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. BALANCE
6. OUTPUT
7. V₊

OP-17



DIE SIZE 0.068 × 0.056 inch, 3808 sq. mils
(1.73 × 1.42mm, 2.46 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. BALANCE
6. OUTPUT
7. V₊

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at V_S = ±15V, T_A = 25° C for OP-15/16/17N, OP-15/16/17G and OP-15/16/17GR devices; T_A = 125° C for OP-15/16/17NT and OP-15/16/17GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-15NT OP-16NT OP-17NT LIMIT	OP-15N OP-16N OP-17N LIMIT	OP-15GT OP-16GT OP-17GT LIMIT	OP-15G OP-16G OP-17G LIMIT	OP-15GR OP-16GR OP-17GR LIMIT	UNITS
Input Offset Voltage	V _{OS}	R _S = 50Ω	0.9	0.5	2.0	1.0	3.0	mV MAX
Large-Signal Voltage Gain	A _{VO}	V _O = ±10V R _L = 2kΩ	35	100	30	75	50	V/mV MIN
Input Voltage Range	IVR		±10.4	±10.5	±10.4	±10.5	±10.3	V MIN
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±IVR	85	86	85	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	V _S = ±10V to ±20V V _S = ±10V to ±15V	57	51	57	51	80	μV/V MAX
Output Voltage Swing	V _O	R _L = 10kΩ R _L = 2kΩ	±12	±12	±12	±12	±12	V MIN
Supply Current	I _{SY}	OP-15 OP-16, OP-17	—	4	—	4	5	mA MAX
Input Bias Current	I _B	OP-15 OP-16, OP-17	±9	—	±14	—	—	nA MAX
Input Offset Current	I _{OS}	OP-15 OP-16, OP-17	7.0	—	11.0	—	—	nA MAX
			8.5	—	14.5	—	—	

NOTES:

For 25° C characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

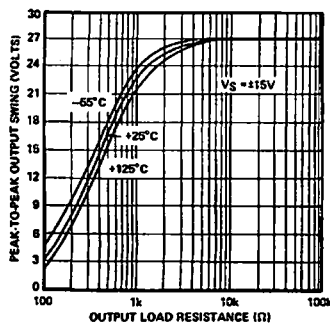
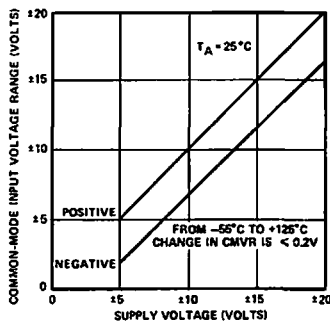
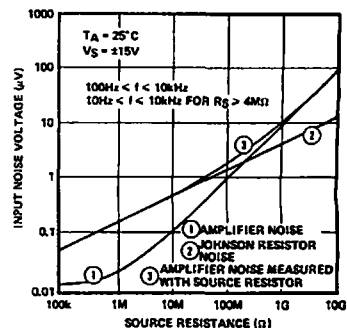
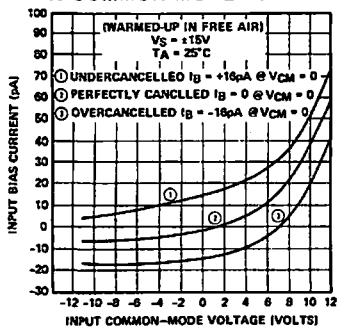
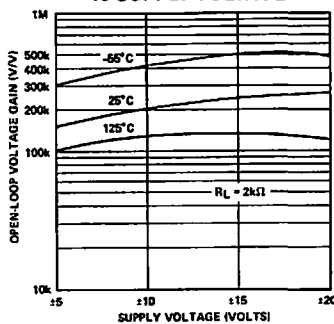
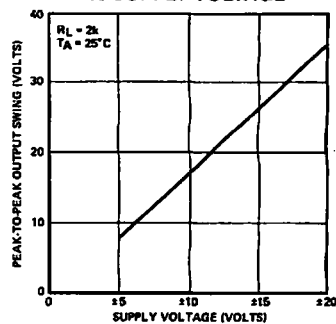
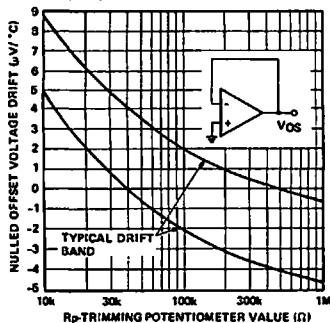
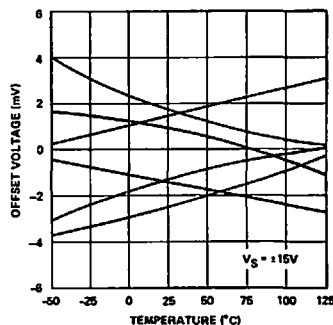
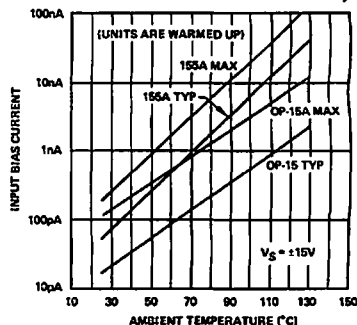
**TYPICAL ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

			OP-15NT OP-16NT OP-17NT TYPICAL	OP-15N OP-16N OP-17N TYPICAL	OP-15GT OP-16GT OP-17GT TYPICAL	OP-15G OP-16G OP-17G TYPICAL	OP-15GR OP-16GR OP-17GR TYPICAL	UNITS			
PARAMETER	SYMBOL	CONDITIONS									
Average Input Offset Drift Unnullled	TCV _{OS}		2	2	3	3	4	μV/°C			
Average Input Offset Drift Nullled	TCV _{OSn}	R _P = 100kΩ	2	2	3	3	4	μV/°C			
Input Offset Current	I _{OS}		3	3	3	3	3	pA			
Input Bias Current	I _B		±15	±15	±15	±15	±15	pA			
Slew Rate	SR	A _{VCL} = +1	OP-15	13	13	11	11	9	V/μs		
			OP-16	25	25	21	21	17			
		A _{VCL} = +5	OP-17	60	60	50	50	40			
Settling Time (see settling time test circuits)	t _S	to 0.01%	OP-15	4.5	4.5	4.5	4.5	4.7	μs		
		to 0.05%		1.5	1.5	1.5	1.5	1.6			
		to 0.10%		1.2	1.2	1.2	1.2	1.3			
		to 0.01%	OP-16	3.8	3.8	3.8	3.8	4.0			
		to 0.05%		1.2	1.2	1.2	1.2	1.3			
		to 0.10%		0.9	0.9	0.9	0.9	1.0			
		to 0.01%	OP-17	1.5	1.5	1.5	1.5	1.6			
		to 0.05%		0.7	0.7	0.7	0.7	0.8			
		to 0.10%		0.6	0.6	0.6	0.6	0.7			
		Gain Bandwidth Product	GBW	OP-15	6.0	6.0	5.7	5.7		5.4	MHz
				OP-16	8.0	8.0	7.6	7.6		7.2	
				OP-17	30	30	28	28		26	
Closed-Loop Bandwidth	CLBW	A _{VCL} = +1	OP-15	14	14	13	13	12	MHz		
			OP-16	19	19	18	18	17			
		A _{VCL} = +5	OP-17	11	11	10	10	9			
Input Noise Voltage Density	e _n	f = 100Hz	20	20	20	20	20	nV/√Hz			
		f = 1000Hz	15	15	15	15	15				
Input Noise Current Density	I _n	f = 100Hz	0.01	0.01	0.01	0.01	0.01	pA/√Hz			
		f = 1000Hz	0.01	0.01	0.01	0.01	0.01				
Input Capacitance	C _{IN}		3	3	3	3	3	pF			

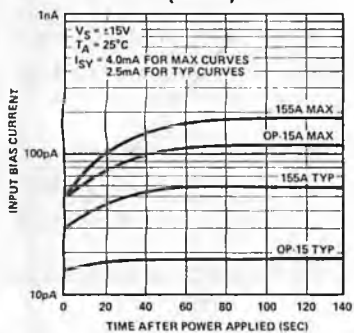
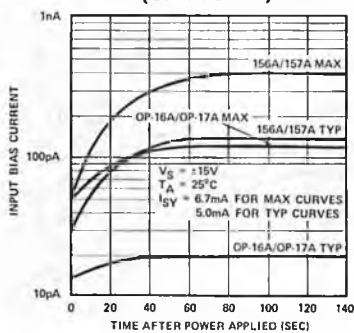
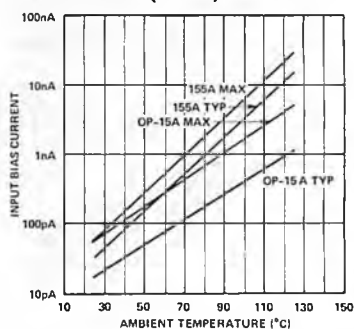
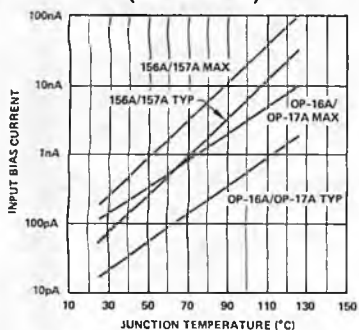
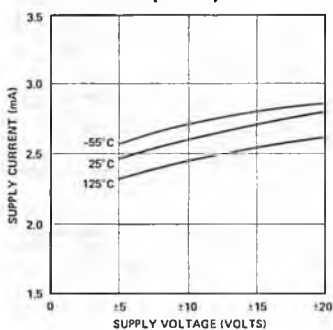
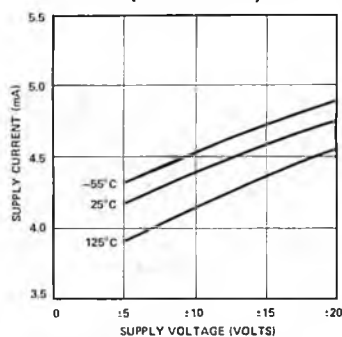
NOTES:

For $25^\circ C$ characteristics of OP-15/16/17NT and OP-15/16/17GT, see OP-15/16/17N and OP-15/16/17G characteristics, respectively.

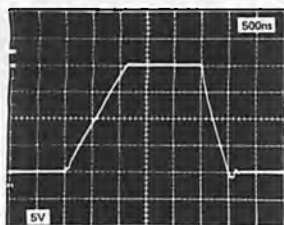
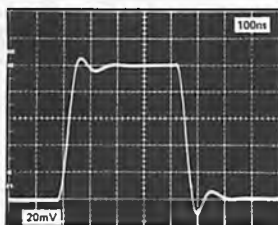
TYPICAL PERFORMANCE CHARACTERISTICS (OP-15/OP-16/OP-17)

MAXIMUM OUTPUT SWING
vs LOAD RESISTANCECOMMON-MODE INPUT
VOLTAGE RANGE
vs SUPPLY VOLTAGEVOLTAGE NOISE vs
SOURCE RESISTANCEINPUT BIAS CURRENT
vs COMMON-MODE VOLTAGEOPEN-LOOP
VOLTAGE GAIN
vs SUPPLY VOLTAGEOUTPUT VOLTAGE SWING
vs SUPPLY VOLTAGENULLED OFFSET
VOLTAGE DRIFT
vs POTENTIOMETER SIZEOFFSET VOLTAGE DRIFT
vs TEMPERATURE OF
REPRESENTATIVE UNITSINPUT BIAS CURRENT vs
AMBIENT TEMPERATURE (UNITS
ARE WARMED-UP IN FREE AIR)

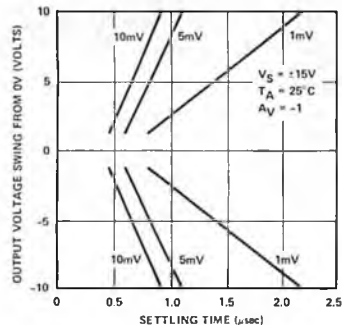
TYPICAL PERFORMANCE CHARACTERISTICS (OP-15/OP-16/OP-17)

 BIAS CURRENT vs TIME
IN FREE AIR
(OP-15)

 BIAS CURRENT vs TIME
IN FREE AIR
(OP-16/OP-17)

 INPUT BIAS CURRENT vs
AMBIENT TEMPERATURE (UNITS
ARE WARMED-UP IN FREE AIR)
(OP-15)

 INPUT BIAS CURRENT vs
AMBIENT TEMPERATURE (UNITS
ARE WARMED-UP IN FREE AIR)
(OP-16/OP-17)

 SUPPLY CURRENT
vs SUPPLY VOLTAGE
(OP-15)

 SUPPLY CURRENT
vs SUPPLY VOLTAGE
(OP-16/OP-17)


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15)

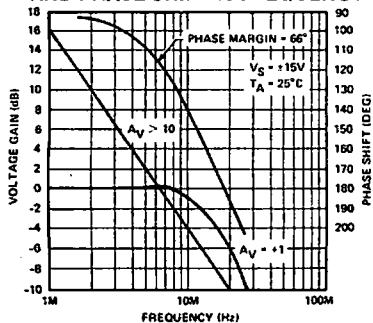
 LARGE-SIGNAL
TRANSIENT RESPONSE

 SMALL-SIGNAL
TRANSIENT RESPONSE


SETTLING TIME

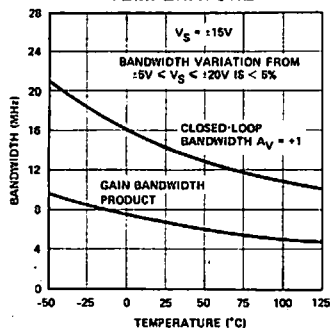


TYPICAL PERFORMANCE CHARACTERISTICS (OP-15)

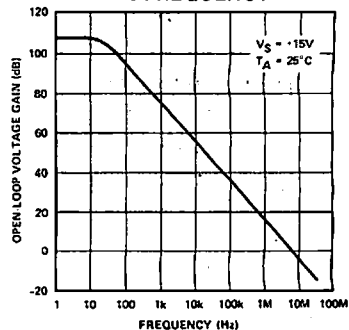
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



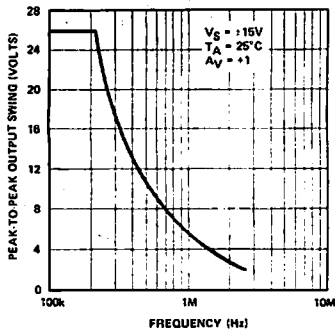
BANDWIDTH vs TEMPERATURE



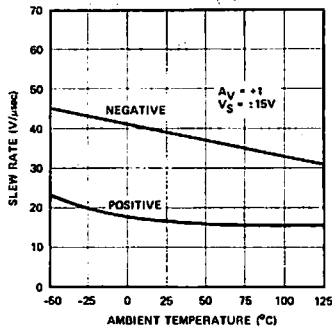
OPEN-LOOP GAIN vs FREQUENCY



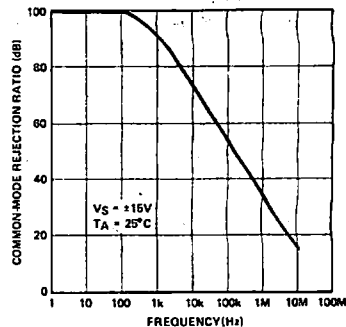
MAXIMUM OUTPUT SWING vs FREQUENCY



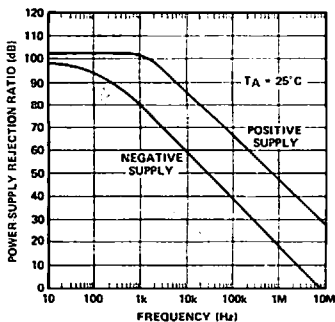
SLEW RATE vs TEMPERATURE



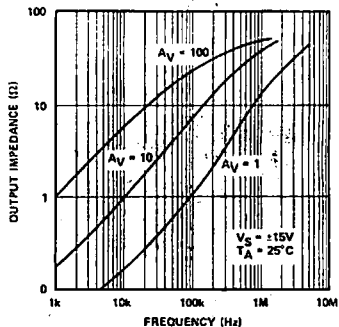
COMMON-MODE REJECTION RATIO vs FREQUENCY



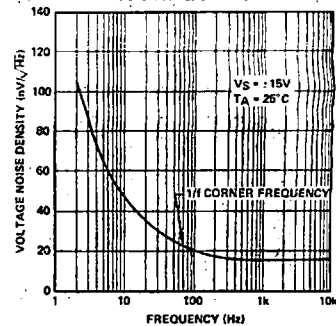
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



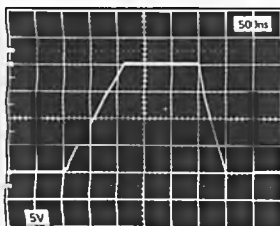
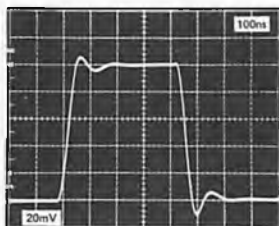
OUTPUT IMPEDANCE vs FREQUENCY



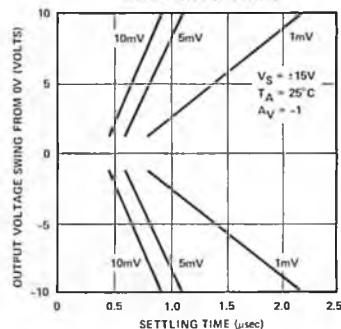
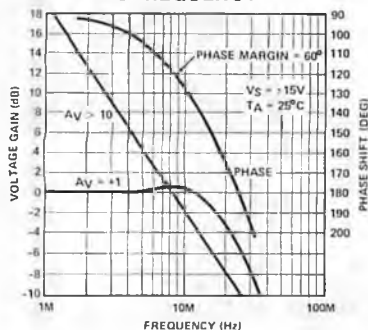
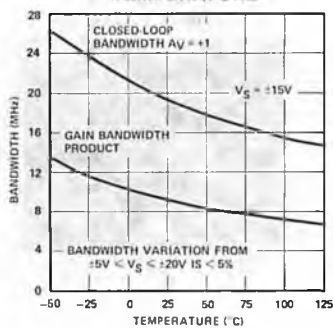
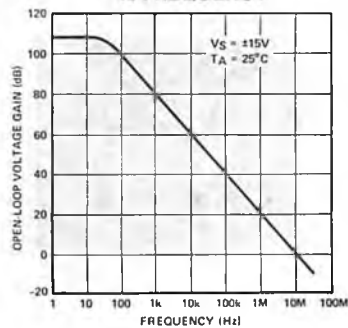
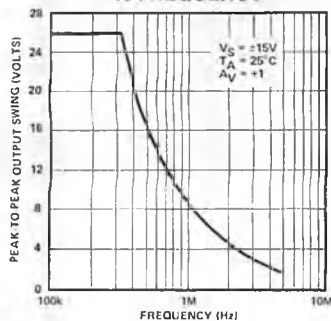
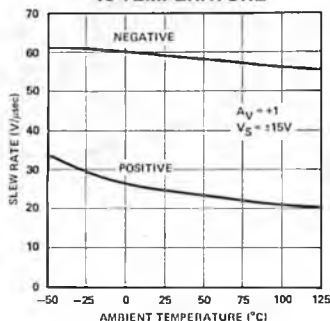
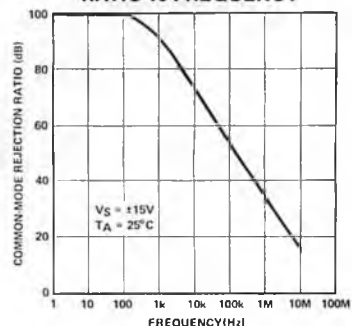
VOLTAGE NOISE DENSITY vs FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS (OP-16)

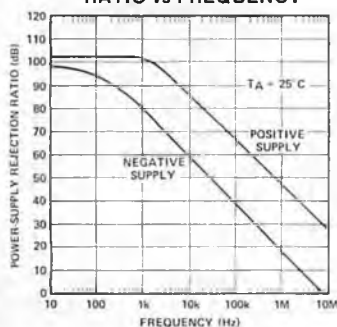
 LARGE-SIGNAL
TRANSIENT RESPONSE

 SMALL-SIGNAL
TRANSIENT RESPONSE


SETTLING TIME

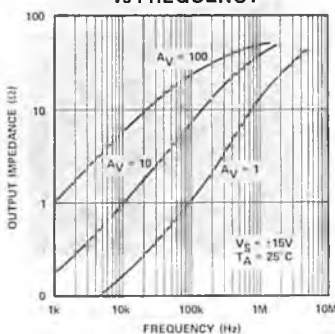

 CLOSED-LOOP BANDWIDTH
AND PHASE SHIFT
vs FREQUENCY

 BANDWIDTH vs
TEMPERATURE

 OPEN-LOOP GAIN
vs FREQUENCY

 MAXIMUM OUTPUT SWING
vs FREQUENCY

 SLEW RATE
vs TEMPERATURE

 COMMON-MODE REJECTION
RATIO vs FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS (OP-16)

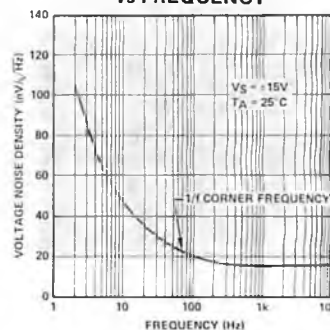
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



OUTPUT IMPEDANCE vs FREQUENCY

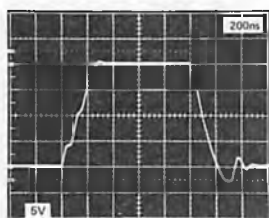


VOLTAGE NOISE DENSITY vs FREQUENCY

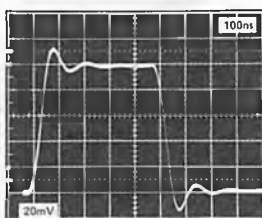


TYPICAL PERFORMANCE CHARACTERISTICS (OP-17)

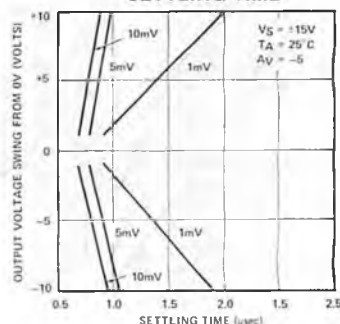
LARGE-SIGNAL TRANSIENT RESPONSE



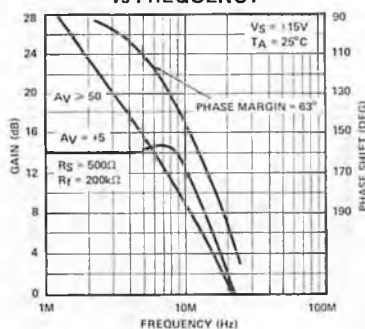
SMALL-SIGNAL TRANSIENT RESPONSE



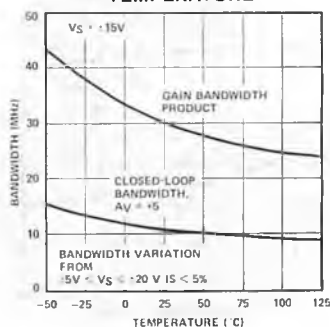
SETTLING TIME



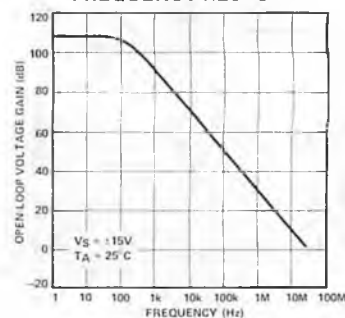
CLOSED-LOOP BANDWIDTH AND PHASE SHIFT vs FREQUENCY



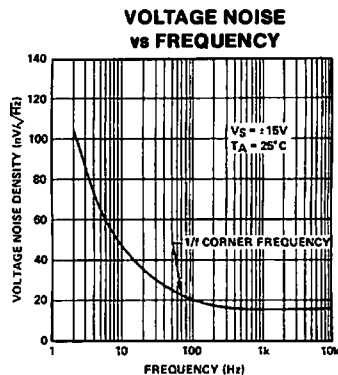
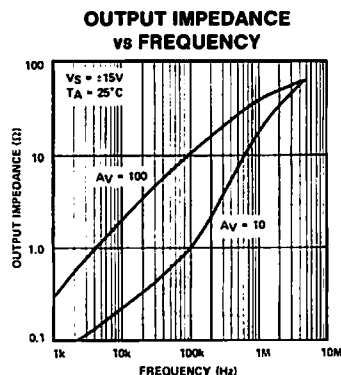
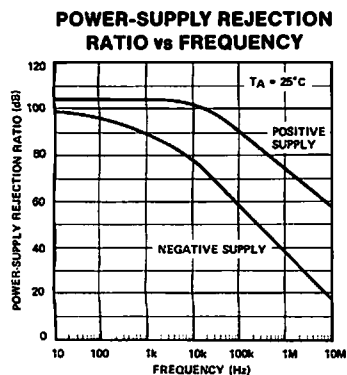
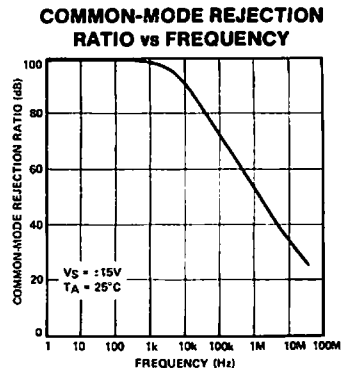
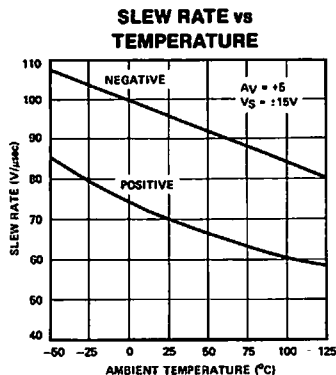
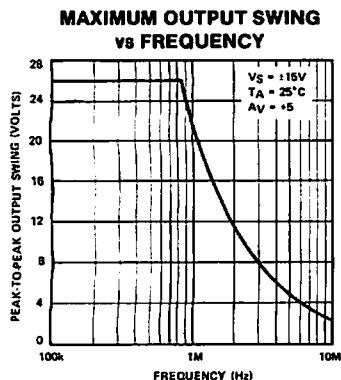
BANDWIDTH vs TEMPERATURE



OPEN-LOOP FREQUENCY RESPONSE

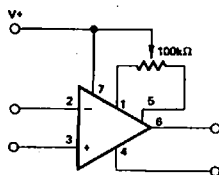


TYPICAL PERFORMANCE CHARACTERISTICS (OP-17)



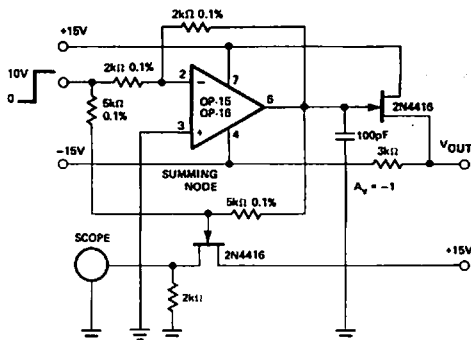
BASIC CONNECTIONS

INPUT OFFSET VOLTAGE NULLING

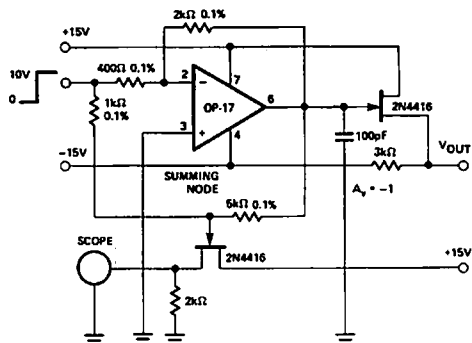


NOTE: V_{OS} CAN BE TRIMMED WITH POTENTIOMETERS RANGING FROM 10k Ω TO 1M Ω . FOR MOST UNITS TCV_{OS} WILL BE MINIMUM WHEN V_{OS} IS ADJUSTED WITH A 100k Ω POTENTIOMETER.

SETTLING-TIME TEST CIRCUIT — OP-15/OP-16

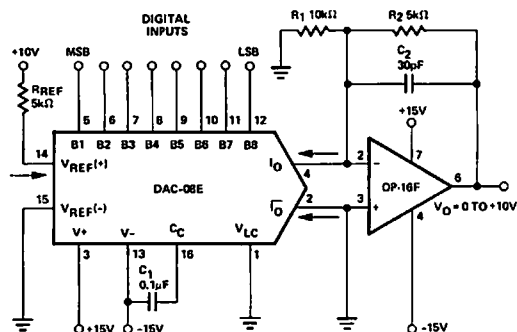


SETTLING-TIME TEST CIRCUIT — OP-17



TYPICAL APPLICATIONS

CURRENT-TO-VOLTAGE AMPLIFIER OUTPUT



APPLICATIONS INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance

from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time-constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback pole time constant.



Precision Monolithics Inc.

OP-20

MICROPOWER OPERATIONAL AMPLIFIER
(SINGLE OR DUAL SUPPLY)

FEATURES

- Low Supply Current 55 μ A Max
- Single-Supply Operation +5V to +30V
- Dual-Supply Operation ± 2.5 V to ± 15 V
- Low Input Offset Voltage 250 μ V Max
- Low Input Offset Voltage Drift 1.5 μ V/ $^{\circ}$ C Max
- High Common-Mode Input Range ... V- to V+ (-1.5V)
- High CMRR and PSRR 100dB Min
- High Open-Loop Gain 120dB Min
- No External Components Required
- 741 Pinout and Nulling

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (μ V)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99	CERDIP	PLASTIC	
250	OP20BJ	OP20BZ	—	MIL
250	OP20FJ	OP20FZ	—	IND
250	—	—	OP20FP	COM
500	OP20CJ	OP20CZ	—	MIL
500	OP20GJ	OP20GZ	—	IND
500	—	—	OP20GP	COM
1000	OP20HJ	OP20HZ	OP20HP	COM
1000	—	—	OP20HS††	COM

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

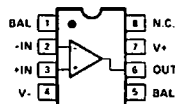
GENERAL DESCRIPTION

The OP-20 is a monolithic micropower operational amplifier that can be operated from a single power supply of +5V to

+30V, or from dual supplies of ± 2.5 V to ± 15 V. The input voltage range extends to the negative rail, therefore input signals down to zero volts can be accommodated when operating from a single supply.

Precision performance in high-gain applications is readily obtained when using the OP-20. The B/F grade features a maximum input offset voltage of 250 μ V, minimum CMRR of 95dB, and open-loop gain of over 500,000. Quiescent supply current is a maximum of only 55 μ A at ± 2.5 V or 80 μ A at ± 15 V. The low input offset, high gain, and low power consumption brings precision performance to portable instruments, satellites, missile control systems, and many other battery-powered applications.

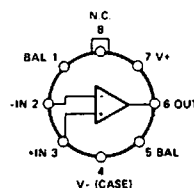
PIN CONNECTIONS



EPOXY MINI-DIP
(P-Suffix)

8-PIN HERMETIC DIP
(Z-Suffix)

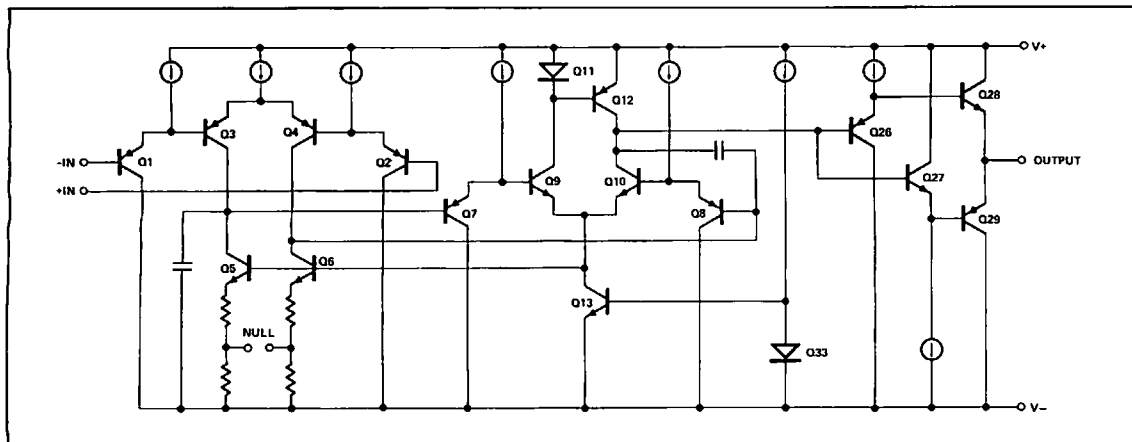
8-PIN SO
(S-Suffix)



TO-99
(J-Suffix)

OPERATIONAL AMPLIFIERS

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage	±18V
Power Dissipation	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C

Operating Temperature Range

OP-20B, OP-20C (J or Z package)	-55°C to +125°C
OP-20F, OP-20G (J or Z package)	-25°C to +85°C
OP-20FP, OP-20GP, OP-20HP	
OP-20HJ, OP-20HZ, OP-20HS	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to +150°C

NOTE:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-20B/F			OP-20C/G			OP-20H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	55	250	—	150	500	—	300	1000	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.15	1.5	—	0.2	2.5	—	0.3	4.0	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	25	—	14	30	—	18	40	nA
Input Voltage Range	IVR	$V^+ = +5V$, $V^- = 0V$	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	-15/13.5	—	—	-15/13.5	—	—	-15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	$V^+ = +5V$, $V^- = 0V$ $0V \leq V_{CM} \leq 3.5V$	95	105	—	90	95	—	85	90	—	dB
		$V_S = \pm 15V$ $-15V \leq V_{CM} \leq 13.5V$	100	110	—	94	105	—	90	100	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ and $V^- = 0V$, $V^+ = 5V$ to $30V$	—	4	6	—	6	10	—	10	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V^+ = +5V$, $V^- = 0V$ $1V \leq V_O \leq 3.5V$	300	500	—	200	500	—	—	500	—	V/mV
		$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 25k\Omega$	1000	2000	—	800	2000	—	500	1000	—	
Output Voltage Swing	V_O	$V^+ = 5V$, $V^- = 0V$ $R_L = 10k\Omega$	0.6/4.1	—	—	0.7/4.1	—	—	0.8/4.0	—	—	V
		$V_S = \pm 15V$, $R_L = 25k\Omega$	± 14.1	—	—	± 14.1	—	—	± 14.0	—	—	
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$, $R_L = 10k\Omega$	—	100	—	—	100	—	—	100	—	kHz
Slew Rate	SR	$V_S = \pm 15V$ $R_L = 25k\Omega$	—	0.05	—	—	0.05	—	—	0.05	—	V/ μs
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	40	55	—	44	63	—	45	70	μA
		$V_S = \pm 15V$, No Load	—	55	80	—	57	85	—	80	95	



ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-20BJ/BZ and OP-20CJ/CZ, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-20FJ/FZ and OP-20GJ/GZ, and $0^\circ C \leq T_A \leq +70^\circ C$ for OP-20FP, OP-20GP, OP-20HP, OP-20HZ and OP-20HJ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-20B/F			OP-20C/G			OP-20H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnull'd	—	0.75	1.5	—	1.0	3.0	—	1.5	7.0	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	155	400	—	250	800	—	500	1700	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	2.5	—	1.0	3.5	—	1.5	5.0	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	27	—	14	33	—	16	45	nA
Input Voltage Range	IVR	$V^+ = +5V, V^- = 0V$ $V_S = \pm 15V$	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	$V^+ = +5V, V^- = 0V$ $0V \leq V_{CM} \leq 3.2V$	90	100	—	85	90	—	80	85	—	dB
		$V_S = \pm 15V$ $-15V \leq V_{CM} \leq 13.2V$	96	110	—	90	105	—	85	100	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	4	10	—	6	18	—	10	32	$\mu V/V$
		$V^- = 0V, V^+ = 5V$ to $30V$	—	4	10	—	6	18	—	10	57	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 50k\Omega$	500	700	—	400	600	—	250	400	—	V/mV
Output Voltage Swing	V_O	$V^+ = 5V, V^- = 0V, R_L = 50k\Omega$	0.6/4.0	—	—	0.9/3.9	—	—	1.0/3.8	—	—	V
		$V_S = \pm 15V, R_L = 50k\Omega$	± 14.0	—	—	± 13.9	—	—	± 13.9	—	—	
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load or $+5V, 0V$	—	50	65	—	53	75	—	55	85	μA
		$V_S = \pm 15V$, No Load	—	64	95	—	68	100	—	72	115	

NOTE:

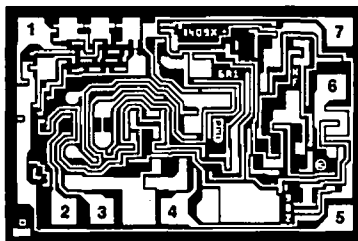
1. Sample tested.

5

OPERATIONAL AMPLIFIERS



DICE CHARACTERISTICS



DIE SIZE 0.069×0.046 inch, 3174 sq. mils
(1.75×1.17 mm, 2.05 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V^-
5. BALANCE
6. OUTPUT
7. V^+

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-20N LIMIT	OP-20G LIMIT	OP-20GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	600	1000	μV MAX
Input Offset Current	I_{OS}		1.5	2.5	4.0	nA MAX
Input Bias Current	I_B		25	30	40	nA MAX
Input Voltage Range	IVR	$V^+ = +5V$, $V^- = 0V$ $V_S = \pm 15V$	0/3.5 -15/13.5	0/3.5 -15/13.5	0/3.5 -15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V^+ = +5V$, $V^- = 0V$, $0V \leq V_{CM} \leq +3.5V$ $V_S = \pm 15V$, $-15V \leq V_{CM} \leq +13.5V$	95 100	90 94	85 90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ $V^- = 0V$, $V^+ = +5V$ to $+30V$	6	10	32	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$ $V_O = \pm 10V$	1000	800	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$, $V^+ = +5V$, $V^- = 0V$ $R_L = 25k\Omega$, $V_S = \pm 15V$	0.7/4.1 ± 14.1	0.8/4.1 ± 14.1	0.9/4.0 ± 14.0	V MIN
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	55 80	63 85	70 95	μA MAX

NOTE:

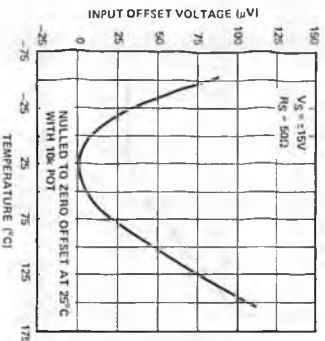
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

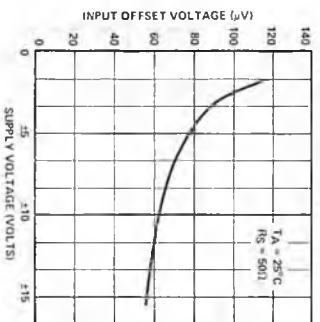
PARAMETER	SYMBOL	CONDITIONS	OP-20N TYPICAL	OP-20G TYPICAL	OP-20GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled	1.0	1.5	2.5	$\mu V/^\circ C$
	TCV_{OSn}	Nullled, $R_p = 10k\Omega$	1.0	1.5	2.5	
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	2000	2000	1000	V/mV

TYPICAL PERFORMANCE CHARACTERISTICS

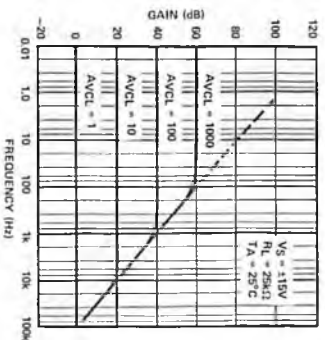
TRIMMED OFFSET VOLTAGE
VS TEMPERATURE



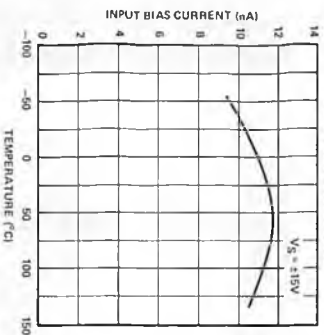
INPUT OFFSET VOLTAGE
VS POWER SUPPLY VOLTAGE



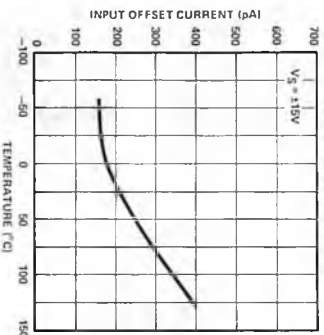
CLOSED-LOOP GAIN
VS FREQUENCY



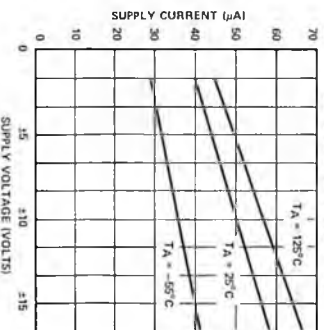
INPUT BIAS CURRENT
VS TEMPERATURE



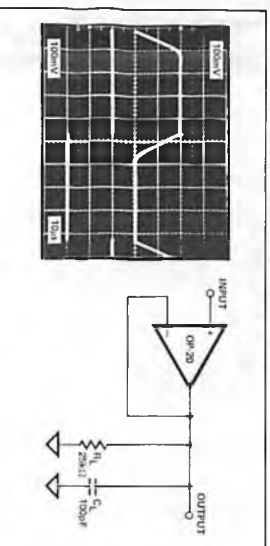
INPUT OFFSET CURRENT
VS TEMPERATURE



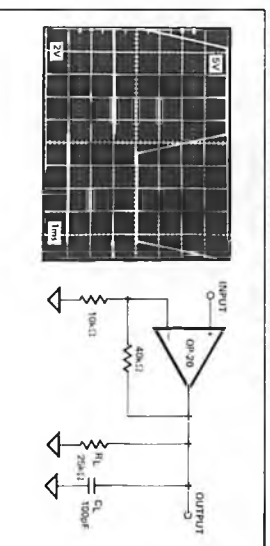
SUPPLY CURRENT
VS SUPPLY VOLTAGE



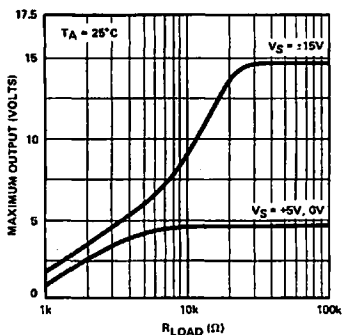
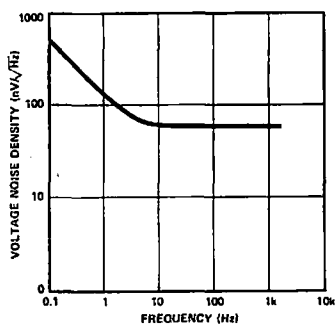
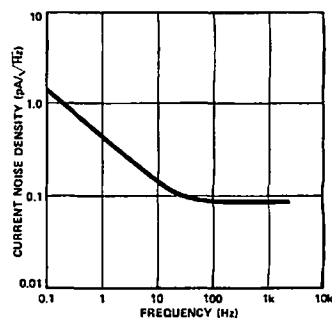
SMALL-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE

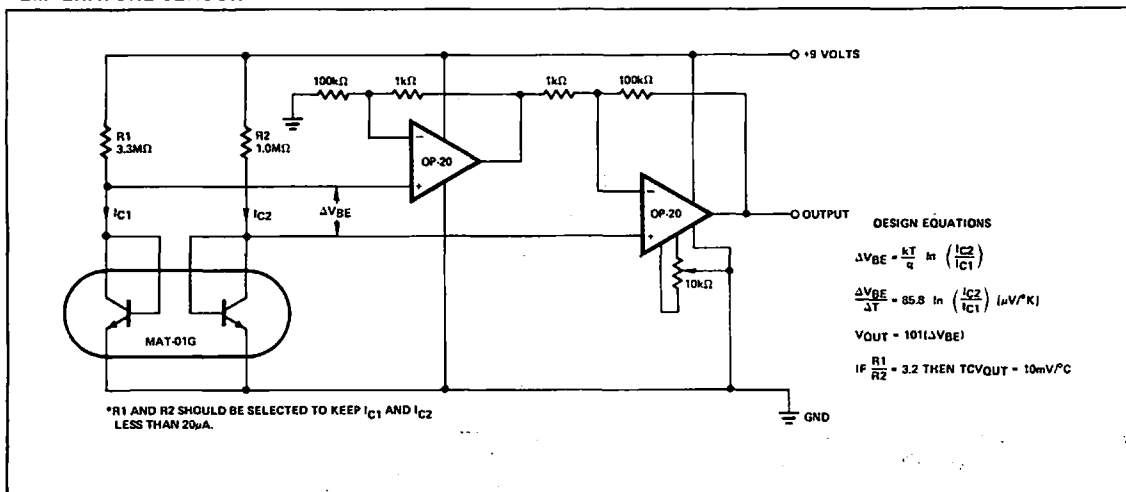


TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCEVOLTAGE NOISE DENSITY
vs FREQUENCYCURRENT NOISE DENSITY
vs FREQUENCY

TYPICAL APPLICATIONS

TEMPERATURE SENSOR





OP-21

LOW-POWER OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Supply Current 230 μ A Max
- Wide Supply Range ± 2.5 V to ± 15 V
- Low Input Offset Voltage 100 μ V Max
- Low Input Offset Voltage Drift 1.0 μ V/ $^{\circ}$ C Max
- High Common-Mode
Input Range V- (+0.5V) to V+ (-1.5V)
- High CMRR and PSRR 100dB Min
- High Open-Loop Gain 1000V/mV Min
- 125 $^{\circ}$ C Temperature Tested Dice

ORDERING INFORMATION†

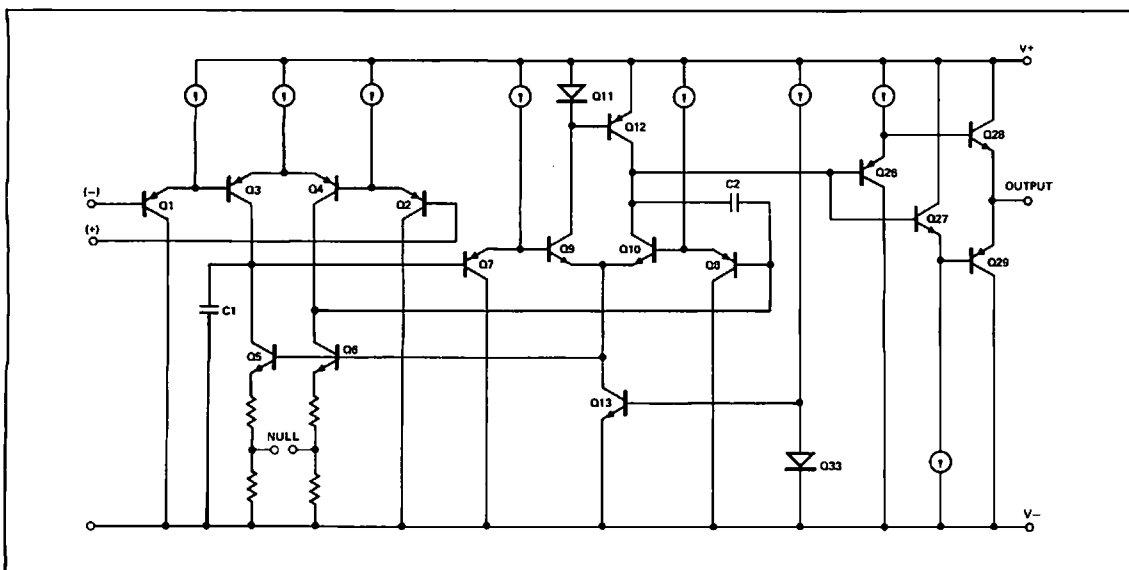
T _A = 25 $^{\circ}$ C V _{OS} MAX (μ V)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99	CERDIP	PLASTIC	
100	OP21AJ	OP21AZ	—	MIL
100	—	OP21EZ	—	IND
200	OP21BJ	OP21BZ	—	MIL
200	OP21FJ	OP21FZ	OP21FP	IND
500	OP21GJ	—	OP21GP	IND
500	—	—	OP21HS††	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

SIMPLIFIED SCHEMATIC

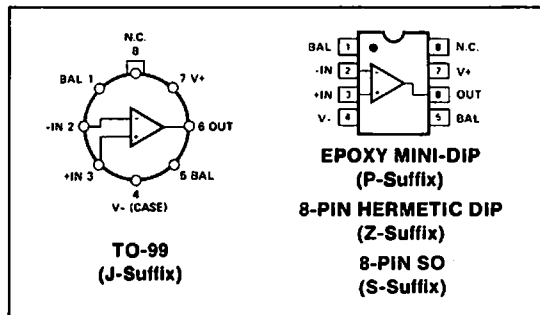


GENERAL DESCRIPTION

The OP-21 is a precision low-power operational amplifier offering the benefits of low offset voltage and high slew rate with the advantages of low power. A supply range of ± 2.5 V to ± 15 V allows a wide range of applications.

Two military temperature range models and three industrial temperature range models are available in TO-99 cans and 8-Pin hermetic DIPs. Industrial temperature range models are also available in 8-Pin epoxy DIPs. See OP-221 for dual and OP-421 for quad versions of the OP-21.

PIN CONNECTIONS



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J and Z Packages	-65°C to +125°C
P Package	-65°C to +125°C
Operating Temperature Range	
OP-21A, OP-21B	-55°C to +125°C
OP-21E, OP-21F, OP-21G	-25°C to +85°C
OP-21HS	0°C to +70°C

DICE Junction Temperature (T_J) -65°C to +150°C
 Lead Temperature Range (Soldering, 60 sec) 300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$ and $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21A/E			OP-21B/F			OP-21G/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$V_S = \pm 15V$	—	40	100	—	150	200	—	300	500	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.6	4	—	0.8	5	—	1.2	6	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	50	100	—	60	120	—	70	150	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	-14.5/13.5	—	—	-14.5/13.5	—	—	-14.5/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V$, No Load $-14.5V \leq V_{CM} \leq 13.5V$	100	110	—	90	105	—	84	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$, No Load	—	2	6	—	4	10	—	10	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$, $V_O \pm 10V$	1000	2000	—	500	1500	—	500	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$	-13.7/14.0	—	—	-13.7/13.9	—	—	-13.6/13.8	—	—	V
Slew Rate	SR	$C_L = 100pF$, $R_L = 25k\Omega$	—	0.25	—	—	0.25	—	—	0.25	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$, $R_L = 10k\Omega$	—	600	—	—	600	—	—	600	—	kHz
Supply Current	I_{SY}	$V_S = \pm 2.5V$, No Load	—	170	230	—	180	275	—	180	300	μA
		$V_S = \pm 15V$, No Load	—	230	300	—	235	360	—	250	420	



ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-21A and OP-21B, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-21E, OP-21F and OP-21G, $0^\circ C \leq T_A \leq 70^\circ C$ for OP-21H, unless otherwise noted.

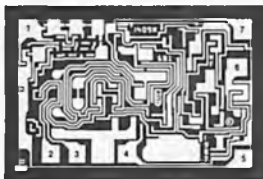
PARAMETER	SYMBOL	CONDITIONS	OP-21A/E			OP-21B/F			OP-21G/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Notes 1, 2)	TCV _{OS} TCV _{OSn}	Unnulled	—	0.5	1.0	—	1.0	2.0	—	2.5	5.0	$\mu V/^\circ C$
		Nulled	—	—	—	—	—	—	—	—	—	
Input Offset Voltage	V _{OS}		—	75	200	—	200	500	—	500	1000	μV
Input Offset Current	I _{OS}	V _{CM} = 0	—	0.7	5	—	0.7	6	—	0.8	8	nA
Input Bias Current	I _B	V _{CM} = 0	—	50	110	—	60	130	—	70	165	nA
Input Voltage Range	IVR		-14.3/13.2	—	—	-14.3/13.2	—	—	-14.3/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	No Load, V _S = $\pm 15V$, -14.5V $\leq$ V _{CM} $\leq 13.2V$	98	105	—	86	100	—	80	95	—	dB
			—	—	—	—	—	—	—	—	—	
Power Supply Rejection Ratio	PSRR	V _S = $\pm 2.5V$ to $\pm 15V$, No Load	—	4	10	—	6	18	—	18	57	$\mu V/V$
Large-Signal Voltage Gain	A _{VO}	V _S = $\pm 15V$, R _L = 20k Ω , V _O = $\pm 10V$	500	1500	—	250	1300	—	250	1000	—	V/mV
Output Voltage Swing	V _O	V _S = $\pm 15V$, R _L = 20k Ω	-13.5/13.8	—	—	-13.5/13.7	—	—	-13.5/13.6	—	—	V
Supply Current	I _{SY}	V _S = $\pm 2.5V$, No Load	—	205	275	—	215	330	—	230	360	μA
		V _S = $\pm 15V$, No Load	—	275	360	—	285	430	—	300	500	

NOTES:

1. Sample tested.
2. TCV_{OSn} is guaranteed by unnulled TCV_{OS} and device design.



DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)

DIE SIZE 0.069 × 0.046 inch, 3174 sq. mils
(1.75 × 1.17 mm, 2.05 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. BALANCE
6. OUTPUT
7. V₊

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-21N, OP-21G and OP-21GR devices; $T_A = 125^\circ C$ for OP-21NT and OP-21GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21NT LIMIT	OP-21N LIMIT	OP-21GT LIMIT	OP-21G LIMIT	OP-21GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	100	500	200	500	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	4	4	5	5	6	nA MAX
Input Bias Current	I_B	$V_{CM} = 0$	100	100	120	120	150	nA MAX
Input Voltage Range	IVR		-14.3 +13.5	-14.5 +13.5	-14.3 +13.5	-14.5 +13.5	-14.5 +13.5	V MIN
Common-Mode Rejection Ratio	CMRR	No Load $CMVR = IVR$	96	100	86	90	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ No Load	10	6	18	10	32	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$, $V_O = \pm 10V$	500	1000	250	500	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$	-13.5 +13.8	-13.7 +14.0	-13.5 +13.8	-13.7 +13.9	-13.6 +13.8	V MIN
Supply Current	I_{SY}	No Load	300	300	360	360	420	μA MAX

NOTES:

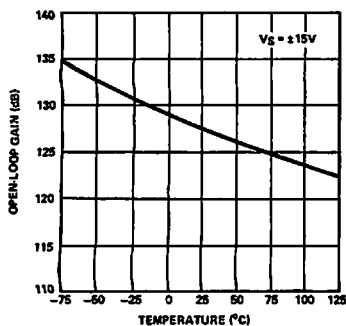
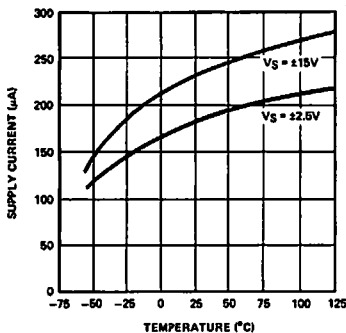
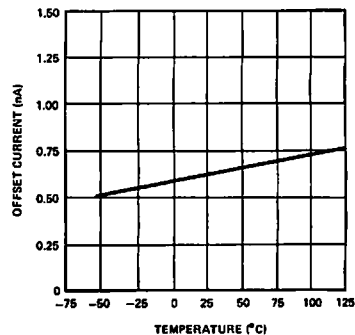
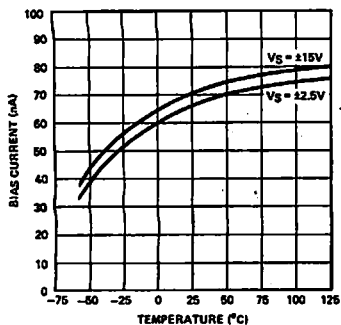
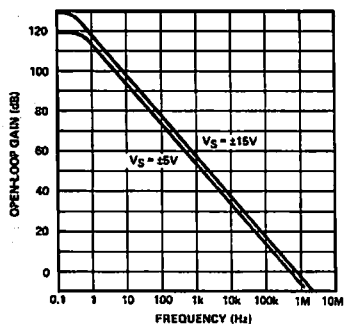
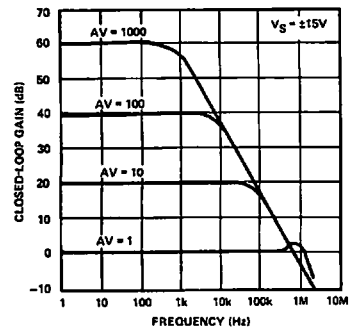
For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

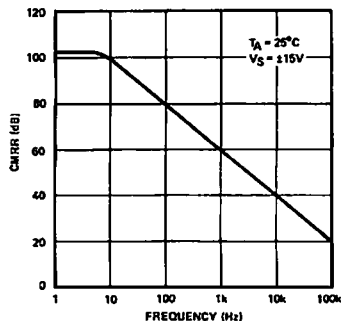
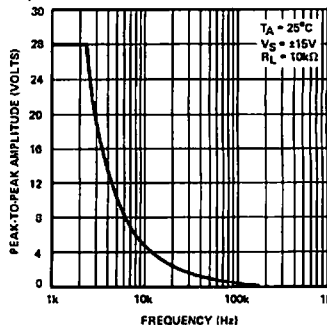
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-21NT TYPICAL	OP-21N TYPICAL	OP-21GT TYPICAL	OP-21G TYPICAL	OP-21GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnulled	0.5	0.5	1	1	2.5	$\mu V/^\circ C$
Nullled Input Offset Voltage Drift	TCV_{OSn}	Nullled, $R_p = 10k\Omega$	0.5	0.5	1	1	2.5	$\mu V/^\circ C$
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$	2000	2000	1500	1500	1000	V/mV
Slew Rate	SR	$R_L = 25k\Omega$ $C_L = 100pF$	0.25	0.25	0.25	0.25	0.25	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ $R_L = 10k\Omega$	600	600	600	600	600	kHz

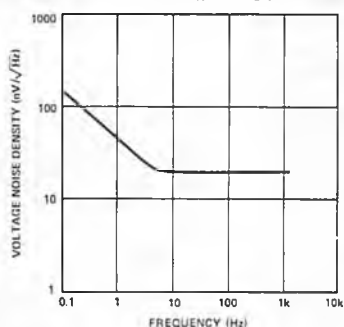
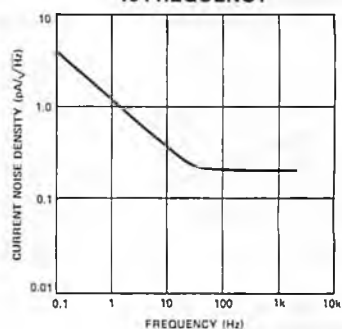
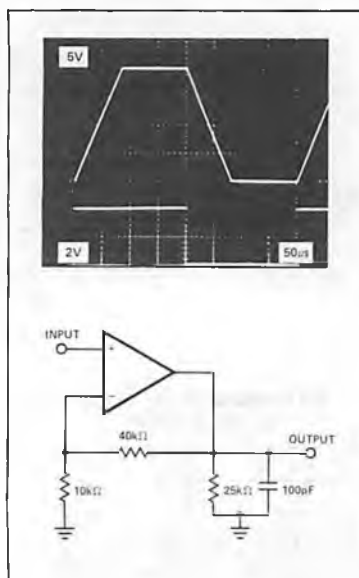
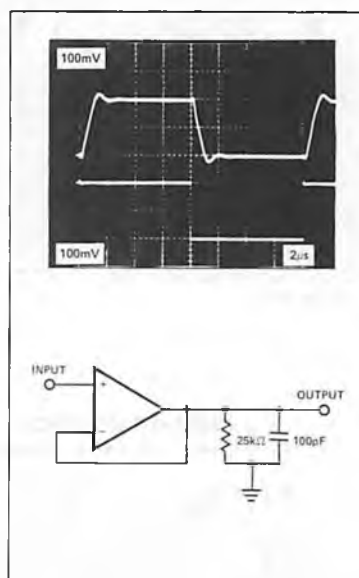
TYPICAL PERFORMANCE CHARACTERISTICS

 OPEN-LOOP GAIN
vs TEMPERATURE

 SUPPLY CURRENT
vs TEMPERATURE

 OFFSET CURRENT
vs TEMPERATURE

 BIAS CURRENT
vs TEMPERATURE

 OPEN-LOOP GAIN
vs FREQUENCY

 CLOSED-LOOP GAIN
vs FREQUENCY


CMRR vs FREQUENCY


 MAXIMUM OUTPUT SWING
vs FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE DENSITY
vs FREQUENCYCURRENT NOISE DENSITY
vs FREQUENCYNONINVERTING
LARGE-SIGNAL RESPONSENONINVERTING
SMALL-SIGNAL RESPONSE

FEATURES

- Programmable Supply Current $1\mu\text{A}$ to $400\mu\text{A}$
- Single Supply Operation $+3\text{V}$ to $+30\text{V}$
- Dual Supply Operation $\pm 1.5\text{V}$ to $\pm 15\text{V}$
- Low Input Offset Voltage $100\mu\text{V}$
- Low Input Offset Voltage Drift $0.75\mu\text{V}/^\circ\text{C}$
- High Common-Mode Input Range ... V^- to V^+ (-1.5V)
- High CMRR and PSRR 115dB
- High Open-Loop Gain 1800V/mV
- $\pm 30\text{V}$ Input Overvoltage Protection
- Unity-Gain Stable
- LM4250 Pinout and Nulling

GENERAL DESCRIPTION

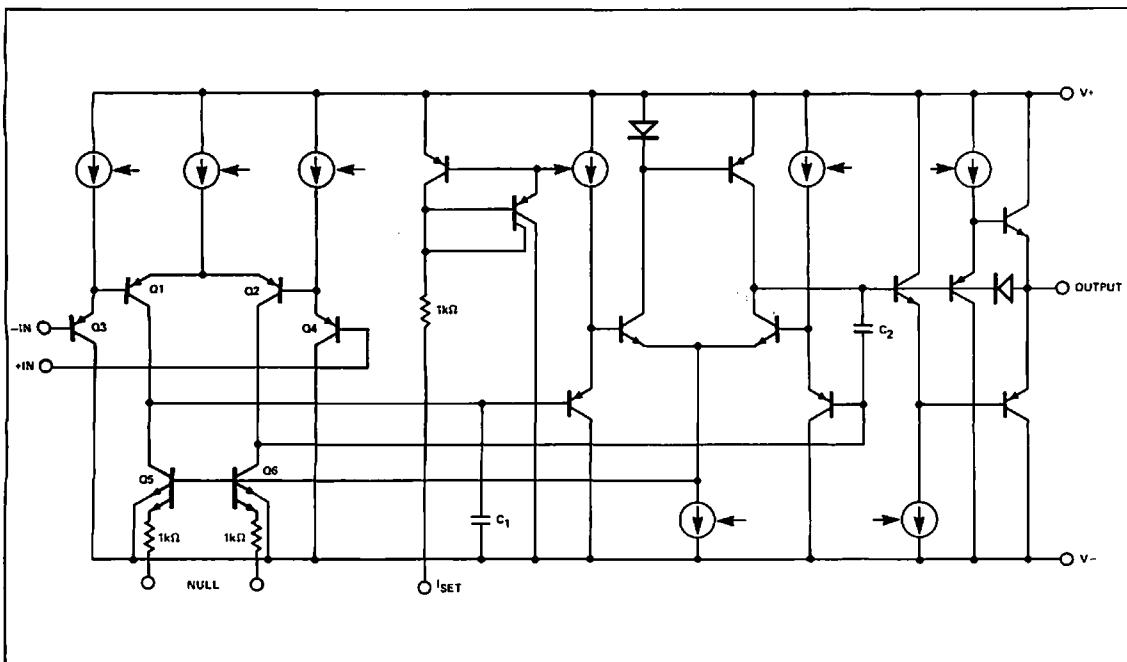
The OP-22 is a monolithic micropower operational amplifier designed to provide excellent accuracy in high-gain applications. Offsets are very low which generally eliminates any need for external nulling of V_{OS} . The OP-22 is internally compensated and unity-gain stable. It also features high open-loop gain, CMRR, and PSRR. This assures good gain accuracy and rejection of power supply variations even when

used in circuits with high closed-loop gain. The low offsets and high gain accuracy of the OP-22 bring precision performance to the micropower field.

The OP-22 is a versatile op amp designed for operation from battery or solar-cell power sources. Supply current is programmable over a range of $1\mu\text{A}$ to $400\mu\text{A}$ with a single external resistor. Input voltage range is very wide and extends down to the negative rail, thus the common-mode input voltage range includes ground when operating from a single supply voltage. This ability to provide high DC performance over a wide input range is particularly useful in single-battery applications. In addition, the OP-22 is characterized over a wide supply range of $\pm 1.5\text{V}$ to $\pm 15\text{V}$, or $+3\text{V}$ to $+30\text{V}$ for single supply.

The OP-22 pin-out and offset nulling are identical to the LM4250 and many other micropower operational amplifiers. This functional commonality allows easy upgrading of system performance. By selection of set resistor value, the circuit designer can readily use the OP-22 in place of such amplifiers as the LM108, LM112, LM4250, $\mu\text{A}776$, and ICL8021 in high-gain, low-frequency applications.

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage		$\pm 18\text{V}$
Power Dissipation (Note 1)		500mW
Differential Input Voltage		$\pm 30\text{V}$
Input Voltage		Supply Voltage
Storage Temperature Range		
J and Z Packages		-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range		
OP-22A (J or Z package)		-55°C to $+125^{\circ}\text{C}$
OP-22E, OP-22F (J or Z package)		-25°C to $+85^{\circ}\text{C}$
OP-22HJ, OP-22HZ		0°C to $+70^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 sec)		300°C
DICE Junction Temperature		-65°C to $+150^{\circ}\text{C}$

NOTES:

1. See table for maximum ambient temperature rating.
2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

	MAXIMUM AMBIENT TEMPERATURE $V_S = \pm 15\text{V}$ and $I_{SET} = 10\mu\text{A}$	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	124°C	—
8-Pin Hermetic DIP (Z)	124°C	—

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5\text{V}$ to $\pm 15\text{V}$, $1\mu\text{A} \leq I_{SET} \leq 10\mu\text{A}$, $T_A = +25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22A/E			OP-22F			OP-22H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	100	300	—	200	500	—	400	1000	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	—	0.5	3	nA
Input Bias Current	I_B	$I_{SET} = 1\mu\text{A}$, $V_{CM} = 0$	—	2.6	5	—	3.0	7.5	—	4.0	10	nA
		$I_{SET} = 10\mu\text{A}$, $V_{CM} = 0$	—	19	30	—	24	35	—	30	50	
Input Voltage Range	IVR	$V_+ = +5\text{V}$, $V_- = 0\text{V}$.	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15\text{V}$	$-15/+13.5$	—	—	$-15/+13.5$	—	—	$-15/+13.5$	—	—	
Common-Mode Rejection Ratio	CMRR (Note 2)	$V_S = \pm 15\text{V}$ $-15\text{V} \leq V_{CM} \leq +13.5\text{V}$	100	115	—	95	105	—	85	95	—	dB
Power Supply Rejection Ratio (Note 1)	PSRR (Note 2)	$V_S = \pm 1.5\text{V}$ to $\pm 15\text{V}$; and $V_- = 0\text{V}$, $V_+ = 3\text{V}$ to 30V .	—	1.8	6	—	6	18	—	10	32	$\mu\text{V/V}$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15\text{V}$, $I_{SET} = 1\mu\text{A}$, $R_L = 100\text{k}\Omega$.	1000	1800	—	500	900	—	250	500	—	V/mV
		$V_S = \pm 15\text{V}$, $I_{SET} = 10\mu\text{A}$, $R_L = 10\text{k}\Omega$.	1000	1800	—	500	900	—	300	500	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 1.5\text{V}$, $I_{SET} = 1\mu\text{A}$, $R_L = 100\text{k}\Omega$ & $I_{SET} = 10\mu\text{A}$, $R_L = 10\text{k}\Omega$.	± 0.8	± 0.82	—	± 0.8	± 0.82	—	± 0.75	± 0.8	—	V
		$V_S = \pm 15\text{V}$, $I_{SET} = 1\mu\text{A}$, $R_L = 100\text{k}\Omega$ & $I_{SET} = 10\mu\text{A}$, $R_L = 10\text{k}\Omega$.	± 14	± 14.2	—	± 14	± 14.2	—	± 13.5	± 14	—	V
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$, $V_S = \pm 15\text{V}$, $I_{SET} = 10\mu\text{A}$, $R_L = 10\text{k}\Omega$.	—	250	—	—	250	—	—	250	—	kHz
Slew Rate	SR	$V_S = \pm 15\text{V}$, $I_{SET} = 10\mu\text{A}$, $R_L = 10\text{k}\Omega$.	—	0.08	—	—	0.08	—	—	0.08	—	V/ μs
Supply Current No Load	I_{SY}	$V_S = \pm 15\text{V}$, $I_{SET} = 1\mu\text{A}$.	—	15	17	—	16	19	—	18	21	μA
		$V_S = \pm 15\text{V}$, $I_{SET} = 10\mu\text{A}$.	—	150	170	—	160	190	—	160	210	
		$V_S = \pm 1.5\text{V}$, $I_{SET} = 1\mu\text{A}$.	—	10.5	12.5	—	14	16	—	17	20	μA
		$V_S = \pm 1.5\text{V}$, $I_{SET} = 10\mu\text{A}$.	—	105	125	—	140	160	—	170	200	

NOTES:

1. Sample tested for single-supply operation, 100% tested for dual-supply operation.
2. Measured with V_{OS} unnullified and I_{SET} constant.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 10\mu A$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-22AJ/AZ, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-22EJ/EZ and OP-22FZ, and $0^\circ C \leq T_A \leq +70^\circ C$ for OP-22HZ, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22A/E			OP-22F			OP-22H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.75	1.5	—	1.0	2.0	—	1.5	3.0	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	175	400	—	350	600	—	500	1200	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.2	1	—	0.3	2	—	0.5	3	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	2	10	—	3	15	—	5	25	$pA/^\circ C$
Input Bias Current	I_B	$I_{SET} = 1\mu A, V_{CM} = 0$	—	2.8	5	—	3.3	7.5	—	4.5	10	nA
		$I_{SET} = 10\mu A, V_{CM} = 0$	—	21	30	—	27	35	—	34	50	
Input Voltage Range	IVR	$V^+ = +5V, V^- = 0V$	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	-15/+13.2	—	—	-15/+13.2	—	—	-15/+13.2	—	—	
Common-Mode Rejection Ratio	$CMRR$ (Note 3)	$V_S = \pm 15V$ $-15V \leq V_{CM} \leq +13.2V$										dB
		$I_{SET} = 1\mu A$	80	105	—	80	99	—	80	90	—	
		$I_{SET} = 10\mu A$	90	115	—	86	105	—	80	90	—	
Power Supply Rejection Ratio	$PSRR$ (Note 3)	$V_S = \pm 1.5V$ to $\pm 15V$ & $V^- = 0V$, $V^+ = 3V$ to $30V$ (Note 2)	—	3.2	10	—	10	32	—	32	56	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $I_{SET} = 1\mu A, R_L = 100k\Omega$	200	400	—	200	400	—	100	250	—	V/mV
		$V_S = \pm 15V$, $I_{SET} = 10\mu A, R_L = 10k\Omega$	500	1000	—	300	750	—	150	300	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 1.5V$, $I_{SET} = 1\mu A, R_L = 100k\Omega$ & $I_{SET} = 10\mu A, R_L = 10k\Omega$	± 0.65	± 0.75	—	± 0.65	± 0.75	—	± 0.6	± 0.7	—	V
		$V_S = \pm 15V$, $I_{SET} = 1\mu A, R_L = 100k\Omega$ & $I_{SET} = 10\mu A, R_L = 10k\Omega$	± 13.8	± 13.8	—	± 13.8	± 13.8	—	± 13.0	± 13.5	—	V
Supply Current No Load	I_{SY}	$V_S = \pm 15V, I_{SET} = 1\mu A$	—	18	18	—	17	20	—	20	25	μA
		$V_S = \pm 15V, I_{SET} = 10\mu A$	—	160	180	—	170	200	—	200	250	μA
		$V_S = \pm 1.5V, I_{SET} = 1\mu A$	—	12	14	—	15	18	—	19	25	μA
		$V_S = \pm 1.5V, I_{SET} = 10\mu A$	—	120	140	—	150	180	—	190	250	μA

NOTES:

- Sample tested.
- $V_{CM} = 1.5V$

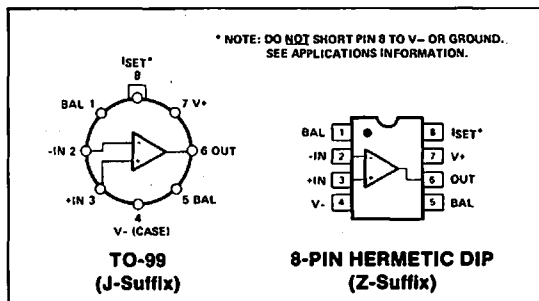
- Measured with V_{OS} unnulled and I_{SET} constant.

ORDERING INFORMATION†

$T_A = 25^\circ C$ $V_{OS} \text{ MAX}$ (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	
300	OP22AJ*	OP22AZ*	MIL
300	OP22EJ	OP22EZ	IND
500	—	OP22FZ	IND
1000	—	OP22HZ	COM

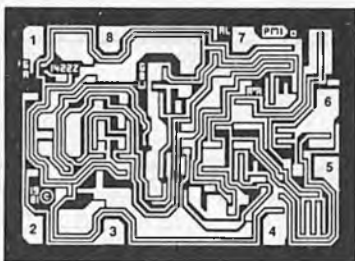
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

PIN CONNECTIONS




DICE CHARACTERISTICS



DIE SIZE 0.070 × 0.050 inch, 3500 sq. mils
(1.78 × 1.27 mm, 2.26 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. BALANCE
6. OUTPUT
7. V₊
8. I_{SET}

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22N LIMIT	OP-22G LIMIT	OP-22GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		300	500	1000	μV MAX
Input Offset Current	I_{OS}	(Note 1)	1	2	3	nA MAX
Input Bias Current	I_B	$I_{SET} = 1\mu A$	5	7.5	10	nA MAX
		$I_{SET} = 10\mu A$ (Note 1)	30	35	50	
Input Voltage Range	IVR	$V_+ = +5V$, $V_- = 0V$	0/3.5	0/3.5	0/3.5	V MIN
		$V_S = \pm 15V$	-15/+13.5	-15/+13.5	-15/+13.5	
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V$, $-15V \leq V_{CM} \leq +13.5V$ (Note 2)	100	95	85	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ $V_- = 0V$, $V_+ = 3V$ to $30V$ (Note 2)	6	18	32	$\mu V/V$ MIN
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$	1000	500	250	V/mV MIN
		$V_S = \pm 15V$, $I_{SET} = 10\mu A$, $R_L = 10k\Omega$	1000	500	300	V/mV MIN
Output Voltage Swing	V_O	$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$	± 0.8	± 0.8	± 0.75	V MIN
		$V_S = \pm 15V$, $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$	± 14	± 14	± 13.5	V MIN
Supply Current No Load	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	17	19	21	μA MAX
		$V_S = \pm 15V$, $I_{SET} = 10\mu A$	170	190	210	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	12.5	16	20	μA MAX
		$V_S = \pm 1.5V$, $I_{SET} = 10\mu A$	125	160	200	

NOTES:

1. $V_{CM} = 0$
2. Measured with V_{OS} unnullled and I_{SET} held constant.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

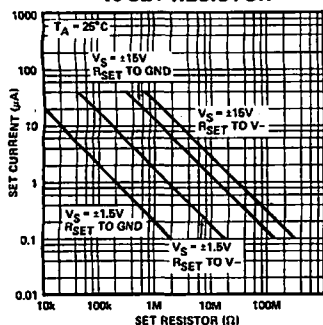
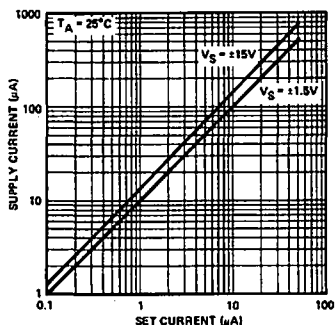
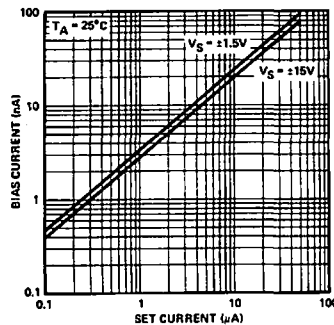
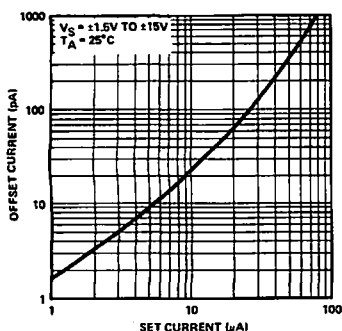
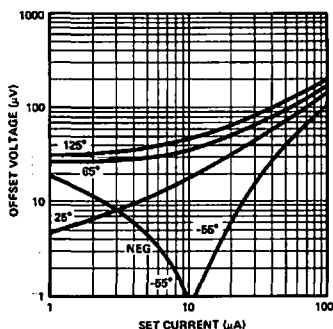
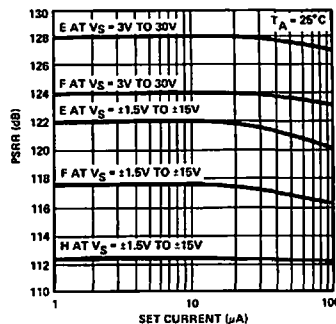
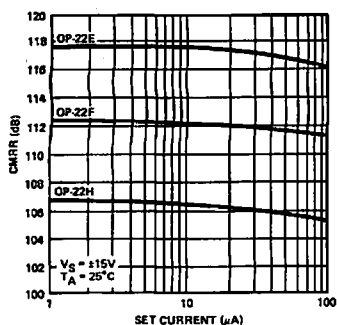
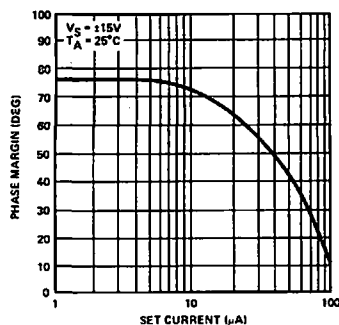
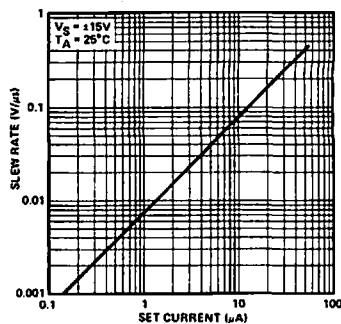
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $1\mu A \leq I_{SET} \leq 10\mu A$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-22N TYPICAL	OP-22G TYPICAL	OP-22GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	Unnullled	1.0	1.5	2.5	$\mu V/^\circ C$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $I_{SET} = 1\mu A$, $R_L = 100k\Omega$ & $I_{SET} = 10\mu A$, $R_L = 10k\Omega$	1800	900	500	V/mV

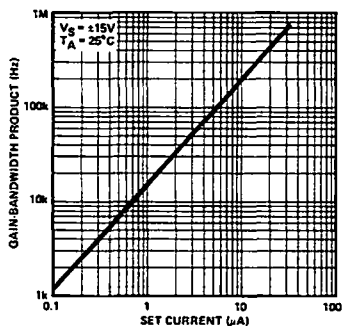
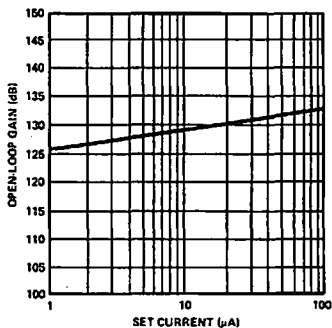
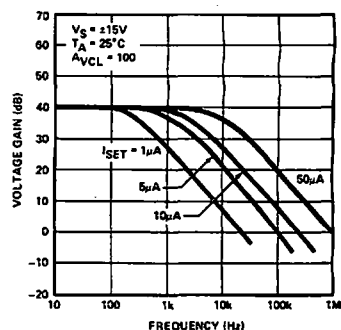
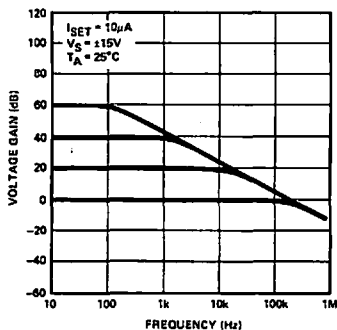
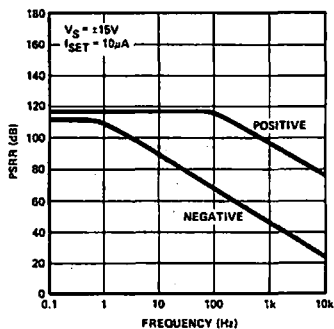
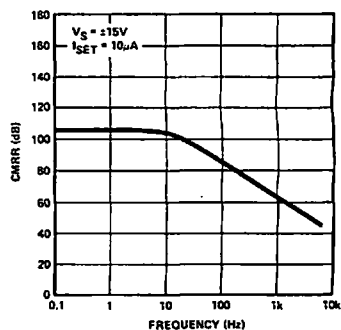
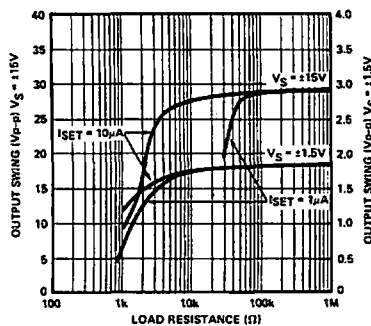
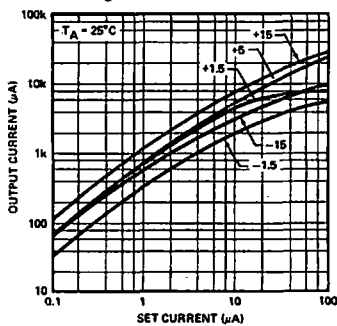
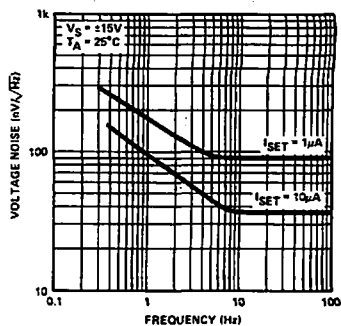
TYPICAL PERFORMANCE CHARACTERISTICS

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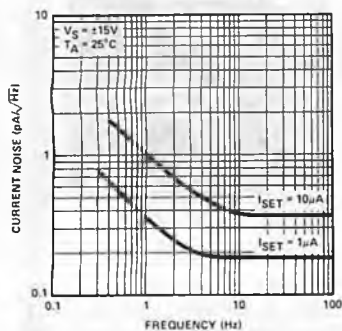
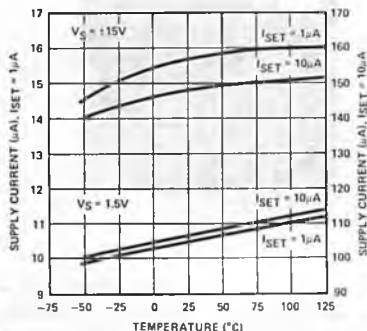
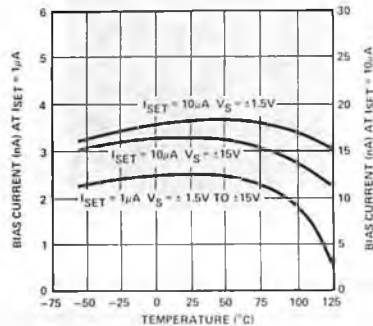
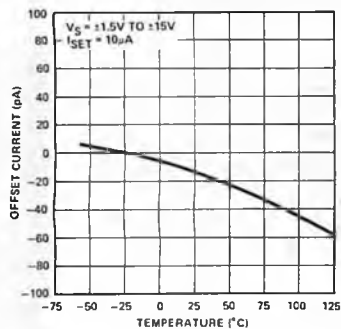
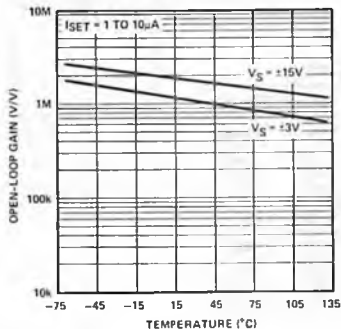
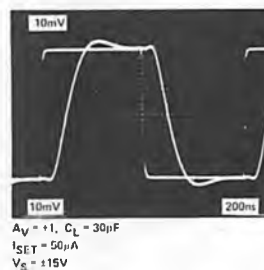
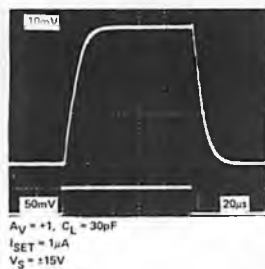
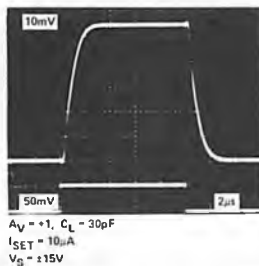
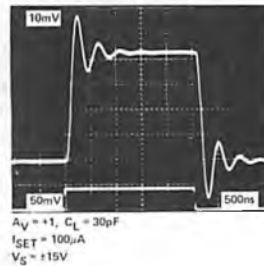
OPERATIONAL AMPLIFIERS

 SET CURRENT
vs SET RESISTOR

 SUPPLY CURRENT
vs SET CURRENT

 BIAS CURRENT
vs SET CURRENT

 OFFSET CURRENT
vs SET CURRENT

 OFFSET VOLTAGE
vs SET CURRENT

 POWER SUPPLY REJECTION
vs SET CURRENT

 COMMON-MODE REJECTION
vs SET CURRENT

 PHASE MARGIN
vs SET CURRENT

 SLEW RATE
vs SET CURRENT


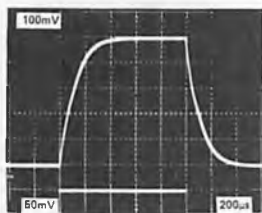
TYPICAL PERFORMANCE CHARACTERISTICS

 GAIN-BANDWIDTH PRODUCT
vs SET CURRENT

 OPEN-LOOP GAIN
vs SET CURRENT

 FREQUENCY RESPONSE
vs SET CURRENT

 CLOSED-LOOP
FREQUENCY RESPONSE

 POWER SUPPLY REJECTION
vs FREQUENCY

 COMMON-MODE REJECTION
vs FREQUENCY

 PEAK-TO-PEAK
OUTPUT SWING
vs LOAD RESISTANCE

 MAXIMUM OUTPUT CURRENT
vs SET CURRENT AT
 $V_S = \pm 15V$, +5 AND ± 1.5

 VOLTAGE NOISE
vs FREQUENCY


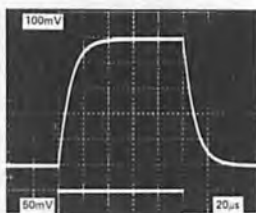
TYPICAL PERFORMANCE CHARACTERISTICS

CURRENT NOISE
vs FREQUENCY

SUPPLY CURRENT
vs TEMPERATURE

BIAS CURRENT
vs TEMPERATURE

OFFSET CURRENT
vs TEMPERATURE

OPEN-LOOP GAIN
vs TEMPERATURE

SMALL-SIGNAL
TRANSIENT RESPONSE

SMALL-SIGNAL
TRANSIENT RESPONSE

SMALL-SIGNAL
TRANSIENT RESPONSE

SMALL-SIGNAL
TRANSIENT RESPONSE


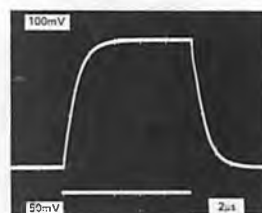
TYPICAL PERFORMANCE CHARACTERISTICS

SMALL-SIGNAL
TRANSIENT RESPONSE

$A_V = +10$, $C_L = 30\text{pF}$
 $I_{SET} = 1\mu\text{A}$
 $V_S = \pm 15\text{V}$

SMALL-SIGNAL
TRANSIENT RESPONSE

$A_V = +10$, $C_L = 30\text{pF}$
 $I_{SET} = 10\mu\text{A}$
 $V_S = \pm 15\text{V}$

SMALL-SIGNAL
TRANSIENT RESPONSE

$A_V = +10$, $C_L = 30\text{pF}$
 $I_{SET} = 100\mu\text{A}$
 $V_S = \pm 15\text{V}$

APPLICATIONS INFORMATION

OP-22 series units may be inserted directly into LM4250, $\mu\text{A}776$ and ICL8021 sockets with or without removal of external nulling components. The value of set resistor for a given supply current varies between types and the manufacturer's data sheets should be consulted for this information. Table 1 compares set resistor values for the OP-22 and the LM4250. (R_{SET} connected to V_-).

TABLE 1
 Supply Current vs. Set Resistor for OP-22 and LM4250

	$I_{SY} = 10\mu\text{A}$		$I_{SY} = 30\mu\text{A}$		$I_{SY} = 100\mu\text{A}$	
V_{SUPPLY}	OP-22	LM4250	OP-22	LM4250	OP-22	LM4250
$\pm 1.5\text{V}$	2.2M Ω	1.3M Ω	680k Ω	430k Ω	220k Ω	120k Ω
$\pm 3.0\text{V}$	6.8M Ω	2.7M Ω	2.2M Ω	910k Ω	680k Ω	270k Ω
$\pm 5.0\text{V}$	13M Ω	4.7M Ω	4.3M Ω	1.5M Ω	1.3M Ω	470k Ω
$\pm 12\text{V}$	33M Ω	12M Ω	11M Ω	3.9M Ω	3.3M Ω	1.2M Ω
$\pm 15\text{V}$	43M Ω	15M Ω	15M Ω	5.1M Ω	4.3M Ω	1.5M Ω
I_{SET}	0.67 μA	1.8 μA	2.0 μA	6.0 μA	6.7 μA	20 μA

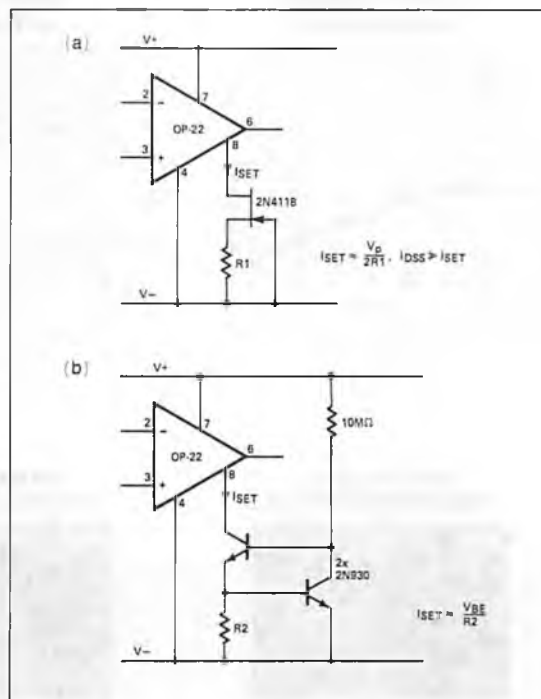
SET-RESISTOR SELECTION

The value of set resistor for selected supply current may be calculated using the "Supply current vs. Set current" curve and the formula;

$$R_{SET} = \frac{(V_{SUPPLY} - 2V_{BE})}{I_{SET}} \quad (1)$$

Alternatively, the "Supply Current vs. Set Current" graph may be used in conjunction with the "Set Current vs. Set Resistor" graph. V_{SUPPLY} in formula (1) refers to the total supply voltage with R_{SET} connected between pin 8 and negative supply. R_{SET} may be connected to ground in which case V_{SUPPLY} in (1) is the positive supply.

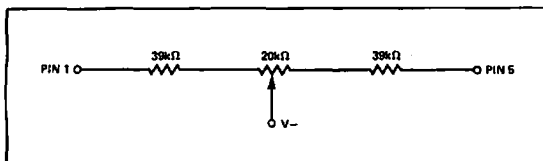
Biasing the OP-22 with a fixed resistor produces a supply current approximately proportional to supply voltage. In applications where a constant drain is required with varying supply, R_{SET} can be replaced by current generators. Two suggested arrangements are shown below:



CAUTION: Shorting of pin 8 to negative supply or ground will cause excessive I_{SET} which in turn will cause excessive supply current to flow. I_{SET} should always be limited.

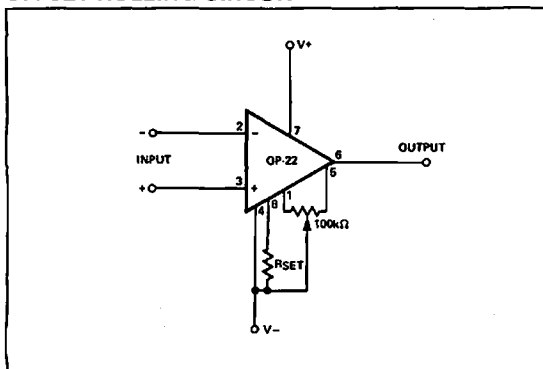
OFFSET VOLTAGE ADJUSTMENT

The offset voltage can be trimmed to zero using a 100k Ω potentiometer (see offset nulling circuit). Adjustment range is approximately $\pm 5\text{mV}$. Resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors as shown below.

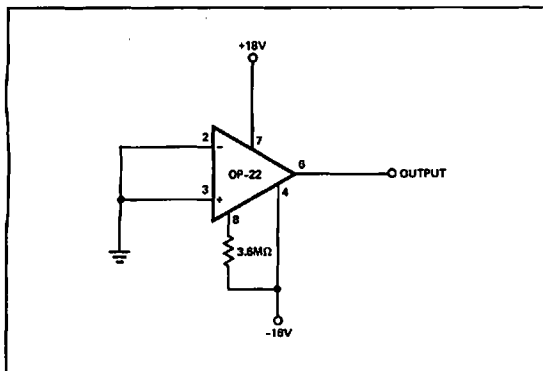


This arrangement has a $\pm 500\mu\text{V}$ adjustment range. Offset nulling of the OP-22 has negligible effect on the value of TCV_{OS} .

OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT*



*Other circuits may apply at PMI's discretion.

APPLICATIONS CIRCUITS

A micropower bandgap voltage reference operating at a quiescent current of $15\mu\text{A}$ may be constructed using an OP-22 and a MAT-01 dual transistor (see Figure 1). The circuit provides a 1.23V reference with better performance than micropower I.C. shunt regulators and has the advantages of being a series regulator.

MICROPOWER 1.23 VOLT BANDGAP REFERENCE

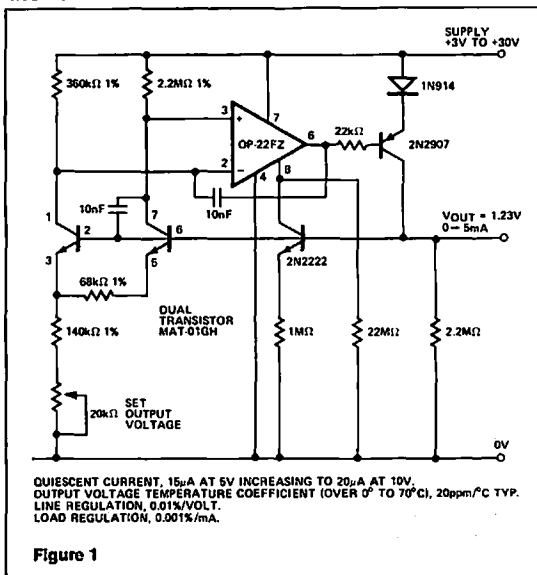


Figure 1

GATED MICROPOWER AMPLIFIER

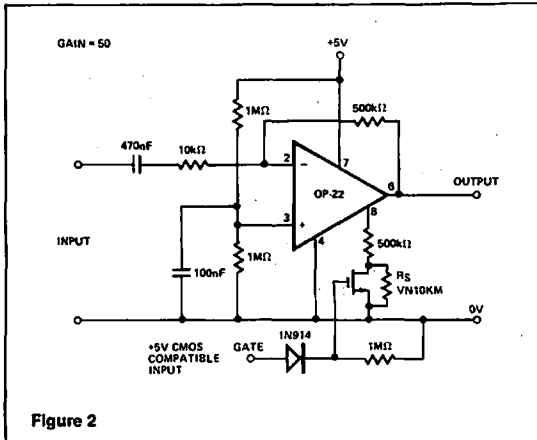
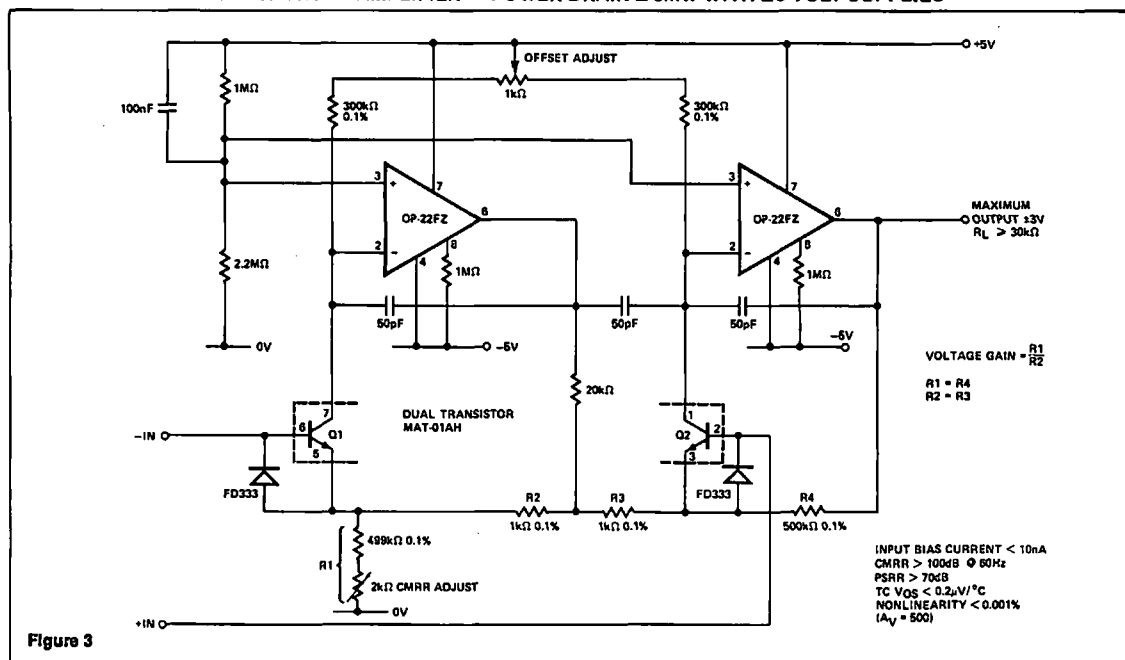


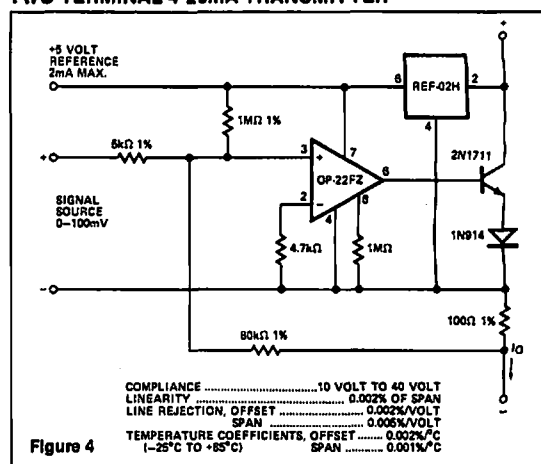
Figure 2

MICROPOWER INSTRUMENTATION AMPLIFIER — POWER DRAIN $\leq 3\text{mW}$ WITH $\pm 5\text{V}$ SUPPLIES

In Figure 2, the OP-22 is used as a gated amplifier where power consumption and bandwidth are controllable. R_S can be selected for a specific lower-power operation or omitted so the amplifier can be completely shut down.

A micropower instrumentation amplifier that consumes less than 3mW with $\pm 5\text{V}$ supplies is shown in Figure 3. Offset voltage drift is less than $0.2\mu\text{V}/^\circ\text{C}$ and common-mode input range is $\pm 3\text{V}$ with CMRR of over 100dB at 60Hz .

Process control systems use two-wire $4\text{-}20\text{mA}$ current transmitters when sending analog signals through noisy environments. The "zero" or "offset" current of 4mA may be used to power the transmitter signal conditioning amplifiers and/or excite a d.c. transducer. This allows remote signal conditioning without having a remote power source. Power is provided at the receiving end where the signal current is monitored by a precision 50Ω resistor. The $4\text{-}20\text{mA}$ transmitter shown in Figure 4 has high stability, excellent linearity, and generates the $4\text{-}20\text{mA}$ current output. A 5V reference is available for powering transducers and micropower amplifiers at a maximum current of 2mA .

TWO TERMINAL $4\text{-}20\text{mA}$ TRANSMITTER

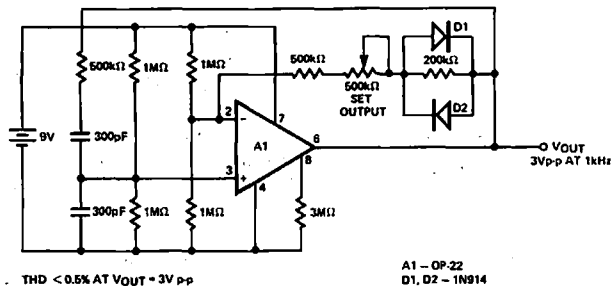
MICROPOWER WIEN-BRIDGE OSCILLATOR ($P_d < 500 \mu W$)

Figure 5

MICROPOWER 5 VOLT REGULATOR

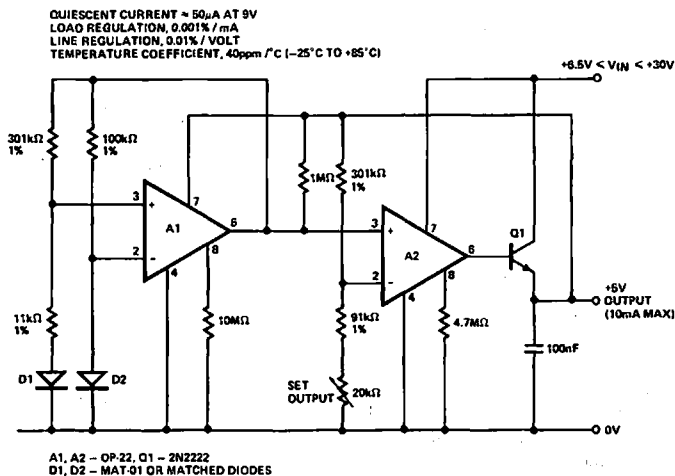


Figure 6

Figure 5 shows a micropower Wien-bridge oscillator designed for battery-powered instrumentation. Output level is controlled by nonlinear elements D1 and D2. When adjusted for 3V p-p output, the distortion level is below 0.5% at 1kHz.

The 5 volt regulator in Figure 6 is intended for instrumentation requiring good power efficiency. Low-power 3-terminal

IC regulators typically draw 2mA to 5mA quiescent current compared to only 50μA with this discrete implementation. Maximum load current is 10mA as shown, and can be increased by changing Q1 to a power transistor and proportionately increasing the set current of A2.

Precision Monolithics Inc.

FEATURES

- Low Noise $80\text{nV}_{\text{p-p}}$ (0.1Hz to 10Hz)
..... $3\text{nV}/\sqrt{\text{Hz}}$
- Low Drift $0.2\mu\text{V}/^\circ\text{C}$
- High Speed $2.8\text{V}/\mu\text{s}$ Slew Rate
..... 8MHz Gain Bandwidth
- Low V_{OS} $10\mu\text{V}$
- Excellent CMRR 126dB at V_{CM} of $\pm 11\text{V}$
- High Open-Loop Gain 1.8 Million
- Fits 725, OP-07, OP-05, AD510, AD517, 5534A sockets

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ $V_{\text{OS}} \text{ MAX}$ (μV)	PACKAGE				OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	LCC	
25	OP27AJ*	OP27AZ*	—	—	MIL
25	OP27EJ	OP27EZ	OP27EP	—	IND/COM
60	OP27BJ*	OP27BZ*	—	OP27BRC/883	MIL
60	OP27FJ	OP27FZ	OP27FP	—	IND/COM
100	OP27CJ	OP27CZ	—	—	MIL
100	OP27GJ	OP27GZ	OP27GP	—	IND/COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

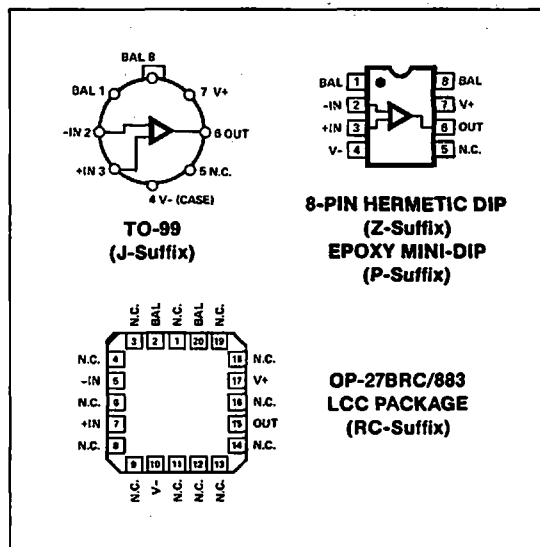
The OP-27 precision operational amplifier combines the low offset and drift of the OP-07 with both high-speed and low-noise. Offsets down to $25\mu\text{V}$ and drift of $0.6\mu\text{V}/^\circ\text{C}$ maximum make the OP-27 ideal for precision instrumentation applications. Exceptionally low noise, $e_n = 3.5\text{nV}/\sqrt{\text{Hz}}$, at 10Hz, a low 1/f noise corner frequency of 2.7Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level signals. A gain-bandwidth product of 8MHz and a $2.8\text{V}/\mu\text{sec}$ slew rate provides excellent dynamic accuracy in high-speed data-acquisition systems.

A low input bias current of $\pm 10\text{nA}$ is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to $\pm 20\text{nA}$ and 15nA respectively.

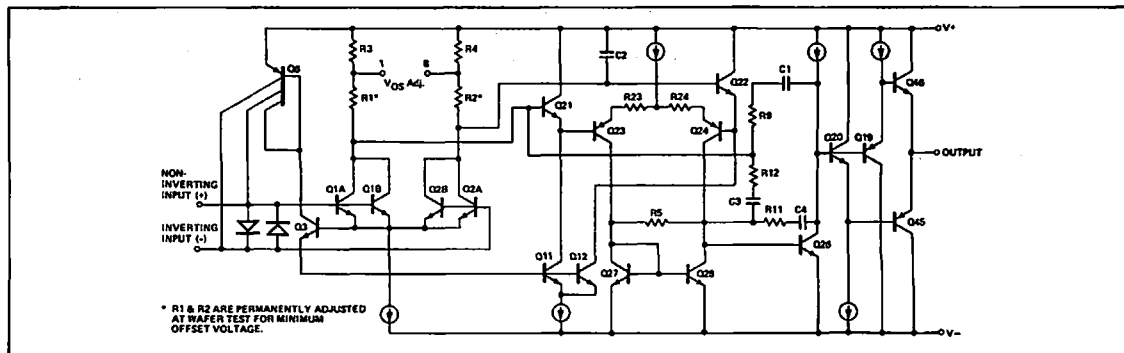
The output stage has good load driving capability. A guaranteed swing of $\pm 10\text{V}$ into 600Ω and low output distortion make the OP-27 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of $0.2\mu\text{V}/\text{month}$, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





Low cost, high-volume production of OP-27 is achieved by using an on-chip zener-zap trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-27 provides excellent performance in low-noise high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP-27 is a direct replacement for 725, OP-06, OP-07 and OP-05 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	-65°C to +150°C

Operating Temperature Range

OP-27A, OP-27B, OP-27C (J, Z, RC)	-55°C to +125°C
OP-27E, OP-27F, OP-27G (J, Z)	-25°C to +85°C
OP-27E, OP-27F, OP-27G (P)	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to +150°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C
LCC	80°C	7.8mW/°C

- The OP-27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.
- For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E			OP-27B/F			OP-27C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	$V_{OS}/Time$	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{n-p-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.08	0.25	$\mu V/p-p$
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	$nV/\sqrt{Hz}$
		$f_O = 30Hz$ (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		$f_O = 1000Hz$ (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	$f_O = 10Hz$ (Notes 3, 6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	$pA/\sqrt{Hz}$
		$f_O = 30Hz$ (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		$f_O = 1000Hz$ (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	G Ω
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	1	10	—	2	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/ μs

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-27A/E			OP-27B/F			OP-27C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Gain Bandwidth Prod.	GBW	(Note 4)	5.0	8.0	—	5.0	8.0	—	5.0	8.0	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	V_O	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	± 4.0	—	—	± 4.0	—	—	± 4.0	—	mV

NOTES:

- Input offset voltage measurements are performed ~ 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.
- Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30

days are typically $2.5\mu V$ — refer to typical performance curve.

- Sample tested.

- Guaranteed by design.

- See test circuit and frequency response curve for 0.1Hz to 10Hz tester.

- See test circuit for current noise measurement.

- Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27A			OP-27B			OP-27C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	± 20	± 60	—	± 28	± 95	—	± 35	± 150	nA
Input Voltage Range	IVR		± 10.3	± 11.5	—	± 10.3	± 11.5	—	± 10.2	± 11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.5	± 13.5	—	± 11.0	± 13.2	—	± 10.5	± 13.0	—	V

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-27J and OP-27Z, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-27P, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27E			OP-27F			OP-27G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2) (Note 3)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	± 14	± 60	—	± 18	± 95	—	± 25	± 150	nA
Input Voltage Range	IVR		± 10.5	± 11.8	—	± 10.5	± 11.8	—	± 10.5	± 11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	98	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.7	± 13.6	—	± 11.4	± 13.5	—	± 11.0	± 13.3	—	V

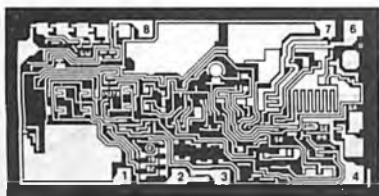
NOTES:

- Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed-up.

- The TCV_{OS} performance is within the specifications unnullled or when nullled with $R_P = 8k\Omega$ to $20k\Omega$. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.

- Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.109×0.055 inch, 5995 sq. mils
(2.77×1.40 mm, 3.88 sq. mm)

1. NULL
2. (-) INPUT
3. (+) INPUT
4. V^-
6. OUTPUT
7. V^+
8. NULL

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-27N, OP-27G, and OP-27GR devices; $T_A = 125^\circ C$ for OP-27NT and OP-27GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27NT LIMIT	OP-27N LIMIT	OP-27GT LIMIT	OP-27G LIMIT	OP-27GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I_{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I_B		± 60	± 40	± 95	± 55	± 80	nA MAX
Input Voltage Range	IVR		± 10.3	± 11	± 10.3	± 11	± 11	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = IVR$	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	10	—	10	20	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ $R_L \geq 600\Omega$, $V_O = \pm 10V$	600 —	1000 800	500 —	1000 800	700 600	V/mV MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	± 11.5 —	± 12.0 ± 10.0	± 11.0 —	± 12.0 ± 10.0	± 11.5 ± 10.0	V MIN
Power Consumption	P_d	$V_O = 0$	—	140	—	140	170	mW MAX

NOTE:

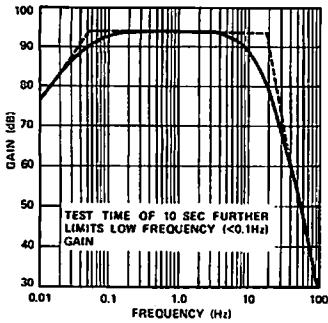
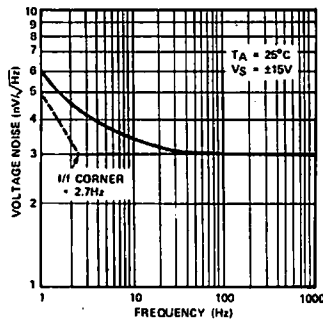
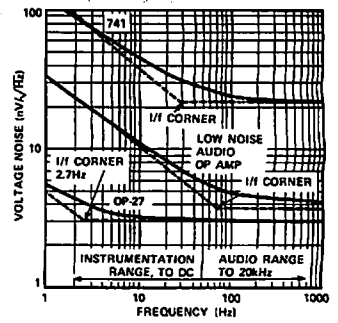
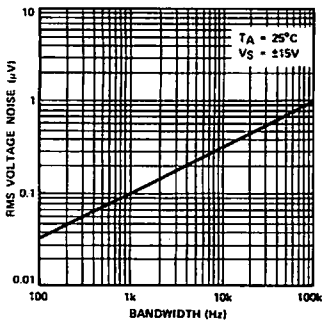
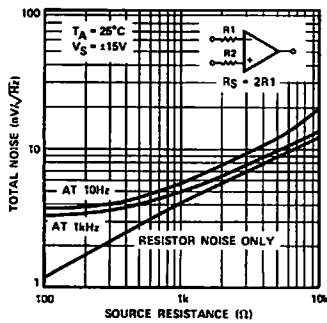
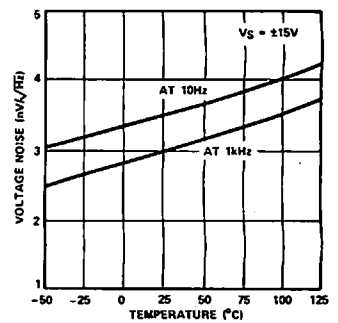
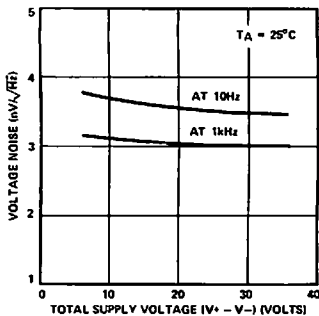
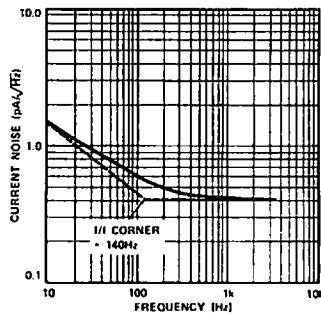
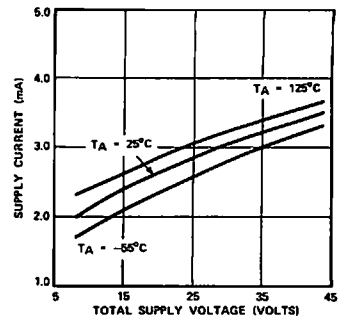
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-27N TYPICAL	OP-27G TYPICAL	OP-27GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS} or TCV_{OSn}	Nullled or Unnullled $R_P = 8k\Omega$ to $20k\Omega$	0.2	0.3	0.4	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		80	130	180	pA/°C
Average Input Bias Current Drift	TCI_B		100	160	200	pA/°C
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	3.5 3.1 3.0	3.5 3.1 3.0	3.8 3.3 3.2	nV/ $\sqrt{Hz}$
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 30Hz$ $f_O = 1000Hz$	1.7 1.0 0.4	1.7 1.0 0.4	1.7 1.0 0.4	pA/ $\sqrt{Hz}$
Input Noise Voltage	e_{n-p-p}	0.1Hz to 10Hz	0.08	0.08	0.09	μV_{p-p}
Slew Rate	SR	$R_L \geq 2k\Omega$	2.8	2.8	2.8	V/ μs
Gain Bandwidth Product	GBW		8	8	8	MHz

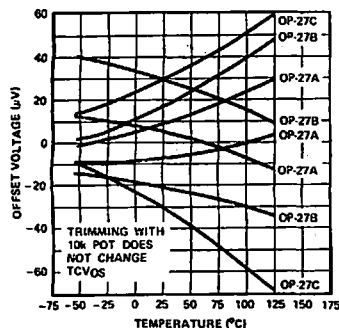
NOTE:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

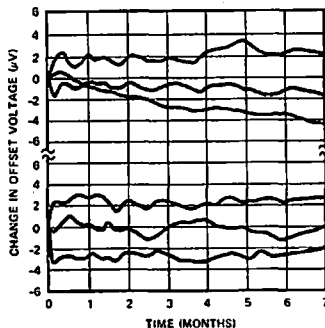
TYPICAL PERFORMANCE CHARACTERISTICS
**0.1Hz TO 10Hz_{pp} NOISE TESTER
FREQUENCY RESPONSE**

**VOLTAGE NOISE DENSITY
vs FREQUENCY**

**A COMPARISON OF
OP AMP VOLTAGE
NOISE SPECTRA**

**INPUT WIDEBAND VOLTAGE
NOISE vs BANDWIDTH (0.1Hz
TO FREQUENCY INDICATED)**

**TOTAL NOISE vs SOURCE
RESISTANCE**

**VOLTAGE NOISE DENSITY
vs TEMPERATURE**

**VOLTAGE NOISE DENSITY
vs SUPPLY VOLTAGE**

**CURRENT NOISE DENSITY
vs FREQUENCY**

**SUPPLY CURRENT vs
SUPPLY VOLTAGE**


TYPICAL PERFORMANCE CHARACTERISTICS

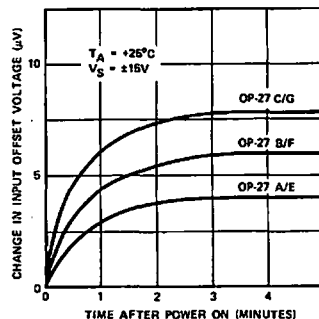
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE



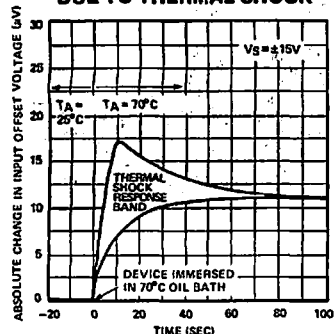
LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS



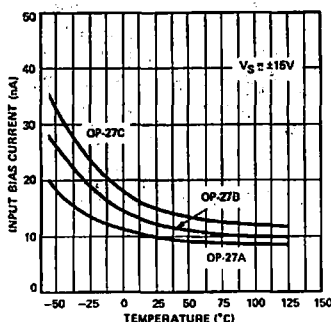
WARM-UP OFFSET VOLTAGE DRIFT



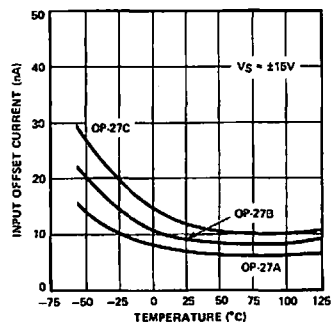
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



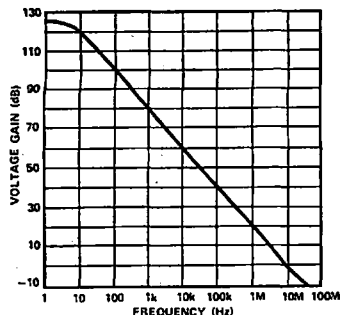
INPUT BIAS CURRENT vs TEMPERATURE



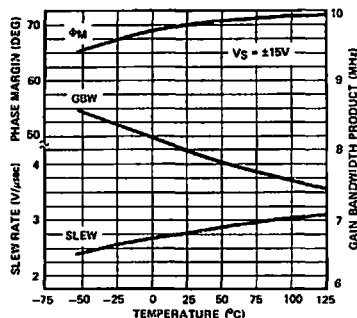
INPUT OFFSET CURRENT vs TEMPERATURE



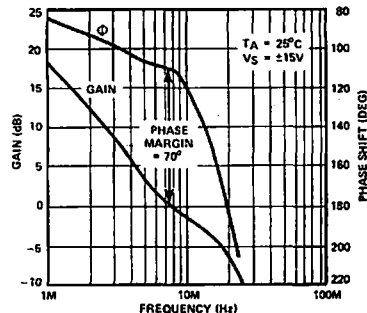
OPEN-LOOP GAIN vs FREQUENCY



SLEW RATE, GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



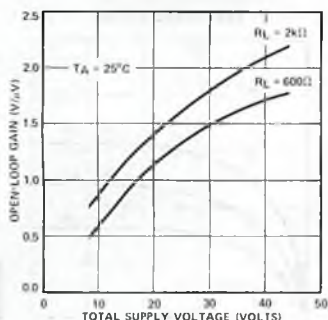
GAIN, PHASE SHIFT vs FREQUENCY



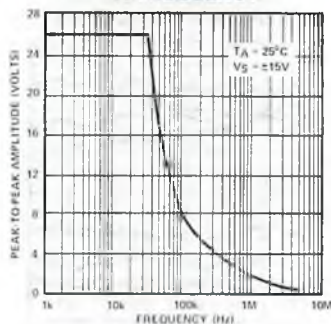
OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS

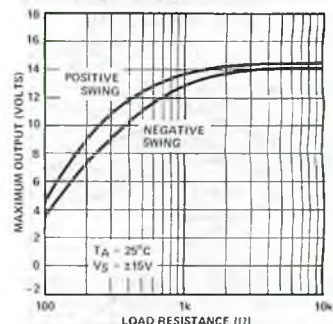
OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE



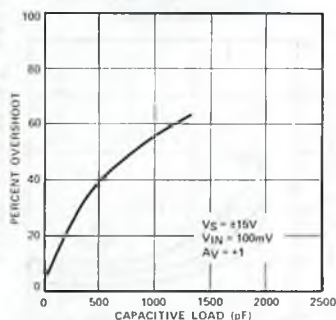
MAXIMUM OUTPUT SWING vs FREQUENCY



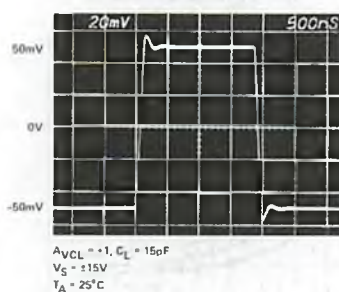
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



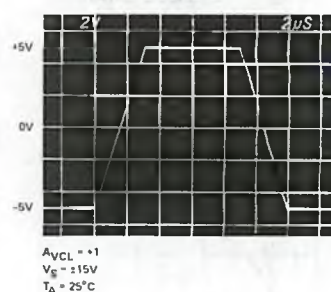
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



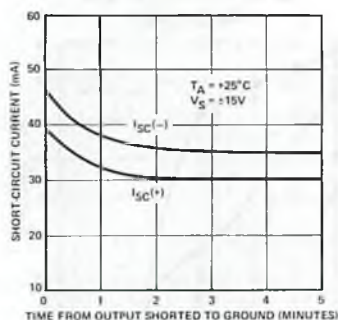
SMALL-SIGNAL TRANSIENT RESPONSE



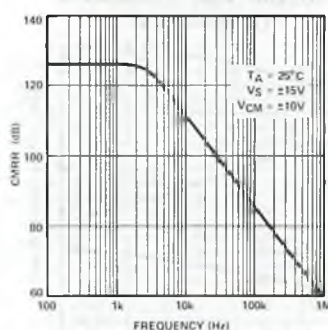
LARGE-SIGNAL TRANSIENT RESPONSE



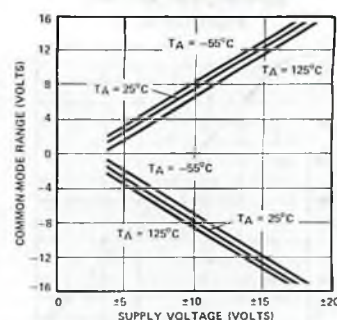
SHORT-CIRCUIT CURRENT vs TIME



CMRR vs FREQUENCY

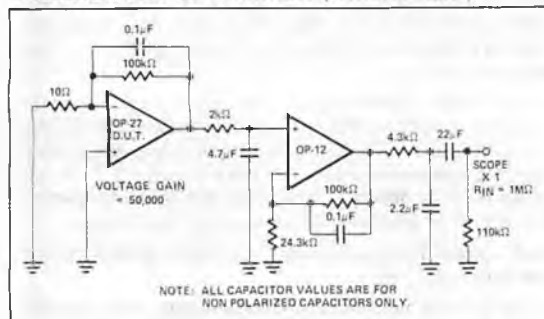


COMMON-MODE INPUT RANGE vs SUPPLY VOLTAGE

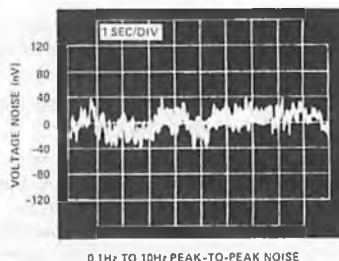


TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz)



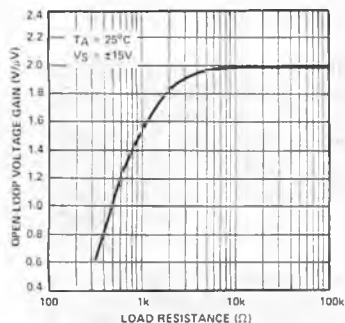
LOW-FREQUENCY NOISE



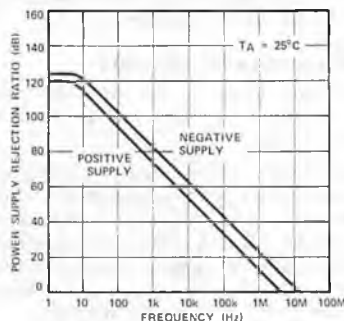
NOTE:

Observation time limited to 10 seconds.

OPEN-LOOP VOLTAGE GAIN vs LOAD RESISTANCE



PSRR vs FREQUENCY



APPLICATIONS INFORMATION

OP-27 Series units may be inserted directly into 725, OP-06, OP-07 and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-27 may be fitted to unnullled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-27 operation. OP-27 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see Offset Nulling Circuit).

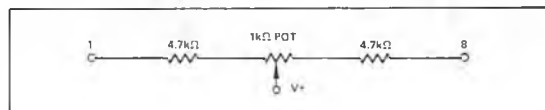
The OP-27 provides stable operation with load capacitances of up to 2000pF and $\pm 10V$ swings; larger capacitances should be decoupled with a 50 Ω resistor inside the feedback loop. The OP-27 is unity-gain stable.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-27 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10k Ω trim potentiometer may be used. TCV_{OS} is not degraded

(see Offset Nulling Circuit). Other potentiometer values from 1k Ω to 1M Ω can be used with a slight degradation (0.1 to 0.2 $\mu V/^{\circ}C$) of TCV_{OS} . Trimming to a value other than zero creates a drift of approximately $(V_{OS}/300) \mu V/^{\circ}C$. For example, the change in TCV_{OS} will be 0.33 $\mu V/^{\circ}C$ if V_{OS} is adjusted to 100 μV . The offset-voltage adjustment range with a 10k Ω potentiometer is $\pm 4mV$. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjunction with fixed resistors. For example, the network below will have a $\pm 280\mu V$ adjustment range.



NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-27 in the 0.1Hz to 10Hz range, the following precautions must be observed:

- (1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage

typically changes $4\mu\text{V}$ due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.

- (2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.
- (3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
- (4) The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.
- (5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the $1/f$ corner frequency.

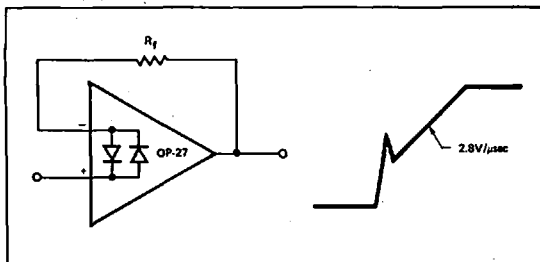
UNITY-GAIN BUFFER APPLICATIONS

When $R_I \leq 100\Omega$ and the input is driven with a fast, large signal pulse ($>1\text{V}$), the output waveform will look as shown in the pulsed operation diagram below.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_I \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20\text{mA}$ at 10V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_I > 2\text{k}\Omega$, a pole will be created with R_I and the amplifier's input capacitance (8pF) that creates additional phase shift and reduces phase margin. A small capacitor (20 to 50pF) in parallel with R_I will eliminate this problem.

PULSED OPERATION



COMMENTS ON NOISE

The OP-27 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-27 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-

bias-current cancellation circuit. The OP-27A/E has I_B and I_{OS} of only $\pm 40\text{nA}$ and 35nA respectively at 25°C . This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers prefer to use direct coupling. The high I_B , V_{OS} , TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-27's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-27 observed total noise with the noise performance of other devices in different circuit applications.

$$\text{Total noise} = \{(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise})^2\}^{1/2}$$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

NOISE vs SOURCE RESISTANCE
(INCLUDING RESISTOR NOISE)
AT 1000Hz.

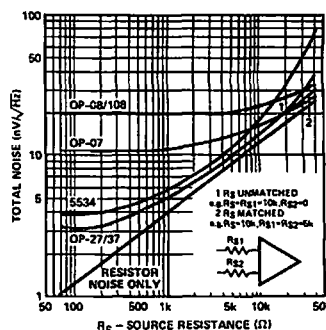


Figure 1

At $R_S < 1\text{k}\Omega$, the OP-27's low voltage noise is maintained. With $R_S > 1\text{k}\Omega$, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of $20\text{k}\Omega$ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-27 and OP-07 and OP-08 noise occurs in the 15-to-40k Ω region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to-5k Ω range depending on whether balanced or unbalanced source resistors are used (at $3\text{k}\Omega$ the I_B , I_{OS} error also can be three times the V_{OS} spec.).

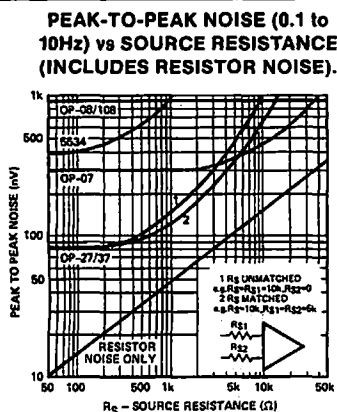


Figure 2

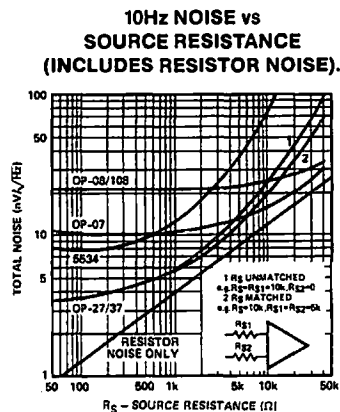


Figure 3

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when $R_S > 3k\Omega$. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-27 I_B can be neglected.
Magnetic phonograph cartridges	<1500Ω	Similar need for low I_B in direct coupled applications. OP-27 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

OPEN-LOOP GAIN

FREQUENCY AT:	OP-07	OP-27	OP-37
3Hz	100dB	124dB	125dB
10Hz	100dB	120dB	125dB
30Hz	90dB	110dB	124dB

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A_1 ; R_1 - R_2 - C_1 - C_2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.¹

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.⁴ (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values.)

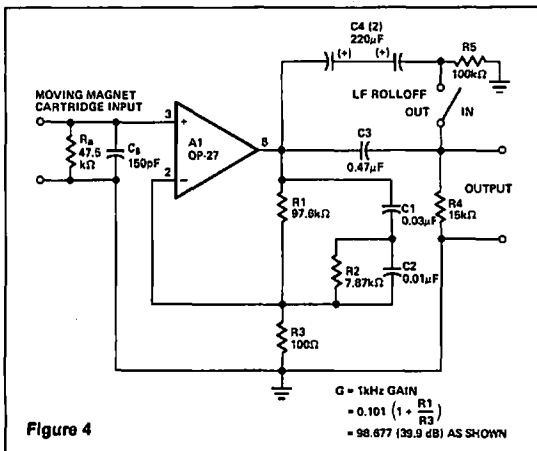


Figure 4

The OP-27 brings a $3.2\text{nV}/\sqrt{\text{Hz}}$ voltage noise and $0.45\text{pA}/\sqrt{\text{Hz}}$ current noise to this circuit. To minimize noise from other sources, R_3 is set to a value of 100Ω , which generates a voltage noise of $1.3\text{nV}/\sqrt{\text{Hz}}$. The noise increases the $3.2\text{nV}/\sqrt{\text{Hz}}$ of the amplifier by only 0.7dB . With a $1\text{k}\Omega$ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

Gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101 \left(1 + \frac{R_1}{R_3} \right)$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R_3 , but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms . At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz .

Capacitor C_3 and resistor R_4 form a simple -6dB-per-octave rumble filter, with a corner at 22Hz . As an option, the switch-selected shunt capacitor C_4 , a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

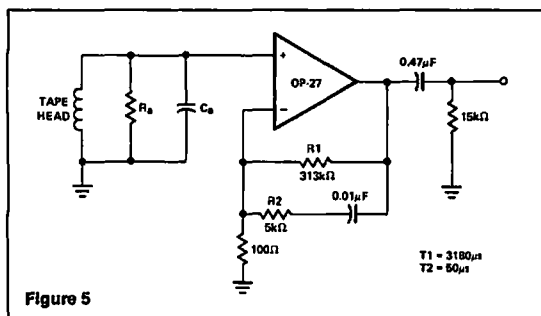


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz ($T_2 = 50\mu\text{s}$), the amplifier need not be stabilized for unity gain. The decompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R_1 and R_2 to optimize frequency response for nonideal tape-head performance and other factors.⁵

The network values of the configuration yield a 50dB gain at 1kHz , and the dc gain is greater than 70dB . Thus, the worst-case output offset is just over 500mV . A single $0.47\mu\text{F}$ output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 80nA with a 400mH , $100\mu\text{in.}$ head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below $1\text{k}\Omega$. For this configuration, the bias-current-induced offset voltage can be greater than the $100\mu\text{V}$ maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB , and has an input impedance of $2\text{k}\Omega$. Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz . As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p , may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a $4\text{nV}/\sqrt{\text{Hz}}$ noise, while the op amp generates a $3.2\text{nV}/\sqrt{\text{Hz}}$ noise. The rms sum of these predominant noise sources will be about $6\text{nV}/\sqrt{\text{Hz}}$, equivalent to $0.9\mu\text{V}$ in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

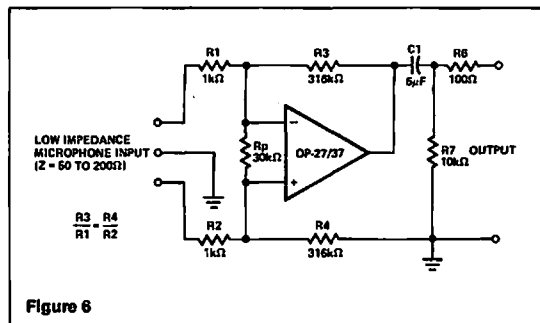


Figure 6

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally-compensated OP-27. T_1 is a JE-115K-E 150 Ω /15k Ω transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.

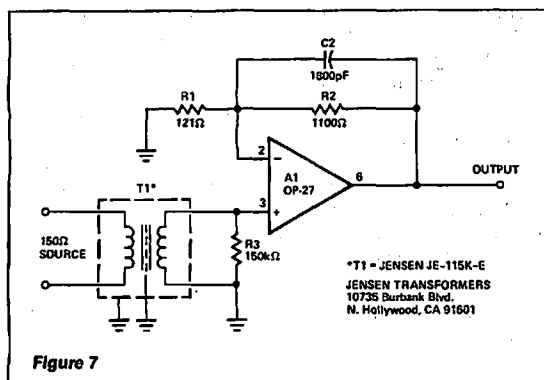


Figure 7

Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1 . Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a 40dB gain. The typical output blocking capacitor can be

eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

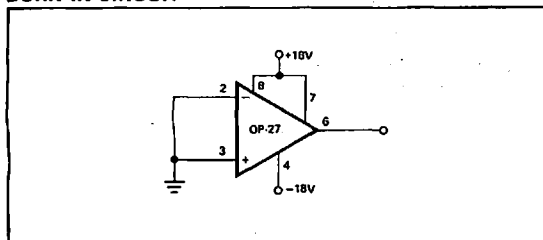
Capacitor C_2 and resistor R_2 form a 2 μ s time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2 μ s time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150 Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or -69.5 referenced to 1mV).

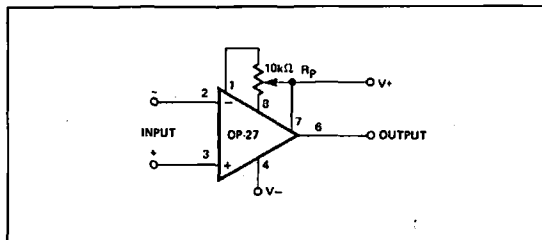
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1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.

BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT





OP-32

HIGH-SPEED ($A_{VCL} \geq 10$) PROGRAMMABLE MICROPOWER OPERATIONAL AMPLIFIER (SINGLE OR DUAL SUPPLY)

Precision Monolithics Inc.

FEATURES

- Programmable Supply Current $1\mu A$ to $2mA$
- Single Supply Operation $+3V$ to $+30V$
- Dual Supply Operation $\pm 1.5V$ to $\pm 15V$
- Low Input Offset Voltage $100\mu V$
- Low Input Offset Voltage Drift $0.5\mu V/^\circ C$
- High Common-Mode Input Range ... V^- to $V^+ (-1.5V)$
- High CMRR and PSRR $115dB$
- High Open-Loop Gain $2000V/mV$
- $\pm 30V$ Input Overvoltage Protection
- Fast $1V/\mu s$ @ $I_{SY} = 300\mu A$
- LM4250 Pinout
- Compensated for Minimum Gain of 10

ORDERING INFORMATION†

$T_A = 25^\circ C$ $V_{OS} \text{ MAX}$ (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	PLASTIC	CERDIP	LCC	
300	—	OP32AZ*	—	MIL
300	OP32EP	OP32EZ	—	IND
500	—	OP32BZ*	OP32BRC/883	MIL
500	OP32FP	OP32FZ	—	IND
1000	OP32GP	OP32GZ	—	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-32 is a high-speed, high-gain programmable operational amplifier. Both offset voltage and offset current are low, and both are stable with changes in temperature, supply voltage, and set current. High CMRR and PSRR ensure

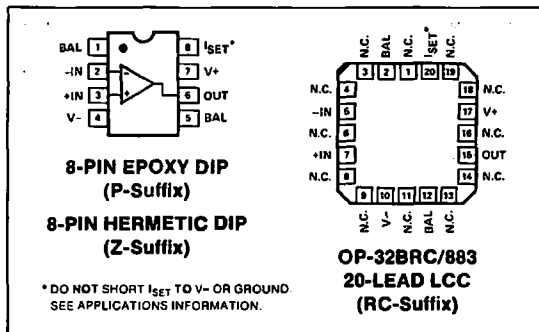
precision performance when the OP-32 is used with an unregulated battery or vehicular electrical system.

The wide input voltage range, including the negative supply or ground, allows use in single-battery applications. The OP-32 is characterized over a wide supply range of $\pm 1.5V$ to $\pm 15V$. This guarantees predictable performance with any commonly available supply.

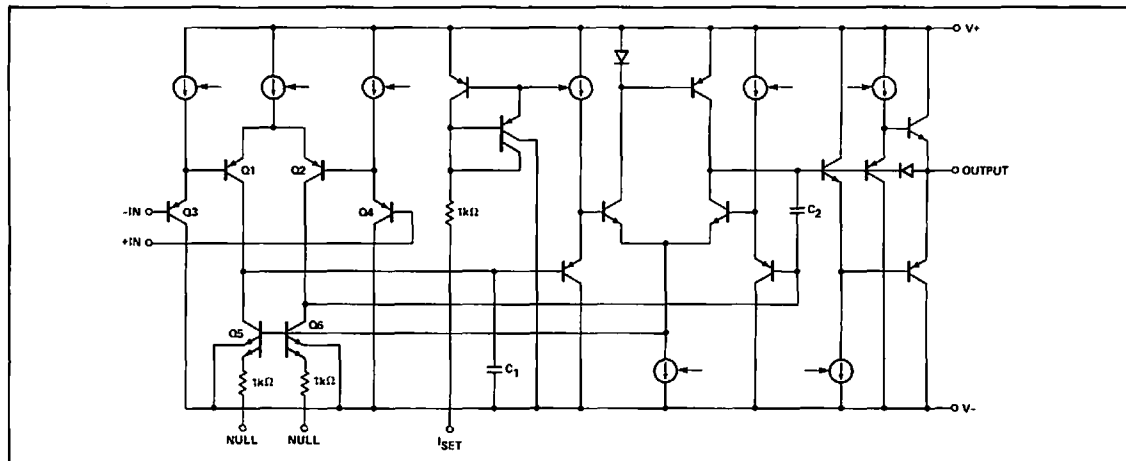
The ability to operate at relatively high speed with low power consumption makes this amplifier ideal for remote applications where power is limited. The programmability allows each amplifier in a system to be set for the minimum power consumption necessary for each specific application. Programmability also makes it possible to adjust the bandwidth and phase shift.

The OP-32 pinout is identical to the LM4250 and many other micropower operational amplifiers. This allows easy upgrading of system performance.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage	±18V
Power Dissipation	500mW
Differential Input Voltage	±30
Input Voltage	Supply Voltage
Storage Temperature Range	
Z Package	-65°C to +150°C
P Package	-55°C to +125°C

Operating Temperature Range

OP-32A, B (Z or RC package)	-55°C to +125°C
OP-32E, F & G (Z or P package)	-25°C to +85°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to +150°C

NOTE:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32A/E			OP-32B/F			OP-32G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	100	300	—	200	500	—	400	1000	μV
Input Offset current	I_{OS}	$V_{CM} = 0$	—	—	2	—	—	2	—	—	3	nA
Input Bias Current (Note 1)	I_B	$I_{SY} = 15\mu A$	—	3	5	—	5	7.5	—	5	10	nA
		$I_{SY} = 150\mu A$	—	20	35	—	24	35	—	30	50	
		$I_{SY} = 450\mu A$	—	60	90	—	70	100	—	80	125	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15.0/13.5	—	—	-15.0/13.5	—	—	-15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 2)	CMRR	$V_S = \pm 15V$ $-15V \leq V_{CM} \leq +13.5V$	100	115	—	95	110	—	85	100	—	dB
Power Supply Rejection Ratio (Note 2)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$; and $V_- = 0V$, $V_+ = 3V$ to $30V$.	—	1	6	—	3	12	—	10	25	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	1000	2000	—	750	1500	—	500	1000	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	$\pm 0.8 \pm 0.88$			$\pm 0.8 \pm 0.88$			$\pm 0.75 \pm 0.85$			V
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$ $R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	$\pm 14 \pm 14.2$			$\pm 14 \pm 14.2$			$\pm 13.8 \pm 14.2$			V
Gain-Bandwidth Product		$I_{SY} = 15\mu A$, $R_L = 100k\Omega$	—	100	—	—	100	—	—	100	—	kHz
		$I_{SY} = 450\mu A$, $R_L = 10k\Omega$	—	4500	—	—	4500	—	—	4500	—	
Slew Rate	SR	$V_S = \pm 15V$, $I_{SY} = 450\mu A$, $R_L = 10k\Omega$	—	1.5	—	—	1.5	—	—	1.5	—	V/ μs
Supply Current No Load (Note 3)	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	15	17	—	15	19	—	15	21	μA
		$I_{SET} = 10\mu A$	—	150	170	—	150	190	—	150	200	
		$I_{SET} = 30\mu A$	—	450	525	—	450	600	—	450	650	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	10.5	12.5	—	11	15	—	11	18	μA
		$I_{SET} = 10\mu A$	—	105	125	—	110	150	—	110	180	
		$I_{SET} = 30\mu A$	—	350	400	—	350	450	—	350	500	

NOTES:

- I_B and I_{OS} are measured at $V_{CM} = 0$.
- PSRR and CMRR measured with V_{OS} unnullified and I_{SET} held constant.
- The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} = 10 + \frac{(V_+) - (V_-)}{6}$$

The range of I_{SY}/I_{SET} is approximately 10.5 to 15 over the specified operating range of $V_S = \pm 1.5V$ to $V_S = \pm 15V$.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

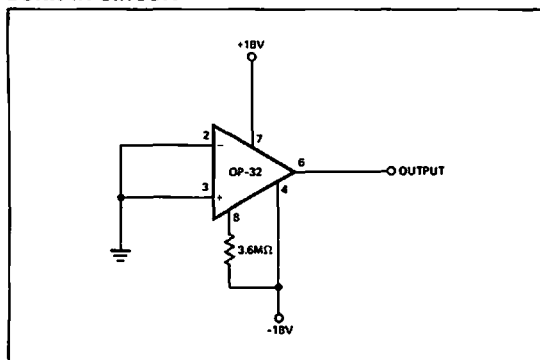
PARAMETER	SYMBOL	CONDITIONS	OP-32A			OP-32B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnull'd	—	0.5	2.0	—	1.0	2.0	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	175	400	—	350	600	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	—	2	—	—	2	nA
Average Input Offset Current Drift	TCI_{OS}	(Notes 1, 2)	—	1	10	—	3	15	$pA/^\circ C$
Input Bias Current (Note 2)	I_B	$I_{SY} = 15\mu A$	—	3	5	—	5	7.5	nA
		$I_{SY} = 150\mu A$	—	20	35	—	25	35	
		$I_{SY} = 450\mu A$	—	60	90	—	70	100	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15.0/13.5	—	—	-15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 3)	CMRR	$V_S = \pm 15V$							dB
		$-15V \leq V_{CM} \leq +13.5V$							
		$I_{SET} = 10\mu A$	90	110	—	86	105	—	
		$I_{SET} = 1\mu A$	80	90	—	80	90	—	
Power Supply Rejection Ratio (Note 3)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V_- = 0V$, $V_+ = 3V$ to $30V$ ($V_{CM} = 1.5V$)	—	2	10	—	2.5	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	200	400	—	200	500	—	V/mV
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	500	1000	—	300	750	—	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 0.65	± 0.75	—	± 0.65	± 0.75	—	V
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$							
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 13.8	± 14.0	—	± 13.0	± 13.5	—	V
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$							
Supply Current No Load (Note 4)	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	16	18	—	16	20	μA
		$I_{SET} = 10\mu A$	—	180	180	—	160	200	
		$I_{SET} = 30\mu A$	—	450	550	—	450	600	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	12	14	—	12	17	μA
		$I_{SET} = 10\mu A$	—	120	140	—	120	170	
		$I_{SET} = 30\mu A$	—	360	450	—	360	500	

NOTES:

- Sample tested.
- I_B and I_{OS} are measured at $V_{CM} = 0$.
- PSRR and CMRR measured with V_{OS} unnull'd and I_{SET} held constant.

- The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} = 10 + \frac{(V_+) - (V_-)}{6}$$

BURN-IN CIRCUIT*

*Other circuits may apply at PMI's discretion.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $15\mu A \leq I_{SY} \leq 450\mu A$, $-25^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32E			OP-32F			OP-32G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnulled	—	0.5	1.5	—	1.0	2.0	—	1.5	3.0	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	100	400	—	200	800	—	500	1200	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	—	2	—	—	2	—	—	3	nA
Average Input Offset Current Drift	TCI_{OS}	(Notes 1, 2)	—	2	10	—	3	15	—	5	25	$pA/^\circ C$
Input Bias Current (Note 2)	I_B	$I_{SY} = 15\mu A$	—	3	5	—	5	7.5	—	5	10	nA
		$I_{SY} = 150\mu A$	—	20	35	—	24	35	—	30	50	
		$I_{SY} = 450\mu A$	—	60	90	—	70	100	—	80	125	
Input Voltage Range	IVR	$V_S = \pm 15V$	-15.0/13.5	—	—	-15.0/13.5	—	—	-15.0/13.5	—	—	V
Common-Mode Rejection Ratio (Note 3)	CMRR	$V_S = \pm 15V$ & $-15V \leq V_{CM} \leq +13.5V$	95	110	—	90	105	—	80	100	—	dB
Power Supply Rejection Ratio (Note 3)	PSRR	$V_S = \pm 1.5V$ to $\pm 15V$ & $V_- = 0V$, $V_+ = 3V$ to $30V$	—	3.2	10	—	10	32	—	32	56	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	750	1000	—	500	1000	—	400	1000	—	V/mV
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$	750	1000	—	500	1000	—	400	1000	—	
Output Voltage Swing	V_O	$V_S = \pm 1.5V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 0.70	± 0.75	—	± 0.65	± 0.75	—	± 0.6	± 0.7	—	V
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$										
		$V_S = \pm 15V$ $R_L = 100k\Omega$, $I_{SY} = 15\mu A$	± 13.8	± 14.1	—	± 13.6	± 14.1	—	± 13.0	± 14.0	—	V
		$R_L = 10k\Omega$, $150\mu A \leq I_{SY} \leq 450\mu A$										
Supply Current No Load (Note 4)	I_{SY}	$V_S = \pm 15V$, $I_{SET} = 1\mu A$	—	18	18	—	18	20	—	16	25	μA
		$I_{SET} = 10\mu A$	—	180	180	—	180	200	—	180	250	
		$I_{SET} = 30\mu A$	—	450	550	—	450	600	—	450	650	
		$V_S = \pm 1.5V$, $I_{SET} = 1\mu A$	—	12	14	—	12	17	—	12	25	μA
		$I_{SET} = 10\mu A$	—	120	140	—	120	170	—	120	200	
		$I_{SET} = 30\mu A$	—	380	450	—	360	500	—	360	550	

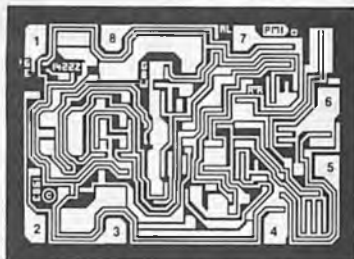
NOTES:

- Sample tested.
- I_B and I_{OS} are measured at $V_{CM} = 0$.
- PSRR and CMRR measured with V_{OS} unnulled and I_{SET} held constant.
- The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V_+) - (V_-)}{6}$$



DICE CHARACTERISTICS

DIE SIZE 0.070 × 0.050 inch, 3500 sq. mils
(1.78 × 1.27 mm, 2.26 sq. mm)

1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
5. BALANCE
6. OUTPUT
7. V₊
8. I_{SET}

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at V_S = ±1.5V to ±15V, 15μA ≤ I_{SY} ≤ 450μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-32N LIMIT	OP-32G LIMIT	OP-32GR LIMIT	UNITS
Input Offset Voltage	V _{OS}		300	500	1000	μV MAX
Input Offset Current	I _{OS}	V _{CM} = 0	2	2	3	nA MAX
Input Bias Current (Note 1)	I _B	I _{SY} = 15μA	5	7.5	10	nA MAX
		I _{SY} = 150μA	35	35	50	
		I _{SY} = 450μA	90	100	125	
Input Voltage Range	IVR	V _S = ±15V	-15/13.5	-15/13.5	-15/13.5	V MIN
Common-Mode Rejection Ratio (Note 2)	CMRR	V _S = ±15V -15V ≤ V _{CM} ≤ +13.5V	100	95	85	dB MIN
Power Supply Rejection Ratio (Note 2)	PSRR	V _S = ±1.5V to ±15V & V ₋ = 0V, V ₊ = 3V to 30V	6	12	25	μV/V MAX
Large-Signal Voltage Gain	A _{VO}	V _S = ±15V, R _L = 100kΩ, I _{SY} = 15μA	1000	750	500	V/mV MIN
		R _L = 10kΩ, 150μA ≤ I _{SY} ≤ 450μA	1000	750	500	
Output Voltage Swing	V _O	V _S = ±1.5V, R _L = 100kΩ, I _{SY} = 15μA	±0.8	±0.8	±0.75	V MIN
		R _L = 10kΩ, 150μA ≤ I _{SY} ≤ 450μA				
		V _S = ±15V, R _L = 100kΩ, I _{SY} = 15μA	±14	±14	±13.8	V MIN
Supply Current No Load (Note 3)	I _{SY}	R _L = 10kΩ, 150μA ≤ I _{SY} ≤ 450μA				
		V _S = ±1.5V, I _{SET} = 1μA	12.5	15	18	μA MAX
		I _{SET} = 10μA	125	150	180	
		I _{SET} = 30μA	400	450	500	
		V _S = ±15V, I _{SET} = 1μA	17	19	21	μA MAX
		I _{SET} = 10μA	170	190	200	
		I _{SET} = 30μA	525	600	650	

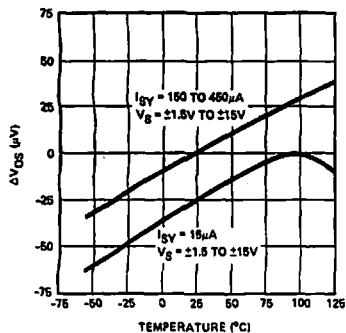
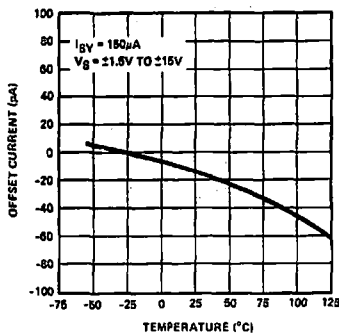
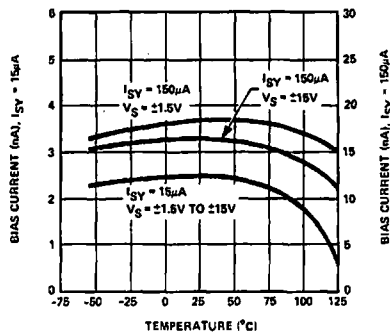
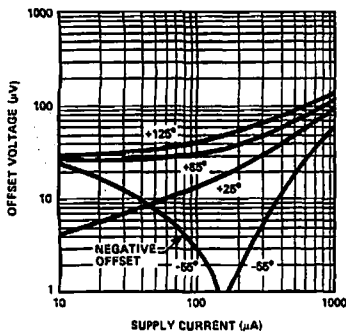
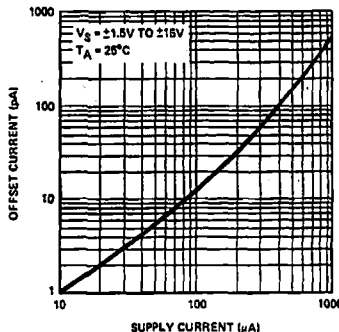
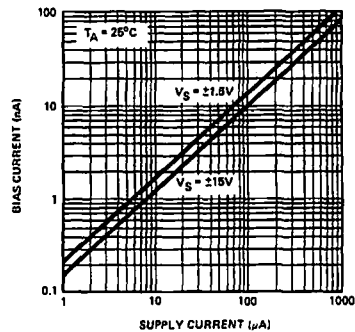
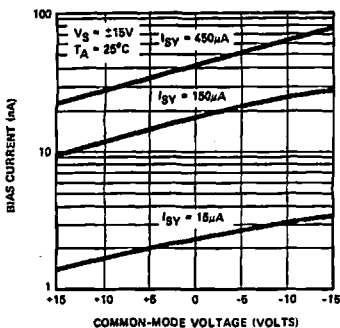
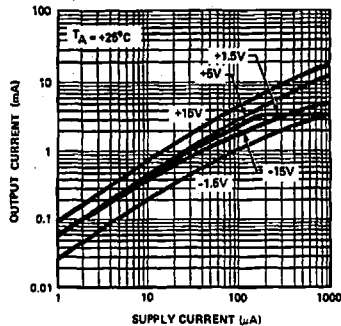
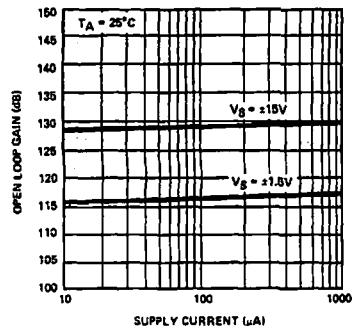
NOTES:

1. I_B and I_{OS} are measured at V_{CM} = 0.
2. PSRR and CMRR measured with V_{OS} unnull and I_{SET} held constant.
3. The supply current (I_{SY}) is dependent on the set current (I_{SET}) and supply voltage as follows:

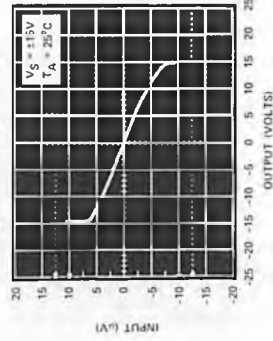
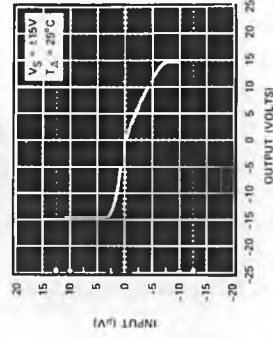
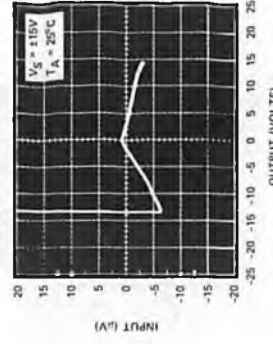
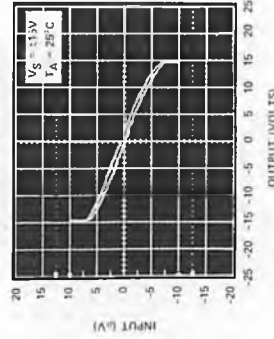
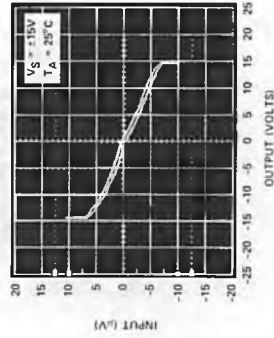
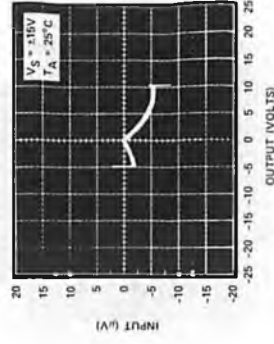
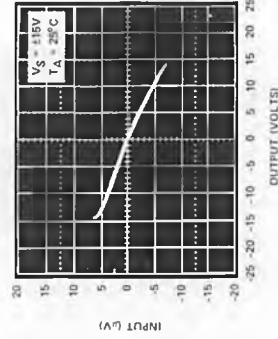
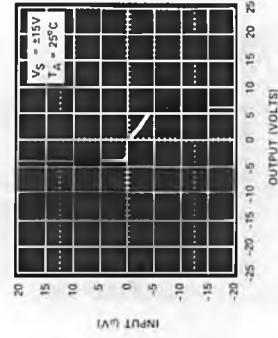
$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{I(V+) - (V-)}{6}$$

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

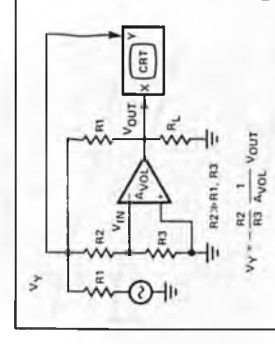
TYPICAL DC PERFORMANCE CHARACTERISTICS

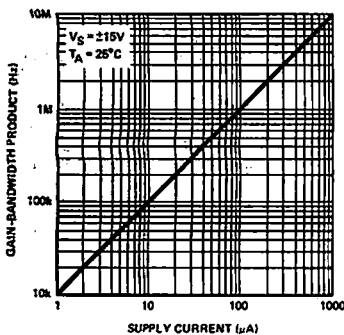
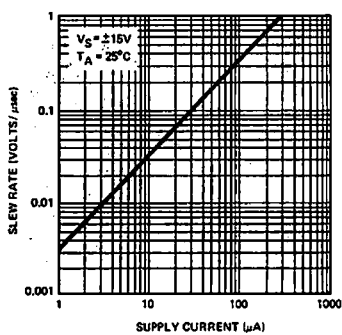
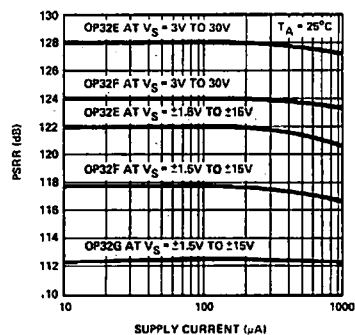
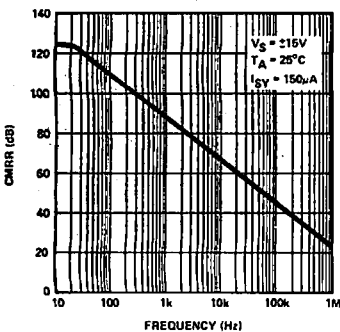
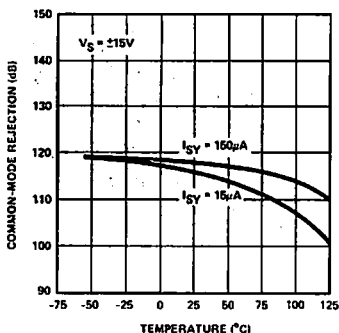
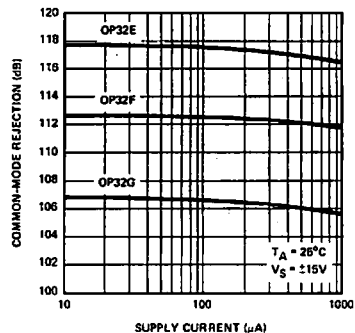
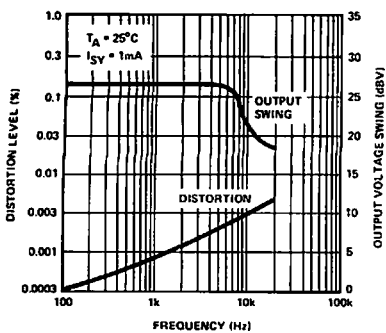
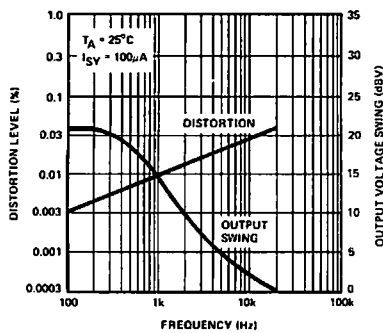
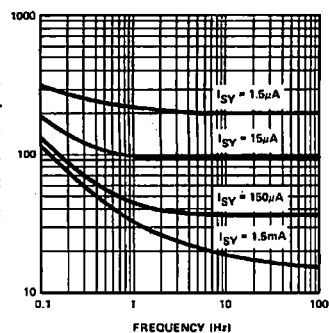
 OFFSET VOLTAGE
vs TEMPERATURE

 OFFSET CURRENT
vs TEMPERATURE

 BIAS CURRENT
vs TEMPERATURE

 OFFSET VOLTAGE
vs SUPPLY CURRENT

 OFFSET CURRENT
vs SUPPLY CURRENT

 BIAS CURRENT
vs SUPPLY CURRENT

 BIAS CURRENT vs
COMMON-MODE VOLTAGE

 MAXIMUM OUTPUT CURRENT
vs SUPPLY CURRENT AT
V_G = ±15V, +5V AND ±1.5V

 OPEN-LOOP GAIN
vs SUPPLY CURRENT


TYPICAL DC OPEN-LOOP INPUT-OUTPUT CHARACTERISTICS

 $I_{SY} = 1\text{mA}$, $R_L = 100\text{k}\Omega$  $I_{SY} = 1\text{mA}$, $R_L = 10\text{k}\Omega$  $I_{SY} = 1\text{mA}$, $R_L = 2\text{k}\Omega$  $I_{SY} = 100\mu\text{A}$, $R_L = 100\text{k}\Omega$  $I_{SY} = 100\mu\text{A}$, $R_L = 10\text{k}\Omega$  $I_{SY} = 100\mu\text{A}$, $R_L = 2\text{k}\Omega$  $I_{SY} = 10\mu\text{A}$, $R_L = 100\text{k}\Omega$  $I_{SY} = 10\mu\text{A}$, $R_L = 10\text{k}\Omega$ 

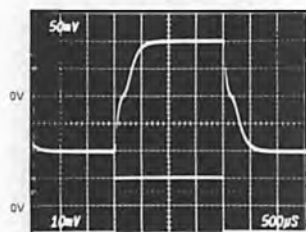
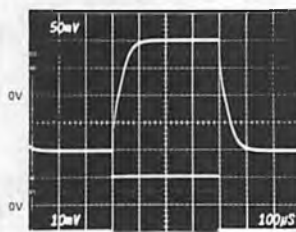
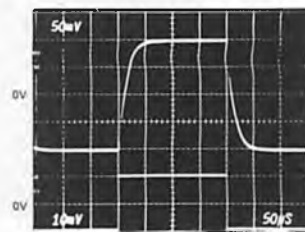
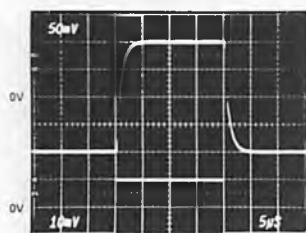
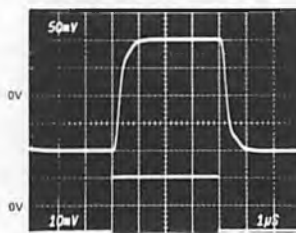
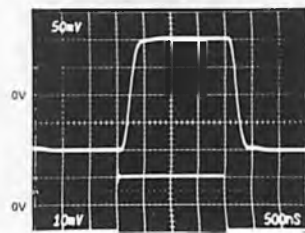
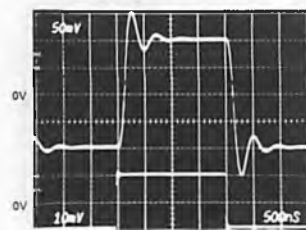
TEST CIRCUIT



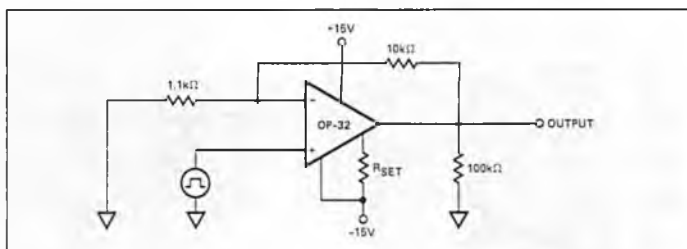
TYPICAL AC PERFORMANCE CHARACTERISTICS
**GAIN-BANDWIDTH PRODUCT
vs SUPPLY CURRENT**

**SLEW RATE vs
SUPPLY CURRENT**

**POWER SUPPLY REJECTION
vs SUPPLY CURRENT**

**COMMON-MODE REJECTION
vs FREQUENCY**

**COMMON-MODE REJECTION
vs TEMPERATURE**

**COMMON-MODE REJECTION
vs SUPPLY CURRENT**

**TOTAL HARMONIC
DISTORTION vs FREQUENCY**

**TOTAL HARMONIC
DISTORTION vs FREQUENCY**

**VOLTAGE NOISE
vs FREQUENCY**


TYPICAL AC PERFORMANCE CHARACTERISTICS

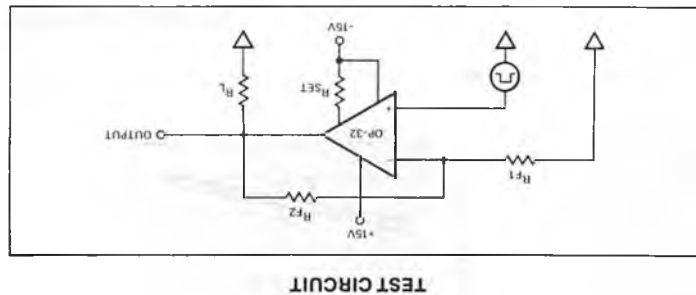
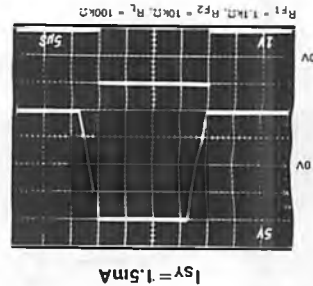
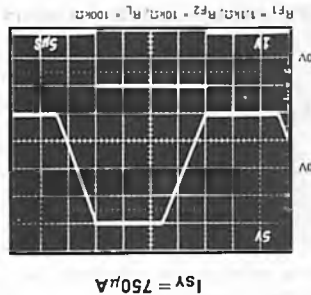
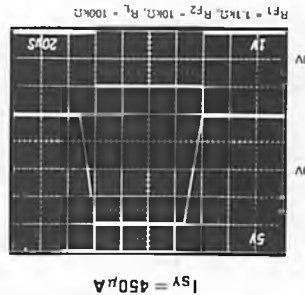
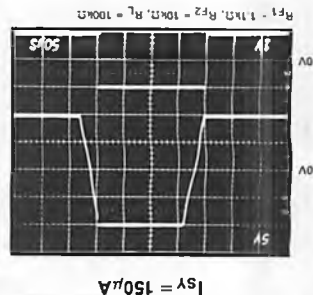
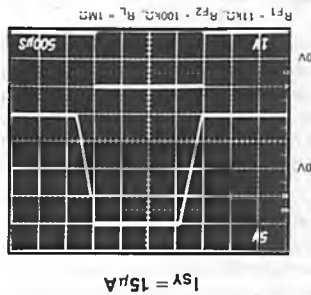
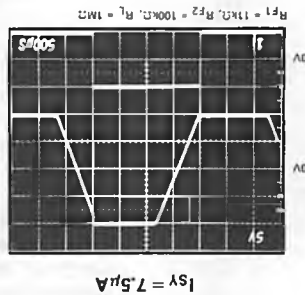
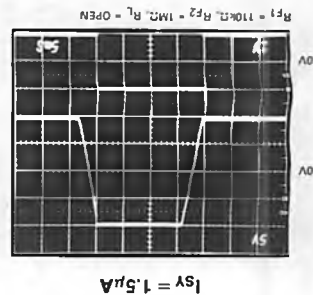
SMALL-SIGNAL TRANSIENT RESPONSE vs SUPPLY CURRENT

 $I_{SY} = 1.5\mu A$  $I_{SY} = 7.5\mu A$  $I_{SY} = 15\mu A$  $I_{SY} = 150\mu A$  $I_{SY} = 450\mu A$  $I_{SY} = 750\mu A$  $I_{SY} = 1.5mA$ 

TEST CIRCUIT



TYPICAL AC PERFORMANCE CHARACTERISTICS
LARGE-SIGNAL TRANSIENT RESPONSE VS SUPPLY CURRENT



APPLICATIONS INFORMATION

SETTING SUPPLY CURRENT

The op amp power supply current is determined by the current flowing out of pin 8. Pin 8 is at the $V+$ voltage less two diode drops, which is approximately $V+$ minus 1.1V. Do not connect pin 8 to ground or $V-$ without a set resistor in series or excessive supply current will be drawn which may damage the OP-32.

The set resistor value is selected to make the power supply current optimum for the specific application. Adjusting the OP-32 power supply current determines the slew-rate, bandwidth, and the output current limits (see Performance Characteristics). The supply current is nominally 15 times the set current and the set resistor value is calculated from:

$$R_S = \frac{(V_{SUPPLY} - 1.1V)}{I_{SET}}, \text{ where } I_{SY} \approx 15 I_{SET} \quad (\text{See graph below})$$

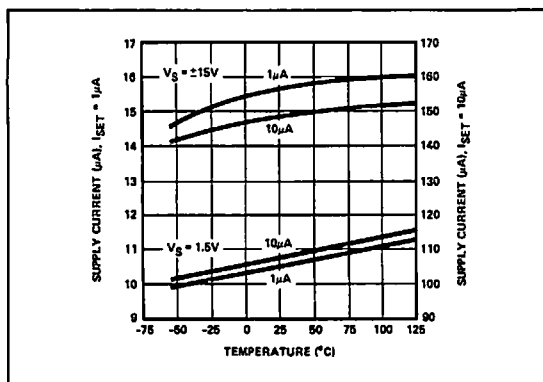
Note that the set resistor can go to either negative supply or to ground. If the set resistor goes to negative supply, then $V_{SUPPLY} = (V+) - (V-)$. For a single-supply circuit, V_{SUPPLY} is simply $(V+)$. If the supply voltage varies widely, set current can be stabilized with circuits (a), (b), or (c).

The relationship between supply voltage, supply current and set current can be approximated by:

$$\frac{I_{SY}}{I_{SET}} \approx 10 + \frac{(V+) - (V-)}{6} \quad (T_A = 25^\circ C)$$

The ratio $\frac{I_{SY}}{I_{SET}}$ increases with temperature by approximately 0.05%/°C.

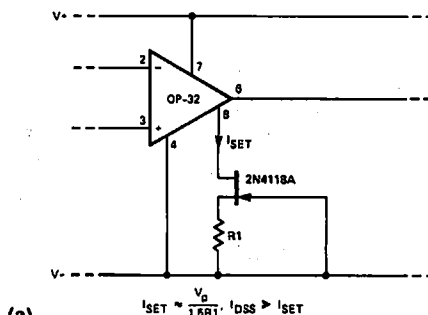
SUPPLY CURRENT vs TEMPERATURE



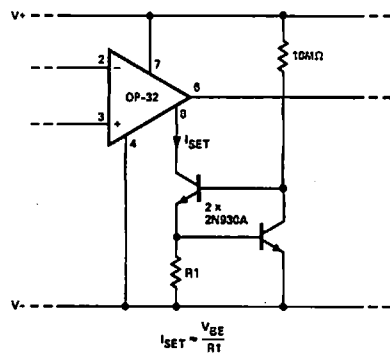
INPUT BIAS CURRENT

Input bias current varies directly with set current. The set current required for a given supply current ranges from $I_{SY}/10.5$ at $\pm 1.5V$ supply voltage to $I_{SY}/15$ at $\pm 15V$. Therefore, I_B will be highest at the minimum supply voltage condition of $\pm 1.5V$ (or 3V) for any given supply current.

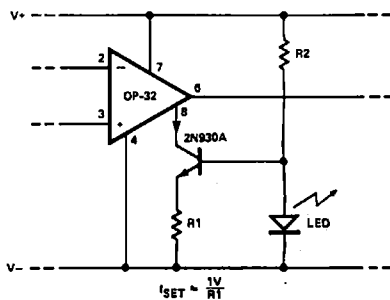
CURRENT SETTING CIRCUITS



(a)

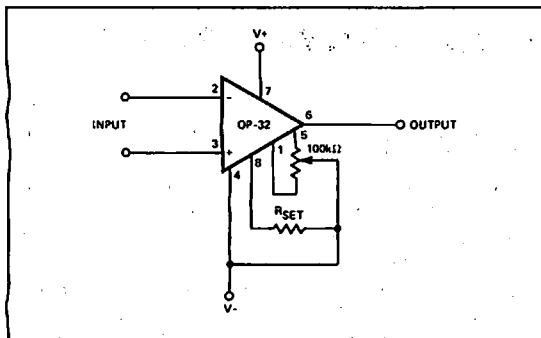


(b)



(c)

OFFSET NULLING CIRCUIT



OFFSET VOLTAGE ADJUSTMENT

The offset voltage can be trimmed to zero using a 100kΩ potentiometer (see offset nulling circuit). Adjusting the pot wiper towards pin 5 causes the output to go positive. Adjustment range is approximately $\pm 5\text{mV}$ at $V_S = \pm 15\text{V}$. The V_{OS} adjust range is proportional to supply voltage. Resolution of the nulling can be increased by using a smaller pot in conjunction with fixed resistors.

If power supply voltages vary widely and the set current is established by a resistor, the op amp supply currents will vary in proportion to the supply voltage changes. V_{OS} will remain almost constant with supply current changes if the null pins (1 and 5) are not used. If a V_{OS} adjust pot is used, current variations may flow through the offset pot causing an apparent V_{OS} change. If a V_{OS} adjust pot is used in combination with widely-varying supply voltages, a set-current stabilizer circuit as shown in (a), (b), or (c) is recommended.

APPLICATIONS EXAMPLE

BATTERY-POWERED, GAIN-OF-100 AMPLIFIER

The simple noninverting amplifier circuit shown in Figure 1 provides an accurate gain-of-100 while operating from a pair of 9V batteries. The circuit requires only 15μA of supply current. Slew-rate is approximately 0.06V/μsec and output swing is $\pm 8\text{V}$.

A value of 500kΩ was chosen for R_2 . For a gain of 100, R_1 is calculated as:

$$A_{VCL} = 1 + \frac{R_2}{R_1}$$

$$100 = 1 + \frac{500\text{k}\Omega}{R_1}$$

$$\therefore R_1 = 5.05\text{k}\Omega$$

BATTERY-POWERED, GAIN-OF-100 AMPLIFIER

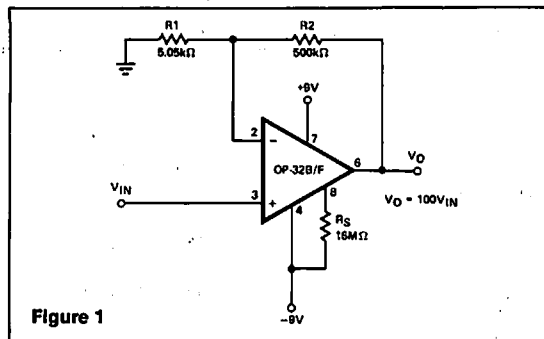


Figure 1

Using an OP-32B/F, we can expect an $I_B + I_{OS}/2$ of less than 8.5nA when operating at I_{SY} of 15μA, so the input offset caused by $I_B R_1$ will be negligible ($8.5\text{nA} \times 5.05\text{k}\Omega \sim 43\mu\text{V}$).

The set resistor R_S needed for a supply current of 15μA is calculated from:

$$R_S = \frac{V_{SUPPLY} - 1.1\text{V}}{I_{SY}/15} = \frac{18\text{V} - 1.1\text{V}}{1\mu\text{A}}$$

$$\therefore R_S = 16.9\text{M}\Omega$$

Offset voltage adjustment is optional. An OP-32B/F has maximum input offset voltage of 500μV which would cause an output offset voltage of 50mV. Drift over temperature is very low, typically less than $1.0\mu\text{V}/^\circ\text{C}$, and is guaranteed to be less than $2.0\mu\text{V}/^\circ\text{C}$. PSRR is also low, only $6\mu\text{V}/\text{V}$, so battery voltage change has negligible effect on offset.

Most micropower programmable op amps lose open-loop gain and CMRR at low supply currents. The OP-32 design overcomes these limitations so accuracy is maintained at supply currents of only a few microamps. The OP-32B/F used in this example has a minimum open-loop gain of over 117dB. Gain error due to finite open-loop gain will be less than $100/750,000$, which is only 133PPM. CMRR will typically be 110dB, an error of 3PPM. Gain accuracy of the circuit is almost entirely dependent on the accuracy of the R_1/R_2 ratio; the op amp contributes less than 0.015% gain error.

Considering all error sources, this simple $\times 100$ battery-powered circuit using an OP-32B/F is capable of achieving excellent accuracy. Without external adjustments of any kind, output offset will be less than 54mV and gain accuracy will be better than $\pm 0.015\%$ (exclusive of R_2/R_1 error). Gain linearity, slew-rate symmetry, and stability over temperature are all excellent with the OP-32, making circuit performance very predictable.

Precision Monolithics Inc.

FEATURES

- Low Noise 80nV p-p (0.1Hz to 10Hz)
..... $3nV/\sqrt{Hz}$ at 1kHz
- Low Drift $0.2\mu V/^\circ C$
- High Speed 17V/ μs Slew Rate
..... 63MHz Gain Bandwidth
- Low Input Offset Voltage 10 μV
- Excellent CMRR ... 126dB (Common-Voltage of $\pm 11V$)
- High Open-Loop Gain 1.8 Million
- Replaces 725, OP-05, OP-06, OP-07, AD510, AD517, SE5534 in Gains > 5

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (μV)	PACKAGE				OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	LCC	
25	OP37AJ*	OP37AZ*	—	—	MIL
25	OP37EJ	OP37EZ	OP37EP	—	IND/COM
60	OP37BJ*	OP37BZ*	—	OP37BRC/883	MIL
60	OP37FJ	OP37FZ	OP37FP	—	IND/COM
100	OP37CJ*	OP37CZ	—	—	MIL
100	OP37GJ	OP37GZ	OP37GP	—	IND/COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-37 provides the same high performance as the OP-27, but the design is optimized for circuits with gains greater than five. This design change increases slew rate to 17V/ μs and gain-bandwidth product to 63MHz.

The OP-37 provides the low offset and drift of the OP-07 plus higher speed and lower noise. Offsets down to 25 μV and drift of 0.6 $\mu V/^\circ C$ maximum make the OP-37 ideal for precision instrumentation applications. Exceptionally low noise

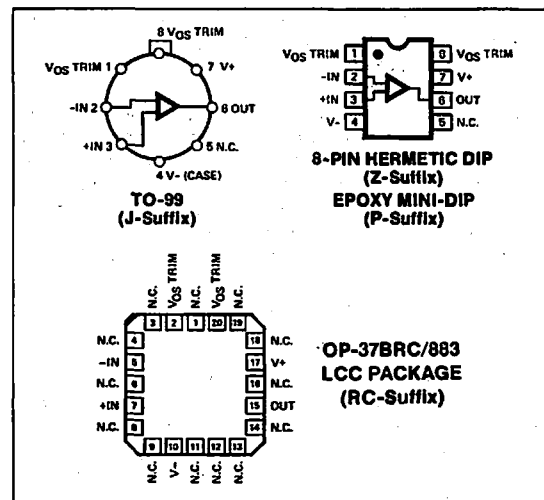
($e_n = 3.5nV/\sqrt{Hz}$ at 10Hz), a low 1/f noise corner frequency of 2.7Hz, and the high gain of 1.8 million, allow accurate high-gain amplification of low-level signals.

The low input bias current of $\pm 10nA$ and offset current of 7nA are achieved by using a bias-current-cancellation circuit. Over the military temperature range this typically holds I_B and I_{OS} to $\pm 20nA$ and 15nA respectively.

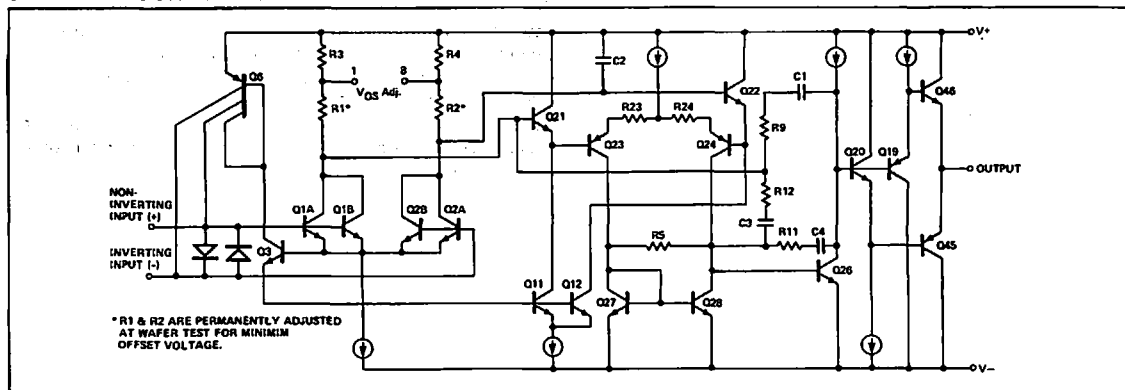
The output stage has good load driving capability. A guaranteed swing of $\pm 10V$ into 600 Ω and low output distortion make the OP-37 an excellent choice for professional audio applications.

PSRR and CMRR exceed 120dB. These characteristics, coupled with long-term drift of 0.2 μV /month, allow the circuit

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of the OP-37 is achieved by using on-chip zener-zap trimming. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP-37 brings low-noise instrumentation-type performance to such diverse applications as microphone, tape-head, and RIAA phono preamplifiers, high-speed signal conditioning for data acquisition systems, and wide-bandwidth instrumentation.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage	$\pm 22\text{V}$
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	$\pm 22\text{V}$
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	$\pm 0.7\text{V}$
Differential Input Current (Note 2)	$\pm 25\text{mA}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$

Operating Temperature Range

OP-37A, OP-37B, OP-37C (J, Z, RC)	-55°C to $+125^\circ\text{C}$
OP-37E, OP-37F, OP-37G (J, Z)	-25°C to $+85^\circ\text{C}$
OP-37E, OP-37F, OP-37G (P)	0°C to $+70^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to $+150^\circ\text{C}$

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	$7.1\text{mW}/^\circ\text{C}$
8-Pin Hermetic DIP (Z)	75°C	$6.7\text{mW}/^\circ\text{C}$
8-Pin Plastic DIP (P)	62°C	$5.6\text{mW}/^\circ\text{C}$
LCC	80°C	$7.8\text{mW}/^\circ\text{C}$

- The OP-37's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds $\pm 0.7\text{V}$, the input current should be limited to 25mA .
- For supply voltages less than $\pm 22\text{V}$, the absolute maximum input voltage is equal to the supply voltage.
- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37A/E			OP-37B/F			OP-37C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	10	25	—	20	60	—	30	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Notes 2, 3)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	$\mu\text{V}/\text{Mo}$
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	± 10	± 40	—	± 12	± 55	—	± 15	± 80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.18	—	0.08	0.18	—	0.09	0.25	$\mu\text{Vp-p}$
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 3)	—	3.5	5.5	—	3.5	5.5	—	3.8	8.0	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 30\text{Hz}$ (Note 3)	—	3.1	4.5	—	3.1	4.5	—	3.3	5.6	
		$f_O = 1000\text{Hz}$ (Note 3)	—	3.0	3.8	—	3.0	3.8	—	3.2	4.5	
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$ (Notes 3, 6)	—	1.7	4.0	—	1.7	4.0	—	1.7	—	$\text{pA}/\sqrt{\text{Hz}}$
		$f_O = 30\text{Hz}$ (Notes 3, 6)	—	1.0	2.3	—	1.0	2.3	—	1.0	—	
		$f_O = 1000\text{Hz}$ (Notes 3, 6)	—	0.4	0.6	—	0.4	0.6	—	0.4	0.6	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	G Ω
Input Voltage Range	IVR		± 11.0	± 12.3	—	± 11.0	± 12.3	—	± 11.0	± 12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11\text{V}$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSSR	$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$	—	1	10	—	1	10	—	2	20	$\mu\text{V}/\text{V}$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 1\text{k}\Omega$, $V_O = \pm 10\text{V}$	800	1500	—	800	1500	—	400	1500	—	
		$R_L = 600\Omega$, $V_O = \pm 1\text{V}$, $V_S = \pm 4\text{V}$, (Note 4)	250	700	—	250	700	—	200	500	—	
Output Voltage Swing	V_O	$R_L \geq 2\text{k}\Omega$ $R_L \geq 600\Omega$	± 12.0 ± 10.0	± 13.8 ± 11.5	—	± 12.0 ± 10.0	± 13.8 ± 11.5	—	± 11.5 ± 10.0	± 13.5 ± 11.5	—	V
Slew Rate	SR	$R_L \geq 2\text{k}\Omega$ (Note 4)	11	17	—	11	17	—	11	17	—	V/ μs
Gain Bandwidth Prod.	GBW	$f_O = 10\text{kHz}$ (Note 4)	45	63	—	45	63	—	45	63	—	MHz
		$f_O = 1\text{MHz}$	—	40	—	—	40	—	—	40	—	

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-37A/E			OP-37B/F			OP-37C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Open-Loop Output Resistance	R_O	$V_O = 0, I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	$V_O = 0$	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	± 4.0	—	—	± 4.0	—	—	± 4.0	—	mV

NOTES:

- Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
- Long-term input offset voltage stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu V$ — refer to typical performance curve.
- Sample tested.
- Guaranteed by design.
- See test circuit and frequency response curve for 0.1Hz to 10Hz tester.
- See test circuit for current noise measurement.
- Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37A			OP-37B			OP-37C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	30	60	—	50	200	—	70	300	μV
Average Input Offset Drift	TCV_{OS}	(Note 2)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	$\mu V/^\circ C$
	TCV_{OSn}	(Note 3)	—	—	—	—	—	—	—	—	—	—
Input Offset Current	I_{OS}		—	15	50	—	22	85	—	30	135	nA
Input Bias Current	I_B		—	± 20	± 60	—	± 28	± 95	—	± 35	± 150	nA
Input Voltage Range	IVR		± 10.3	± 11.5	—	± 10.3	± 11.5	—	± 10.2	± 11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	100	119	—	94	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	—	2	20	—	4	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1200	—	500	1000	—	300	800	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.5	± 13.5	—	± 11.0	± 13.2	—	± 10.5	± 13.0	—	V

ELECTRICAL CHARACTERISTICS for $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-37J and OP-37Z, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-37P, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37E			OP-37F			OP-37G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	20	50	—	40	140	—	55	220	μV
Average Input Offset Drift	TCV_{OS}	(Note 2)	—	0.2	0.6	—	0.3	1.3	—	0.4	1.8	$\mu V/^\circ C$
	TCV_{OSn}	(Note 3)	—	—	—	—	—	—	—	—	—	—
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	± 14	± 60	—	± 18	± 95	—	± 25	± 150	nA
Input Voltage Range	IVR		± 10.5	± 11.8	—	± 10.5	± 11.8	—	± 10.5	± 11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.7	± 13.6	—	± 11.4	± 13.5	—	± 11.0	± 13.3	—	V

NOTES:

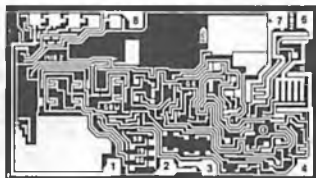
- Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.
- The TCV_{OS} performance is within the specifications unnullled or when nullled with $R_P = 8k\Omega$ to $20k\Omega$. TCV_{OS} is 100% tested for A/E grades, sample tested for B/C/F/G grades.
- Guaranteed by design.



DICE CHARACTERISTICS

DIE SIZE 0.098 × 0.056 inch, 5488 sq. mils
(2.49 × 1.42 mm, 3.54 sq. mm)

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.



1. NULL
2. (-) INPUT
3. (+) INPUT
4. V₋
5. OUTPUT
6. V₊
7. NULL

WAFER TEST LIMITS at V_S = ±15V, T_A = 25° C for OP-37N, OP-37G and OP-37GR devices; T_A = 125° C for OP-37NT and OP-37GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37NT LIMIT	OP-37N LIMIT	OP-37GT LIMIT	OP-37G LIMIT	OP-37GR LIMIT	UNITS
Input Offset Voltage	V _{OS}	(Note 1)	60	35	200	60	100	μV MAX
Input Offset Current	I _{OS}		50	35	85	50	75	nA MAX
Input Bias Current	I _B		±60	±40	±95	±55	±80	nA MAX
Input Voltage Range	IVR		±10.3	±11	±10.3	±11	±11	V MIN
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±11V	108	114	100	106	100	dB MIN
Power Supply Rejection Ratio	PSRR	T _A = 25° C, V _S = ±4V to ±18V	10	10	10	10	20	μV/V MAX
		T _A = 125° C, V _S = ±4.5V to ±18V	16	—	20	—	—	
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2kΩ, V _O = ±10V	600	1000	500	1000	700	V/mV MIN
		R _L ≥ 1kΩ, V _O = ±10V	—	800	—	800	—	
Output Voltage Swing	V _O	R _L ≥ 2kΩ	±11.5	±12.0	±11.0	±12.0	±11.5	V MIN
		R _L ≥ 600Ω	—	±10.0	—	±10.0	±10.0	
Power Consumption	P _d	V _O = 0	—	140	—	140	170	mW MAX

NOTES:

For 25° C characteristics of OP-37NT and OP-37GT devices, see OP-37N and OP-37G characteristics, respectively.

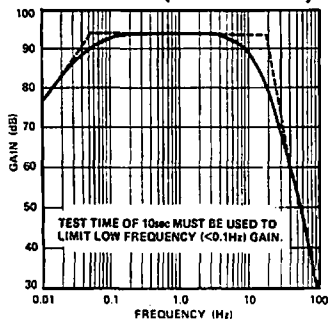
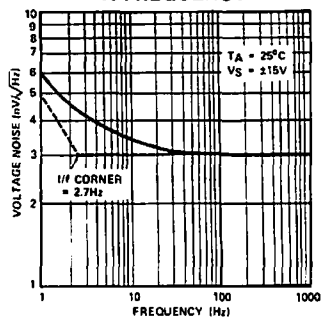
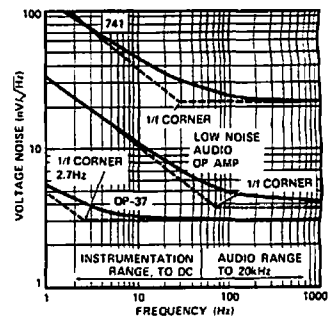
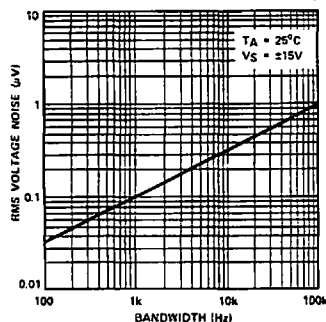
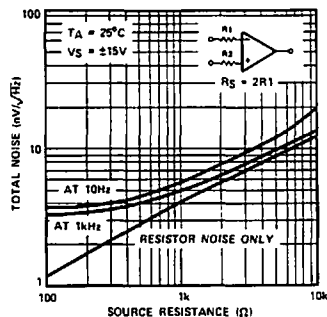
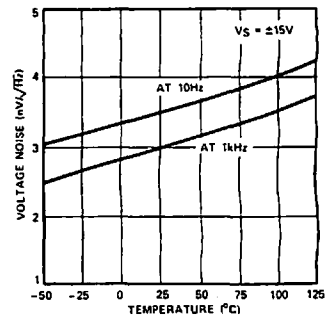
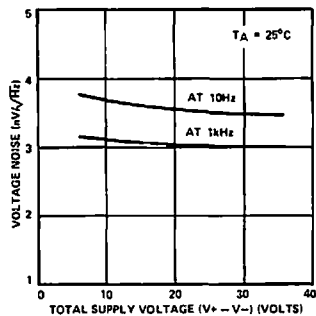
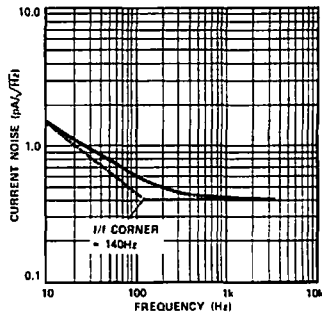
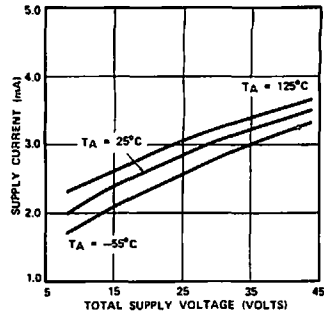
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-37NT TYPICAL	OP-37N TYPICAL	OP-37GT TYPICAL	OP-37G TYPICAL	OP-37GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV _{OS} or TCV _{OSn}	Nullled or Unnullled R _P = 8kΩ to 20kΩ	0.2	0.2	0.3	0.3	0.4	μV/° C
Average Input Offset Current Drift	TCI _{OS}		80	80	130	130	180	pA/° C
Average Input Bias Current Drift	TCI _B		100	100	160	160	200	pA/° C
Input Noise Voltage Density	e _n	f _O = 10Hz	3.5	3.5	3.5	3.5	3.8	nV/√ Hz
		f _O = 30Hz	3.1	3.1	3.1	3.1	3.3	
		f _O = 1000Hz	3.0	3.0	3.0	3.0	3.2	
Input Noise Current Density	i _n	f _O = 10Hz	1.7	1.7	1.7	1.7	1.7	pA/√ Hz
		f _O = 30Hz	1.0	1.0	1.0	1.0	1.0	
		f _O = 1000Hz	0.4	0.4	0.4	0.4	0.4	
Input Noise Voltage	e _{np-p}	0.1Hz to 10Hz	0.08	0.08	0.08	0.08	0.09	μV _{p-p}
Slew Rate	SR	R _L ≥ 2kΩ	17	17	17	17	17	V/μs
Gain Bandwidth Product	GBW	f _O = 10kHz	63	63	63	63	63	MHz

NOTE:

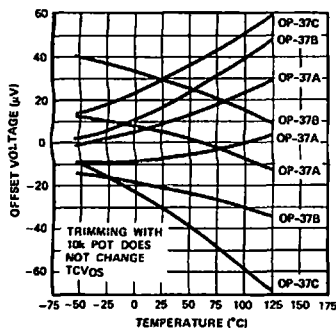
1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

TYPICAL PERFORMANCE CHARACTERISTICS
NOISE-TESTER FREQUENCY RESPONSE (0.1Hz TO 10Hz)

VOLTAGE NOISE DENSITY vs FREQUENCY

A COMPARISON OF OP AMP VOLTAGE NOISE SPECTRA

INPUT WIDEBAND VOLTAGE NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)

TOTAL NOISE vs SOURCE RESISTANCE

VOLTAGE NOISE DENSITY vs TEMPERATURE

VOLTAGE NOISE DENSITY vs SUPPLY VOLTAGE

CURRENT NOISE DENSITY vs FREQUENCY

SUPPLY CURRENT vs SUPPLY VOLTAGE


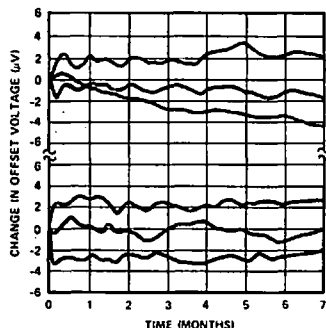


TYPICAL PERFORMANCE CHARACTERISTICS

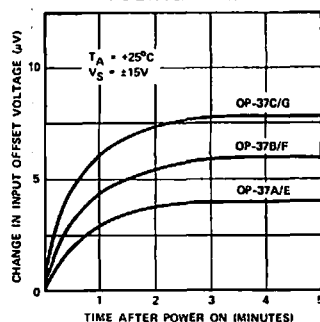
OFFSET VOLTAGE DRIFT OF EIGHT REPRESENTATIVE UNITS vs TEMPERATURE



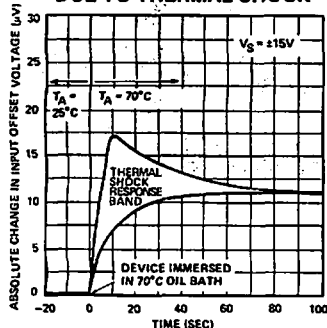
LONG-TERM OFFSET VOLTAGE DRIFT OF SIX REPRESENTATIVE UNITS



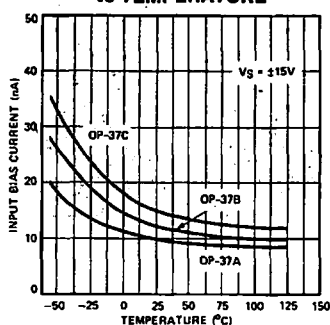
WARM-UP OFFSET VOLTAGE DRIFT



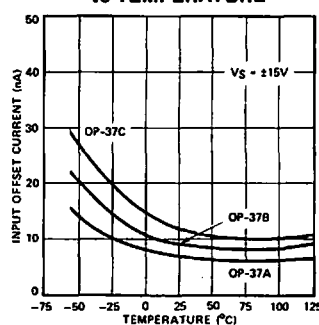
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



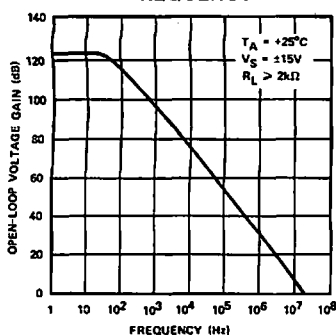
INPUT BIAS CURRENT vs TEMPERATURE



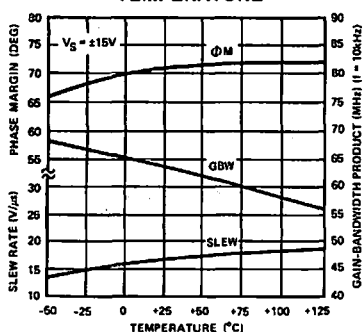
INPUT OFFSET CURRENT vs TEMPERATURE



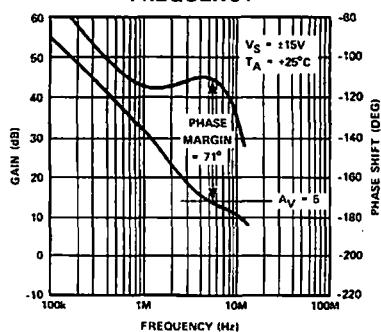
OPEN-LOOP GAIN vs FREQUENCY



SLEW RATE, GAIN BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE

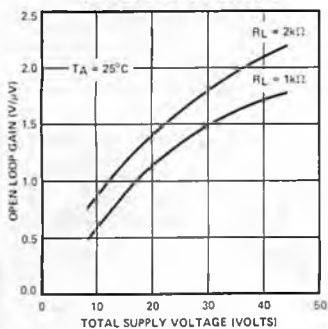
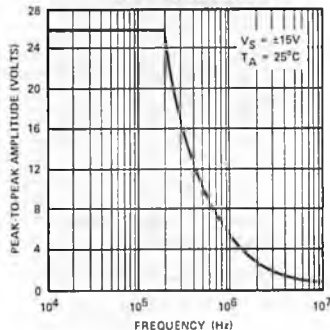
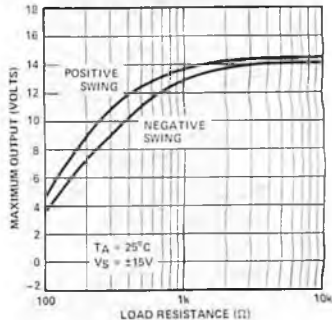
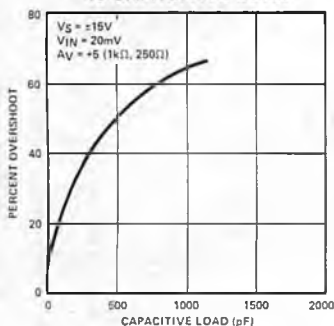
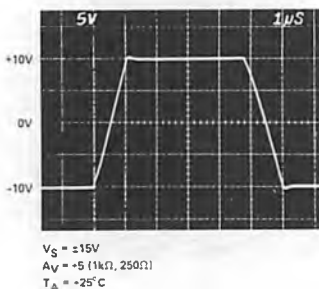
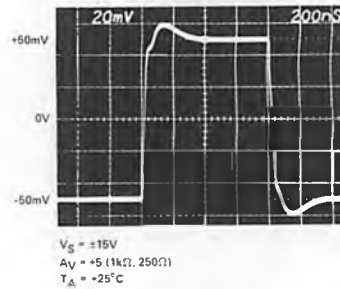
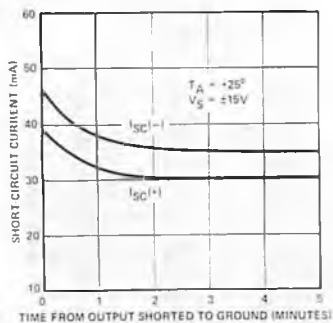


GAIN, PHASE SHIFT vs FREQUENCY

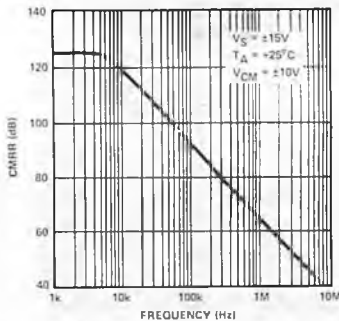
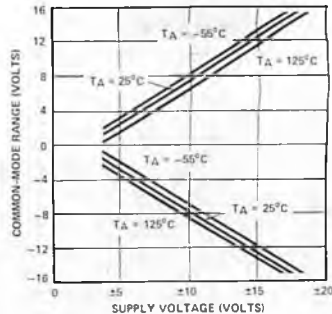


OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS

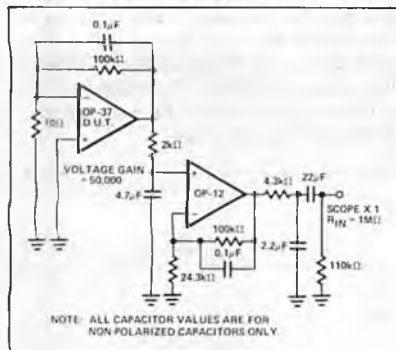
OPEN-LOOP VOLTAGE GAIN
vs SUPPLY VOLTAGEMAXIMUM OUTPUT SWING
vs FREQUENCYMAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCESMALL-SIGNAL OVERSHOOT
vs CAPACITIVE LOADLARGE-SIGNAL TRANSIENT
RESPONSESMALL-SIGNAL TRANSIENT
RESPONSESHORT-CIRCUIT CURRENT
vs TIME

CMRR vs FREQUENCY

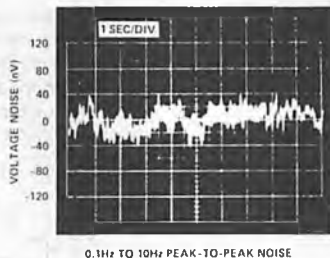
COMMON-MODE INPUT RANGE
vs SUPPLY VOLTAGE

TYPICAL PERFORMANCE CHARACTERISTICS

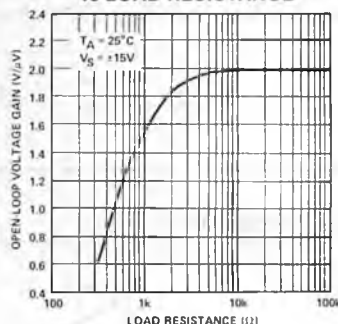
NOISE TEST CIRCUIT (0.1Hz TO 10Hz)



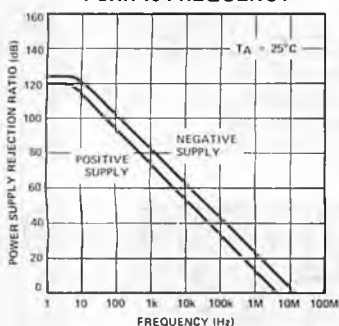
LOW-FREQUENCY NOISE



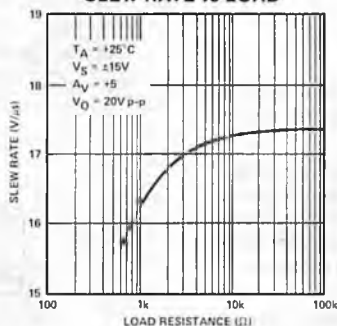
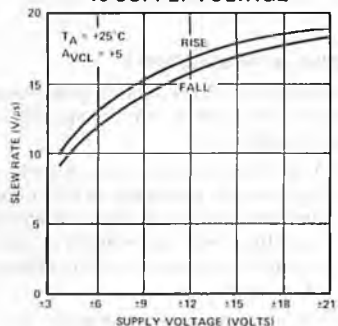
NOTE:
Observation time limited to 10 seconds.

 OPEN-LOOP VOLTAGE GAIN
vs LOAD RESISTANCE


PSRR vs FREQUENCY



SLEW RATE vs LOAD


 SLEW RATE
vs SUPPLY VOLTAGE


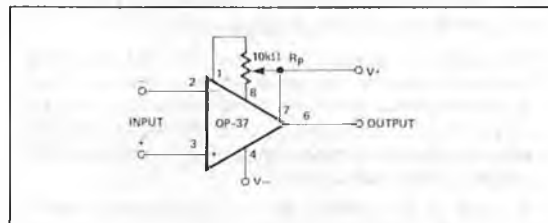
APPLICATIONS INFORMATION

OP-37 Series units may be inserted directly into 725, OP-06, OP-07, and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, the OP-37 may be fitted to unnulling 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP-37 operation. OP-37 offset voltage may be nulled to zero (or other desired setting) using a potentiometer (see offset nulling circuit).

The OP-37 provides stable operation with load capacitances of up to 1000pF and $\pm 10V$ swings; larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop. Closed-loop gain must be at least five. For closed-loop gain between five to ten, the designer should consider both the OP-27 and the OP-37. For gains above ten, the OP-37 has a clear advantage over the unity-gain-stable OP-27.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

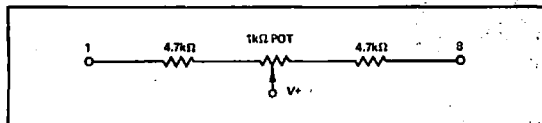
OFFSET NULLING CIRCUIT



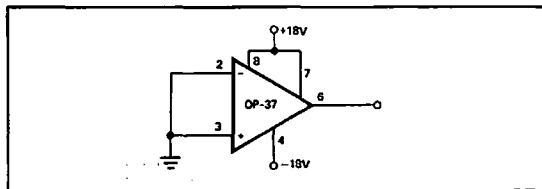
OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP-37 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10kΩ trim potentiometer may be used. TCV_{OS} is not degraded (see offset nulling circuit). Other potentiometer values from 1kΩ to 1MΩ can be used with a slight degradation (0.1 to 0.2 $\mu V/^{\circ}C$) of TCV_{OS} . Trimming to a value other than zero creates a drift of approximately $(V_{OS}/300) \mu V/^{\circ}C$. For exam-

pie, the change in TCV_{OS} will be $0.33\mu V/^{\circ}C$ if V_{OS} is adjusted to $100\mu V$. The offset-voltage adjustment range with a $10k\Omega$ potentiometer is $\pm 4mV$. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjunction with fixed resistors. For example, the network below will have a $\pm 280\mu V$ adjustment range.



BURN-IN CIRCUIT



NOISE MEASUREMENTS

To measure the $80nV$ peak-to-peak noise specification of the OP-37 in the $0.1Hz$ to $10Hz$ range, the following precautions must be observed:

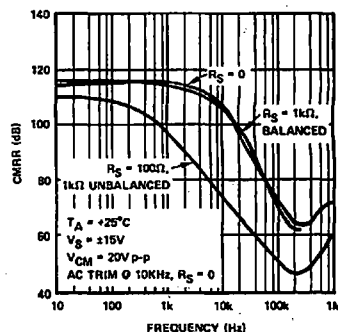
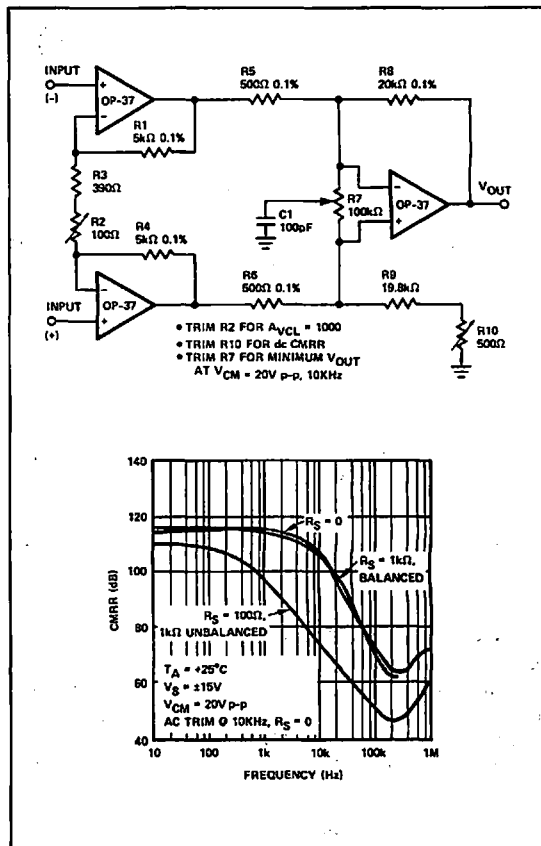
- (1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes $4\mu V$ due to increasing chip temperature after power-up. In the 10 second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
- (2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.
- (3) Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.
- (4) The test time to measure $0.1Hz$ -to- $10Hz$ noise should not exceed 10 seconds. As shown in the noise-tester frequency response curve, the $0.1Hz$ corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below $0.1Hz$.
- (5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A $10Hz$ noise-voltage-density measurement will correlate well with a $0.1Hz$ -to- $10Hz$ peak-to-peak noise reading, since both results are determined by the white noise and the location of the $1/f$ corner frequency.

OPTIMIZING LINEARITY

Best linearity will be obtained by designing for the minimum output current required for the application. High gain and excellent linearity can be achieved by operating the op amp with a peak output current of less than $\pm 10mA$.

INSTRUMENTATION AMPLIFIER

A three-op-amp instrumentation amplifier provides high gain and wide bandwidth. The input noise of the circuit below is $4.9nV/\sqrt{Hz}$. The gain of the input stage is set at 25 and the gain of the second stage is 40; overall gain is 1000. The amplifier bandwidth of $800kHz$ is extraordinarily good for a precision instrumentation amplifier. Set to a gain of 1000, this yields a gain-bandwidth product of $800MHz$. The full-power bandwidth for a $20V_{p-p}$ output is $250kHz$. Potentiometer R7 provides quadrature trimming to optimize the instrumentation amplifier's AC common-mode rejection.



COMMENTS ON NOISE

The OP-37 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP-37 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input-bias-current cancellation circuit. The OP-37A/E has I_B and I_{OS} of only $\pm 40nA$ and $35nA$ respectively at $25^{\circ}C$. This is particularly important when the input has a high source-resistance. In addition, many audio amplifier designers

NOISE vs SOURCE RESISTANCE (INCLUDING RESISTOR NOISE) AT 1000Hz

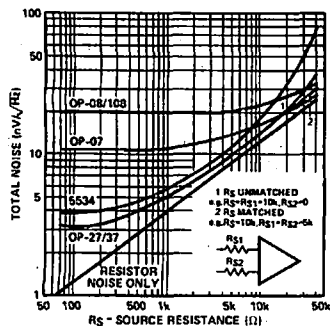


Figure 1

PEAK-TO-PEAK NOISE (0.1 to 10Hz) vs SOURCE RESISTANCE (INCLUDES RESISTOR NOISE)

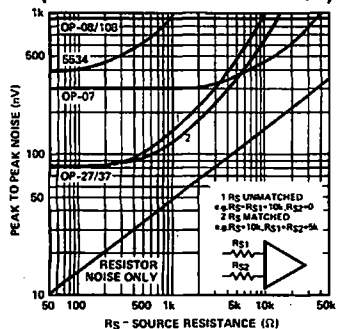


Figure 2

prefer to use direct coupling. The high I_B , TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square-root of bias current, but current noise is proportional to the square-root of bias current. The OP-37's noise advantage disappears when high source-resistors are used. Figures 1, 2, and 3 compare OP-37 observed total noise with the noise performance of other devices in different circuit applications.

$$\text{Total noise} = [(\text{Voltage noise})^2 + (\text{current noise} \times R_S)^2 + (\text{resistor noise}^2)]^{1/2}$$

Figure 1 shows noise-versus-source-resistance at 1000Hz. The same plot applies to wideband noise. To use this plot, just multiply the vertical scale by the square-root of the bandwidth.

At $R_S < 1k\Omega$, the OP-37's low voltage noise is maintained. With $R_S > 1k\Omega$, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only

10Hz NOISE vs SOURCE RESISTANCE (INCLUDES RESISTOR NOISE)

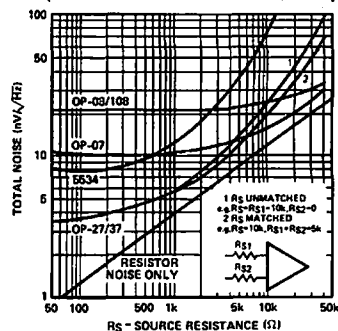


Figure 3

beyond R_S of 20k Ω that current noise starts to dominate. The argument can be made that current noise is not important for applications with low-to-moderate source resistances. The crossover between the OP-37 and OP-07 and OP-08 noise occurs in the 15-to-40k Ω region.

Figure 2 shows the 0.1Hz-to-10Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible, current noise becomes important because it is inversely proportional to the square-root of frequency. The crossover with the OP-07 occurs in the 3-to-5k Ω range depending on whether balanced or unbalanced source resistors are used (at 3k Ω the I_B , I_{OS} error also can be three times the V_{OS} spec.).

Therefore, for low-frequency applications, the OP-07 is better than the OP-27/37 when $R_S > 3k\Omega$. The only exception is when gain error is important. Figure 3 illustrates the 10Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table 1.

Table 1

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500 Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500 Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-37 I_B can be neglected.
Magnetic phonograph cartridges	<1500 Ω	Similar need for low I_B in direct coupled applications. OP-37 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500 Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

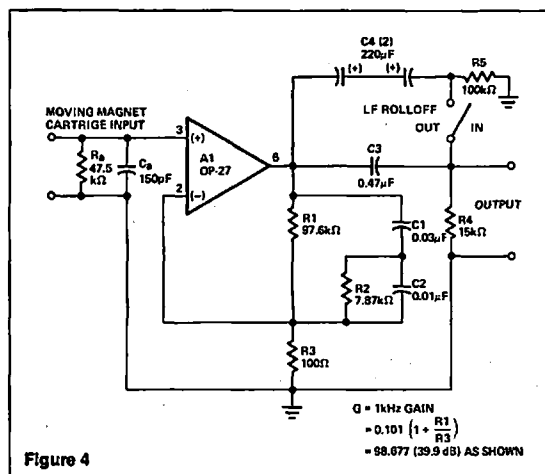


Figure 4

Figure 4 is an example of a phono pre-amplifier circuit using the OP-27 for A₁; R₁-R₂-C₁-C₂ form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75μs.¹

For initial equalization accuracy and stability, precision metal-film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.⁴ (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors, and somewhat lower dielectric absorption—can be considered for small values or where space is at a premium.)

The OP-27 brings a 3.2nV/√Hz voltage noise and 0.45 pA/√Hz current noise to this circuit. To minimize noise from other sources, R₃ is set to a value of 100Ω, which generates a voltage noise of 1.3nV/√Hz. The noise increases the 3.2nV/√Hz of the amplifier by only 0.7dB. With a 1kΩ source, the circuit noise measures 63dB below a 1mV reference level, unweighted, in a 20kHz noise bandwidth.

Gain (G) of the circuit at 1kHz can be calculated by the expression:

$$G = 0.101 \left(1 + \frac{R_1}{R_3} \right)$$

For the values shown, the gain is just under 100 (or 40dB). Lower gains can be accommodated by increasing R₃, but gains higher than 40dB will show more equalization errors because of the 8MHz gain-bandwidth of the OP-27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms. At 3V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20kHz.

Capacitor C₃ and resistor R₄ form a simple -6dB-per-octave rumble filter, with a corner at 22Hz. As an option, the switch-selected shunt capacitor C₄, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Fig. 4 can be readily modified for tape use, as shown by Fig. 5.

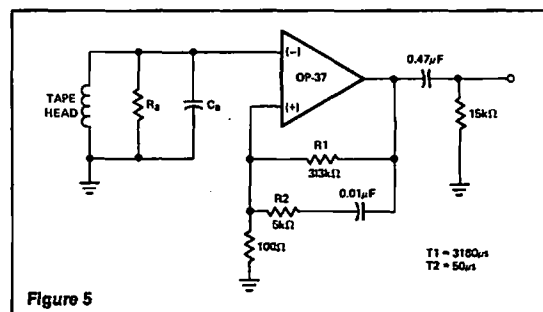


Figure 5

While the tape-equalization requirement has a flat high-frequency gain above 3kHz (T₂ = 50μs), the amplifier need not be stabilized for unity gain. The uncompensated OP-37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R₁ and R₂ to optimize frequency response for nonideal tape-head performance and other factors.⁵

The network values of the configuration yield a 50dB gain at 1kHz, and the dc gain is greater than 70dB. Thus, the worst-case output offset is just over 500mV. A single 0.47μF output capacitor can block this level without affecting the dynamic range.

The tape head can be coupled directly to the amplifier input, since the worst-case bias current of 85nA with a 400mH, 100 μin. head (such as the PRB2H7K) will not be troublesome.

One potential tape-head problem is presented by amplifier bias-current transients which can magnetize a head. The OP-27 and OP-37 are free of bias-current transients upon power up or power down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 170μV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Fig. 6) amplifies differential signals from low-impedance microphones by 50dB, and has an input impedance of 2k Ω . Because of the high working gain of the circuit, an OP-37 helps to preserve bandwidth, which will be 110kHz. As the OP-37 is a decompensated device (minimum stable gain of 5), a dummy resistor, R_p , may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

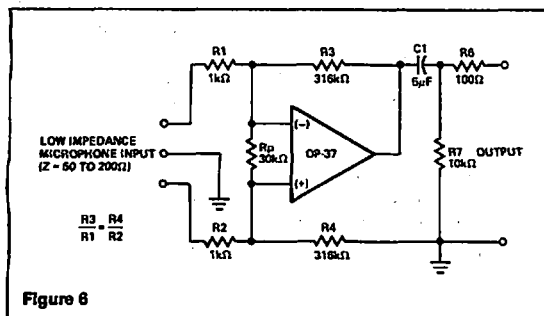


Figure 6

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R_4 should be trimmed for best CMRR. All resistors should be metal-film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R_1 and R_2 than by the op amp, as R_1 and R_2 each generate a $4\text{nV}/\sqrt{\text{Hz}}$ noise, while the op amp generates a $3.2\text{nV}/\sqrt{\text{Hz}}$ noise. The rms sum of these predominant noise sources will be about $6\text{nV}/\sqrt{\text{Hz}}$, equivalent to 0.9 μV in a 20kHz noise bandwidth, or nearly 61dB below a 1mV input signal. Measurements confirm this predicted performance.

For applications demanding appreciably lower noise, a high-quality microphone-transformer-coupled preamp (Fig. 7) incorporates the internally compensated OP-27. T_1 is a JE-115K-E 150 Ω /15k Ω transformer which provides an optimum source resistance for the OP-27 device. The circuit has an overall gain of 40dB, the product of the transformer's voltage setup and the op amp's voltage gain.

Gain may be trimmed to other levels, if desired, by adjusting R_2 or R_1 . Because of the low offset voltage of the OP-27, the output offset of this circuit will be very low, 1.7mV or less, for a

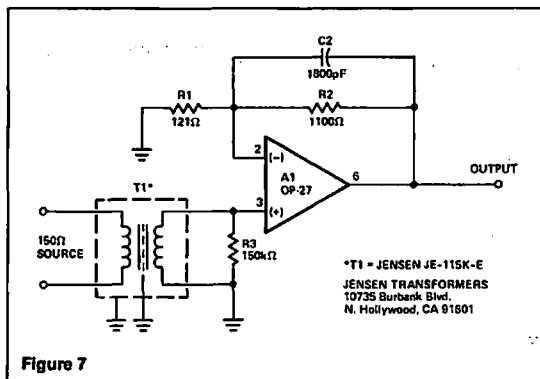


Figure 7

40dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

Capacitor C_2 and resistor R_2 form a 2 μs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C_2 in use, A_1 must have unity-gain stability. For situations where the 2 μs time constant is not necessary, C_2 can be deleted, allowing the faster OP-37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150 Ω resistor and R_1 and R_2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20kHz bandwidth, or 73dB below a 1mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP-27 and T_1 specified, the additional noise degradation will be close to 3.6dB (or -69.5 referenced to 1mV).

References

1. Lipshitz, S.P., "On RIAA Equalization Networks," *JAES*, Vol. 27, June 1979, p. 458-481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February & March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw Hill, 1976.



OP-41

LOW-BIAS-CURRENT, HIGH-STABILITY JFET OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Bias Current 5pA Max
- Low Current Consumption 1.0mA Max
- High Gain 1000V/mV Min
- High Common-Mode Rejection 100dB Min
- Symmetrical Slew-Rates $\pm 1.0V/\mu s$ Min
- Low Harmonic Distortion <0.01% at 5kHz
- Phase Margin 77° Typ

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	PLASTIC DIP 8-PIN	
500	OP-41AJ*	—	MIL
250	OP-41EJ	—	IND
1000	OP-41BJ*	—	MIL
750	OP-41FJ	—	IND
2000	—	OP-41GP	COM

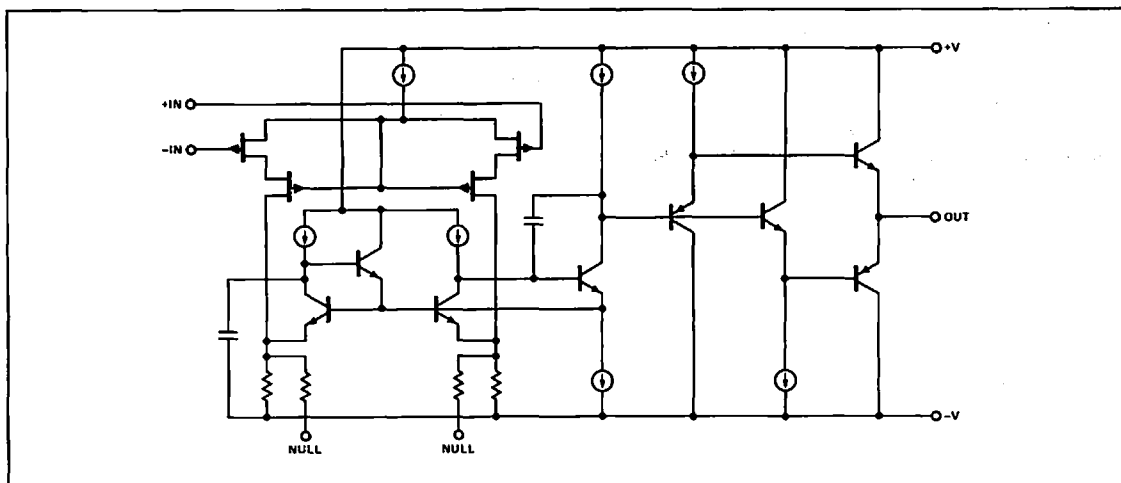
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-41 JFET-input op amp features a 5pA max bias current with an open-loop gain of over 1 million. 77° of phase margin provides exceptional stability, even in unity-gain with capacitive loads. The output is guaranteed stable with 250pF loads at unity-gain, and will typically drive several thousand pF. Transient response is extremely clean, and is considerably improved over industry-standard JFET amplifiers.

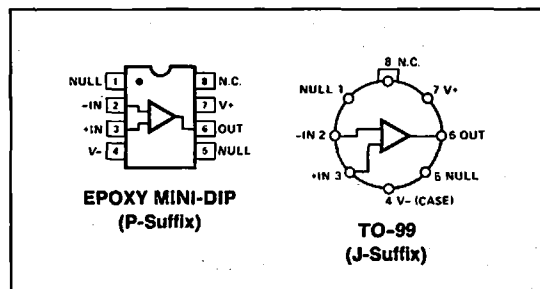
SIMPLIFIED SCHEMATIC



Manufactured under the following U.S. patent: 4,538,115.

The OP-41's cascode input stage boosts CMR to over 100dB, improves CMR linearity, and stabilizes bias current with changing common-mode voltage. The linear common-mode rejection of 100dB min is unusually good for a FET input amplifier. The OP-41 consumes only 750 μA supply current and has a power-supply rejection ratio of 25 $\mu V/V$, making it an ideal choice for battery-operated systems. Despite the low supply-drain, the slew-rate is a respectable 1.3V/ μs , and symmetrical. Using zener-zap trimming techniques, offset voltage is adjusted to below 500 μV which eliminates the need for external nulling in many applications. The OP-41's guaranteed gain of 1 million into a 2k Ω load, combined with the linear 100dB minimum CMR, vastly improves linearity over competitive low-cost devices. Linearity is excellent in both low-gain and high-gain amplifier configurations. In voltage follower applications CMR effects dominate linearity, and in high-gain applications open-loop gain dominates linearity, hence the performance advantage of the OP-41.

PIN CONNECTIONS





The device exhibits rapid recovery from signal overload. Following saturation at the positive supply, the output recovers in only 6 μ s, and from a negative overdrive in only 100ns.

The combination of low-power, low bias current, and high-gain, plus the superior CMR and PSRR performance of the OP-41, make it suitable in a wide variety of demanding applications. The device makes an excellent output amplifier for CMOS DACs. Where low-power consumption is needed in portable instrumentation, the OP-41 permits high-gain and high-accuracy amplification with good speed performance. The low and stable bias current makes it an excellent choice as a photodiode amplifier in medical applications.

A standard 741 pin-out allows existing JFET designs and low-power bipolar designs to be upgraded by switching to the OP-41.

ABSOLUTE MAXIMUM RATINGS

(Note 3)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 2)	$\pm 18\text{V}$
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	$\pm 18\text{V}$
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	
OP-41A, B (J)	-55°C to $+125^{\circ}\text{C}$
OP-41E, F (J)	-25°C to $+85^{\circ}\text{C}$
OP-41G (P)	0°C to $+70^{\circ}\text{C}$

Lead Temperature Range (Soldering, 60 sec) 300°C
Junction Temperature -65°C to $+150^{\circ}\text{C}$

NOTES:

- See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/ $^{\circ}\text{C}$
8-Pin Plastic DIP (P)	62°C	5.6mW/ $^{\circ}\text{C}$

- For supply voltages less than $\pm 18\text{V}$, the absolute maximum input voltage is equal to the supply voltage.
- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-41A/E			OP-41B/F			OP-41G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}	OP-41E/F/G OP-41A/B	—	200	250	—	400	750	—	500	2000	μV
Offset Current	I_{OS}	(Note 1)	—	0.04	1	—	0.05	2	—	0.05	5	pA
Bias Current	I_B	(Note 1)	—	3.0	5	—	3.5	10	—	3.5	20	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{V}$	1000	5000	—	500	4000	—	500	4000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2\text{k}\Omega$	± 12.3	± 12.6	—	± 12.0	± 12.6	—	± 12.0	± 12.6	—	V
Supply Current	I_{SY}	$V_O = 0\text{V}$	—	.75	1.0	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	I_{VR}	(Note 2)	± 11	+15 -11.5	—	± 11	+15 -11.5	—	± 11	+15 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{V}$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10\text{V}$ to $\pm 18\text{V}$	—	5	25	—	10	80	—	10	80	$\mu\text{V/V}$
Noise Voltage Density Referred to Input	e_n	1kHz	—	32	—	—	32	—	—	32	—	nV/ $\sqrt{\text{Hz}}$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 12	+20 -18	± 36	± 12	+20 -18	± 36	± 6	+20 -18	± 36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	1	1.3	—	V/ μs
Gain Bandwidth	GBW		—	500	—	—	500	—	—	500	—	kHz
Power Bandwidth	BW_P		—	20	—	—	20	—	—	20	—	kHz

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-41A/E			OP-41B/F			OP-41G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Settling Time	t_s	10V Step $A_V = -1$ to 0.1% to 0.01%	—	10 12	—	—	10 12	—	—	10 12	—	μs
Overload Recovery		Positive Going Negative Going	—	0.1 6.0	—	—	0.1 6.0	—	—	0.1 6.0	—	μs
Capacitive Load Stability		$A_V = +1$ (Note 3)	250	>1000	—	250	>1000	—	250	>1000	—	pF
Open-Loop Output Resistance	R_O		—	150	—	—	150	—	—	150	—	Ω

NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -55^\circ C/+125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-41A			OP-41B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	400	1000	—	600	2000	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	2.5	5	—	3.5	10	$\mu V/^\circ C$
Offset Current	I_{OS}	(Note 1)	—	40	1000	—	50	2000	pA
Bias Current	I_B	(Note 1)	—	4000	7500	—	4500	15000	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12.0	± 12.5	—	± 11.5	± 12.5	—	V
Supply Current	I_{SV}	$V_O = 0V$	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	± 11	+15 -11.5	—	± 11	+15 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	105	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	40	—	10	100	$\mu V/V$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6	+12 -17	± 36	± 6	+12 -17	± 36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	V/ μs
Gain Bandwidth	GBW		—	500	—	—	500	—	kHz
Power Bandwidth	BW_p		—	20	—	—	20	—	kHz
Capacitive Load Stability		$A_V = +1$ (Note 3)	100	>1000	—	100	>1000	—	pF

NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

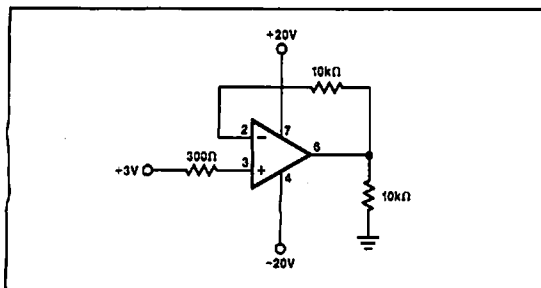
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -25^\circ C/+85^\circ C$ for E/F grades and $0^\circ C/70^\circ C$ for G grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-41E			OP-41F			OP-41G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	250	750	—	500	1750	—	500	2500	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	3.5	8	—	7.5	—	—	7.5	—	$\mu V/^\circ C$
Offset Current	I_{OS}	(Note 1)	—	5	100	—	10	200	—	20	—	pA
Bias Current	I_B	(Note 1)	—	240	500	—	300	1000	—	100	500	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	500	4000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12.0	± 12.6	—	± 11.5	± 12.5	—	± 11.5	± 12.5	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	0.75	1.2	—	0.75	1.2	—	0.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	± 11	+15 -11.5	—	± 11	+15 -11.5	—	± 11	+15 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	110	—	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	40	—	10	100	—	10	100	$\mu V/V$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6	+16 -18	± 36	± 6	+16 -18	± 36	± 6	+20 -18	± 36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	1	1.3	—	V/ μs
Gain Bandwidth	GBW		—	500	—	—	500	—	—	500	—	kHz
Power Bandwidth	BW_P		—	20	—	—	20	—	—	20	—	kHz
Capacitive Load Stability		$A_V = +1$ (Note 3)	100	>1000	—	100	>1000	—	100	>1000	—	pF

NOTES:

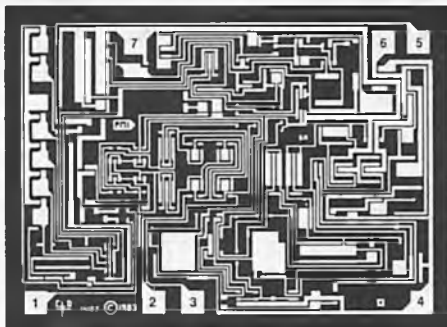
1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

BURN-IN CIRCUIT





DICE CHARACTERISTICS



DIE SIZE 0.103×0.074 inch, 7622 sq. mils
(2.62×1.88 mm, 4.92 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-41N LIMIT	UNITS
Offset Voltage	V_{OS}		1000	μV MAX
Bias Current	I_B	(Note 1)	20	pA MAX
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12	V MIN
Supply Current	I_{SY}	$V_O = 0V$	1.2	mA MAX
Input Voltage Range	IVR	(Note 2)	± 11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	80	$\mu V/V$ MAX
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6 ± 36	mA MIN mA MAX
Slew Rate	SR		1	V/ μs MIN
Capacitive Load Stability	$A_V = +1$	(Note 3)	250	pF MIN

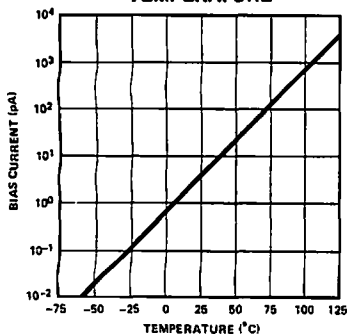
NOTES:

1. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

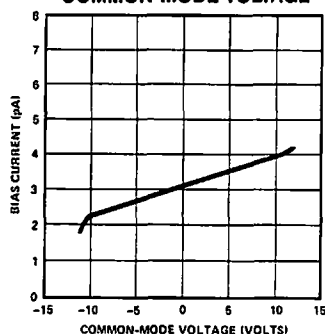
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

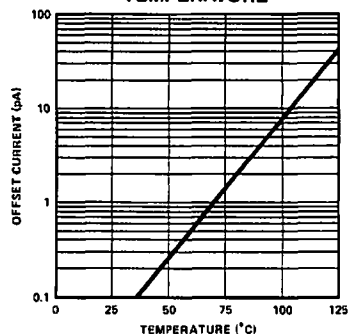
BIAS CURRENT vs TEMPERATURE



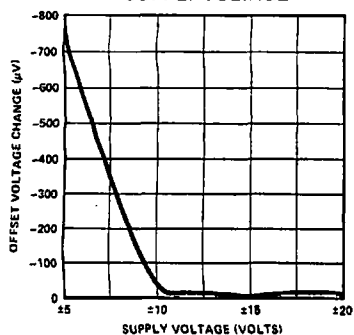
BIAS CURRENT vs COMMON-MODE VOLTAGE



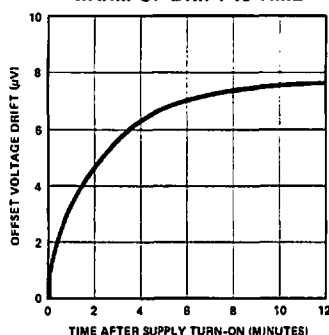
OFFSET CURRENT vs TEMPERATURE



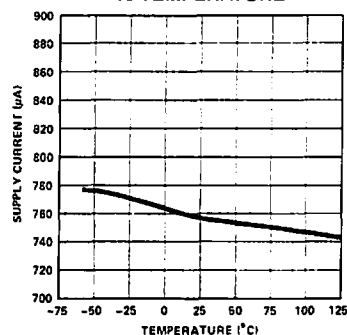
OFFSET VOLTAGE vs SUPPLY VOLTAGE



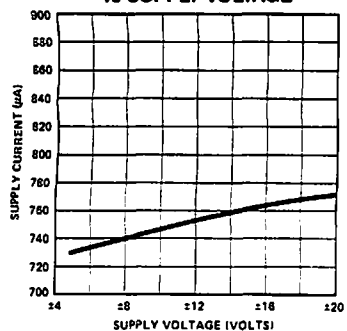
WARM-UP DRIFT vs TIME



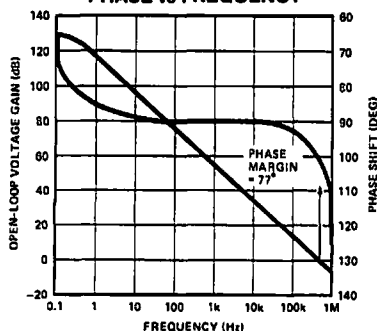
SUPPLY CURRENT vs TEMPERATURE



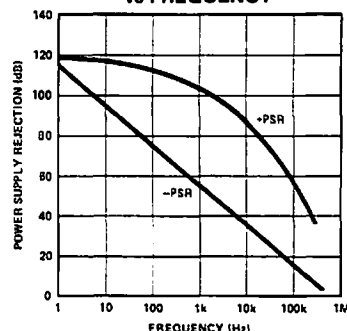
SUPPLY CURRENT vs SUPPLY VOLTAGE



OPEN-LOOP GAIN AND PHASE vs FREQUENCY

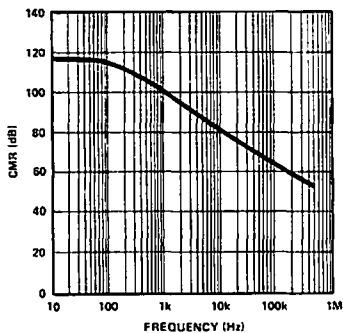
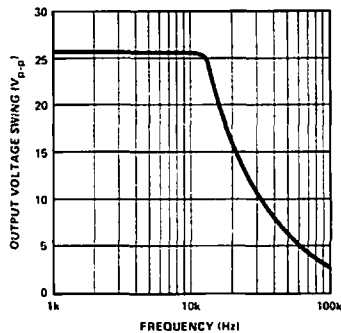
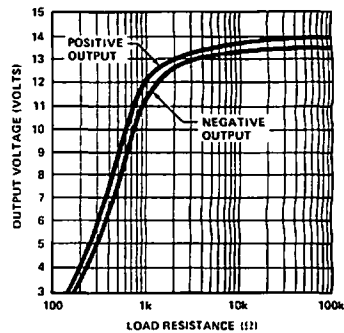
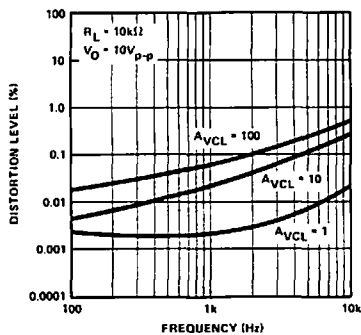
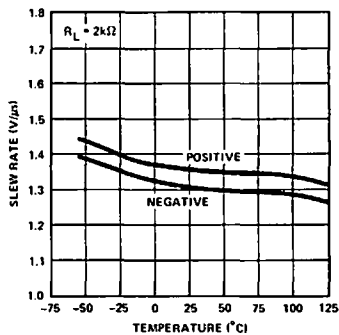


POWER SUPPLY REJECTION vs FREQUENCY

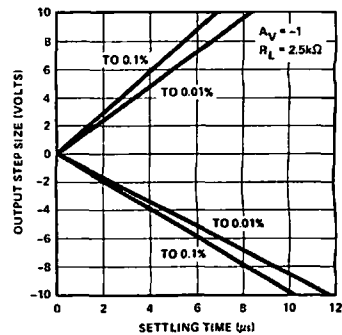
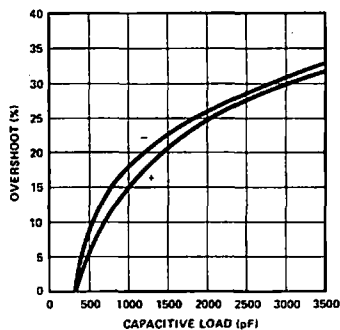


OPERATIONAL AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS

COMMON-MODE REJECTION
vs FREQUENCY

MAXIMUM OUTPUT SWING
vs FREQUENCY

MAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCE

TOTAL HARMONIC
DISTORTION vs FREQUENCY

SLEW RATE vs
TEMPERATURE


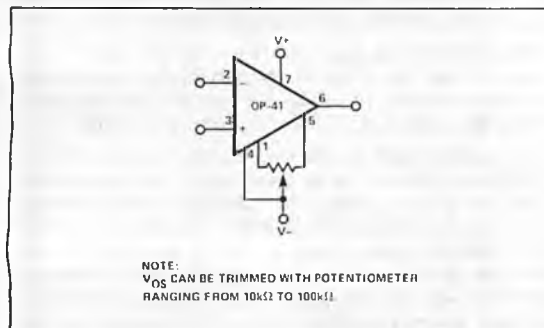
SETTLING TIME


SMALL-SIGNAL OVERSHOOT
vs CAPACITIVE LOAD


OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted by a potentiometer of 10k Ω to 100k Ω resistance. This potentiometer should be connected between pins 1 and 5 with the wiper connected to the V₋ supply. (See Figure 1.) Nulling V_{OS} will change TCV_{OS} by no more than 5 μ V/ $^{\circ}$ C per millivolt of V_{OS} change.

FIGURE 1: INPUT OFFSET VOLTAGE NULLING



APPLICATIONS INFORMATION

TYPICAL AC PERFORMANCE CHARACTERISTICS

Figure 2 shows the overload recovery time after the output saturates at each supply. A high degree of slew-rate symmetry is maintained even during severe input overload. The photo also shows the well controlled linear characteristics of the amplifier and freedom from oscillations. The OP-41's symmetry greatly reduces the generation of large DC components in the output when the amplifier is overdriven. This significantly reduces system recovery time after an overload.

Figure 3 shows the unity-gain small-signal transient response of the OP-41. Note the clean symmetrical waveform.

Figure 4 illustrates the high degree of stability even when loaded with 1000pF at unity-gain. Heavy capacitive loading will cause stability problems with many amplifiers.

Figure 5 illustrates the use of the OP-41 in a high sensitivity, wide-dynamic-range light detector. This circuit will produce an output voltage proportional to the light input over a 60dB range.

FIGURE 2: OVERLOAD RECOVERY TIME AT A_V = 10

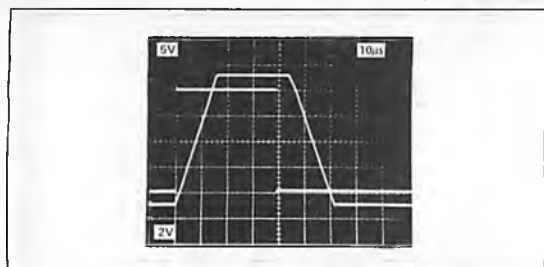


FIGURE 3: SMALL-SIGNAL TRANSIENT RESPONSE

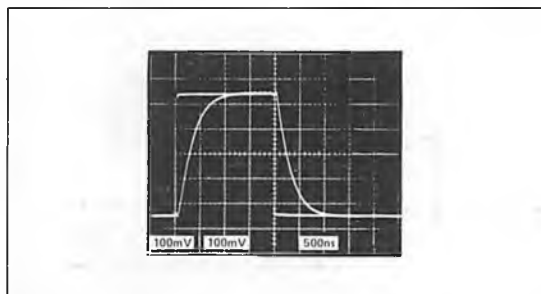


FIGURE 4: SMALL-SIGNAL TRANSIENT RESPONSE WITH 1000pF LOAD

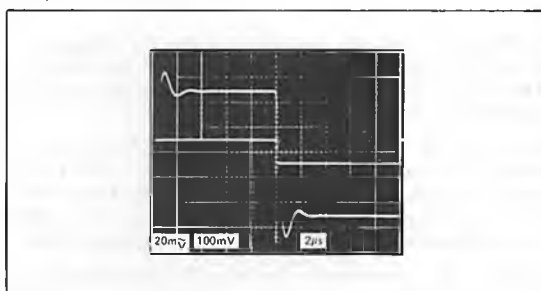
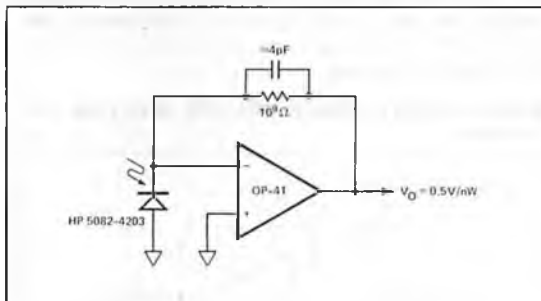


FIGURE 5: WIDE-DYNAMIC-RANGE LIGHT DETECTOR

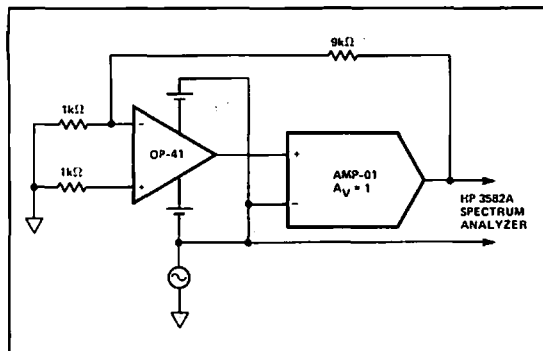


CMR MEASUREMENT METHODS

Two separate methods are used to measure the CMR. The first method is used over the range of 10Hz to 20kHz. This method grounds the input circuitry and applies the common-mode signal to the remainder of the op amp, Figure 6.

The AMP-01 eliminates loading on the output stage. This assures that the OP-41 output is not required to deliver current into the feedback circuit. The effects of the DUT open-loop gain changing with frequency are therefore significantly reduced. The circuit does not require tight resistor matching. DC data sheet limits may be verified using this method. Circuit accuracy is dependent on the high CMR of the AMP-01.

FIGURE 6: CIRCUIT USED TO MEASURE CMR FROM 10kHz TO 20kHz

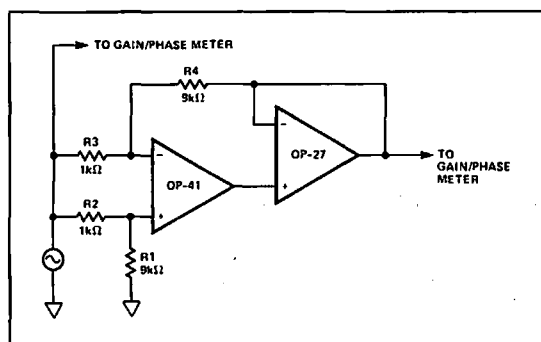


An alternate circuit may be used to make high-frequency measurements from 2kHz to 500kHz, Figure 7. The 2kHz to 20kHz data overlap can be used to verify the accuracy of the respective test methods.

This method drives the input stage with the test signal and requires an accurate ratio of resistors, $R_4/R_3 = R_1/R_2$. To measure CMR to 100dB requires ratio matching to better than 10ppm. For this reason, it is not practical to use the second method at low frequencies where CMR is greater than 80-100dB.

The DUT output is normally connected directly to R_4 which may cause problems. If the DUT is not buffered with a broadband low-output-impedance amplifier, the frequency-dependent output impedance of the DUT, in series with R_4 , rapidly unbalances the resistor ratios. This causes frequency dependent errors. The OP-27 provides good performance over the range of frequencies used.

FIGURE 7: CIRCUIT USED TO MEASURE CMR FROM 2kHz TO 500kHz



GUARDING AND SHIELDING

In applications where the input is at high impedance, careful shielding is required to prevent hum pickup from power line sources or detection of RF from radio stations and nearby radar

transmitters. Loss of accuracy can also occur from surface and bulk leakages in printed circuit boards. Both of these conditions can be avoided by the following methods.

Hum and RF pickup are eliminated or reduced by keeping all high impedance leads, including feedback resistor leads, inside shielded enclosures. In addition to shielding, power supply lines should be bypassed where they pass through the shielding. This will prevent noise from being retransmitted from the power supply lines inside the shielded enclosure.

Noise can also be created by the flexing of coax cable. These signals can be caused by mechanical vibrations inside or outside the shielding. Prevention consists of securely supporting all high-impedance shielded lines to prevent motion.

Printed circuit board leakage currents can easily exceed the OP-41 bias currents or the incoming signal. Leakage currents can be minimized by using Teflon insulators to support wires instead of using PC traces. An alternate method is guarding the high impedance traces. When the OP-41 is in the inverting mode, the signal traces should have grounded guard traces on both sides, Figure 8. The opposite side of the board should be used as a ground plane and shield, if not otherwise used. A ground plane is implemented by leaving copper on all areas that are not being used for signal or power conduction. Ground connection should be made to all areas of isolated copper. In the noninverting configuration, the OP-41's output signal or a portion of it should be used to drive the guard traces, Figure 9. When the guard drive voltage is equal to the input signal, leakage currents will be effectively eliminated.

FIGURE 8: CURRENT-TO-VOLTAGE CONVERTER

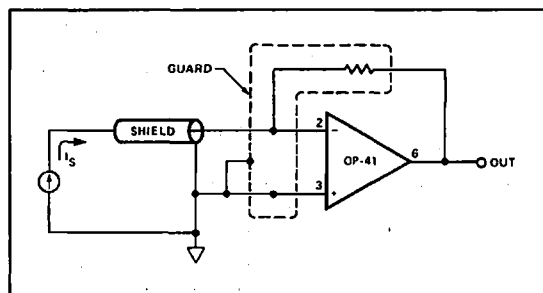
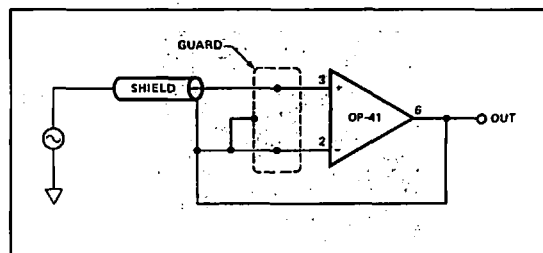
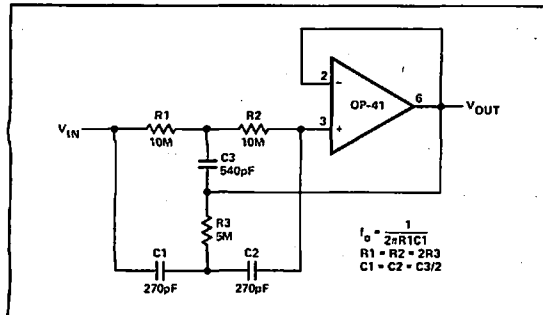


FIGURE 9: VERY HIGH IMPEDANCE NONINVERTING AMPLIFIER



The High Q Notch Filter benefits from the low bias current and high input impedance of the OP-41, Figure 10. These features enable small value capacitors and large resistors to be used in this 60Hz notch filter. The 5pA bias current only develops 100μV across R1 and R2.

FIGURE 10: HIGH Q NOTCH FILTER



Low power consumption, low bias current, and low offset voltage make the OP-41 an ideal current-to-voltage converter, Figure 11.

In this application, the PM-7541 and the OP-41 provide complete 12-bit digital-to-analog conversion with less than 3mA supply current.

FIGURE 11: DAC CIRCUIT USING THE OP-41

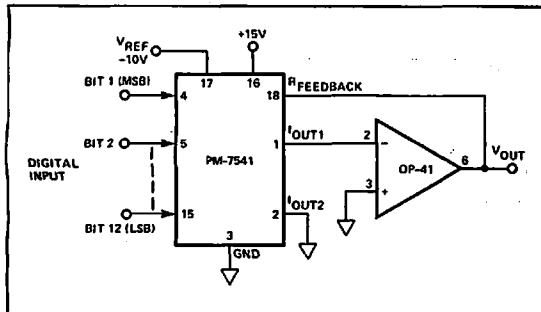
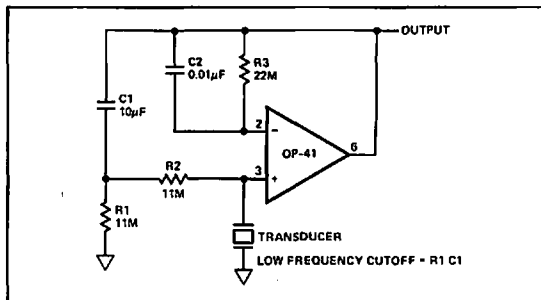


Figure 12 shows an amplifier for high-impedance ac transducers like a piezoelectric accelerometer. These sensors normally require a high-input-resistance amplifier. The OP-41 can provide input resistance in the range of $10^{12}\Omega$, however, a dc return for bias current is needed. To maintain a high R_{IN} , large value resistors above 22MΩ are often required. These may not be practicable.

Using the circuit in Figure 12, input resistances that are orders of magnitude greater than the values of the dc return resistors can be obtained. This is accomplished by bootstrapping the resistors to the output. With this arrangement, the lower cutoff frequency is determined more by the RC product of R1 and C1 than it is by resistor values and the equivalent capacitance of the transducer.

FIGURE 12: AMPLIFIER FOR PIEZOELECTRIC TRANSDUCERS



WIDE RANGE LOW-CURRENT AMMETER

The circuit shown in Figure 13 can measure currents from 100pA to 100μA without the use of high value resistors. Accuracy is better than 1% over most of the range, depending upon the accuracy of the divider resistor and the input bias current of the op amp. Using the OP-41 as the input amplifier allows low end measurement down to a few pA due to the 3.5pA input bias current.

One of the requirements for a good current meter is low series voltage drop. Since the voltage across the inputs of an op amp is forced to virtually zero, it makes a good choice for the input of a current meter. Amplifier A1 is used as an inverting amplifier for the input. This ensures less than 500μV drop at any current level.

Feedback around the op amp is accomplished with a transistor, rather than a resistor. The op amp forces the collector current of Q1A to equal the input current. This causes the emitter-base voltage of Q1A to be proportional to the log of the input current. Resistors R1, R2, R3 and capacitors C1, C2 frequency compensate the log circuit since Q1A provides gain in the feedback loop.

The output of the log amplifier is taken from the emitter of Q1A to drive Q1B. Q1B anti-logs the output and drives the meter. The output of Q1B is proportional to the log of the input current scaled by a constant, which is proportional to the voltage from the divider, selected by S1. For transistors operating at different current levels, the V_{be} difference equals:

$$\Delta V_{be} = \frac{kT}{q} \ln \frac{IC2}{IC1}$$

solving for IC2

$$IC2 = IC1 e^{\left(\frac{\Delta V_{be} q}{kT}\right)}$$

Where IC1 and IC2 are the collector currents of Q1A and Q1B; Q is the charge of an electron; k is Boltzmann's constant; T is temperature in degrees Kelvin; and V_{be} is the voltage applied to the base of Q1B. If V_{be} varies as absolute temperature, the exponent will be a constant.

[illegible]

Figure 14 is the test circuit used to measure the settling time. This circuit uses the "false sum-node" technique. When the system is initially set up, the 200 Ω pot is adjusted until the DC output voltage to the scope is unchanged when the input is changed from +10V to -10V. The 2N4416 FET buffer isolates the sum node from the scope probe load capacitance. The pulse generator must be properly terminated and have ringing below the expected error signal. (2.5mV in a 5V pulse for 0.1% overshoot measurement.)

The circuit diagram shows a differential amplifier with a DUT in the feedback loop. The non-inverting input (pin 3) is connected to ground. The inverting input (pin 2) is connected to a voltage divider consisting of a 4.99kΩ 1% resistor and a 200Ω resistor. The output (pin 6) is connected to the DUT, which is also connected to the inverting input (pin 2) via a 4.99kΩ 1% resistor. The DUT is also connected to ground via a 4.99kΩ 1% resistor. The output (pin 6) is connected to a load resistor of 4.99kΩ 1% and a 0.1μF capacitor to ground. The input signal V_{IN} is applied to the non-inverting input (pin 3) through a 1kΩ resistor. The circuit is powered by +15V and -15V supplies.



OP-42

HIGH-SPEED, FAST-SETTLING PRECISION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

Fast

- **Slew Rate** 50V/ μ s Min
- **Settling-Time (0.01%)** 1 μ s Max
- **Gain-Bandwidth Product** 10MHz Typ

Precise

- **Common-Mode Rejection** 88dB Min
- **Open-Loop Gain** 500V/mV Min
- **Offset Voltage** 750 μ V Max
- **Bias Current** 200pA Max

Excellent Radiation Hardness

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	HERMETIC LCC 20-PIN	
1.0	OP42AJ*	OP42AZ*	OP42ARC/883	MIL
0.75	OP42EJ	OP42EZ	—	IND
1.5	OP42FJ	OP42FZ	—	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

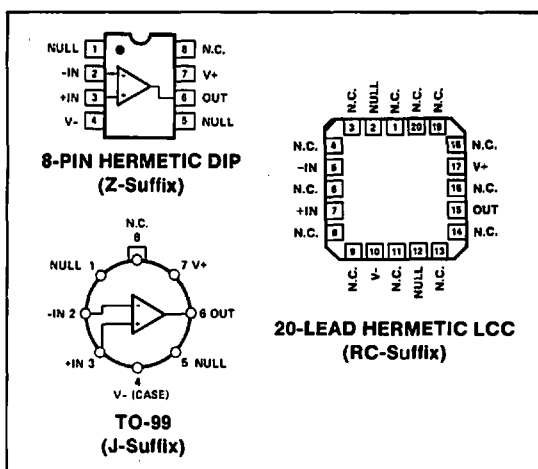
GENERAL DESCRIPTION

The OP-42 is a fast precision JFET-input operational amplifier. Similar in speed to PMI's OP-17, the OP-42 offers a symmetric 58V/ μ s slew rate and is internally compensated for unity-gain operation. OP-42 speed is achieved with a supply current of less than 6mA. Unity-gain stability, a wide

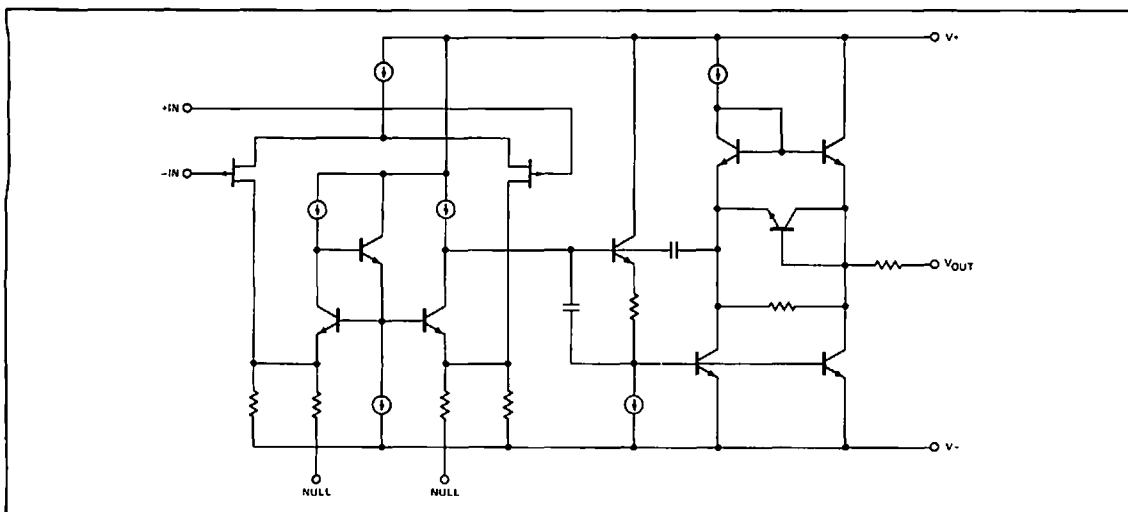
full-power bandwidth of 900kHz, and a fast settling-time of 800ns to 0.01% make the OP-42 an ideal output amplifier for fast digital-to-analog converters.

Equal attention was given to both speed and precision in the OP-42 design. Its tight 750 μ V maximum input offset voltage combined with well-controlled drift of less than 10 μ V/°C eliminates the need for external nulling in many circuits. The OP-42's common-mode rejection of 88dB minimum over a $\pm$ 11V input voltage range is exceptional for a high-speed amplifier. High CMR combined with a minimum 500V/mV

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





gain into 10k Ω load ensure excellent linearity in both non-inverting and inverting gain configurations. The low input bias and offset currents provided by the JFET input stage suit the OP-42 for use in high-speed sample and hold circuits, peak detectors, and log amplifiers. Excellent radiation hardness characteristics make the OP-42 ideal for military and aerospace applications.

The OP-42 conforms to the standard 741 pinout with nulling to V-. The OP-42 upgrades the performance of circuits using the AD544, AD611, AD711, and LF400 by direct replacement. In circuits without nulling, the OP-42 offers an upgrade for designs using the OP-16, OP-17, LT1022, LT1056, and HA2510.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	$\pm 20V$
Internal Power Dissipation (Note 3)	500mW
Input Voltage (Note 2)	$\pm 20V$
Differential Input Voltage (Note 2)	40V

Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to 175°C
Operating Temperature Range	
OP42A (J,Z)	-55°C to +125°C
OP42E,F (J,Z)	-25°C to +85°C
Junction Temperature	-65°C to 175°C
Lead Temperature Range (Soldering, 60 sec.)	300°C

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than $\pm 20V$, the absolute maximum input voltage is equal to the supply voltage.
3. See table for maximum ambient temperature rating and derating factor.

PACKAGE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	OPERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
Hermetic 8-Pin DIP (Z)	75°C	6.7mW/°C
Hermetic 20-Lead LCC (RC)	72°C	7.8mW/°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-42E			OP-42F			OP-42A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	0.3	0.75	—	0.4	1.5	—	0.3	1.0	mV
Input Bias Current	I_B	$V_{CM} = 0V$ $T_J = 25^\circ C$	—	80	200	—	130	250	—	80	200	pA
Input Offset Current	I_{OS}	$V_{CM} = 0V$ $T_J = 25^\circ C$	—	4	40	—	6	50	—	4	40	pA
Input Voltage Range	IVR	(Note 1)	± 11	+12.5 -12.0	—	± 11	+12.5 -12.0	—	± 11	+12.5 -12.0	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	88	98	—	80	92	—	86	96	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	9	40	—	12	50	—	9	40	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ $V_O = \pm 10V$	500	900	—	500	900	—	500	900	—	V/mV
		$R_L = 2k\Omega$ $T_J = 25^\circ C$	200	260	—	200	260	—	200	260	—	
		$R_L = 1k\Omega$	100	170	—	100	170	—	100	170	—	
Output Voltage Swing	V_O	$R_L = 1k\Omega$	± 11.5	+12.5 -11.9	—	± 11.5	+12.5 -11.9	—	± 11.5	+12.5 -11.9	—	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	± 20	+33 -28	± 60	± 20	+33 -28	± 60	± 20	+33 -28	± 60	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	—	5.1	6.0	—	5.1	6.5	—	5.1	6.0	mA
Slew Rate	SR		50	58	—	40	50	—	45	52	—	V/ μs
Full-Power Bandwidth	BW_P	(Note 2)	750	900	—	600	800	—	700	850	—	kHz
Gain-Bandwidth Product	GBW	$f_O = 10kHz$	—	10	—	—	10	—	—	10	—	MHz
Settling-Time	t_s	10V Step 0.01% (Note 3)	—	0.8	1.0	—	0.9	1.2	—	0.8	1.0	μs
Overload Recovery Time	t_{OR}		—	700	—	—	700	—	—	700	—	ns
Phase Margin	ϕ_0	0dB Gain	—	47	—	—	47	—	—	47	—	degrees
Gain Margin	A_{180}	180° Open-Loop Phase Shift	—	9	—	—	9	—	—	9	—	dB
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 4)	100	300	—	100	300	—	100	300	—	pF

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-42E			OP-42F			OP-42A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input Impedance	Z_{IN}		—	$10^{12} \parallel 6$	—	—	$10^{12} \parallel 6$	—	—	$10^{12} \parallel 6$	—	$\Omega \parallel pF$
Open-Loop Output Resistance	R_O		—	50	—	—	50	—	—	50	—	Ω
Voltage Noise	$e_{n\ p-p}$	0.1Hz to 10Hz	—	2	—	—	2	—	—	2	—	μV_{p-p}
Voltage Noise Density	e_n	$f_O = 10Hz$	—	38	—	—	38	—	—	38	—	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	16	—	—	16	—	—	16	—	
		$f_O = 1kHz$	—	13	—	—	13	—	—	13	—	
		$f_O = 10kHz$	—	12	—	—	12	—	—	12	—	
Current Noise Density	i_n	$f_O = 1kHz$	—	0.007	—	—	0.007	—	—	0.007	—	$pA/\sqrt{Hz}$
External V_{OS} Trim Range	R_{pot}	$20k\Omega$	—	4	—	—	4	—	—	4	—	mV
Long-Term V_{OS} Drift			—	5	—	—	5	—	—	5	—	$\mu V/month$
Supply Voltage Range	V_S		± 8	± 15	± 20	± 8	± 15	± 20	± 8	± 15	± 20	V

NOTES:

1. Guaranteed by CMR test.
2. Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{PEAK})$.

3. Settling-time is sample tested for A and E grades. Test circuit is shown in Figure 4. Settling-time for F grade is guaranteed but not tested.
4. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$ for E/F grades, and $-55^\circ C \leq T_A \leq 125^\circ C$ for A grade, unless otherwise noted.

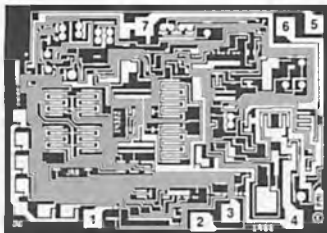
PARAMETER	SYMBOL	CONDITIONS	OP-42E			OP-42F			OP-42A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	0.4	1.2	—	0.6	2.5	—	0.5	2.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		—	4	10	—	8	—	—	4	10	$\mu V/^\circ C$
Input Bias Current	I_B	(Note 1)	—	0.5	1.2	—	0.6	2.0	—	6	20	nA
Input Offset Current	I_{OS}	(Note 1)	—	0.05	0.2	—	0.06	0.4	—	0.2	1.0	nA
Input Voltage Range	IVR	(Note 2)	± 11	$+12.5$ -12.0	—	± 11	$+12.5$ -12.0	—	± 11	$+12.5$ -12.0	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	86	96	—	80	94	—	80	94	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	2	40	—	6	50	—	10	50	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$ (Note 1)	200	500	—	200	500	—	160	350	—	V/mV
		$R_L = 2k\Omega$ $V_O = \pm 10V$	100	160	—	100	160	—	80	110	—	
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 11.0	$+12.3$ -11.8	—	± 11.0	$+12.3$ -11.8	—	± 11.0	$+12.3$ -11.8	—	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	± 8	—	± 60	± 8	—	± 60	± 8	—	± 60	mA
Supply Current	I_{SV}	No Load $V_O = 0V$	—	5.1	6.0	—	5.1	6.5	—	5.1	6.0	mA
Slew Rate	SR	$R_L = 2k\Omega$	45	57	—	40	50	—	40	52	—	$V/\mu s$
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 3)	100	250	—	100	250	—	100	250	—	pF

NOTES:

1. $T_J = 85^\circ C$ for E/F Grades; $T_J = 125^\circ C$ for A grade.
2. Guaranteed by CMR test.
3. Guaranteed but not tested.



DICE CHARACTERISTICS



DIE SIZE 0.098×0.070 inch, 6860 sq. mils
(2.49×1.78 mm, 4.43 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_j = 25^\circ C$, unless otherwise noted.

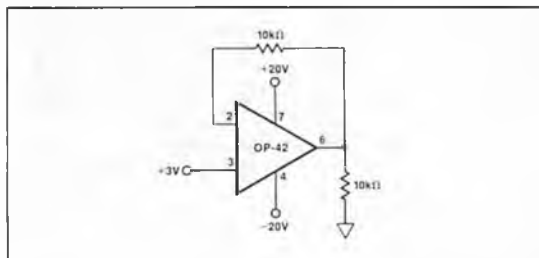
PARAMETER	SYMBOL	CONDITIONS	OP-42N LIMIT	UNITS
Offset Voltage	V_{OS}		1.5	mV MAX
Input Bias Current	I_B	$V_{CM} = 0V$	250	pA MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	50	pA MAX
Input Voltage Range	IVR	(Note 1)	± 11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	80	dB MIN
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	50	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$	500	V/mV MIN
		$R_L = 2k\Omega$	200	
		$R_L = 1k\Omega$	100	
Output Voltage Swing	V_O	$R_L = 1k\Omega$	± 11.5	V MIN
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	$\pm 20/\pm 60$	mA MIN/MAX
Supply Current	I_{SY}	No Load $V_O = 0V$	6.5	mA MAX
Slew Rate	SR		40	V/ μs MIN
Capacitive Load Drive Capability	C_L	Unity-Gain Stable (Note 2)	100	pF MIN

NOTES:

1. Guaranteed by CMR test.
2. Guaranteed but not tested.

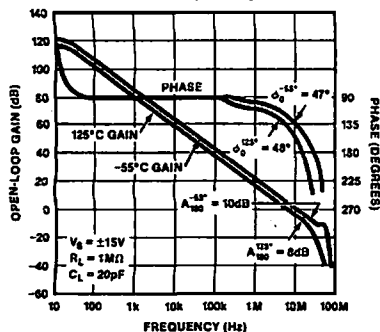
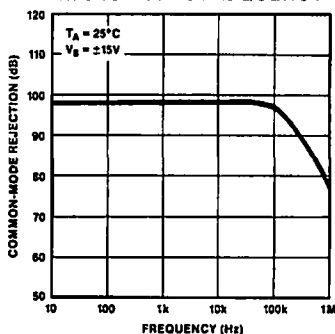
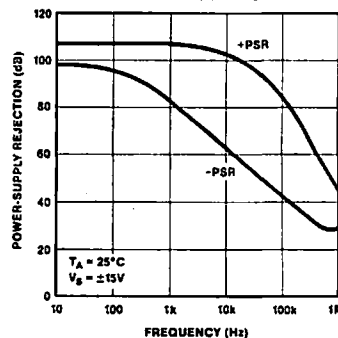
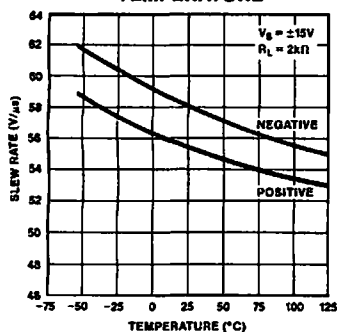
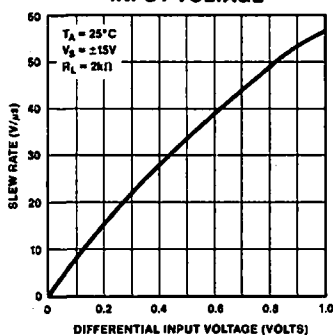
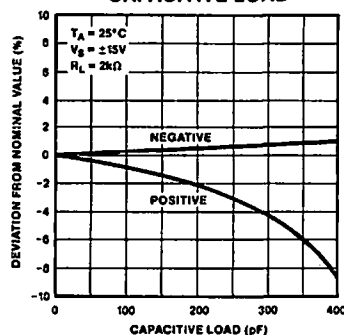
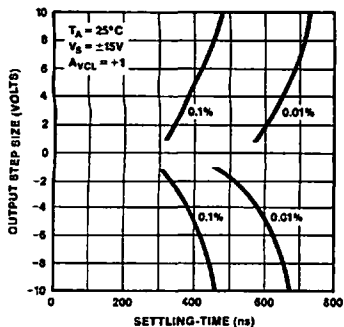
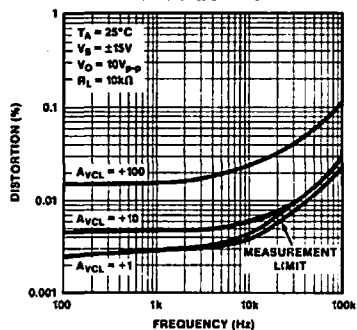
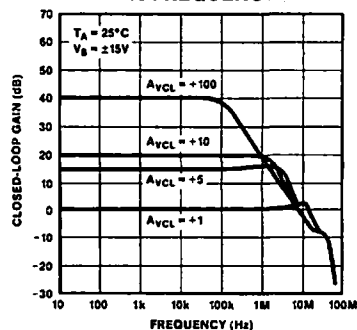
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

BURN-IN CIRCUIT



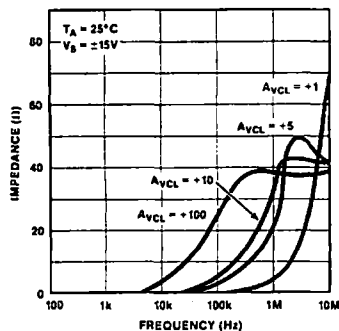
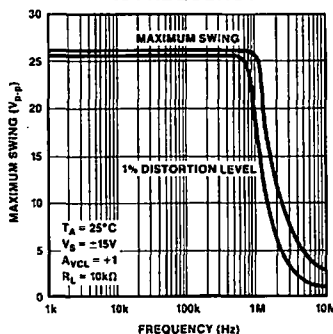
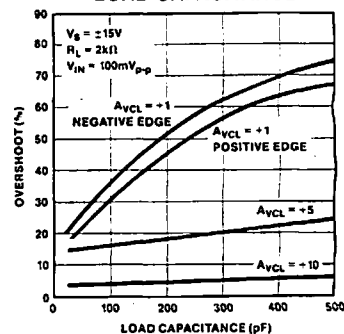
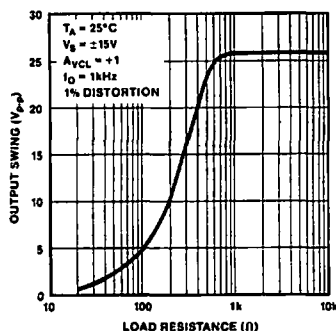
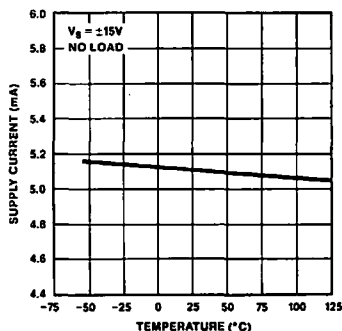
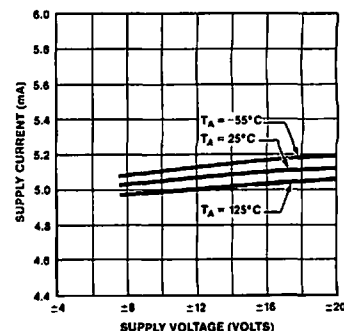
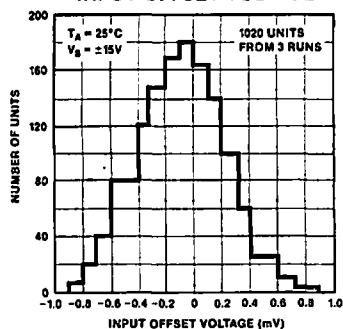
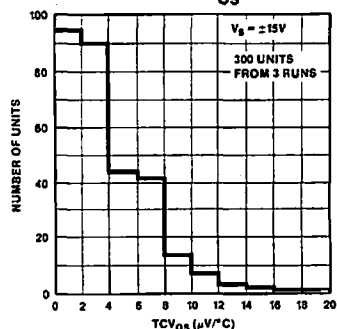
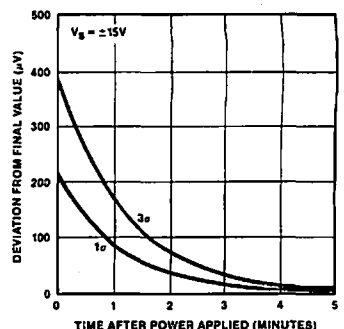


TYPICAL PERFORMANCE CHARACTERISTICS

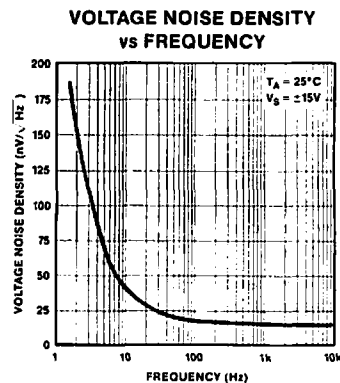
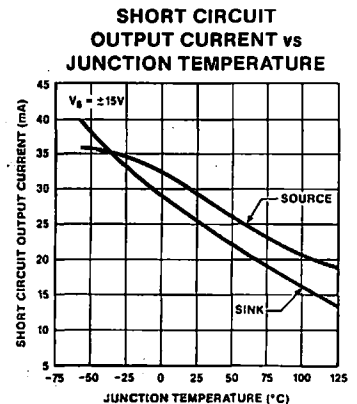
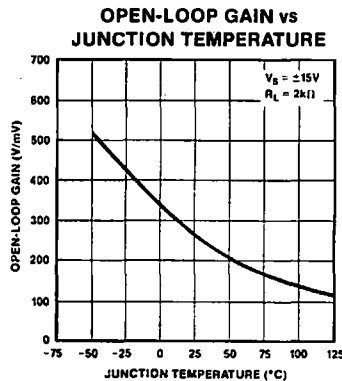
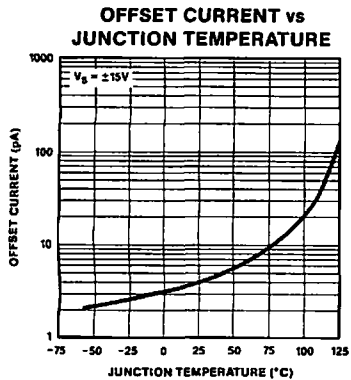
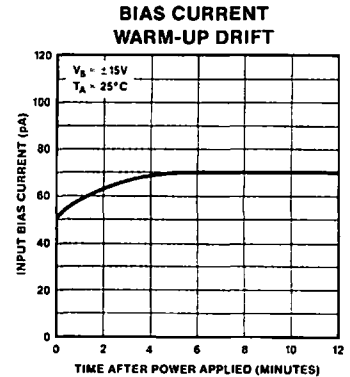
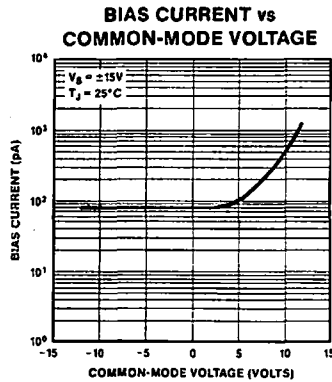
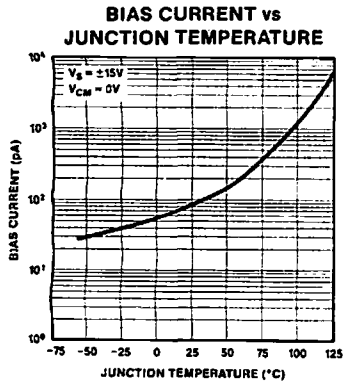
OPEN-LOOP GAIN, PHASE
vs FREQUENCYCOMMON-MODE
REJECTION vs FREQUENCYPOWER-SUPPLY REJECTION
vs FREQUENCYSLEW RATE vs
TEMPERATURESLEW RATE vs
DIFFERENTIAL
INPUT VOLTAGESLEW RATE vs
CAPACITIVE LOADSETTLING-TIME
vs STEP SIZEDISTORTION
vs FREQUENCYCLOSED-LOOP GAIN
vs FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS

CLOSED-LOOP
OUTPUT IMPEDANCE
vs FREQUENCYMAXIMUM OUTPUT SWING
vs FREQUENCYSMALL-SIGNAL
OVERSHOOT vs
LOAD CAPACITANCEOUTPUT SWING vs
LOAD RESISTANCESUPPLY CURRENT
vs TEMPERATURESUPPLY CURRENT vs
SUPPLY VOLTAGETYPICAL DISTRIBUTION OF
INPUT OFFSET VOLTAGETYPICAL DISTRIBUTION
OF TCV_{OS} OFFSET VOLTAGE
WARM-UP DRIFT

TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

The OP-42 combines speed with a high level of input precision usually found only with slower devices. Well-behaved AC performance in the form of clean transient response, symmetrical slew-rates and a high degree of forgiveness to supply decoupling are the hallmarks of this amplifier. AC gain and phase response are quite independent of temperature or supply voltage. Figure 1 shows the OP-42's small-signal response. Even with 75pF loads, there is minimal ringing in the output waveform. Large-signal response is shown in Figure 2. This figure clearly shows the OP-42's exceptionally close matching between positive and negative slew-rates. Slew-rate symmetry decreases the DC offset a system encounters when processing high-frequency signals, and thus reduces the DC current necessary for load driving.

FIGURE 1: Small-Signal Transient Response,
 $Z_L = 2k\Omega || 75pF$

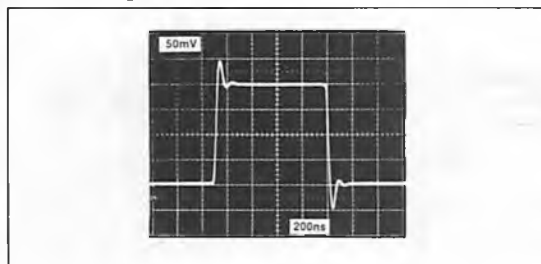
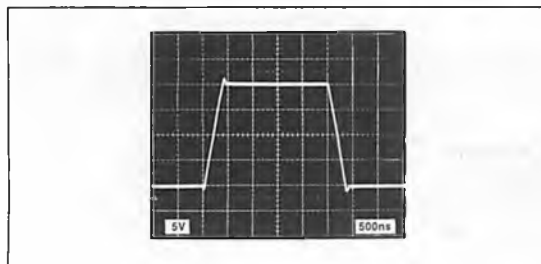


FIGURE 2: Large-Signal Transient Response,
 $Z_L = 2k\Omega || 75pF$



As with most JFET-input amplifiers, the output of the OP-42 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier.

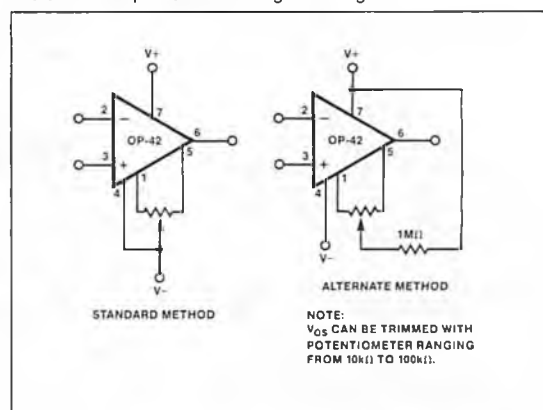
For most applications a 0.1 μ F to 0.01 μ F capacitor should be placed between each supply pin and ground.

The OP-42 displays excellent resistance to radiation. Radiation hardness data is available by contacting the factory.

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted with a 10k Ω to 100k Ω potentiometer as shown in Figure 3. The potentiometer should be connected between pins 1 and 5 with its wiper connected to the V^- supply. Nulling V_{OS} in this manner changes TCV_{OS} by no more than 5 μ V/ $^{\circ}$ C per millivolt of V_{OS} change. Alternately, V_{OS} may be nulled by attaching the potentiometer wiper through a 1M Ω resistor to the positive supply rail.

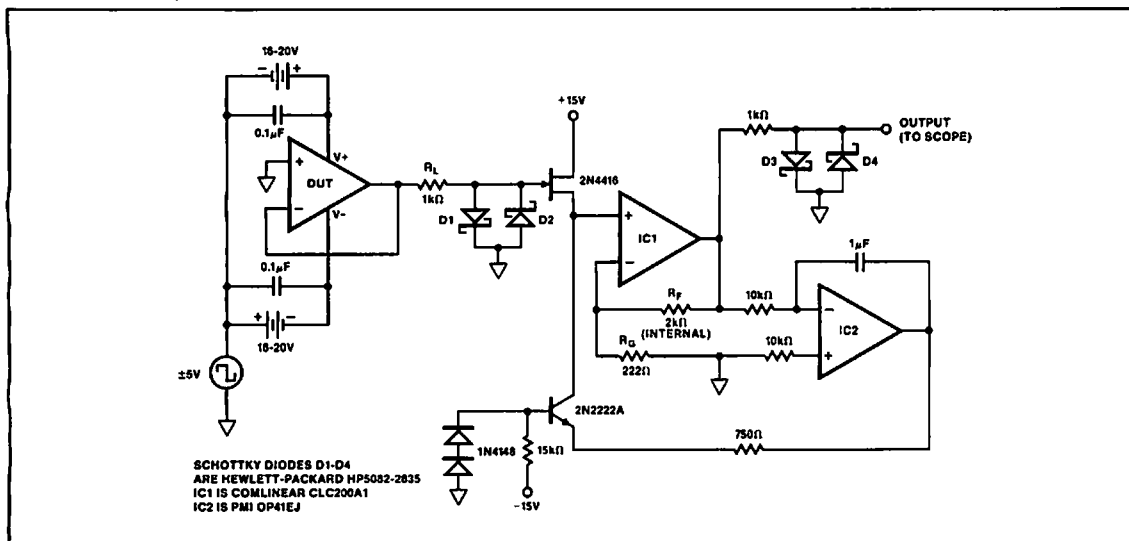
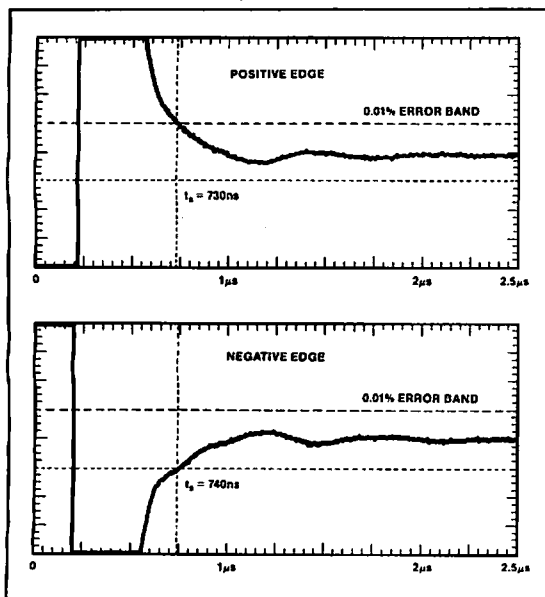
FIGURE 3: Input Offset Voltage Nulling



SETTLING-TIME

Guaranteed fast-settling is assured by sample-testing during production. The OP-42 is configured as a unity-gain follower in the test circuit of Figure 4. This test method has advantages over false-sum-node techniques in that the actual output of the amplifier is measured, instead of an error-voltage at the sum node. Common-mode settling effects are exercised in this circuit, in addition to the slew-rate and bandwidth effects measured by the false-sum-node method. A reasonably flat-top pulse is required as a stimulus.

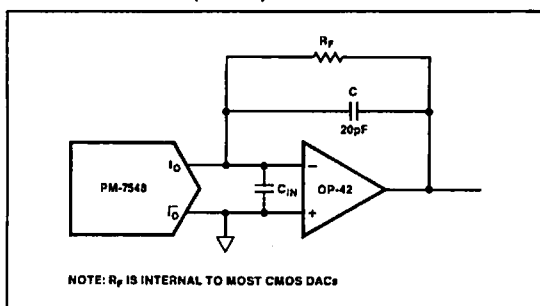
The output waveform of the OP-42 being tested is clamped by Schottky diodes and buffered by the JFET source-follower. The signal is amplified by a factor of ten by the fast amplifier IC1, then Schottky-clamped before being output. The OP-41 provides overall offset nulling. Analysis of the waveform using a digitizing oscilloscope determines the op amp's settling-time.

FIGURE 4: Settling-Time Test Fixture

FIGURE 5: OP-42 Settling-Characteristics


DAC OUTPUT AMPLIFIER

The OP-42 is an excellent choice for a DAC output amplifier, since its high speed and fast settling-time allow quick transitions between codes, even for full-scale changes in output level. The DAC output capacitance appears at the operational amplifier inputs, and must be compensated to ensure

optimal settling speed. Compensation is achieved with capacitor C in Figure 6. C must be adjusted to account for the DAC's output capacitance, the op amp's input capacitance, and any stray capacitance at the inputs. With a bipolar DAC, an additional shunt resistor may be used to optimize response. This technique is described in PMI's application note AN-24.

FIGURE 6: DAC Output Amplifier Circuit


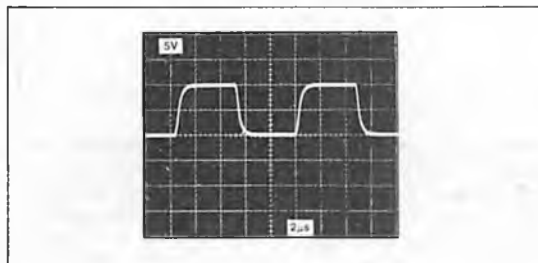
Highest speed is achieved using bipolar DACs such as PMI's DAC-08, DAC-10 or DAC-312. The output capacitances of these converters are up to an order of magnitude lower than their CMOS counterparts, resulting in substantially faster settling-times. The high output impedance of bipolar DACs allows the output amplifier to operate in a true current-to-voltage mode, with a noise gain of unity, thereby retaining the amplifier's full bandwidth. Offset voltage has minimal effect on linearity with bipolar converters.

CMOS digital-to-analog converters have higher output capacitances and lower output resistances than bipolar DACs.

This results in slower settling-times, higher sensitivity to offset voltages and a reduction in the output amplifier's bandwidth. These trade-offs must be balanced against the CMOS DAC's advantages in terms of interfacing capability, power dissipation, accuracy levels and cost. Using the internal feedback resistor which is present on most CMOS converters, the gain applied to offset voltage varies between 4/3 and 2, depending upon output code. Contributions to linearity error will be as much as $2/3V_{OS}$. In a 10-volt 12-bit system, this may add up to an additional 1/5LSB DNL with the OP-42E. Amplifier bandwidth is reduced by the same gain factor applied to offset voltage, however the OP-42's 10MHz gain-bandwidth product results in no reduction of the CMOS converter's multiplying bandwidth.

Individual DAC data-sheets should be consulted for more complete descriptions of the converters and their circuit applications.

FIGURE 7: DAC Output Amplifier Response (PM-7545 DAC)



DRIVING A HIGH-SPEED ADC

The OP-42's open-loop output resistance is approximately 50Ω . When feedback is applied around the amplifier, output resistance decreases in proportion to open-loop gain divided by closed-loop gain (A_{VOL}/A_{VCL}). Output impedance increases as open-loop gain rolls-off with frequency. High-speed analog-to-digital converters require low source impedances at high frequency. Output impedance at 1MHz is typically 5Ω for an OP-42 operating at unity-gain. If lower output impedances are required, an output buffer may be placed at the output of the OP-42.

HIGH-CURRENT OUTPUT BUFFER

The circuit in Figure 8 shows a high-current output stage for the OP-42. Output current is limited by R1 and R2. For good tracking between the output transistors Q1, Q2 and their biasing diodes D1 and D2, thermal contact must be maintained between the transistor and its associated diode. If good thermal contact is not maintained, R1 and R2 must be increased to 5-6 Ω in order to prevent thermal runaway. Using 5Ω resistors, the circuit easily drives a 75Ω load (Figure 9). Output resistance is decreased and heavier loads may be driven by decreasing R1 and R2.

Base current and biasing for Q1 and Q2 are provided by two current sources, the MAT-02 and the JFET. The $2k\Omega$ potentiometer in the JFET current source should be trimmed for optimum transient performance. The case of the MAT-02 should be connected to V_{-} and decoupled to ground with a

$0.1\mu F$ capacitor. Compensation for the OP-42's input capacitance is provided by C_C . The circuit may be operated at any gain, in the usual op amp configurations.

FIGURE 8: High-Current Output Buffer

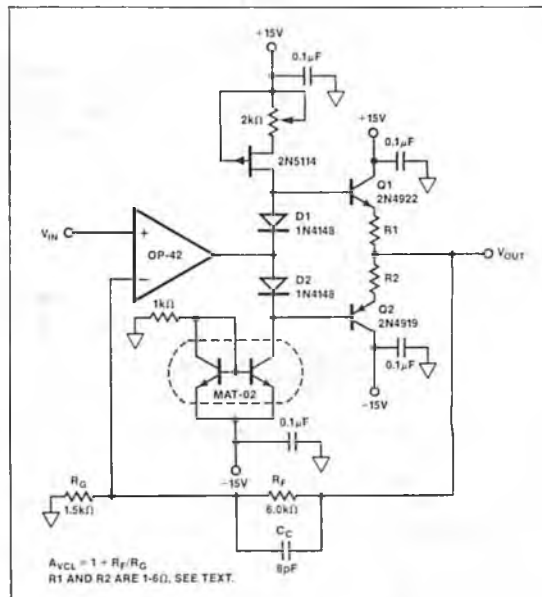
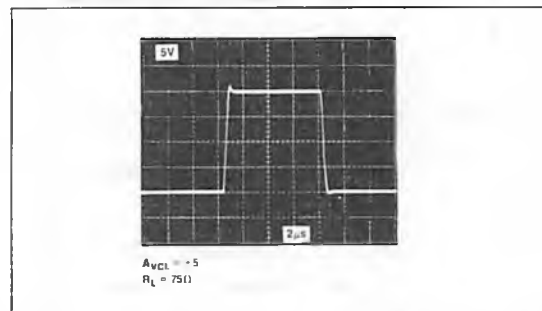


FIGURE 9: Output Buffer Large-Signal Response



DRIVING CAPACITIVE LOADS

Best performance will always be achieved by minimizing input and load capacitances around any high-speed amplifier. However, the OP-42 is guaranteed capable of driving a $100pF$ capacitive load over its full operating temperature range while operating at any gain including unity. Typically, an OP-42 will drive more than $250pF$ at any temperature. Supply decoupling does affect capacitive load driving ability. Extra care should be given to ensure good decoupling when driving capacitive loads, and a larger decoupling capacitor between $1\mu F$ and $10\mu F$ should be placed in parallel with the usual decoupling capacitor on each supply.

Large capacitive loads may be driven utilizing the circuit shown in Figure 10. R1 and C1 introduce a small amount of feedforward compensation around the amplifier to counteract the phase lag induced by the output impedance and load capacitance. At DC and low frequencies, R1 is contained within the feedback loop. At higher frequencies, feedforward compensation becomes increasingly dominant, and R1's effect on output impedance will become more noticeable.

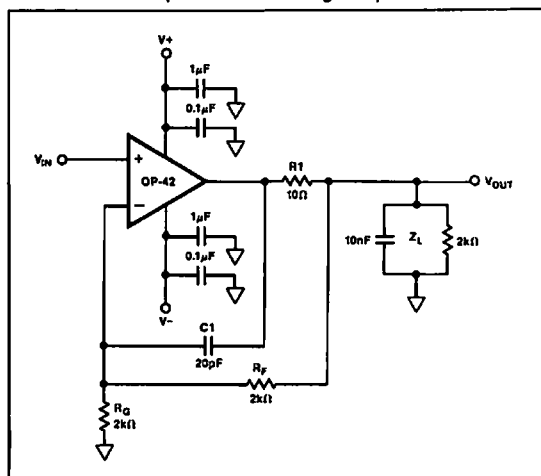
When driving very large capacitances, slew-rate will be limited by the short-circuit current limit. Although the unloaded slew-rate is insensitive to variations in temperature, the output current limit has a negative temperature coefficient, and is asymmetrical with regards to sourcing and sinking current. Therefore, slew-rate into excessive capacities will decrease with increasing temperature, and will lose symmetry.

COMPUTER SIMULATIONS

Many electronic design and analysis programs include models for op amps which calculate AC performance from the location of poles and zeros. As an aid to designers utilizing such a program, major poles and zeros of the OP-42 are listed below. Their location will vary slightly between production lots. Typically, they will be within $\pm 15\%$ of the frequency listed. Use of this data will enable the designer to evaluate gross circuit performance quickly, but should not supplant rigorous characterization of a breadboarded circuit.

POLES	ZEROS
20Hz	1MHz
300kHz	
3MHz	

FIGURE 10: Compensation for Large Capacitive Loads

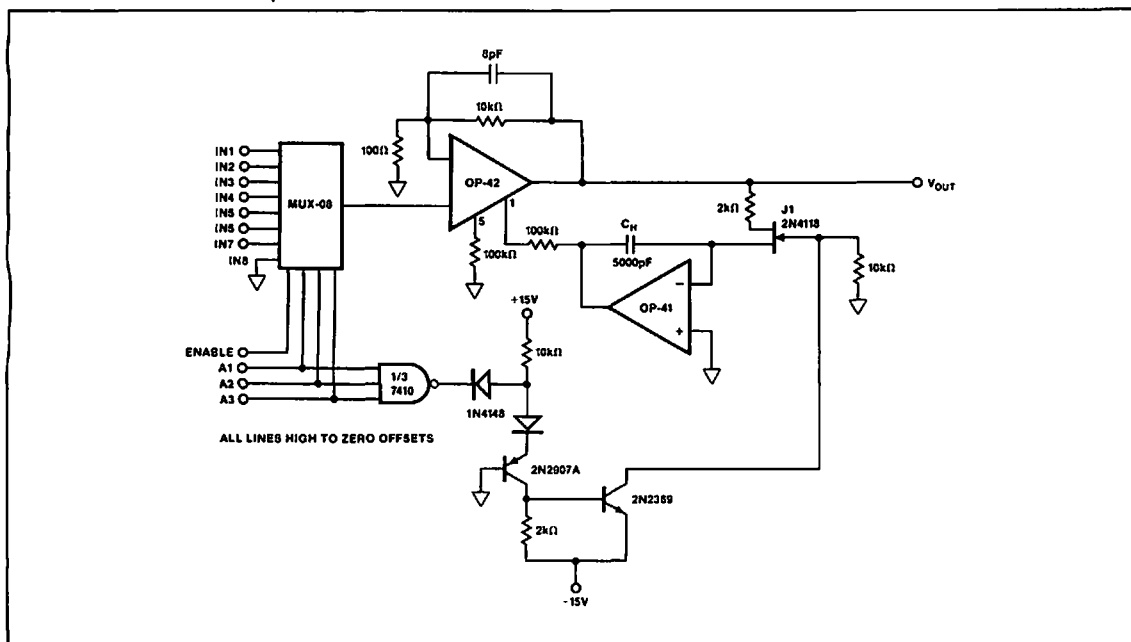


AUTOZEROING OFFSET VOLTAGE

Figure 11 describes a circuit for automatic offset voltage and drift correction. The OP-41 is used in a servo loop to force the OP-42 output equal to the OP-41's offset voltage. Thus, the OP-42's effective input offset is held below $10\mu\text{V}$ ($1\text{mV}/A_{VCL} = 100$) despite any temperature variations. This circuit will be most advantageous in high-gain applications.

Feedback is accomplished using the OP-42's null pins, leaving both inputs free for other purposes. In the application

FIGURE 11: OP-41 Servo Amplifier Provides Offset Correction





shown, the OP-42 has seven multiplexed inputs, while the eighth input provides a ground reference. Nulling is accomplished by addressing the grounded channel. This address should be held for at least 200 μ s. After this time, the address may be changed to another channel. The MUX-08 ENABLE pin must be high during the entire nulling cycle. During this time, JFET switch J1 turns on, completing feedback around

the OP-41 servo amplifier. A charge is developed across C_H to compensate for the OP-42's offset voltage. When another channel is addressed, J1 turns off, and the correction charge is maintained across C_H by the OP-41. Droop is exceptionally low — only 1.3 μ V/s at 25°C. A correction range of more than 4mV allows nulling of minor system offsets as well as the OP-42's offset voltage.

FEATURES

- Low Bias Current 5pA Max
- High Slew-Rate $\pm 5V/\mu s$ Min
- Low Current Consumption 1.0mA Max
- High Gain 1000V/mV Min
- High Common-Mode Rejection 100dB Min
- Gain-Bandwidth Product 2.4MHz Typ
- Power Bandwidth 100kHz Typ
- Fast Overload Recovery Time 3.5 μs Typ
- Low Harmonic Distortion <0.01% at 5kHz

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	PLASTIC DIP 8-PIN	
250	OP-43EJ	—	IND
750	OP-43FJ	—	IND
500	OP-43AJ*	—	MIL
1000	OP-43BJ*	—	MIL
1500	—	OP-43GP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

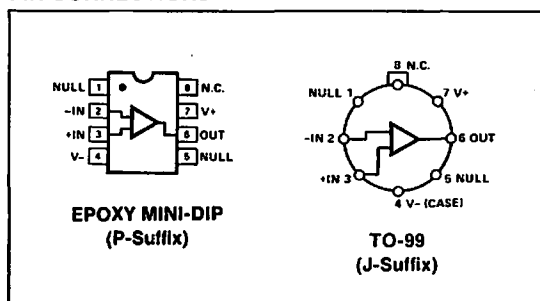
GENERAL DESCRIPTION

The OP-43 JFET operational amplifier is a high-speed version of the OP-41, featuring a slew rate of 6V/ μs , gain-bandwidth product of 2.4MHz, and power bandwidth of 100kHz. Its high

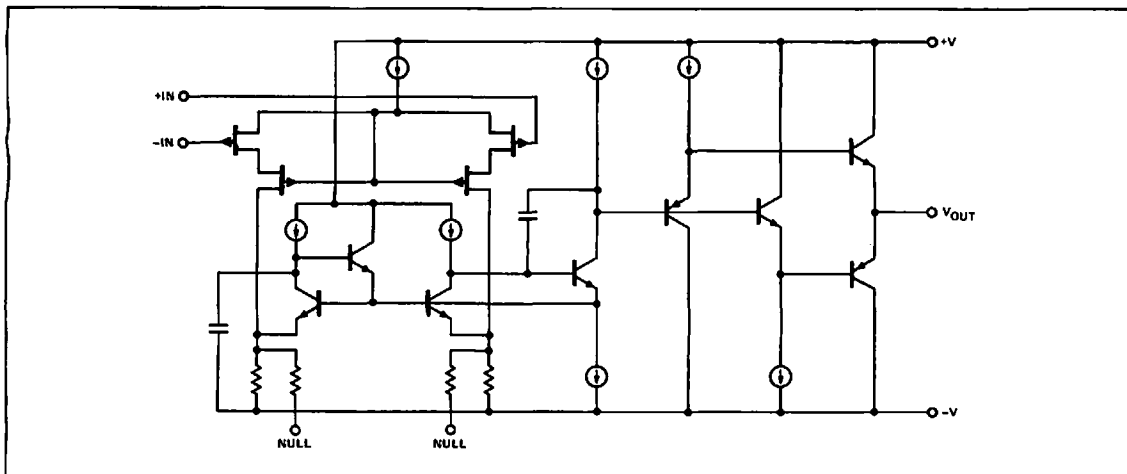
speed is achieved without compromising the low supply current, which is typically 750 μA . The OP-43 has a bias current of only 5pA, and an open-loop gain of over 1 million. Common-mode rejection is an outstanding 115dB, far beyond that available with most FET op amps. The OP-43 is guaranteed stable for unity-gain circuits with $\leq 100pF$ loads. It is ideal for price-sensitive applications requiring low power-consumption combined with high speed and high accuracy.

The cascode input stage gives the OP-43 its exceptional CMR while improving CMR linearity with changing common-mode voltage. This input stage also stabilizes the bias current over the common-mode range. With its low power-consumption and a power-supply rejection ratio of 25 $\mu V/V$, the OP-43 is an ideal choice for battery-operated systems. Using zener-zap trimming techniques, offset voltage is adjusted to below 250 μV , thus eliminating the need for external nulling in many applications. In noninverting amplifier configurations, the outstanding CMR

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





of the OP-43 insures linearity, while in high-gain configurations, linearity and accuracy are insured by the OP-43's guaranteed gain of 1 million into a $2k\Omega$ load.

The OP-43 exhibits rapid recovery from signal overload. Following saturation at the positive supply, the output recovers in only $3.5\mu s$. Recovery from saturation at the negative supply is even faster.

The combination of low offset and drift, low power, low bias current, high speed, and high gain plus the superior CMR and PSRR performance of the OP-43, makes the device suitable for a wide range of demanding applications including DAC output amplifiers. Where low power-consumption is required in battery-powered or portable instrumentation, the OP-43 permits high-gain and high-accuracy amplification along with high-speed. The low and stable bias current, combined with its high input impedance, makes it an excellent choice for interfacing with high impedance transducers or low-level current sources.

In applications where speed is not essential, and superb capacitive load driving capabilities are required, the OP-41 is recommended.

The standard "741" pin-out allows existing JFET designs and low-power bipolar designs, to be upgraded by direct replacement with the OP-43.

ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage	$\pm 18V$
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 2)	$\pm 18V$
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	$\pm 18V$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature Range	
OP-43A, B (J)	$-55^{\circ}C$ to $+125^{\circ}C$
OP-43E, F (J)	$-25^{\circ}C$ to $+85^{\circ}C$
OP-43G (P)	$0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature Range (Soldering, 60 sec)	$300^{\circ}C$
Junction Temperature	$-65^{\circ}C$ to $+150^{\circ}C$

NOTES:

- See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
T.O.-99 (J)	$80^{\circ}C$	$7.1mW/^{\circ}C$
8-Pin Plastic DIP (P)	$62^{\circ}C$	$5.6mW/^{\circ}C$

- For supply voltages less than $\pm 18V$, the absolute maximum input voltage is equal to the supply voltage.
- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-43A/E			OP-43B/F			OP-43G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}	OP-43 E/F/G OP-43 A/B	—	200	250	—	400	750	—	500	1500	μV
Offset Current	I_{OS}	(Note 1)	—	0.04	1	—	0.05	2	—	0.05	5	pA
Bias Current	I_B	(Note 1)	—	3.0	5	—	3.5	10	—	3.5	25	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	300	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12.3	± 12.6	—	± 12.0	± 12.6	—	± 11.0	± 12.6	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	0.75	1.0	—	0.75	1.2	—	0.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	± 11.0	-15.0 -11.5	—	± 11.0	$+15.0$ -11.5	—	± 11.0	$+15.0$ -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	25	—	10	80	—	10	80	$\mu V/V$
Noise Voltage Density Referred to Input	e_n	1kHz	—	32	—	—	32	—	—	32	—	$nV/\sqrt{Hz}$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 12	$+20$ -18	± 36	± 12	$+20$ -18	± 36	± 6	$+20$ -18	± 36	mA
Slew Rate	SR		5	6	—	5	6	—	5	6	—	V/ μs
Gain Bandwidth	GBW		—	2.4	—	—	2.4	—	—	2.4	—	MHz
Power Bandwidth	BW_P		—	100	—	—	100	—	—	100	—	kHz

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-43A/E			OP-43B/F			OP-43G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Settling Time	t_s	10V Step $A_V = -1$ to 0.1% to 0.01%	—	2.5	—	—	2.5	—	—	2.5	—	μs
			—	5	—	—	5	—	—	5	—	
Overload Recovery	t_{or}	Positive Going Negative Going	—	1	—	—	1	—	—	1	—	μs
			—	3.5	—	—	3.5	—	—	3.5	—	
Capacitive Load Stability	C_L	$A_V = +1$ (Note 3)	100	250	—	100	250	—	100	250	—	pF
Open-Loop Output Resistance	R_O		—	150	—	—	150	—	—	150	—	Ω
Supply Voltage	V_S	Rated Performance Derated Performance	— ± 4.5	± 15 —	— ± 18	— ± 4.5	± 15 —	— ± 18	— ± 4.5	± 15 —	— ± 18	V

NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -55^\circ C/+125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-43A			OP-43B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	400	1000	—	600	2000	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	2.5	5	—	3.5	10	$\mu V/^\circ C$
Offset Current	I_{OS}	(Note 1)	—	40	1000	—	50	2000	pA
Bias Current	I_B	(Note 1)	—	4000	7500	—	4500	15000	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12.0	± 12.5	—	± 11.5	± 12.5	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	0.75	1.2	—	0.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	± 11.0	+15.0 -11.5	—	± 11.0	+15.0 -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	105	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	40	—	10	100	$\mu V/V$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6	+12 -17	± 36	± 6	+12 -17	± 36	mA
Slew Rate	SR		5	6	—	5	6	—	V/ μs
Gain Bandwidth	GBW		—	2.4	—	—	2.4	—	MHz
Power Bandwidth	BW_P		—	100	—	—	100	—	kHz
Capacitive Load Stability	C_L	$A_V = +1$ (Note 3)	100	250	—	100	250	—	pF

NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

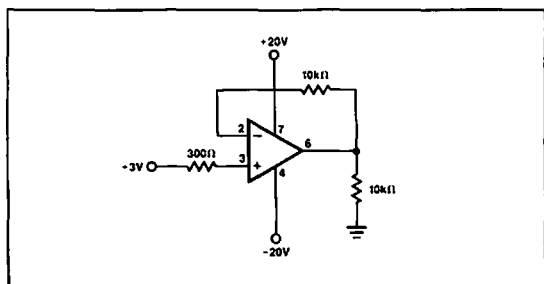


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -25^\circ C/+85^\circ C$ for E/F grades and $0^\circ C/70^\circ C$ for G grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-43E			OP-43F			OP-43G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	250	750	—	500	1750	—	500	2000	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	3.5	8	—	7.5	—	—	7.5	—	$\mu V/^\circ C$
Offset Current	I_{OS}	(Note 1)	—	5	100	—	10	200	—	20	—	pA
Bias Current	I_B	(Note 1)	—	240	500	—	300	1000	—	100	500	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	300	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12.0	± 12.6	—	± 11.5	± 12.5	—	± 11.0	± 12.6	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	0.75	1.2	—	0.75	1.2	—	0.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	± 11.0	$+15.0$ -11.5	—	± 11.0	$+15.0$ -11.5	—	± 11.0	$+15.0$ -11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	110	—	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	40	—	10	100	—	10	100	$\mu V/V$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	± 6	$+16$ -18	± 36	± 6	$+16$ -18	± 36	± 6	$+20$ -18	± 36	mA
Slew Rate	SR		5	6	—	5	6	—	5	6	—	V/ μs
Gain Bandwidth	GBW		—	2.4	—	—	2.4	—	—	2.4	—	MHz
Power Bandwidth	BW_p		—	100	—	—	100	—	—	100	—	kHz
Capacitive Load Stability	C_L	$A_V = +1$ (Note 3)	100	250	—	100	250	—	100	250	—	pF

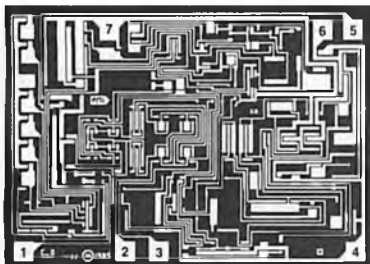
NOTES:

1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.103×0.074 inch, 7622 sq. mils
(2.62×1.88 mm, 4.92 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-43N	
			LIMIT	UNITS
Offset Voltage	V_{OS}		750	μV MAX
Bias Current	I_B	(Note 1)	20	pA MAX
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 2k\Omega$	± 12	V MIN
Supply Current	I_{SY}	$V_O = 0V$	1.2	mA MAX
Input Voltage Range	IVR	(Note 2)	± 11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	80	$\mu V/V$ MAX
Short Circuit Output Current	I_{sc}	Short Circuit to Ground	± 12	mA MIN
Slew Rate	SR		5	V/ μs MIN
Capacitive Load Stability	C_L	$A_V = +1$ (Note 3)	100	pF MIN

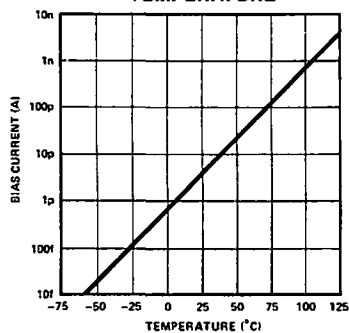
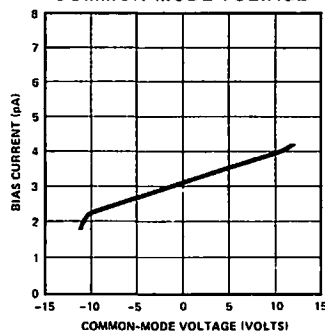
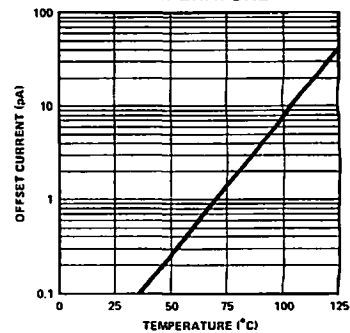
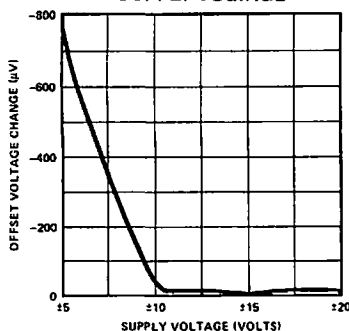
NOTES:

1. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

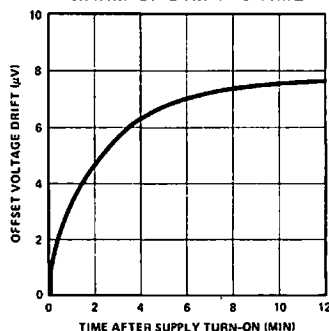
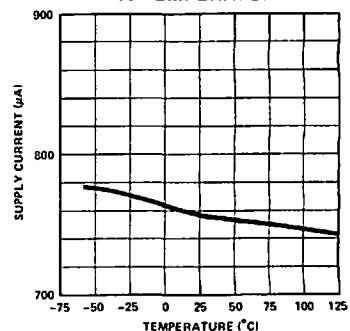
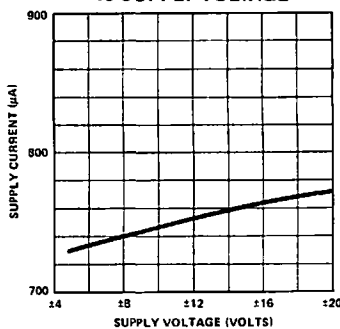
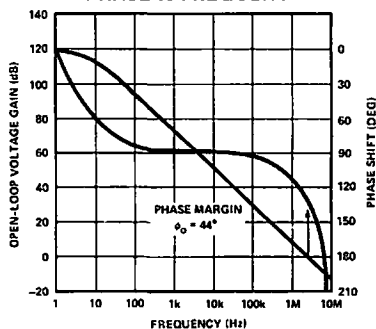
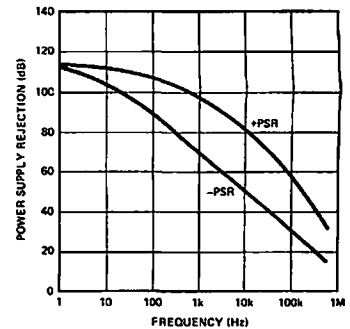
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



TYPICAL PERFORMANCE CHARACTERISTICS

BIAS CURRENT vs
TEMPERATUREBIAS CURRENT vs
COMMON-MODE VOLTAGEOFFSET CURRENT vs
TEMPERATUREOFFSET VOLTAGE vs
SUPPLY VOLTAGE

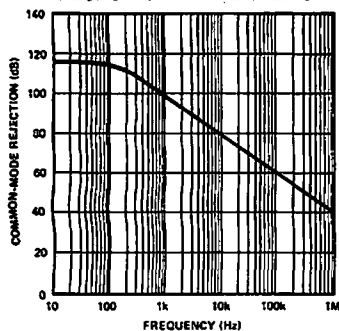
WARM-UP DRIFT vs TIME

SUPPLY CURRENT
vs TEMPERATURESUPPLY CURRENT
vs SUPPLY VOLTAGEOPEN-LOOP GAIN AND
PHASE vs FREQUENCYPOWER SUPPLY REJECTION
vs FREQUENCY

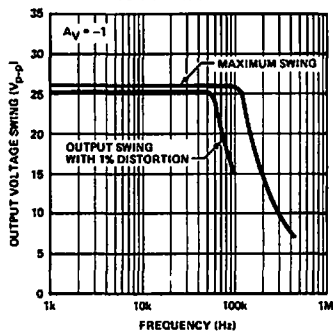


TYPICAL PERFORMANCE CHARACTERISTICS

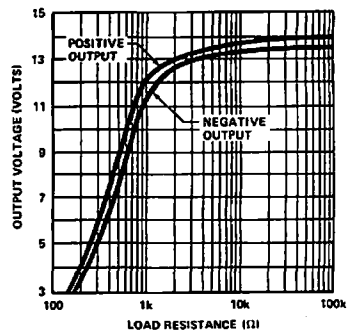
COMMON-MODE REJECTION vs FREQUENCY



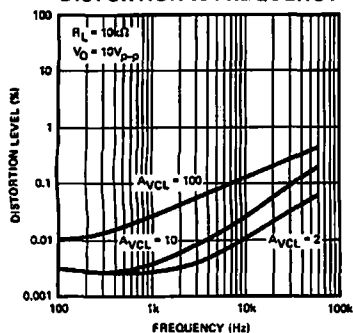
MAXIMUM OUTPUT SWING vs FREQUENCY



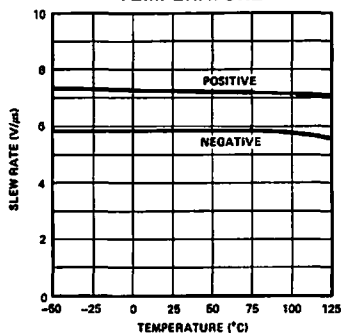
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



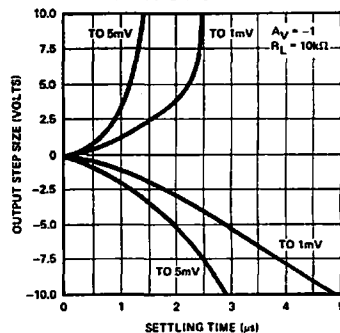
TOTAL HARMONIC DISTORTION vs FREQUENCY



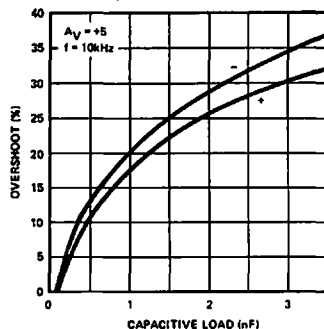
SLEW RATE vs TEMPERATURE



SETTLING TIME vs OUTPUT STEP SIZE



SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



APPLICATIONS INFORMATION

TYPICAL AC PERFORMANCE

The OP-43 is a high-speed op amp featuring a symmetrical $5V/\mu s$ minimum slew rate and a 2.4MHz gain-bandwidth product. It is guaranteed stable with a 100pF load over temperature. Typically, the OP-43 is capable of driving several hundred pF.

Figure 1 shows the OP-43's rapid overload recovery time. This is the time required for the output to return to its linear operating region, after the output saturates at each supply. Many op amps may be used in a system, and following a system overload, timing delays are necessary to allow all devices to stabilize. The fast recovery time of the OP-43 allows these delays to be much shorter, thus speeding overall system recovery. The photo also shows the well-controlled

FIGURE 1: Overload Recovery Time at $A_{VCL} = 10$

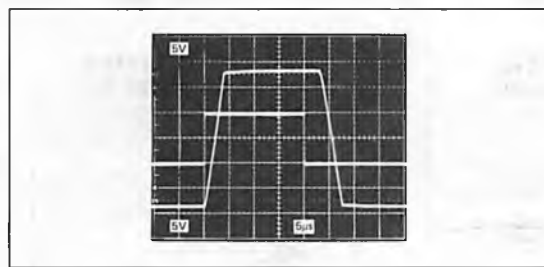


FIGURE 2: Small-Signal Transient Response at $A_{VCL} = -1$

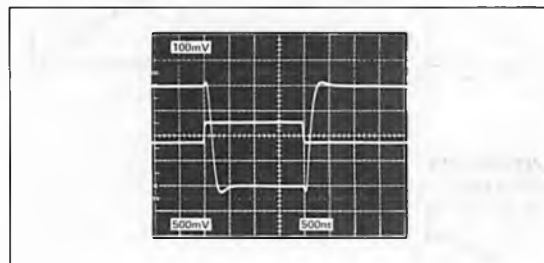
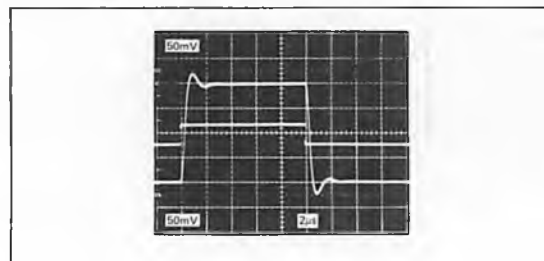


FIGURE 3: Small-Signal Transient Response at $A_{VCL} = 5$ with 1000pF Load



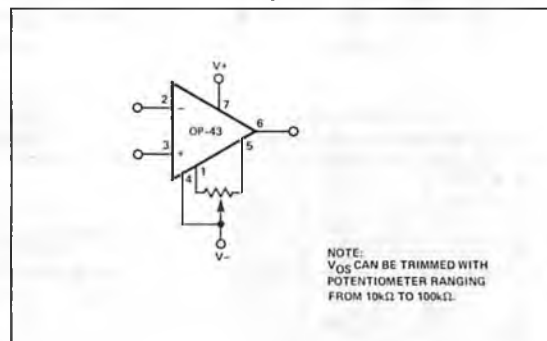
linear characteristics of the amplifier and its freedom from oscillations.

Figure 2 shows the small-signal transient response of the OP-43 with a gain of +1. When operated at higher closed-loop gains, transient response is further improved. In a gain of +5, there is essentially no overshoot with a 100pF load, and even with a 1000pF load, overshoot is minimal (Figure 3).

OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted by a potentiometer of 10k Ω to 100k Ω resistance. This potentiometer should be connected between pins 1 and 5 with the wiper connected to the V_{-} supply. (See Figure 4.) Nulling V_{OS} will change TCV_{OS} by no more than $5\mu V/^{\circ}C$ per millivolt of V_{OS} change.

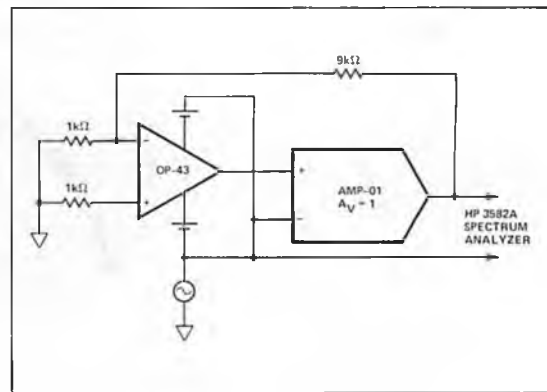
FIGURE 4: Input Offset Voltage Nulling



CMR MEASUREMENT METHODS

Two separate methods are used to measure the CMR. The first method is used over the range of 10Hz to 20kHz. This method grounds the input circuitry and applies the common-mode signal to the remainder of the op amp (Figure 5).

FIGURE 5: Circuit Used To Measure CMR
From 10Hz to 29kHz



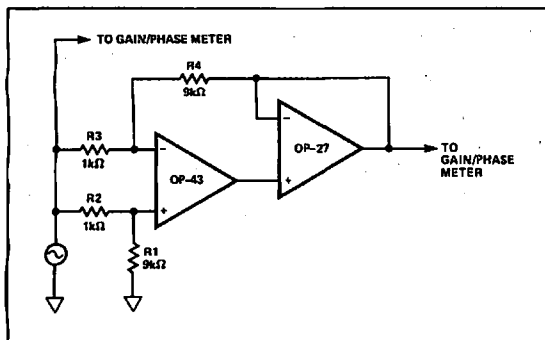
The AMP-01 eliminates loading on the output stage. This assures that the OP-41 output is not required to deliver current into the feedback circuit. The effects of the DUT open-loop gain changing with frequency are therefore significantly reduced. The circuit does not require tight resistor-matching. DC data sheet limits may be verified using this method. Circuit accuracy is dependent on the high CMR of the AMP-01.

An alternate circuit may be used to make high-frequency measurements from 2kHz to 500kHz (Figure 6). The 2kHz to 20kHz data overlap can be used to verify the accuracy of the respective test methods.

This method drives the input stage with the test signal and requires an accurate ratio of resistors, $R_4/R_3 = R_1/R_2$. To measure CMR to 100dB requires ratio matching to better than 10ppm. For this reason, it is not practical to use the second method at low frequencies where CMR is greater than 80—100dB.

Connecting the DUT directly to R_4 can cause measurement errors. If the DUT is not buffered with a broadband low-output-impedance amplifier, the frequency-dependent output impedance of the DUT, in series with R_4 , rapidly unbalances the resistor ratios. This causes frequency dependent errors. The OP-27 provides good performance over the range of frequencies used.

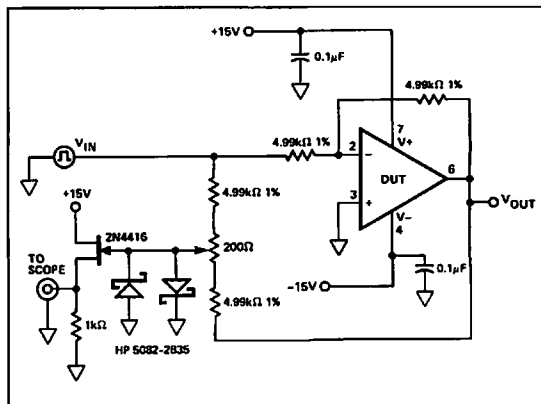
FIGURE 6: Circuit Used To Measure CMR From 2kHz to 500kHz



SETTLING-TIME MEASUREMENT

Figure 7 is the test circuit used to measure the settling time. This circuit uses the "false sum-node" technique. When the system is initially set up, the 200Ω pot is adjusted until the DC output voltage to the scope is unchanged when the input is changed from +10V to -10V. The 2N4416 FET buffer isolates the sum node from the scope probe load-capacitance. The pulse generator must be properly terminated and have ringing below the expected error signal. (2.5mV in a 5V pulse for 0.1% overshoot measurement.)

FIGURE 7: Settling-Time Test Circuit



GUARDING AND SHIELDING

High input impedances and low currents present a host of problems in a real circuit design. Unshielded high-impedance lines act as antennae, picking up line-frequency hum (50 or 60Hz) and noise from radio and television transmissions, as well as local radar installations and airports. Low currents are easily overwhelmed by leakage currents of 100pA or more existing on a clean PC board. To avoid these problems, careful attention must be paid to the physical design and layout of the circuit.

Hum and RF pickup are minimized by keeping all high-impedance leads inside shielded enclosures. Feedback and input resistors should be kept as close to the device as possible. A separate, shielded power supply should be used to prevent line noise from being retransmitted inside the shielded enclosure. Shielded cables should be used for all connections to devices outside the enclosure. These cables should be held rigid to prevent capacitively-coupled noise originating from mechanical flexing and vibration. The choice of exactly what type of cable to use depends heavily on the frequency range of interest. For high precision work, two-wire twisted-pair cable with an additional shield gives the best protection against interference and noise coupling. This type of cable will give good performance for most frequencies used with the OP-43. At frequencies above ~100kHz, however, the capacitance of this type of transmission line can seriously degrade performance. In this case, regular coaxial cable should be used.

For best results, the shield should be driven by a low impedance voltage of the same level as the input signal. This will minimize the differential voltage across the cable insulation, greatly reducing leakages and the effective input capacitance of the cable. Shielding should be connected in such a manner as to avoid ground loops. For the operating frequencies of the OP-43, this means connecting one end of the shield while the other is left free. The choice of which end is connected is dependent upon the specific application.

When the shield is grounded, and a transducer is being used which requires a ground reference, it is generally preferable to make the connection at the remote side. If the shield is being driven by the OP-43 as discussed below, the connection must be at the op amp end. Using these techniques, noise induced by electric fields can be virtually eliminated.

In a noninverting amplifier configuration, the shield may be attached to the inverting input of the op amp if the feedback voltage divider is of low impedance. Since the amplifier keeps the two inputs at the same potential, the shield will track the signal. This method is shown in Figure 8. If the shield is long, its inherent capacitance can present an excessive load on the input of the device. In this case, or if the feedback network causes the input to be a high impedance node, an OP-41 may be used as a buffer to drive the shield. (See Figure 9.) Since the OP-41 is driven by only a portion of the output signal, its slew-rate requirement is reduced. The circuit is stable with gains of 2 or more, but for optimal shielding the gain should be greater than 5. This will optimize the OP-41 buffer's ability to track the signal.

FIGURE 8: Guard Connections For Noninverting Amplifier

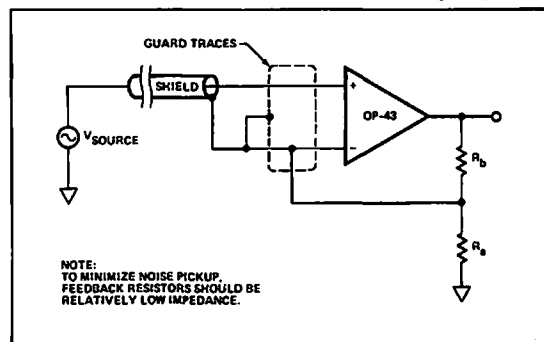
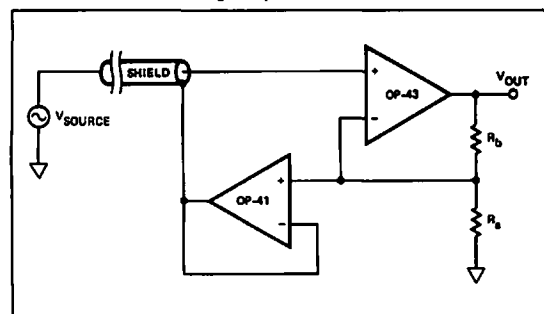


FIGURE 9: Noninverting Amplifier With Shield Driver



When the op amp is used as an inverting amplifier, it is not practical to drive the shield at the same potential as the signal, unless there are shield drivers associated with the signal source. In the case where the source lacks shield drivers, the shield is grounded.

The leakage currents on a PC board, even a clean one, can easily exceed the signals being amplified by a low-bias-current op amp. The best method of eliminating this problem is to use Teflon* insulators to support the wires and components to the inputs and feedback on the op amp. The op amp itself should be placed in a Teflon socket, if possible. This eliminates contact with the PC board for the sensitive high-impedance, low current inputs.

An alternative method is to guard all high impedance traces on the PC board. Guard traces should be placed on both sides of the PC board, around the inputs of the OP-43 and the signal traces. If the op amp is being used in the inverting mode, the guard traces should be connected to ground. In the noninverting mode, the guard traces should be driven by a portion of the OP-43's output signal, in the same manner as used with a cable shield (Figures 8, 9). Again, the idea is to minimize the differential voltages between the signal lines and the guard traces. When the guard drive voltage is equal to the input signal, leakage currents will be effectively eliminated.

CURRENT-TO-VOLTAGE CONVERSION

One of the most common applications of low-bias-current amplifiers is as a current-to-voltage converter. A wide-range photodetector is shown in Figure 10, which has excellent sensitivity and speed. It demonstrates a method of achieving higher gains without using large feedback resistors, by taking the feedback from a fraction of the output. Not only will this method reduce the noise associated with the resistors, but it allows the use of more easily obtained components. This circuit makes an excellent receiver for fiber optic uses.

ACTIVE FILTERS

The low bias current and high speed of the OP-43 make it well suited to active filter applications, allowing the use of smaller capacitors and larger resistors to obtain low frequency poles. Two configurations based upon the Sallen & Key type filters are shown in Figures 11 and 12.

For the highpass design, the cutoff frequency f_0 and quality factor Q of the filter are defined by

$$f_0 = \frac{1}{2\pi RC} \quad K = 1 + \frac{R_b}{R_a}$$

$$Q = \frac{1}{3 - K} \quad H = K$$

where K is the gain of the voltage-controlled-voltage-source (i.e. the noninverting op amp), and H is the overall gain of the filter. The transfer function of this filter is

$$\frac{V_{OUT}(\omega)}{V_{IN}(\omega)} = \frac{H(j\omega)^2}{(j\omega)^2 + j\left(\frac{\omega_0}{Q}\right)\omega + \omega_0^2}$$

where $\omega = 2\pi f$ and $j = \sqrt{-1}$.

*Teflon is a registered trademark of the Dupont Company.

FIGURE 10: Photodetector/Fiber-Optic Receiver

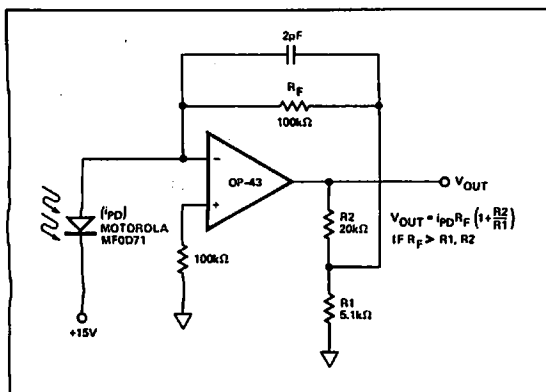


FIGURE 11: Highpass Filter

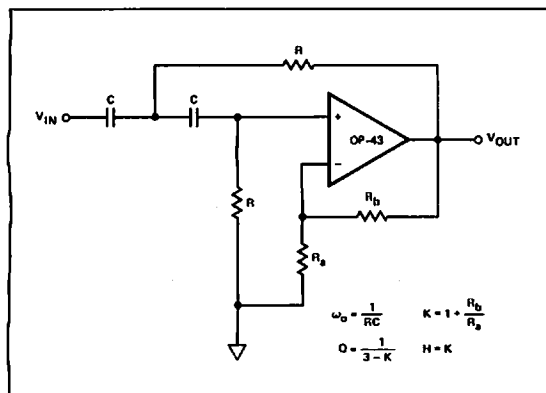
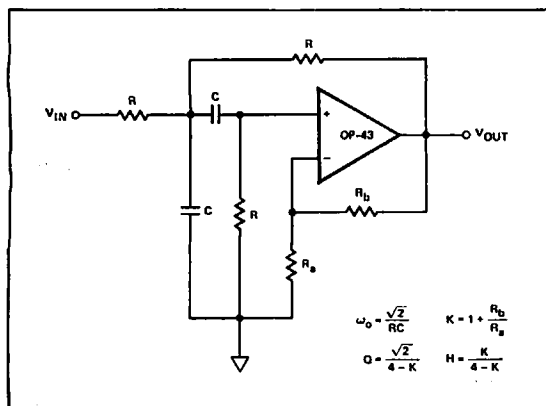


FIGURE 12: Bandpass Filter



As an example, consider a filter with a cutoff frequency of 10kHz and a Q of 5. This will give a steep rolloff with a peak at the edge of the passband. We choose 100pF as a convenient

capacitor value, then solving for R and K, we arrive at values of 158kΩ and 2.8, respectively. R_a and R_b are chosen to be 10kΩ and 18kΩ to arrive at the required gain (K) of 2.8, thus giving the desired configuration. The resultant filter displays the desired transfer function and enters a high-frequency rolloff when the op amp goes into slew-rate limiting, about 100kHz for the OP-43 with a $\pm 10V$ output swing.

The bandpass filter has a center frequency f_0 and Q defined by

$$f_0 = \frac{\sqrt{2}}{2\pi RC} \quad K = 1 + \frac{R_b}{R_a}$$

$$Q = \frac{\sqrt{2}}{4 - K} \quad H = \frac{K}{4 - K}$$

and its transfer function is

$$\frac{V_{OUT}(\omega)}{V_{IN}(\omega)} = \frac{H \left(\frac{\omega_0}{Q} \right) j\omega}{(j\omega)^2 + j \left(\frac{\omega_0}{Q} \right) \omega + \omega_0^2}$$

Several other designs are possible, with both the highpass and the bandpass filter topographies shown, using unequal values for the resistors and capacitors. For a more complete treatment, consult one of the many books available on active filters, such as **Daryanani: Principles of Active Network Synthesis and Design** (Wiley, 1976) or **Huelsenman and Allen: Introduction to the Theory and Design of Active Filters** (McGraw-Hill, 1980).

INTERFACING TO HIGH IMPEDANCE TRANSDUCERS

Because of its low bias current and very high input impedance, many high impedance transducers may be directly interfaced with the OP-43. When connecting transducers in this manner, it should be remembered that a return path for the DC bias current, no matter how small it is, must always be provided. If this is neglected, the bias current will charge stray capacitances around the input and create drift problems. With the OP-43, the drift will be significantly smaller than that found with other low-cost devices, but one must still avoid the temptation to eliminate all DC current paths.

Figure 13 shows the OP-43 as a differential amplifier with a piezoelectric pressure transducer. The common-mode rejection of this circuit is primarily dependent upon the resistor matching. A high input impedance is necessary to obtain good low-frequency response. The OP-43's low bias current allows high value resistors to be used in this low-cost circuit, giving it the required impedance. In addition, the cable shield should be grounded to prevent excessive noise pickup. The differential input impedance is

$$R_D = R_1 + R_3$$

while the gain of the circuit is

$$A_{CL} = \frac{R_2}{R_1}$$

The OP-43 is especially attractive in this application, where it allows a high-input-impedance differential amplifier to be constructed at minimal cost, while retaining the speed necessary to record transient phenomena.

Extremely high input-impedance is achieved at both inputs using the two op amp instrumentation amplifier shown in Figure 14. The input impedance is that of each OP-43. Common-mode rejection is again dependent upon matching the resistor ratios. The gain of the circuit is given by

$$A_{CL} = 2 \left(1 + \frac{R}{R_G} \right)$$

Since each device operates with a gain of 2, the common-mode range is only $\pm 5.5V$.

FIGURE 13: Differential Amplifier

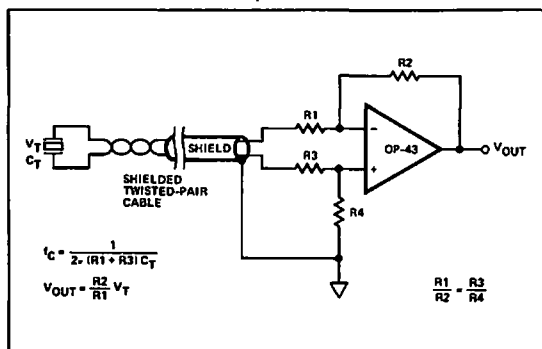
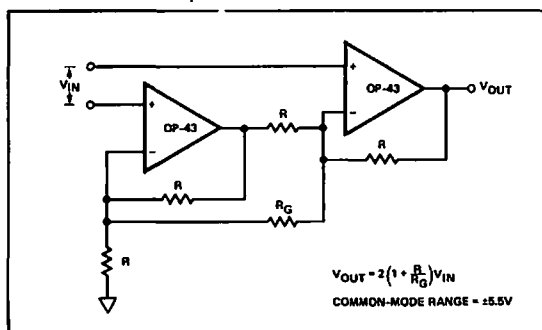


FIGURE 14: High Input-Impedance Instrumentation Amplifier



ISOLATION AMPLIFIER

In conjunction with two optocouplers, or a dual optocoupler such as the Hewlett-Packard HCPL-2530, three OP-43's can be combined to create an isolation amplifier. In this sort of amplifier, the input and the output operate on separate power supplies, allowing extremely high common-mode voltages to be dealt with. In industrial applications, an isolation amplifier protects instrumentation from high voltages at the sensing site. When interfacing with a computing system, an isolation

amplifier will protect the rest of the system from a sensor which accidentally becomes shorted to a high voltage.

The basic isolation amplifier circuit is shown in Figure 15(a). The circuit operates on the principle that the nonlinearities of one optocoupler will be tracked by the nonlinearities of another, if they are well matched. By using an optocoupler in the feedback loop of the second OP-43, the nonlinearities of the isolating optocoupler will be cancelled. The operation of the isolation amplifier can be better understood by examining the individual sections of the circuit.

Figure 15(b) shows the isolated input section of the circuit. The output of the OP-43 drives a current through LED_a. Resistor R_{3a} provides a constant bias for the LED, allowing it to operate at full speed. Since the bias current of the OP-43 is negligible, the current flowing through LED_a will be

$$I_{Fa} = \frac{V_{IN}}{R_{2a}} + \frac{V_{-2} - V_{IN}}{R_{3a}}$$

Each LED will induce a current I_C in its associated phototransistor. This current is given by

$$I_{Ca} = K_a \left[\frac{I_{Fa}}{I_{Fa}'} \right]^{n_a} \quad I_{Cb} = K_b \left[\frac{I_{Fb}}{I_{Fb}'} \right]^{n_b}$$

Thus, the current flowing through the output transistor on the a side will be

$$I_{Ca} = K_a \left[\frac{\frac{V_{IN}}{R_{2a}} + \frac{V_{-1} - V_{IN}}{R_{3a}}}{I_{Fa}'} \right]^{n_a}$$

Similarly, by analyzing the currents flowing through LED_b, we arrive at an equation for I_{Cb} , which is

$$I_{Cb} = K_b \left[\frac{\frac{V_O}{R_{2b}} + \frac{V_{-2} - V_O}{R_{3b}}}{I_{Fb}'} \right]^{n_b}$$

These currents, flowing through resistors R₄, form the input for the b side of the isolation amplifier, as shown in Figure 15(c). The feedback on the op amp through the optocoupler, forces the noninverting input to the same potential as the inverting input. Note that the output transistor in the optocoupler inverts the polarity of the signal, causing negative feedback through the noninverting input. This effectively reverses the function of the op amp's input pins. The feedback voltage on the noninverting input will be $V_{IN+} = V_{IN-}$, or $I_{Ca} R_{4a} = I_{Cb} R_{4b}$.

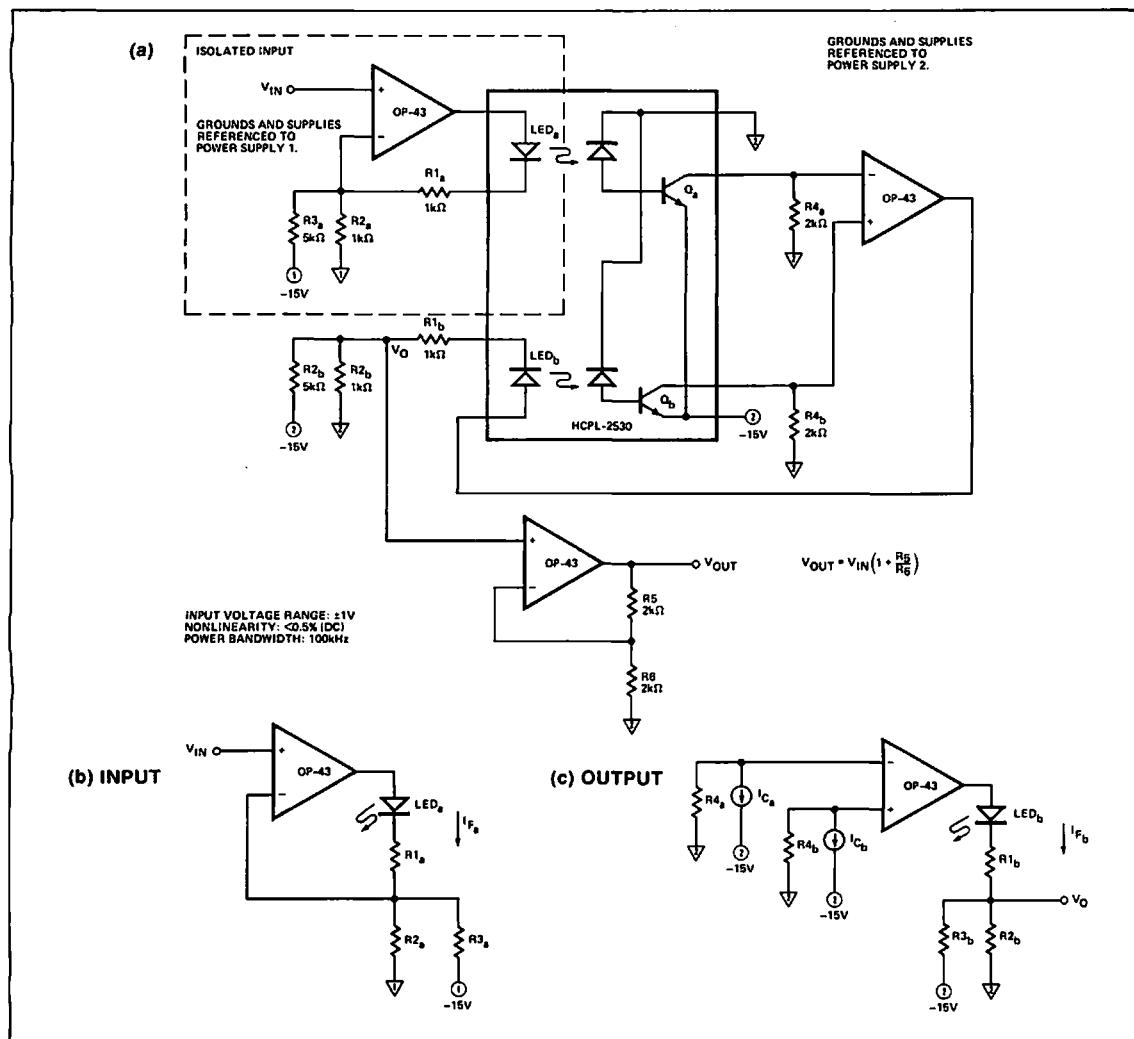
At this point, we make the assumption that the two optocouplers are well matched, i.e. their current transfer ratios K , as well as their nonlinear response defined by n and I_F' , are similar. In addition, since the LEDs are being biased directly from the power supplies, we assume that the supplies for the two sides are both stable and matched in their voltage level. Since the resistors for the a and b sides are the same values, it can be seen by inspection of the above equations for I_{Ca} and I_{Cb} that $V_O = V_{IN}$. In reality, the optocouplers are not perfectly matched, giving rise to offset and nonlinearity effects.

The last OP-43 is an output buffer for the isolation amplifier. The input to this amplifier is V_O from Figure 15(b), which was shown above to be equivalent to V_{IN} . The low bias current ensures that it does not affect the voltage it is amplifying. Gain is realized in this stage, and any offsets induced in the previous stages may be corrected by offsetting this op amp. Although shown in the circuit as a simple gain stage, this output amplifier may take any form desired. It may be configured as a filter or other waveshaping circuit as needed. The only requirement is that the buffer not disturb the currents in the optocoupler feedback circuit, thus non-inverting amplifier configurations are preferred. For highest linearity, the currents in the two LEDs should track as closely as possible.

In the circuit shown, the LEDs have been biased by resistor R3. For greater accuracy, a precision current sink of approximately 3mA could be substituted for the resistors. In addition, the collectors of the optocoupler output transistors could be connected to a more stable voltage source than the power supplies. These measures would decrease the sensitivity of the amplifier to the power supplies.

With stable supplies, the circuit has excellent response and displays less than 0.5% DC nonlinearity with a $2V_{p-p}$ signal. The high speed of the OP-43 gives the circuit a power bandwidth of 100kHz, while the majority of the power budget is consumed in biasing the LEDs. The dual optocoupler provides isolation against 600VDC common-mode voltages. Higher isolations may be achieved using two separate optocouplers, such as HP's 6N136.

FIGURE 15: Isolation Amplifier





OP-44

HIGH-SPEED, PRECISION
OPERATIONAL AMPLIFIER ($A_{VCL} \geq 3$)

Precision Monolithics Inc.

FEATURES

- Slew Rate 100V/ μ s Min
- Gain-Bandwidth Product 15MHz Min
- Common-Mode Rejection 86dB Min
- Open-Loop Gain 500V/mV Min
- Offset Voltage 750 μ V Max
- Bias Current 200pA Max
- Excellent AC CMR and PSR
- Radiation Hard

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99	HERMETIC DIP	LCC	
1.00	OP44AJ*	OP44AZ*	OP44ARC/883*	MIL
0.75	OP44EJ	OP44EZ	—	IND
1.50	OP44FJ	OP44FZ	—	IND

Plastic Mini-Dip and SOIC to be announced.

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

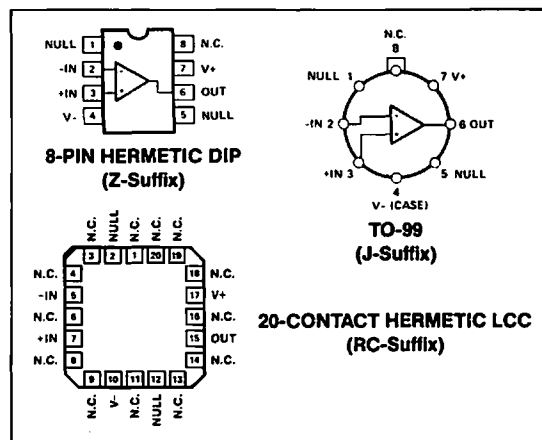
GENERAL DESCRIPTION

The OP-44 is a fast precision JFET-input operational amplifier delivering a 120V/ μ s typical slew rate in closed-loop gains of three or more. Full-power bandwidth is 2MHz for a 20V_{p-p} sine-wave, and 4MHz for a 10V_{p-p} signal. Gain-bandwidth product is typically 23MHz. Settling time to 0.1% is 200ns, and to

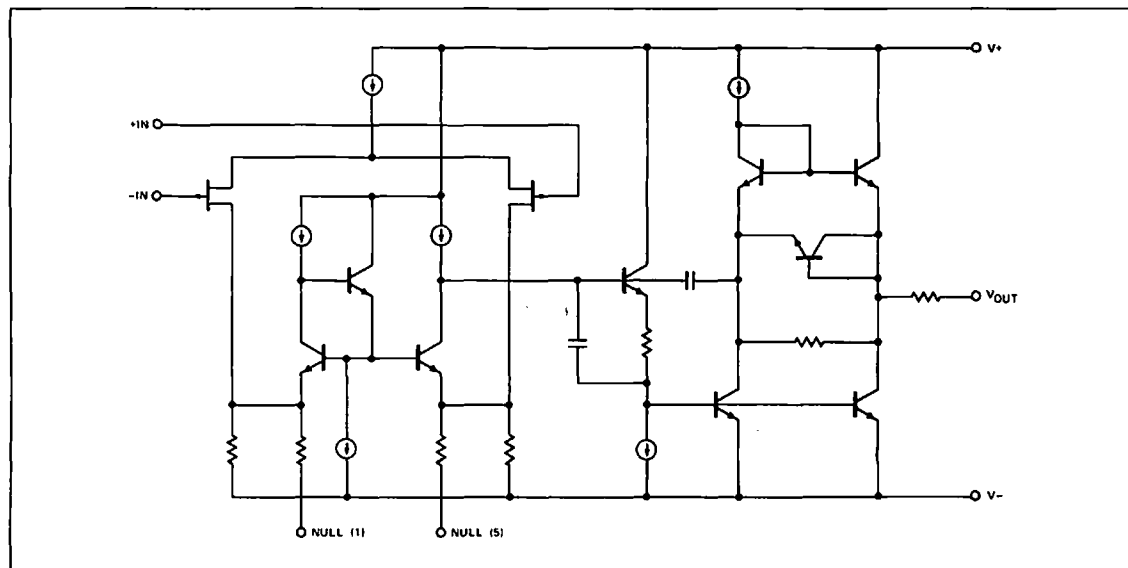
12 bits (0.01%) is 800ns, typical. Wideband noise is minimized by only 12nV/ $\sqrt{\text{Hz}}$ flatband noise.

Excellent DC precision makes the OP-44 unique among high-speed amplifiers. Offset voltage below 750 μ V and 10 μ V/ $^\circ\text{C}$ maximum drift eliminates the need for external nulling potentiometers in most applications. Common-mode rejection of 86dB minimum and an open-loop gain of 500V/mV ensures high linearity. Errors due to bias current are virtually eliminated with the OP-44's 200pA maximum input current.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





Applications for the OP-44 include data acquisition systems, pulse amplifiers, RF, IF and video amplifiers, and signal generators.

The OP-44 conforms to the standard 741 pinout with nulling to V-. It offers an excellent upgrade for circuits using the LF400 and AD509. The HA-2520/22/25 are easily upgraded by removing any external nulling components.

For a unity-gain stable amplifier sharing many of the OP-44's characteristics, consult the OP-42 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±20V
Internal Power Dissipation (Note 3)	500mW
Input Voltage (Note 2)	±20V
Differential Input Voltage (Note 2)	40V
Peak Output Current	50mA
Storage Temperature Range	-65°C to 175°C

Operating Temperature Range

OP-44A (J, Z)	-55°C to +125°C
OP-44E, F (J, Z)	-25°C to +85°C
Junction Temperature	-65°C to 175°C
Lead Temperature Range (Soldering, 60 sec)	300°C

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±20V, the absolute maximum input voltage is equal to the supply voltage.
3. See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
Hermetic 8-Pin DIP (Z)	75°C	6.7mW/°C
Hermetic 20-Contact LCC (RC)	72°C	7.8mW/°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-44E			OP-44F			OP-44A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	0.3	0.75	—	0.4	1.5	—	0.3	1.0	mV
Input Bias Current	I_B	$V_{CM} = 0V$, $T_I = 25^\circ C$	—	80	200	—	130	250	—	80	200	pA
Input Offset Current	I_{OS}	$V_{CM} = 0V$, $T_I = 25^\circ C$	—	4	40	—	6	50	—	4	40	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5 -12.0	—	±11	+12.5 -12.0	—	±11	+12.5 -12.0	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	86	96	—	80	92	—	86	96	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	9	40	—	12	50	—	9	40	μV/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$, $V_O = \pm 10V$	500	900	—	500	900	—	500	900	—	V/mV
		$R_L = 2k\Omega$, $T_I = 25^\circ C$	200	260	—	200	260	—	200	260	—	
		$R_L = 1k\Omega$	100	170	—	100	170	—	100	170	—	
Output Voltage Swing	V_O	$R_L = 1k\Omega$	±11.5	+12.5 -11.9	—	±11.5	+12.5 -11.9	—	±11.5	+12.5 -11.9	—	V
Output Current	I_{OUT}		±20	+33 -28	—	±20	+33 -28	—	±20	+33 -28	—	mA
Supply Current	I_{SV}	No Load $V_O = 0V$	—	6.5	7.5	—	6.5	7.5	—	6.5	7.5	mA
Slew Rate	SR	$R_L = 2k\Omega$ $C_L = 50pF$	100	120	—	80	100	—	100	120	—	V/μs
Full-Power Bandwidth	BW_p	$V_O = \pm 10V$ (Note 2)	1.5	2.0	—	1.2	1.6	—	1.5	2.0	—	MHz
Gain-Bandwidth Product	GBW	$A_V = 10$ (Note 3)	15	23	—	15	23	—	15	23	—	MHz
Settling Time	t_s	10V Step 0.1% (Note 4)	—	0.2	—	—	0.2	—	—	0.2	—	μs
Rise Time	t_r	$V_O = \pm 200mV$ (Note 3, 4)	—	25	50	—	25	50	—	25	50	ns
Overshoot		$V_O = \pm 200mV$ (Note 3, 4)	—	25	40	—	25	50	—	25	40	%
Overload Recovery Time	t_{OR}		—	700	—	—	700	—	—	700	—	ns
Capacitive Load Drive Capability	C_L	$A_{VCL} \geq 3$ (Note 3)	50	150	—	50	150	—	50	150	—	pF

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-44E			OP-44F			OP-44A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Resistance	R_{IN}	(Note 3)	10^8	10^{12}	—	10^8	10^{12}	—	10^8	10^{12}	—	Ω
Open-Loop Output Resistance	R_O		—	50	—	—	50	—	—	50	—	Ω
Voltage Noise	$e_{n\text{ p-p}}$	0.1Hz to 10Hz	—	2	—	—	2	—	—	2	—	$\mu V_{\text{p-p}}$
Voltage Noise Density	e_n	$f_O = 10\text{Hz}$	—	38	—	—	38	—	—	38	—	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	16	—	—	16	—	—	16	—	
		$f_O = 1\text{kHz}$	—	13	—	—	13	—	—	13	—	
		$f_O = 10\text{kHz}$	—	12	—	—	12	—	—	12	—	
Current Noise Density	i_n	$f_O = 1\text{kHz}$	—	0.007	—	—	0.007	—	—	0.007	—	$pA/\sqrt{\text{Hz}}$
External V_{OS} Trim Range		$R_{\text{pot}} = 10\text{k}\Omega$	—	4	—	—	4	—	—	4	—	mV
Long-Term V_{OS} Drift			—	5	—	—	5	—	—	5	—	$\mu V/\text{month}$
Supply Voltage Range	V_S	(Note 3)	± 8	± 15	± 20	± 8	± 15	± 20	± 8	± 15	± 20	V

NOTES:

- Guaranteed by CMR test.
- Guaranteed by slew-rate test and formula $BW_p = SR/(2\pi 10V_{\text{PEAK}})$.
- Guaranteed but not tested.
- See test circuit, page 7.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$ for E/F grades, and $-55^\circ C \leq T_A \leq 125^\circ C$ for A grade, unless otherwise noted.

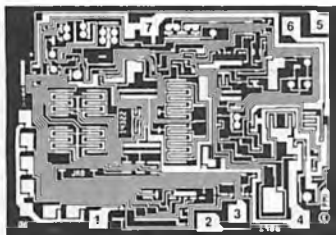
PARAMETER	SYMBOL	CONDITIONS	OP-44E			OP-44F			OP-44A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	0.4	1.2	—	0.6	2.5	—	0.5	2.0	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		—	4	10	—	8	—	—	4	10	$\mu V/^\circ C$
Input Bias Current	I_B	(Note 1)	—	0.5	1.2	—	0.6	2.0	—	6	20	nA
Input Offset Current	I_{OS}	(Note 1)	—	0.05	0.2	—	0.06	0.4	—	0.2	1.0	nA
Input Voltage Range	IVR	(Note 2)	± 11	+12.5 -12.0	—	± 11	+12.5 -12.0	—	± 11	+12.5 -12.0	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	84	94	—	80	92	—	84	94	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	—	2	40	—	6	50	—	10	50	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L = 10\text{k}\Omega$ (Note 1)	200	500	—	200	500	—	160	350	—	V/mV
		$R_L = 2\text{k}\Omega$ $V_O = \pm 10V$	100	160	—	100	160	—	80	110	—	
Output Voltage Swing	V_O	$R_L = 2\text{k}\Omega$	± 11.0	+12.3 -11.8	—	± 11.0	+12.3 -11.8	—	± 11.0	+12.3 -11.8	—	V
Output Current	I_{OUT}		± 8	—	—	± 8	—	—	± 8	—	—	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	—	6.5	7.5	—	6.5	7.5	—	6.5	7.5	mA
Slew Rate	SR	$R_L = 2\text{k}\Omega$; $C_L = 50\text{pF}$	80	100	—	70	90	—	80	100	—	V/ μs
Capacitive Load Drive Capability	C_L	$A_{VCL} \geq 3$ (Note 3)	50	100	—	50	100	—	50	100	—	pF

NOTES:

- $T_J = 85^\circ C$ for E/F Grades; $T_J = 125^\circ C$ for A grade.
- Guaranteed by CMR test.
- Guaranteed but not tested.



DICE CHARACTERISTICS



DIE SIZE 0.098×0.070 inch, 6860 sq. mils
(2.49×1.78 mm, 4.43 sq. mm)

1. OFFSET VOLTAGE NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. NEGATIVE SUPPLY
5. OFFSET VOLTAGE NULL
6. AMPLIFIER OUTPUT
7. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_j = 25^\circ C$, unless otherwise noted.

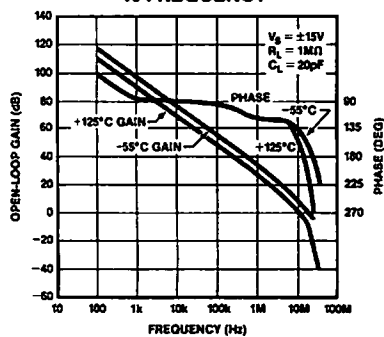
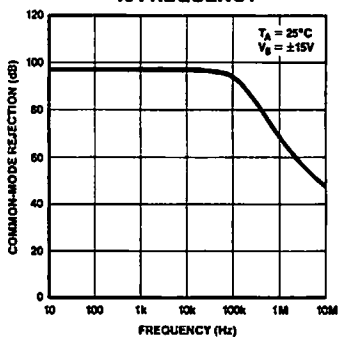
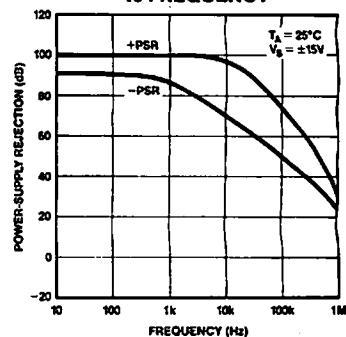
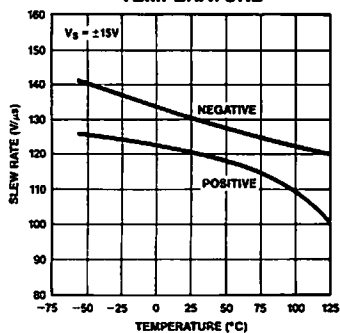
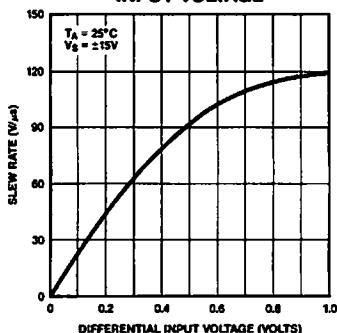
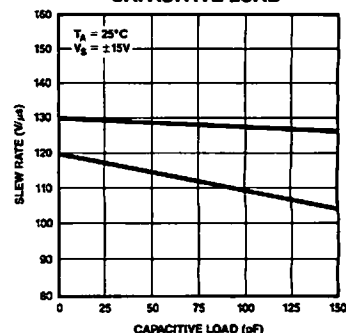
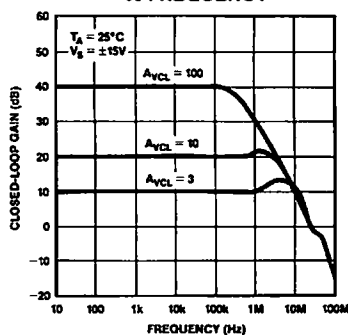
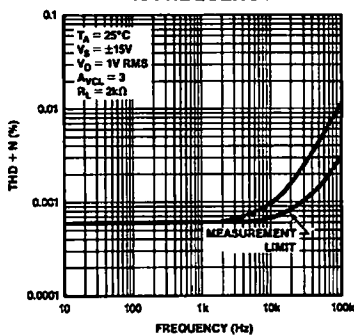
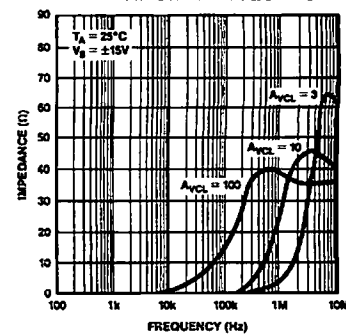
PARAMETER	SYMBOL	CONDITIONS	OP-44N	UNITS
			LIMIT	
Offset Voltage	V_{OS}		1.5	mV MAX
Input Bias Current	I_B	$V_{CM} = 0V$	250	pA MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	50	pA MAX
Input Voltage Range	IVR	(Note 1)	± 11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	80	dB MIN
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 20V$	50	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 10k\Omega$	500	V/mV MIN
		$R_L = 2k\Omega$	200	
		$R_L = 1k\Omega$	100	
Output Voltage Swing	V_O	$R_L = 1k\Omega$	± 11.5	V MIN
Output Current	I_{OUT}		± 20	mA MIN
Supply Current	I_{SY}	No Load $V_O = 0V$	7.5	mA MAX
Slew Rate	SR		80	V/ μs MIN
Capacitive Load Drive Capability	C_L	$A_{VCL} \geq 3$ (Note 2)	50	pF MIN

NOTES:

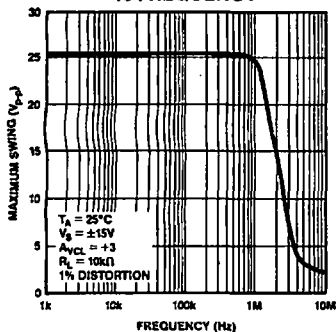
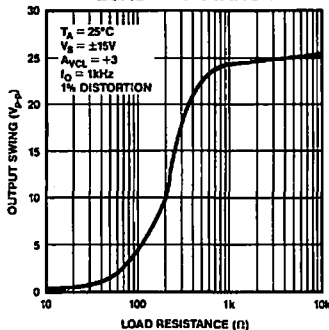
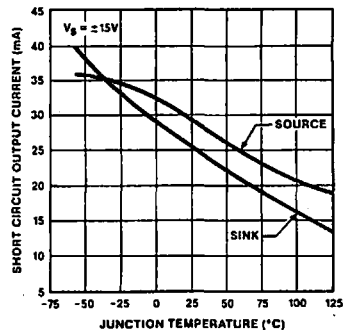
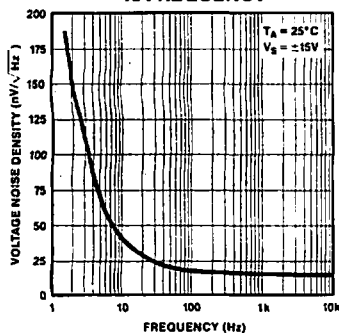
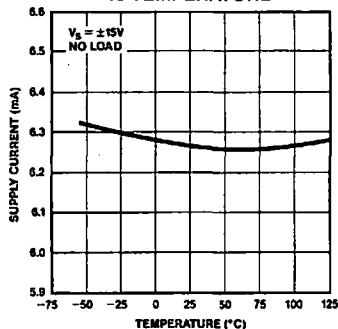
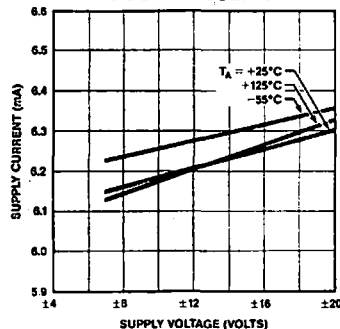
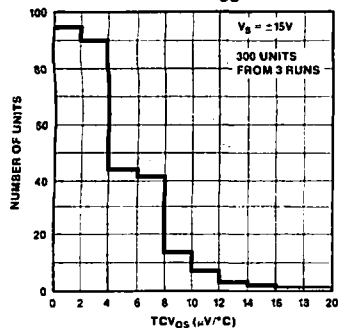
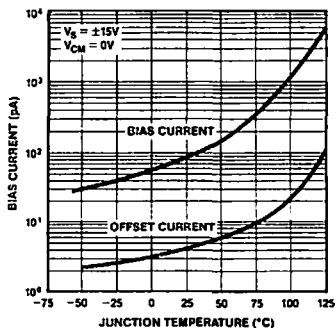
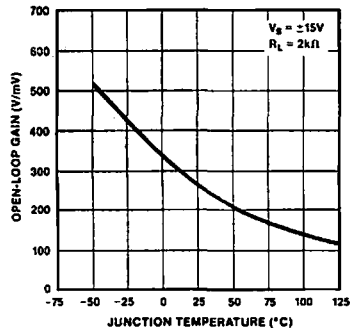
1. Guaranteed by CMR test.
2. Guaranteed but not tested.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

 OPEN-LOOP GAIN, PHASE
vs FREQUENCY

 COMMON-MODE REJECTION
vs FREQUENCY

 POWER-SUPPLY REJECTION
vs FREQUENCY

 SLEW RATE vs
TEMPERATURE

 SLEW RATE vs DIFFERENTIAL
INPUT VOLTAGE

 SLEW RATE vs
CAPACITIVE LOAD

 CLOSED-LOOP GAIN
vs FREQUENCY

 TOTAL HARMONIC
DISTORTION + NOISE
vs FREQUENCY

 CLOSED-LOOP OUTPUT
IMPEDANCE vs FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS

 MAXIMUM OUTPUT SWING
vs FREQUENCY

 OUTPUT SWING vs
LOAD RESISTANCE

 SHORT CIRCUIT
OUTPUT CURRENT vs
JUNCTION TEMPERATURE

 VOLTAGE NOISE DENSITY
vs FREQUENCY

 SUPPLY CURRENT
vs TEMPERATURE

 SUPPLY CURRENT
vs SUPPLY VOLTAGE

 TYPICAL DISTRIBUTION
OF TCV_{OS}

 BIAS, OFFSET CURRENT
vs JUNCTION TEMPERATURE

 OPEN-LOOP GAIN vs
JUNCTION TEMPERATURE


APPLICATIONS INFORMATION

The OP-44 is a high-speed amplifier internally compensated for closed-loop gains of 3 or more. Slew rate is typically $120\text{V}/\mu\text{s}$, which allows the OP-44 output to handle a $20\text{V}_{\text{p-p}}$ sine wave at 2MHz . Stability is ensured by the OP-44's guaranteed capacitive load drive ability of 50pF .

The input capacitance of high-speed op amps often causes a noticeable degradation of pulse response, resulting in excessive overshoot and ringing. The pole introduced by the input capacitance can be compensated by placing a similar capacitance in the feedback loop of the amplifier. For the OP-44, the input capacitance is typically 6pF .

Small-signal and large-signal transient responses are shown in Figures 1 and 2. These photos were taken using the gain of 3 test circuit shown in Figure 3.

As with most JFET-input op amps, the output of the OP-44 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up.

FIGURE 1: Small-Signal Transient Response
($A_{\text{VCL}} = +3$, $C_{\text{L}} = 50\text{pF}$)

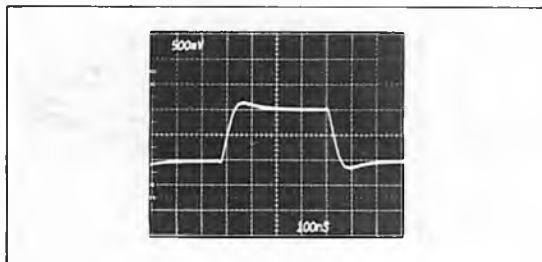
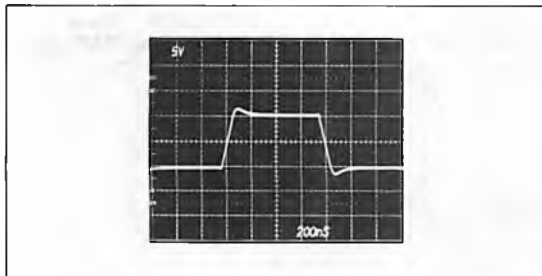


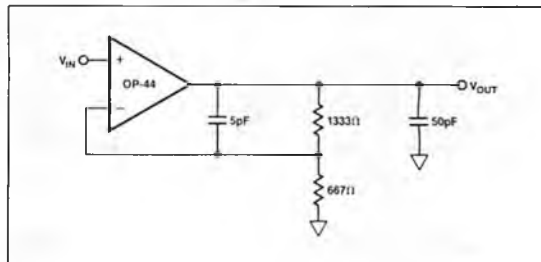
FIGURE 2: Large-Signal Transient Response
($A_{\text{VCL}} = +3$, $C_{\text{L}} = 50\text{pF}$)



Supply decoupling must be used to overcome inductance and resistance associated with the supply lines to the amplifier. For most applications, a $0.1\mu\text{F}$ to $0.01\mu\text{F}$ placed between each supply pin and ground is adequate. If supply lines are extremely long and/or noisy, an additional tantalum capacitor between $3.3\mu\text{F}$ and $10\mu\text{F}$ should be placed in parallel with each of the smaller decoupling capacitors.

The OP-44 displays excellent resistance to radiation. Radiation hardness data is available by contacting the factory.

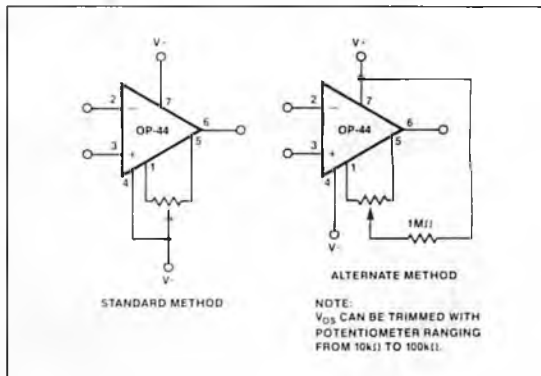
FIGURE 3: Transient Response Test Circuit



OFFSET VOLTAGE ADJUSTMENT

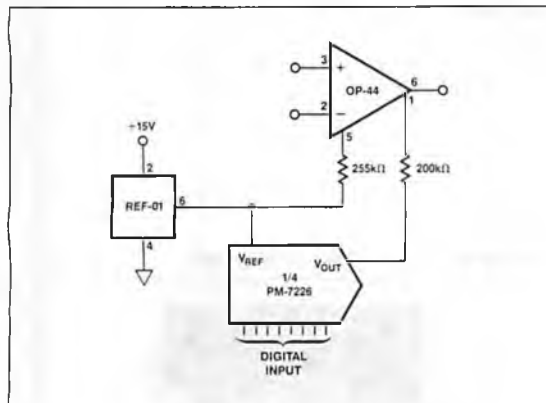
Offset voltage is adjusted with a $10\text{k}\Omega$ to $100\text{k}\Omega$ potentiometer as shown in Figure 4. The potentiometer is connected between pins 1 and 5 with its wiper connected to the V^- supply. Nulling V_{OS} in this manner changes TCV_{OS} by no more than $5\mu\text{V}/^\circ\text{C}$ per millivolt of V_{OS} change. Alternately, V_{OS} may be nulled by attaching the potentiometer wiper through a $1\text{M}\Omega$ resistor to the positive supply rail.

FIGURE 4: Input Offset Voltage Nulling



Digital offset correction is possible using the nulling pins. The circuit of Figure 5 will correct for greater than $\pm 4\text{mV}$ of offset, allowing correction of some system errors in addition to the OP-44's offset voltage. One of the four voltage-output DACs on the PM-7226 is used to apply a voltage between 0V and 10V to the 200k Ω resistor, while the 255k Ω resistor is tied to the +10V reference. One LSB of the 8-bit PM-7226 is equivalent to approximately 35 μV of offset change around the zero offset point.

FIGURE 5: Digital Offset Correction



A common problem with many high-speed amplifiers is a requirement for more DC precision than the amplifier's capability. While the OP-44 already offers an order of magnitude or more improvements in precision over previous high-speed amplifiers, some users may find a need for even greater precision.

Figure 6 shows a combination amplifier melding the precision DC characteristics of an OP-97 with the high speed of the OP-44. The OP-97 reacts for low-frequency and DC signals, while the OP-44 is dominant at higher frequencies. Over-compensation of the OP-97 ensures that it operates only at low frequencies. Resistor matching is important to optimize this circuit's transient response. The overall supply current of this combination amplifier is only slightly higher than that of the OP-44 alone. This is due to the minimal consumption of the OP-97, only 600 μA . Transient response of this circuit is shown in Figure 7. Its initial offset voltage is 20 μV , while TCV_{OS} is less than 0.6 $\mu\text{V}/^\circ\text{C}$.

FIGURE 6: High-Speed, Low-Offset, Low-Drift Amplifier

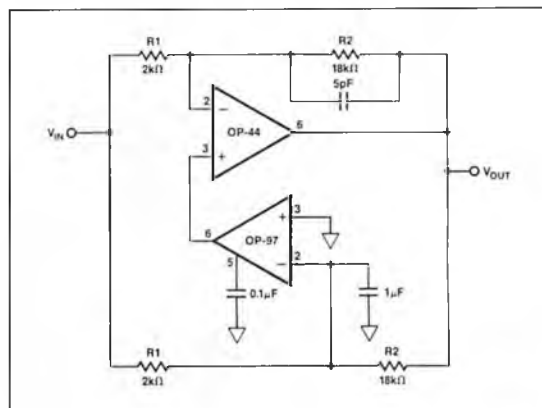


FIGURE 7: Combination Amplifier Transient Response

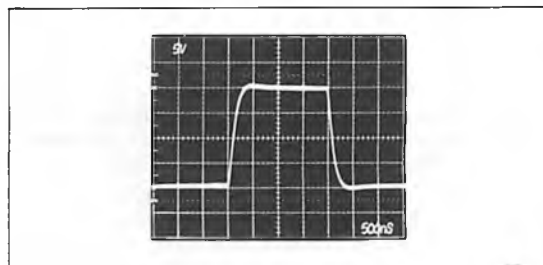


FIGURE 8: Combination Amplifier V_{OS} vs Temperature

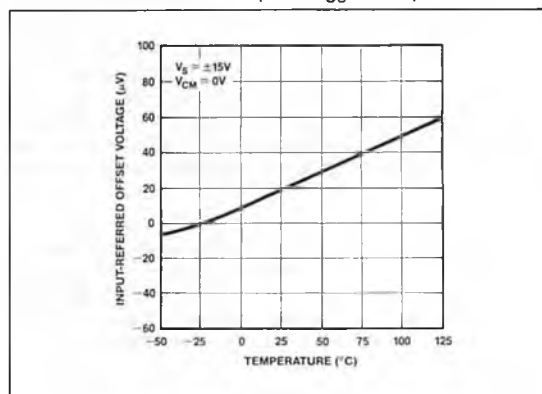
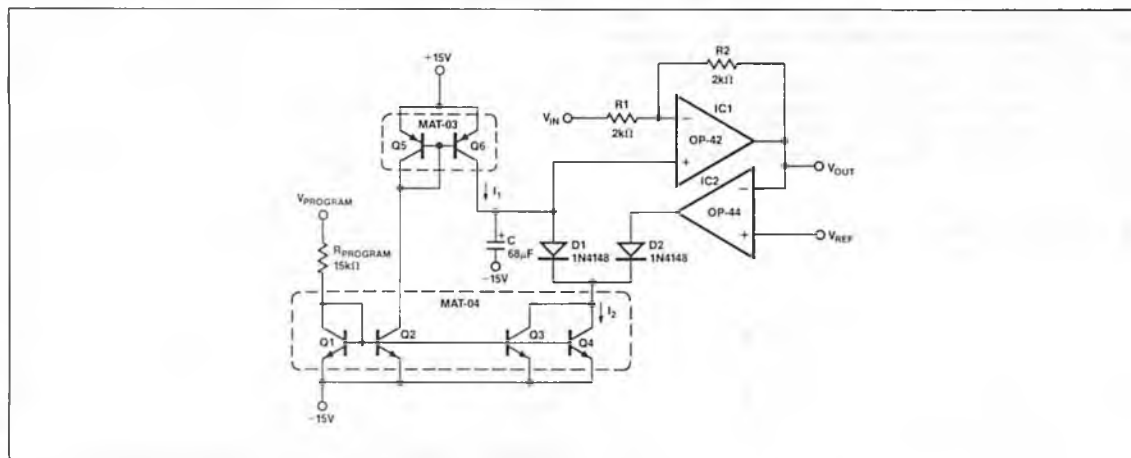


FIGURE 9: Programmable Baseline Restorer



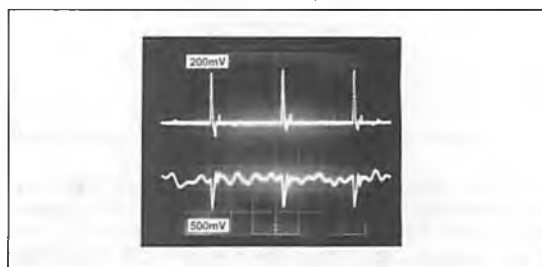
Baseline restoration is another useful technique for correcting errors introduced by amplifier drift, or by electromagnetic pickup. High-impedance sources, such as a human body, are notorious for large DC drifts. In many cases, where pulse or AC measurements are being made, and the pulse height above a nominal DC line contains the important information.

While a simple high-pass filter may be adequate for some situations, the baseline restorer shown in Figure 9 allows a wide degree of flexibility for analog adaptive filtering techniques, and offers some benefits not available with a frequency-domain filter.

The baseline restorer behaves as a nonlinear filter, acting upon the slew rate of the input signal rather than its frequency. Its output will restore the base of the pulses to an arbitrary level, set by V_{REF} . The slew rate cutoff of the filter is set by the current flowing through Q1, which is in turn set by $V_{PROGRAM}$. V_{REF} and $V_{PROGRAM}$ may be controlled by a voltage-output DAC such as the PM-7226. If current programming is desired, $R_{PROGRAM}$ may be removed and replaced by a current-source, such as a bipolar DAC.

To understand the circuit's operation, assume that capacitor C has charged to the DC baseline. If the output swings above the baseline, IC2 swings low, reverse biasing diode D2. D1 is pulled low, and forward biases. A current ($I_2 - I_1$) discharges the capacitor until equilibrium is restored. If the output drops below the baseline, IC2 swings high, and D2 becomes forward biased. I_2 is supplied by the output of IC2 while I_1 charges C until the baseline is restored. The rate of restoration depends upon the current available to charge or discharge C.

FIGURE 10: Baseline Restorer Response



For symmetric operation, with the same restoration rate for positive or negative excursions from the baseline, I_2 must be twice I_1 . This provides an equal current for charging and discharging the capacitor. I_1 is set by the current flowing through Q1 in the MAT-04. An identical current flows through each transistor. The MAT-03 matched PNP pair, Q5 and Q6, act as a current mirror to reflect the current through Q2 (I_1). Q3 and Q4 create I_2 , which is twice I_1 . I_1 may be set anywhere between a few nanoamps to several mA. Higher currents will result in rejection of faster-slewing signals, while lower currents will allow passage of slower signals.

The OP-44 is configured for a gain of -1 , but gain is adjustable by $R1$ and $R2$, and is simply $-(R2/R1)$. OP-44 stability is maintained by the dominant pole introduced by C.



OP-50

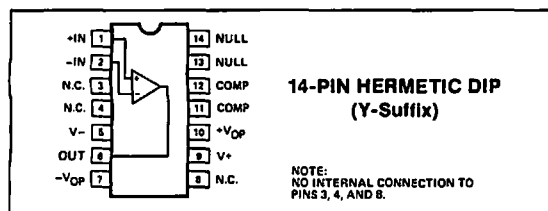
HIGH-OUTPUT-CURRENT
OPERATIONAL AMPLIFIER ($A_{VCL} \geq 5$)

Precision Monolithics Inc.

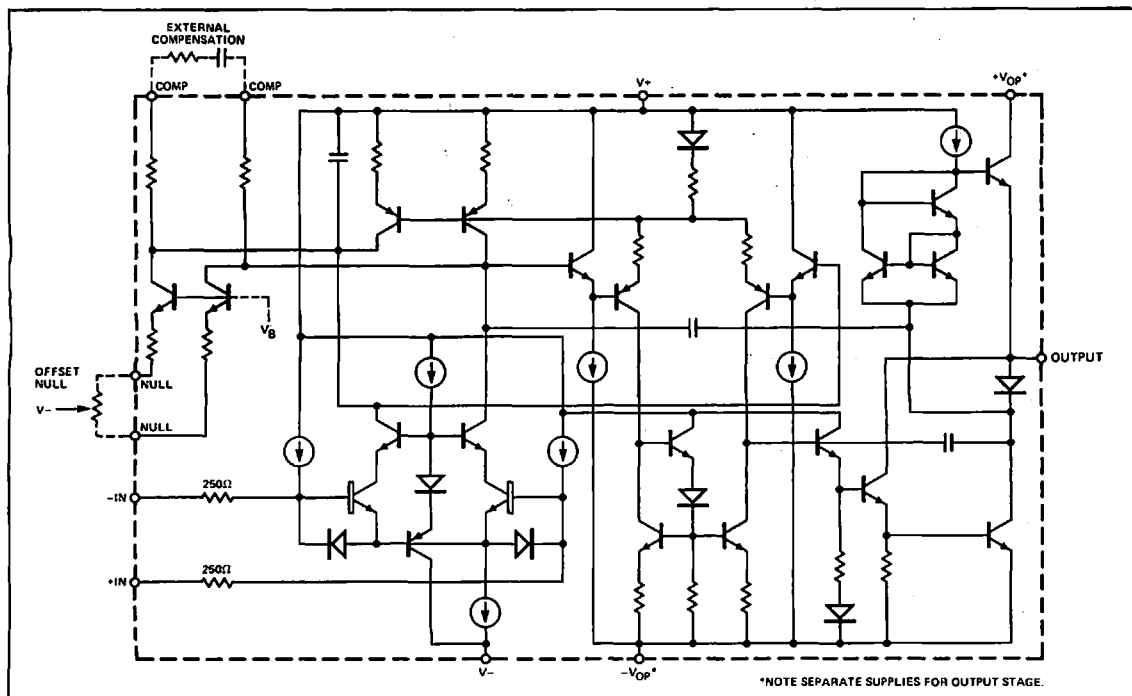
FEATURES

- Open-Loop Gain 10,000,000V/V Min
- Low Input Offset Voltage 25 μ V Max
- Low Input Bias Current 5nA Max
- Excellent TCV_{OS} 0.3 μ V/ $^{\circ}$ C Max
- High CMRR 126dB Min
- High PSRR 126dB Min
- Low Noise 5.5nV/ $\sqrt{\text{Hz}}$ @ f = 10Hz
4.5nV/ $\sqrt{\text{Hz}}$ @ f = 1kHz
- High Output Current ± 50 mA
- Drives Capacitive Loads up to 10nF
- On-Board Thermal Shutdown Circuit

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



ORDERING INFORMATION†

T _A = 25 $^{\circ}$ C V _{OS} MAX (μ V)	PACKAGE	OPERATING TEMPERATURE RANGE
	CERDIP 14-PIN	
25	OP-50AY*	MIL
100	OP-50BY*	MIL
25	OP-50EY	IND
100	OP-50FY	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1888 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-50 eliminates the need for an output buffer in applications which require high load-driving capability coupled with premium amplifier performance. The output stage can drive ± 50 mA into 50 Ω loads. In addition, the output is stable with capacitive loads of up to 10nF. This load driving ability makes the OP-50 ideal for amplifying small signals for transmission through long cables. The amplifier features open-loop voltage gain of over 10 million with common-mode rejection and power supply rejection of greater than 126dB (A/E grades).

The OP-50 is stable for closed-loop gains above 50, and can be externally compensated for closed-loop gains in the range of 5 to 50. The amplifier is designed for use in high-gain and/or high-output-current applications. For example, an OP-07 coupled with an output buffer can be replaced by a single OP-50 amplifier.

Ion-implanted superbeta transistors, combined with a patented input bias current cancellation circuit, provide an input bias current of only 5nA and input offset current of 1nA. Over the full military temperature range, input bias current and input offset current for an A-grade device does not exceed 8nA and 3nA, respectively. Input offset voltages are trimmed to a maximum of 25 μ V (A/E grades) and 100 μ V (B/F grades) using PMI's zener-zapping technique. This low offset eliminates the need for an offset trimpot in most applications.

Low voltage-noise, typically 4.5nV/ $\sqrt{\text{Hz}}$ at 1kHz, is achieved in the OP-50 with minimum sacrifice of input protection. Overload protection is provided by input resistors of 250 Ω and emitter-base diodes. The input resistors provide current limit protection against differential inputs of up to ± 10 V; and the diodes prevent avalanche breakdown which could degrade the I_B , I_{OS} , and matching of the input stage transistors. External resistors can be added to the input to guard against higher input voltages; however, the added resistors will degrade noise voltage performance. When minimum noise voltage is required, source resistance should be kept below a few hundred ohms.

Separate output-stage power supply pins are provided on the OP-50 to allow control of device power dissipation and output voltage swing. The maximum voltage which may be applied across the power supply pins is ± 18 V. The guaranteed specifications are based on operating both stages at ± 15 V; however, there is minimal effect on DC performance when the main amplifier is operated at ± 15 V and the output stage is operated at a reduced voltage. When operating both the main amplifier and the output stage at the same voltages, the corresponding power supply pins may be tied together. Decoupling capacitors are recommended between the power supply pins and analog ground. It is necessary to use decoupling capacitors on each power supply pin when operating the output stage at supply voltages less than the amplifier supply voltage. Do not operate the output-stage negative power supply pin at a more negative voltage than the negative supply pin (V-).

A thermally-symmetric die layout, which differs from other op amp designs by the positioning of more devices along the center line, provides the OP-50 with a thermal drift of less than 0.3 μ V/ $^{\circ}\text{C}$. This layout feature is critical to the maintenance of high open-loop gain when driving large-current loads and dissipating hundreds of milliwatts in the device. The use of a heatsink is recommended to reduce internal temperature rise when operating at high output power levels. The use of standard dual-in-line package heatsinks will help to dissipate heat to the environment. Other techniques, such as the use of external voltage-dropping resistors, allow heat to be dissipated outside of the package. See Figure 5, "Driving 50 Ω Loads", in the applications section.

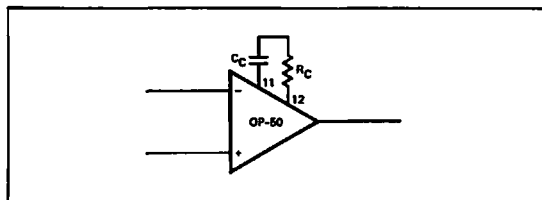
A thermal-shutdown circuit protects the OP-50 from overdisipation. When the die temperature reaches approximately 165 $^{\circ}\text{C}$, the output stage automatically shuts down. The amplifier input stage remains fully operational, thereby protecting the signal source from any loading changes caused by a complete shutdown.

COMPENSATION FOR GAINS BETWEEN 5 AND 50

The OP-50 can be compensated for inverting gains between 5 and 50 using a series resistor and capacitor. These values can be adjusted to minimize overshoot for a given application. The recommended compensation is:

GAIN RANGE	R_C	C_C
$5 \leq A_{VCL} \leq 20$	560 Ω	4.7nF
$20 \leq A_{VCL} \leq 50$	3.3k Ω	1nF
$A_{VCL} \geq 50$	No compensation required	

COMPENSATION



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2)	± 18 V
Internal Power Dissipation (Note 3)	500mW
Input Voltage	Supply Voltage
Differential Input Voltage (Note 4)	± 10 V
Differential Input Current (Note 4)	± 20 mA
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$
Operating Temperature Range	
OP-50A, B	-55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$
OP-50E, F	-25 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	300 $^{\circ}\text{C}$
DICE Junction Temperature (T_j)	-65 $^{\circ}\text{C}$ to +150 $^{\circ}\text{C}$

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	106 $^{\circ}\text{C}$	11.3mW/ $^{\circ}\text{C}$

NOTES:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Supply voltage rating applies to all power supply pins. No device pins should be connected to a voltage more negative than the supply to V-, pin 5.
3. See table for maximum ambient temperature rating and derating factor.
4. The OP-50's inputs are protected by 250 Ω series resistors and protection diodes. If the differential input voltage exceeds ± 10 V, the input current must be limited to ± 20 mA.



ELECTRICAL CHARACTERISTICS at $V_+ = +V_{OP} = +15V$, $V_- = -V_{OP} = -15V$, $T_A = 25^\circ C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50A/E			OP-50B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	10	25	—	50	100	μV
Input Bias Current	I_B		—	± 1	± 5	—	± 1	± 10	nA
Input Offset Current	I_{OS}		—	0.1	1	—	0.1	3	nA
Input Voltage Range	IVR	CMRR $\geq 100dB$	± 12	—	—	± 12	—	—	V
Output Voltage Swing	V_O	$R_L \geq 500\Omega$	± 13	± 13.4	—	± 13	± 13.4	—	V
		$R_L \geq 50\Omega$ (Note 1)	± 2.5	± 4.0	—	± 2.5	± 4.0	—	V
Output Voltage Swing	V_O	$V_+ = +V_{OP} = +5V$, $V_- = -V_{OP} = -5V$							V
		$R_L = 500\Omega$	± 3.5	± 3.8	—	± 3.5	± 3.8	—	V
		$R_L = 50\Omega$	± 2.5	± 2.8	—	± 2.5	± 2.8	—	V
Slew Rate	SR	$R_L \geq 2k\Omega$ $R_C = 560\Omega$ $C_C = 4.7nF$	2.5	3.0	—	2.5	3.0	—	V/ μs
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	126	140	—	110	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	0.1	0.5	—	0.5	1	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 1k\Omega$	10	20	—	7.5	15	—	V/ μV
Gain-Bandwidth Product	GBW	$A_{VCL} = 50$ (Note 2)	15	25	—	15	25	—	MHz
Offset Voltage Range Adjust		$R_P = 100k\Omega$	± 1.0	± 2.5	—	± 1.0	± 2.5	—	mV
Input Noise Voltage	e_{np-p}	$f = 0.1Hz$ to $10Hz$	—	0.12	—	—	0.12	—	μV_{p-p}
Noise Voltage Density	e_n	$f = 10Hz$	—	5.5	8.5	—	5.5	8.5	$nV/\sqrt{Hz}$
		$f = 1kHz$ (Note 3)	—	4.5	6.0	—	4.5	6.0	
Noise Current	i_{np-p}	$f = 0.1Hz$ to $10Hz$	—	2	—	—	2	—	pA_{p-p}
Noise Current Density	i_n	$f = 100Hz$	—	0.3	—	—	0.3	—	$pA/\sqrt{Hz}$
		$f = 1kHz$	—	0.23	—	—	0.23	—	
Quiescent Supply Current	I_{SY}	No Load	—	2.6	3.3	—	2.6	3.3	mA
Positive Current Limit	$+I_{SC}$	Output shorted to Ground	60	95	120	60	95	120	mA
Negative Current Limit	$-I_{SC}$	Output shorted to Ground	60	85	120	60	85	120	mA
Differential-Mode Input Resistance	R_{IND}		—	2	—	—	2	—	M Ω
Common-Mode Input Resistance	R_{INCM}		—	20	—	—	20	—	G Ω
Capacitive Load Capability	C_L	$A_{VCL} \geq 5$							nF
		$R_C = 560\Omega$ (Note 2) $C_C = 4.7nF$	10	—	—	10	—	—	
Settling-Time	t_s	Settling to 0.01%, $V_O = 20V_{p-p}$							μs
		$A_{VCL} = 500$ $A_{VCL} = 1000$	—	30	—	—	30	—	
			—	60	—	—	60	—	

NOTES:

1. Guaranteed by current limit tests.
2. Guaranteed by design.
3. Sample tested.



ELECTRICAL CHARACTERISTICS at $V_+ = +V_{OP} = +15V$, $V_- = -V_{OP} = -15V$, $-25^\circ C \leq T_A \leq +85^\circ C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50E			OP-50F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	20	45	—	50	150	μV
Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.15	0.3	—	0.3	1	$\mu V/^\circ C$
Input Bias Current	I_B		—	± 2	± 7	—	± 2	± 25	nA
Input Offset Current	I_{OS}		—	0.2	2.5	—	0.2	20	nA
Input Offset Current Drift	TCI_{OS}		—	3	—	—	5	—	$pA/^\circ C$
Input Bias Current Drift	TCI_B		—	20	—	—	50	—	$pA/^\circ C$
Input Voltage Range	IVR	$CMRR \geq 100dB$	± 11.5	—	—	± 11.5	—	—	V
Output Voltage Swing	V_O	$R_L \geq 500\Omega$	± 12	± 13.4	—	± 12	± 13.4	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	120	130	—	105	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	0.5	1.25	—	0.5	1.25	$\mu V/V$
Quiescent Supply Current	I_{SV}	No Load	—	2.8	4	—	2.8	4	mA
Open-Loop Gain	A_{VO}	$V_{OUT} = \pm 10V$, $R_L = 1k\Omega$ (Note 2)	4	15	—	4	15	—	$V/\mu V$

NOTES:

1. TCV_{OS} tested on E grade, guaranteed by design on F grade specification.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_+ = +V_{OP} = +15V$, $V_- = -V_{OP} = -15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, no compensation, unless otherwise noted.

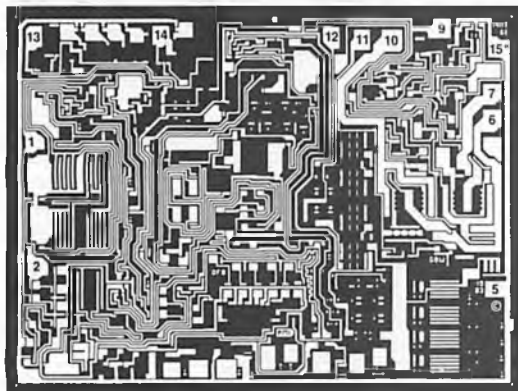
PARAMETER	SYMBOL	CONDITIONS	OP-50A			OP-50B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	20	55	—	50	200	μV
Input Offset Voltage Drift	TCV_{OS}		—	0.15	0.3	—	0.3	1	$\mu V/^\circ C$
Input Bias Current	I_B		—	± 2	± 8	—	± 2	± 20	nA
Input Offset Current	I_{OS}		—	0.5	3	—	0.5	12	nA
Input Offset Current Drift	TCI_{OS}		—	3	—	—	5	—	$pA/^\circ C$
Input Bias Current Drift	TCI_B		—	20	—	—	50	—	$pA/^\circ C$
Input Voltage Range	IVR	$CMRR \geq 100dB$	± 11.5	—	—	± 11.5	—	—	V
Output Voltage Swing	V_O	$R_L \geq 500\Omega$	± 12	± 13.2	—	± 12	± 13.2	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	120	130	—	105	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	0.5	1.25	—	0.5	1.25	$\mu V/V$
Quiescent Supply Current	I_{SV}	No Load	—	2.8	4	—	2.8	4	mA
Open-Loop Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 1k\Omega$ (Note 1)	4	10	—	4	10	—	$V/\mu V$

NOTE:

1. Tested at $+125^\circ C$, guaranteed by design at $-55^\circ C$.



DICE CHARACTERISTICS



DIE SIZE 0.149×0.111 inch, 16,539 sq. mils
 $(3.78 \times 2.82$ mm, 10.66 sq. mm)

1. NONINVERTING INPUT
2. INVERTING INPUT
5. V^-
6. OUTPUT
7. $-V_{OP}$
9. V^+
10. $+V_{OP}$
11. COMPENSATION
12. COMPENSATION
13. NULL
14. NULL
15. V^- (OPTIONAL BONDING PAD)*

For additional DICE ordering information, refer
 to 1988 Data Book, Section 2.

5

OPERATIONAL AMPLIFIERS

WAFER TEST LIMITS at $V^+ = +V_{OP} = +15V$, $V^- = -V_{OP} = -15V$, $T_A = 25^\circ C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50G LIMIT	UNITS
Input Offset Voltage	V_{OS}		100	μV MAX
Input Bias Current	I_B		± 10	nA MAX
Input Offset Current	I_{OS}		3	nA MAX
Output Voltage Swing	V_O	$R_L \geq 500\Omega$	± 13	V MIN
Output Voltage Swing	V_O	$V^+ = +V_{OP} = +5V$, $V^- = -V_{OP} = -5V$		
		$R_L = 500\Omega$	± 3.5	V MIN
		$R_L = 50\Omega$	± 2.5	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	1	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$, $R_L = 1k\Omega$	7.5	V/ μV MIN
Positive Current Limit	$+I_{SC}$	Output shorted to Ground	60	mA MIN
Negative Current Limit	$-I_{SC}$	Output shorted to Ground	60	mA MIN
Quiescent Supply Current	I_{SY}	No Load	3.3	mA MAX

NOTE:

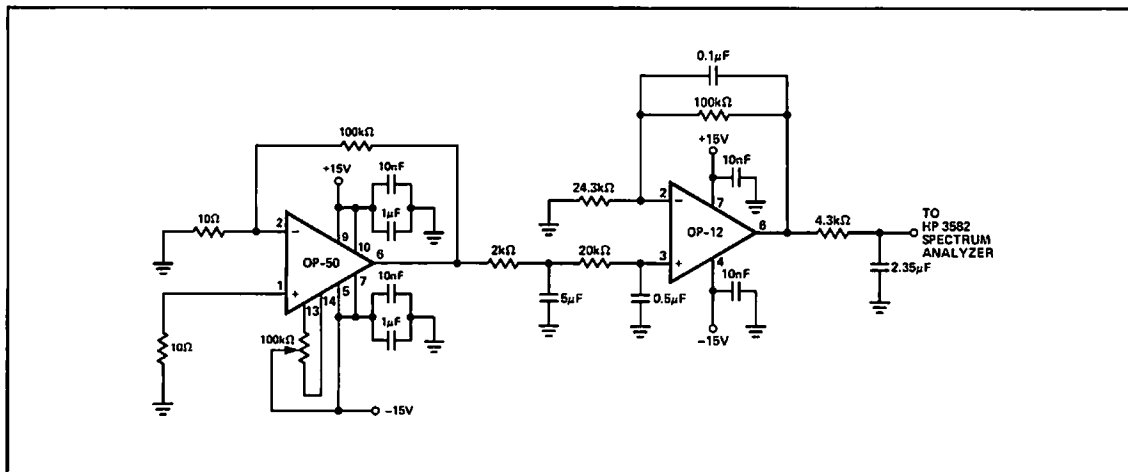
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



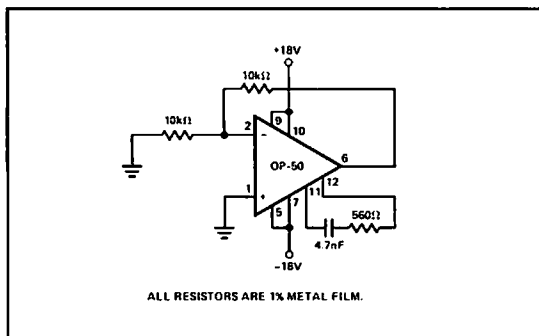
TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = +V_{OP} = +15V$, $V_- = -V_{OP} = -15V$, $T_A = 25^\circ C$, no compensation, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-50G TYPICAL	UNITS
Slew Rate	SR	$R_L \geq 2k\Omega$ $R_C = 560\Omega$ $C_C = 4.7nF$	3	$V/\mu s$
Noise Voltage Density	e_n	$f = 10Hz$ $f = 1kHz$	5.5 4.5	$nV/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	$f = 0.1Hz$ to $10Hz$	0.12	μV_{p-p}
Noise Current Density	i_n	$f = 10Hz$ $f = 1kHz$	0.2 0.15	$pA/\sqrt{Hz}$
Capacitive Load Capability	C_L	$A_{VCL} \geq 5$ $R_C = 560\Omega$ $C_C = 4.7nF$	10	nF

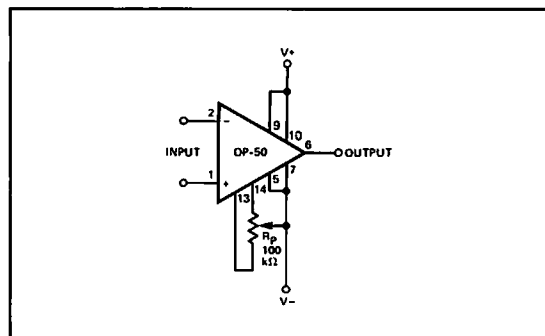
NOISE TEST CIRCUIT (0.1 TO 10Hz)



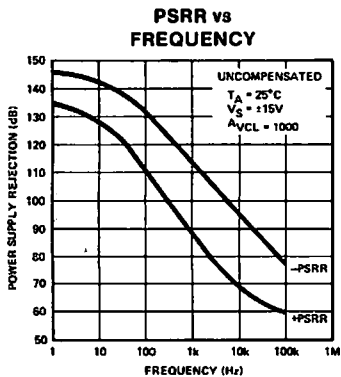
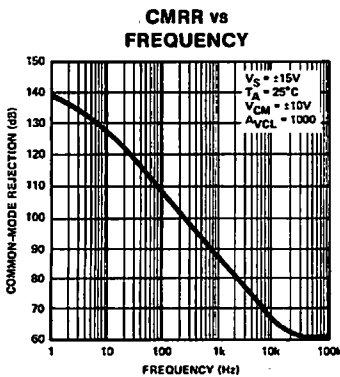
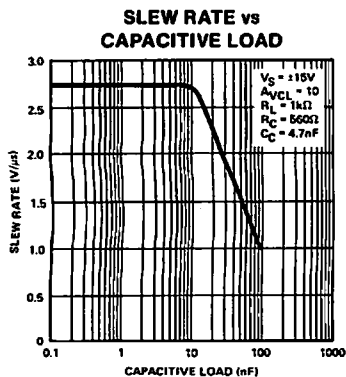
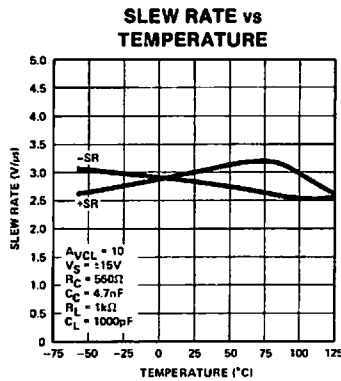
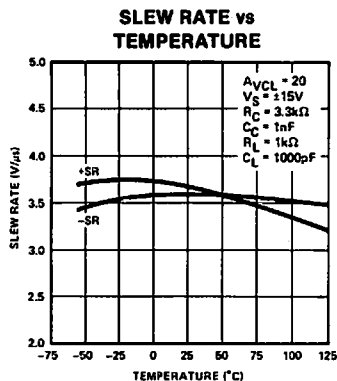
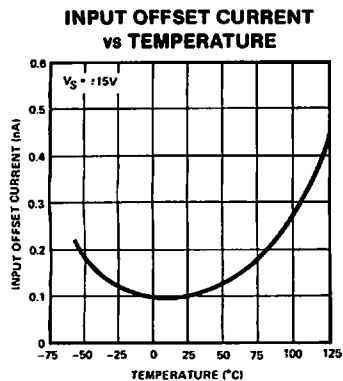
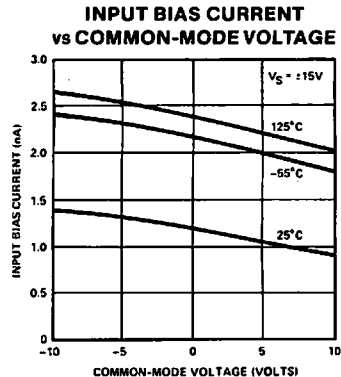
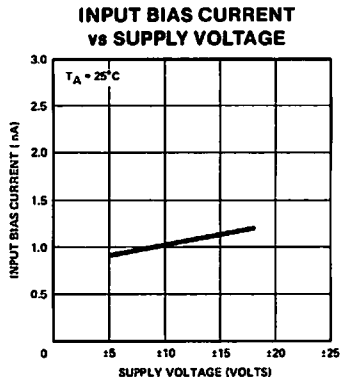
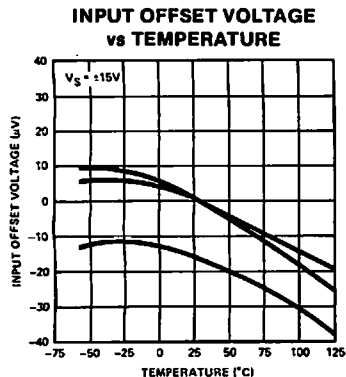
BURN-IN CIRCUIT



OFFSET NULLING CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTICS

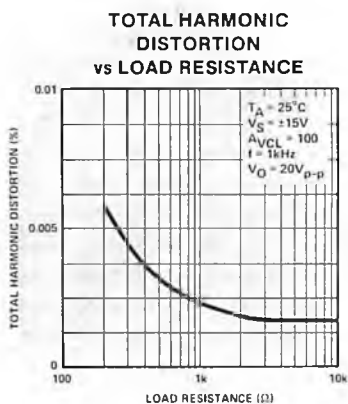
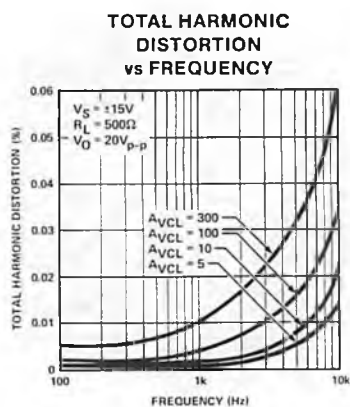
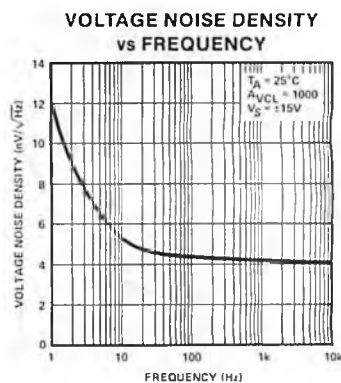
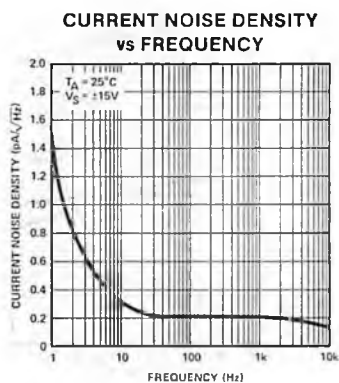
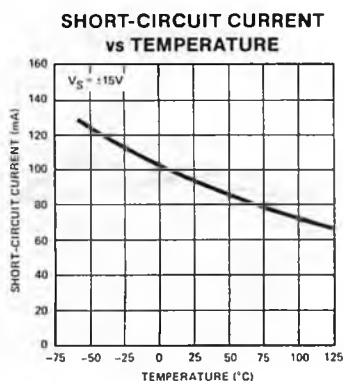
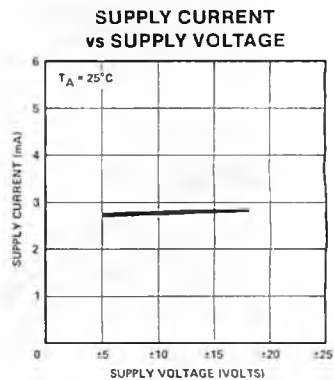
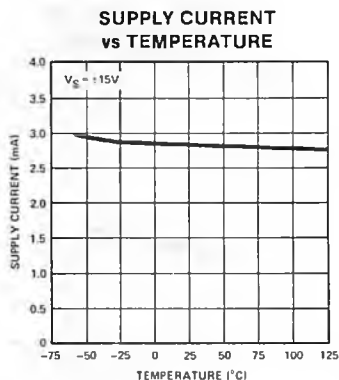
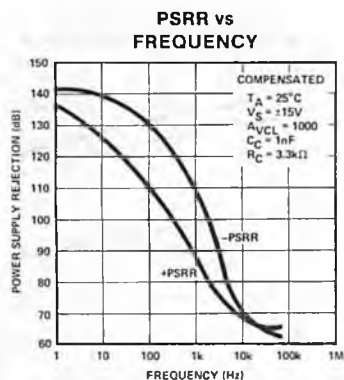
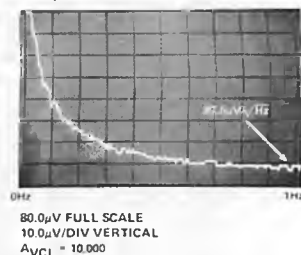


NOTE:
The symbol $\pm V_S$ is used to indicate the supply voltages when the main amplifier and the output stage are being operated at the same voltages.

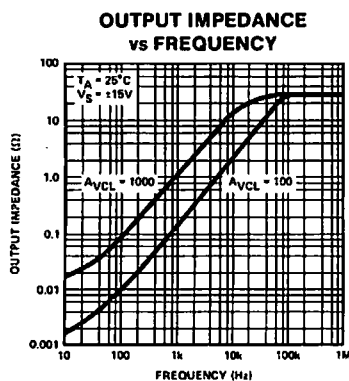
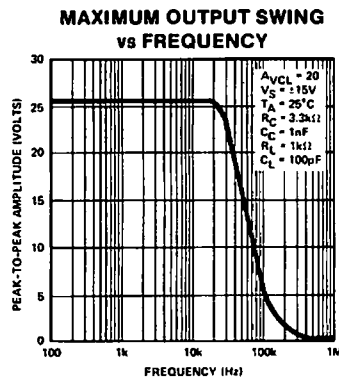
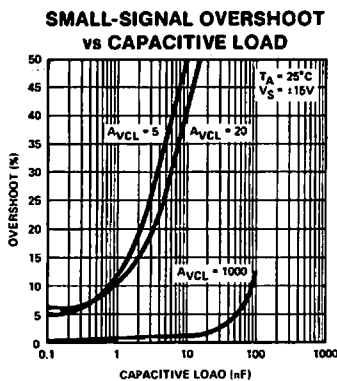
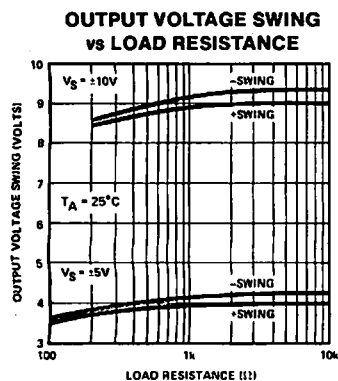
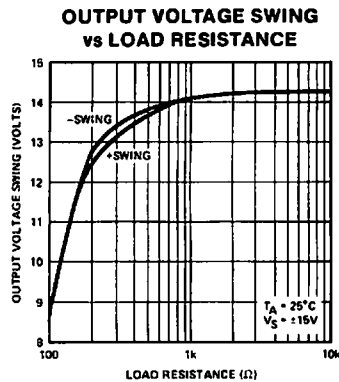
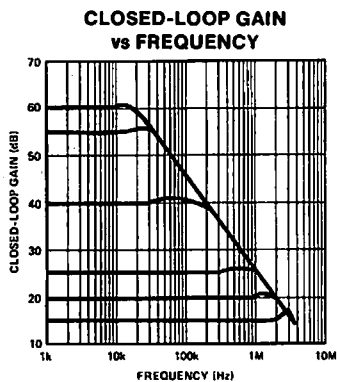
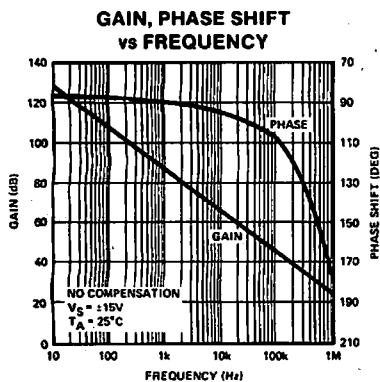
OPERATIONAL AMPLIFIERS

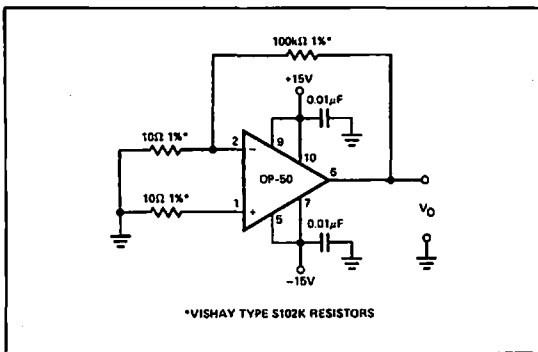
5

TYPICAL PERFORMANCE CHARACTERISTICS

0 TO 1Hz
NOISE VOLTAGE DENSITY

TYPICAL PERFORMANCE CHARACTERISTICS



TCV_{OS} TEST CIRCUIT

APPLICATIONS INFORMATION

HIGH-SENSITIVITY VOLTAGE COMPARATOR

A comparator capable of resolving a submicrovolt difference signal is shown in Figure 1. The OP-50, operating without feedback, drives a second gain stage which generates a TTL-compatible output signal. Schottky-clamp diodes prevent

overdriving of the long-tailed transistor pair and stop saturation of the output transistor. Power supply voltage is set to $\pm 5V$ to lower the quiescent power dissipation and minimize thermal feedback due to output stage dissipation. Operating from $\pm 5V$ supplies also reduces the OP-50 rise and fall times as the output slews over a reduced voltage range. This, in turn, reduces the output response time.

It is common practice with voltage comparators to ground one input terminal and to use a single-ended input. The historic reason is poor common-mode rejection on the input stage. In contrast, the OP-50 has very high common-mode rejection and is capable of detecting microvolt level differences in the presence of large common-mode signals.

The comparator is not fast, but it is very sensitive and can detect signal differences as low as $0.3\mu V$. With large input overdrives, the circuit responds in approximately $3\mu s$. If sharp transitions are needed, the use of a TTL Schmitt-trigger input is recommended. A table of Response Time vs. Input Overdrive is shown below.

INPUT OVERDRIVE	100mV	10mV	1mV	100μV	10μV
Positive Output Delay	3.2μs	5μs	40μs	340μs	2.4ms
Negative Output Delay	1.8μs	5μs	50μs	380μs	4.5ms

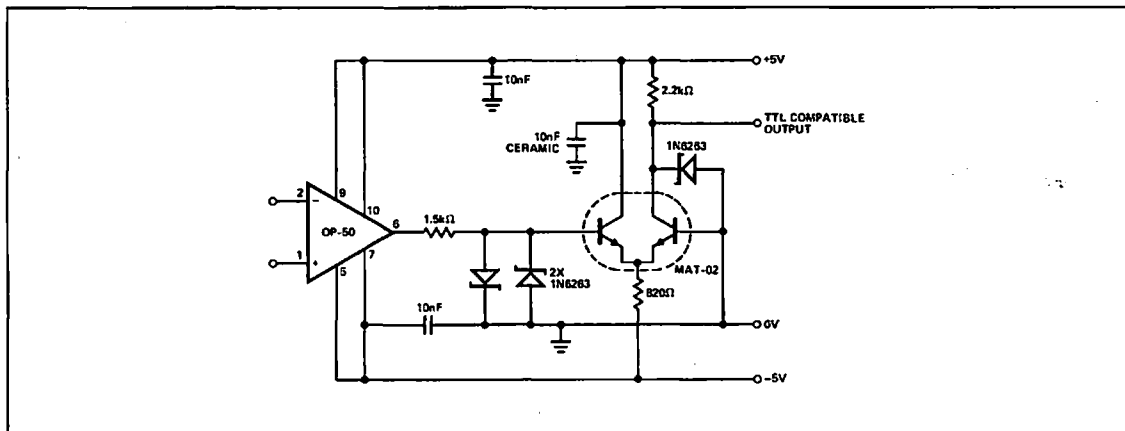


FIGURE 1: HIGH-SENSITIVITY VOLTAGE COMPARATOR

INTEGRATOR AND UNITY-GAIN BUFFER

Figure 2 shows a method of obtaining unity-gain in a buffer configuration. The R1 and C1 network provides input compensation to circumvent the minimum gain requirement. Figure 3 shows the same technique applied in the inverting mode to form a high precision integrator.

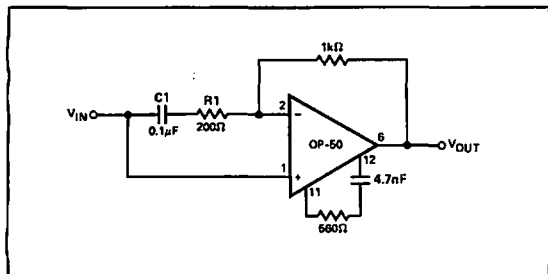


FIGURE 2: UNITY GAIN BUFFER

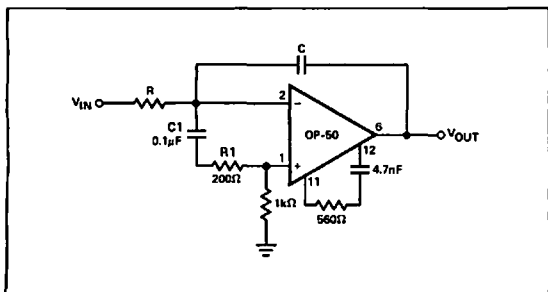


FIGURE 3: INTEGRATOR

20mA CURRENT SOURCE

The 20mA current source exploits the high output current and high linearity capabilities of the OP-50. Five precision resistors and a trim potentiometer are required in this circuit configuration, known as the Howland Current Pump. The trim potentiometer is used to balance the resistive feedback dividers. This maximizes the current-source output impedance. Compensation is selected for a voltage gain of 10.

Compliance is better than $\pm 11V$ at an output current of 20mA and the trimmed output resistance is typically $2M\Omega$ with $R_L \leq 500\Omega$. The transfer function is given by:

$$I_{OUT} = \frac{V_{IN(DIFF)} \times 10.1}{101} \text{ Amps}$$

$V_{IN(DIFF)}$ is the differential input voltage. For the resistor values shown in Figure 4, the maximum $V_{IN(DIFF)}$ is 200mV.

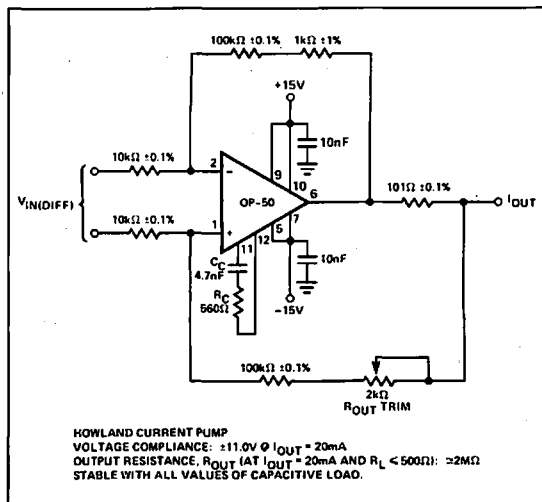


FIGURE 4: 20mA CURRENT SOURCE

DRIVING 50Ω LOADS

The OP-50 can provide up to 50mA into a 50Ω load and up to 26mA into a 500Ω load. The output is stable driving capacitive loads of up to 10nF.

Applications that make use of the high output current capability of the OP-50 will cause increased power dissipation in the amplifier. To reduce internal dissipation in these applications, external voltage dropping resistors can be connected in series with the output-stage power supply pins. As shown in Figure 5, 130Ω resistors can be attached to pin 7 ($-V_{OP}$) and to pin 10 ($+V_{OP}$). To maintain stability and specified performance levels, $0.047\mu F$ decoupling capacitors should be used as indicated from pin 7 and pin 10 to ground.

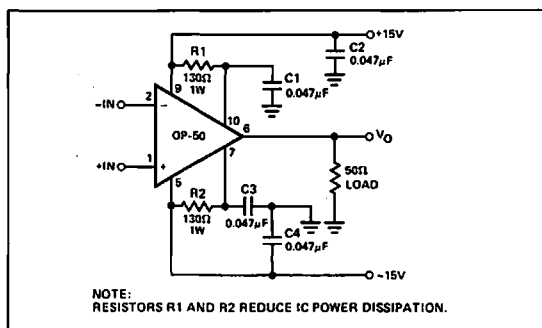


FIGURE 5: DRIVING 50Ω LOADS



OP-62/OP-63/OP-64

HIGH-SPEED, HIGH-BANDWIDTH
PRECISION OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

OP-62

- High Slew Rate 15V/ μ s Typ
- High Gain Bandwidth 50MHz Typ
- Very Low Offset Voltage 200 μ V Max
- Very High Gain 350V/mV Min
- Very Low Noise 2.5nV/ $\sqrt{\text{Hz}}$ @ 1kHz Typ
- Low Supply Current 7mA Max
- Unity-Gain Stable
- Standard 741 Pinout

OP-63

- Very High Slew Rate 50V/ μ s Typ
- High Gain Bandwidth 50MHz Typ
- Low Offset Voltage 750 μ V Max
- High Gain 100V/mV Min
- Low Noise 7nV/ $\sqrt{\text{Hz}}$ @ 1kHz Typ
- Low Supply Current 7mA Max
- Unity-Gain Stable
- Standard 741 Pinout

OP-64

- Extremely High Slew Rate 200V/ μ s Typ
- Very High Gain Bandwidth ($A_v \geq +5$) 200MHz Typ
- Low Offset Voltage 750 μ V Max
- High Gain 100V/mV Min
- Low Noise 7nV/ $\sqrt{\text{Hz}}$ @ 1kHz Typ
- Low Supply Current 7mA Max
- Standard 741 Pinout

ORDERING INFORMATION†

PACKAGE				OPERATING TEMPERATURE RANGE
TO-99	CERDIP	PLASTIC	LCC	
OP62AJ*	OP62AZ*	—	OP62ARC/883	MIL
OP62EJ	OP62EZ	—	—	XIND
OP62FJ	OP62FZ	—	—	XIND
—	—	OP62GP	—	XIND
—	—	OP62GS††	—	XIND
OP63AJ*	OP63AZ*	—	OP63ARC/883	MIL
OP63EJ	OP63EZ	—	—	XIND
OP63FJ	OP63FZ	—	—	XIND
—	—	OP63GP	—	XIND
—	—	OP63GS††	—	XIND
OP64AJ*	OP64AZ*	—	OP64ARC/883	MIL
OP64EJ	OP64EZ	—	—	XIND
OP64FJ	OP64FZ	—	—	XIND
—	—	OP64GP	—	XIND
—	—	OP64GS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

PMI's OP-62/63/64 series of operational amplifiers offer precision performance with outstanding speed and bandwidth. Advanced processing techniques have enabled PMI to make the OP-62/63/64 series superior in both cost and performance to many dielectrically-isolated and hybrid op amps.

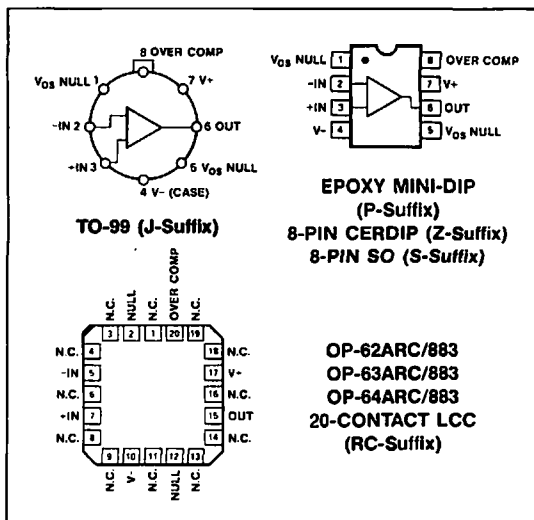
The OP-62 features an exceptional combination of precision and dynamic performance. The input offset voltage is under 200 μ V eliminating the need for offset nulling. Open-loop gain exceeds 350,000 into a 2k Ω load insuring excellent gain accuracy and linearity, even in high closed-loop gain applications. The slew rate of the OP-62 is 15V/ μ s with a wide gain bandwidth of 50MHz. Input noise voltage density is only 2.5nV/ $\sqrt{\text{Hz}}$ @ 1kHz, reducing overall system noise.

The OP-63 utilizes emitter degeneration to increase the slew rate to 50V/ μ s. Gain bandwidth remains unchanged at 50MHz. Input offset voltage of the OP-63 is under 750 μ V with an open-loop gain of over 100,000 into a 2k Ω load.

The OP-64 is decompensated and is stable in gains of 5 or greater. Slew rate of the OP-64 is a very fast 200V/ μ s with a gain bandwidth of 200MHz. The OP-64 has an input offset voltage below 750 μ V and an open-loop gain above 100,000 into a 2k Ω load. Input noise voltage density of the OP-63 and OP-64 is a low 7nV/ $\sqrt{\text{Hz}}$ @ 1kHz.

In other high-speed, high-bandwidth amplifiers, speed and bandwidth are increased at the expense of added supply

PIN CONNECTIONS



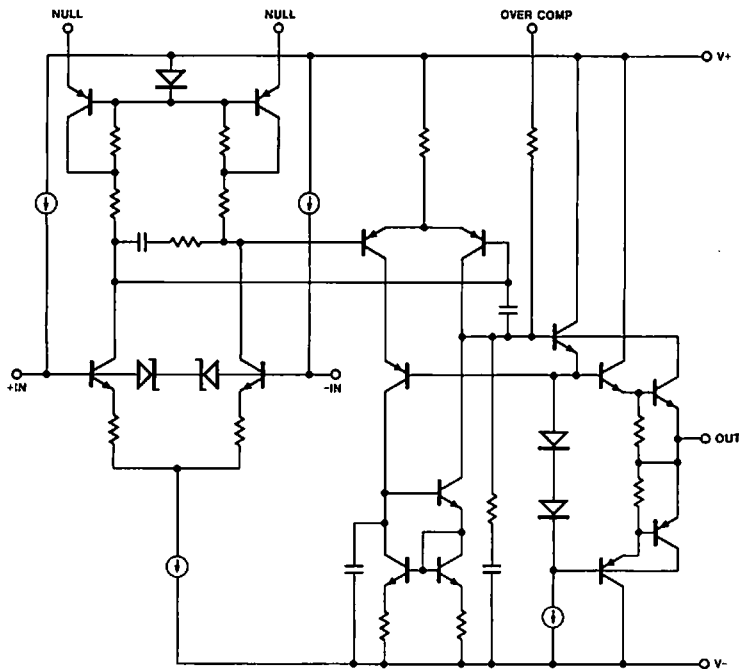
This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

current. With a supply current under 7mA, the OP-62/63/64 series is a significant improvement over other high-speed, high-bandwidth amplifiers. The OP-62/63/64 series conforms to the standard 741 pinout with nulling to V_+ .

The outstanding precision and dynamic performance of the OP-62/63/64 series make these amplifiers ideally suited to applications requiring accurate signal processing over a wide

frequency range. Other applications include high frequency active filters, oscillators, RF and pulse amplifiers, and high-speed comparators. The frequency response of the OP-62/63/64 can be adjusted to exact design requirements by means of an optional external bandwidth control capacitor connected to the over-compensation pin. This reduces system noise and increases stability with large capacitive loads.

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS (Note 2)**

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	
P, RC, S, Z Package	500mW
Differential Input Voltage (Note 3)	±5.0V
Differential Input Current (Note 3)	±25mA
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
P, RC, S, Z Package	–65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature (T _J)	–65°C to +150°C
Operating Temperature Range	
All A Grades	–55°C to +125°C
All E, F & G Grades	–40°C to +85°C

NOTES:

1. See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Cerdip (Z)	75°C	6.7mW/°C
20-Contact LCC (RC)	72°C	7.8mW/°C

2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

3. The OP-62/63/64's inputs are protected by back-to-back zener diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ±5.0V, the input current should be limited to ±25mA.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS		OP-62E OP-63E OP-64E			OP-62A/F OP-63A/F OP-64A/F			OP-62G OP-63G OP-64G			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}		OP-62 OP-63/64	—	—	200	—	—	300	—	—	500	μV
				—	—	750	—	—	1000	—	—	1500	
Input Bias Current	I _B	V _{CM} = 0V		—	—	300	—	—	400	—	—	500	nA
Input Offset Current	I _{OS}	V _{CM} = 0V		—	—	100	—	—	150	—	—	200	nA
Large-Signal Voltage Gain	A _{VO}	R _L ≥ 2kΩ V _O = ±10V	OP-62 OP-63/64	350	—	—	300	—	—	200	—	—	V/mV
				100	—	—	75	—	—	50	—	—	
Common-Mode Rejection	CMR	V _{CM} = ±11V		110	—	—	110	—	—	100	—	—	dB
Power Supply Rejection Ratio	PSRR	V _S = ±8V to ±18V	OP-62 OP-63/64	—	—	5.6	—	—	5.6	—	—	10	μV/V
				—	—	10	—	—	10	—	—	17.8	
Input Voltage Range	IVR	(Note 1)		±13.5	—	—	±13.5	—	—	±13.5	—	—	V
Output Voltage Swing	V _O	R _L = 600Ω		±12	—	—	±12	—	—	±12	—	—	V
Input Noise Voltage Density	e _n	f _O = 1kHz	OP-62 OP-63/64	—	2.5	—	—	2.5	—	—	2.5	—	nV/√Hz
				—	7	—	—	7	—	—	7	—	
Gain Bandwidth	GBW	A _{VCL} = +1 A _{VCL} = +5	OP-62/63 OP-64	—	50	—	—	50	—	—	50	—	MHz
				—	200	—	—	200	—	—	200	—	
Slew Rate	SR	A _{VCL} = +1 A _{VCL} = +1 A _{VCL} = +5	OP-62 OP-63 OP-64	—	15	—	—	15	—	—	15	—	V/μs
				—	50	—	—	50	—	—	50	—	
				—	200	—	—	200	—	—	200	—	
Supply Current	I _{SY}	No Load		—	—	7	—	—	7	—	—	7	mA

NOTE:

1. Guaranteed by CMR test.

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- **Very High Slew Rate** 200V/ μ s Typ
- **Very High Bandwidth** 150MHz Typ
- **High Output Drive** ± 50 mA Min
- **Low Offset Voltage** 2mV Max
- **High Gain** 100,000 Min
- **Low Power Consumption** 250mW Max
- **Unity-Gain Stable**
- **Standard 8-Pin Packages**

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE				OPERATING TEMPERATURE RANGE
	TO-99	CERDIP	PLASTIC	LCC	
2	OP65EJ	OP65EZ	—	—	XIND
3	OP65AJ*	OP65AZ*	—	OP65ARC/883	MIL
3	OP65FJ	OP65FZ	—	—	XIND
4	—	—	OP65GP	—	XIND
4	—	—	OP65GS††	—	XIND

* For devices processed in total compliance to MIL-8TD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip and TO-can packages. For ordering information see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

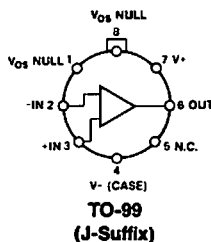
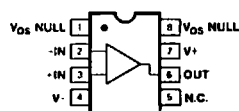
GENERAL DESCRIPTION

PMI's OP-65 features a gain-bandwidth of over 150MHz, a slew rate of 200V/ μ s and a full-power bandwidth of 9MHz for a 7V_{p-p} sine wave. The OP-65 has an input offset voltage under 2mV with an open-loop gain over 100,000 into a 500 Ω load, insuring

high gain accuracy. Power consumption of the OP-65 is under 250mW.

The unity-gain stability of the OP-65 makes it an ideal choice for video and pulse amplifier applications requiring low closed-loop gains. Other applications for the OP-65 include high-speed data acquisition systems, extremely fast sample-and-hold circuits, high frequency oscillators, and wideband ampli-

PIN CONNECTIONS



EPOXY MINI-DIP

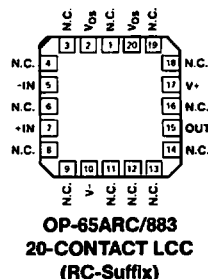
(P-Suffix)

8-PIN CERDIP

(Z-Suffix)

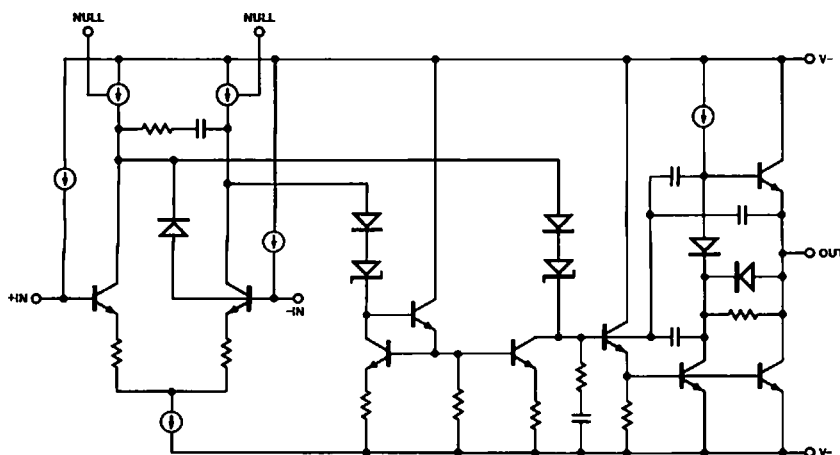
8-PIN SO

(S-Suffix)



OP-65ARC/883
20-CONTACT LCC
(RC-Suffix)

SIMPLIFIED SCHEMATIC



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



fiers. The OP-65 conforms to the standard OP-07 pinout with nulling to V+ and is available in the space-saving 8-pin package. The footprint of the OP-65 matches the HA-2541. The OP-65 can upgrade the HA-2541 in reduced supply applications.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±7V
Internal Power Dissipation (Note 1)	
P, RC, S, Z Packages	500mW
Differential Input Voltage	±5V
Input Voltage	Supply Voltage
Storage Temperature Range	
P, RC, S, Z Packages	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

DICE Junction Temperature (T_j) -65°C to +150°C

Operating Temperature Range

 OP-65A -55°C to +125°C

 OP-65E, OP-65F, OP-65G -40°C to +85°C

NOTES:

1. See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Cerdip (Z)	75°C	6.7mW/°C
20-Contact LCC (RC)	72°C	7.8mW/°C

2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 5V$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-65E			OP-65A/F			OP-65G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	—	2	—	—	3	—	—	4	mV
Input Bias Current	I_B	$V_{CM} = 0V$	—	—	2.5	—	—	4	—	—	5	μA
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	—	2	—	—	3	—	—	4	μA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 3.5V$ $R_L \geq 500\Omega$	100	—	—	35	—	—	25	—	—	V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm 2.5V$	85	—	—	85	—	—	80	—	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 6V$	—	—	32	—	—	56	—	—	56	$\mu\text{V/V}$
Input Voltage Range	IVR	(Note 1)	±2.5	—	—	±2.5	—	—	±2.5	—	—	V
Output Voltage Swing	V_O	$R_L = 500\Omega$	±3.5	—	—	±3.5	—	—	±3.5	—	—	V
Output Current	I_O		±50	—	—	±50	—	—	±50	—	—	mA
Gain Bandwidth	GBW	$A_V = +10$	—	150	—	—	150	—	—	150	—	MHz
Slew Rate	SR	$A_V = +1$	—	200	—	—	200	—	—	200	—	V/ μs
Supply Current	I_{SY}	No Load	—	—	25	—	—	25	—	—	25	mA

NOTES:

1. Guaranteed by CMR test.

Precision Monolithics Inc.

FEATURES

- Outstanding Gain Linearity
- Ultra High Gain 5000V/mV Min
- Low V_{OS} Over Temperature 60 μ V Max
- Excellent TCV_{OS} 0.3 μ V/ $^{\circ}$ C Max
- High PSRR 3 μ V/V Max
- High CMRR 1.0 μ V/V Max
- Low Power Consumption 60mW Max
- Fits OP-07, 725, 108A/308A, 741 Sockets

ORDERING INFORMATION†

PACKAGE				OPERATING TEMPERATURE RANGE
TO-99	CERDIP	PLASTIC	LCC	
OP77AJ*	OP77AZ*	—	—	MIL
OP77EJ	OP77EZ	—	—	IND
—	—	OP77EP	—	COM
OP77BJ*	OP77BZ*	—	OP77BRC/883	MIL
OP77FJ	OP77FZ	—	—	IND
—	—	OP77FP	—	COM
—	—	OP77GP	—	COM
—	—	OP77GS††	—	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

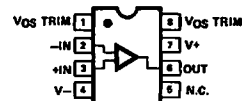
GENERAL DESCRIPTION

The OP-77 significantly advances the state-of-the-art in precision op amps. The OP-77's outstanding gain of 10,000,000 or more is maintained over the full ± 10 V output range. This exceptional gain-linearity eliminates incorrectable system nonlinearities common in previous monolithic op amps, and provides superior performance in high closed-loop-gain applications.

Low initial V_{OS} drift and rapid stabilization time, combined with only 50mW power consumption, are significant improvements over previous designs. These characteristics, plus the exceptional TCV_{OS} of 0.3 μ V/ $^{\circ}$ C maximum and the low V_{OS} of 25 μ V maximum, eliminates the need for V_{OS} adjustment and increases system accuracy over temperature.

PSRR of 3 μ V/V (110dB) and CMRR of 1.0 μ V/V maximum virtually eliminate errors caused by power supply drifts and common-mode signals. This combination of outstanding characteristics makes the OP-77 ideally suited for high-resolution instrumentation and other tight error budget systems.

PIN CONNECTIONS



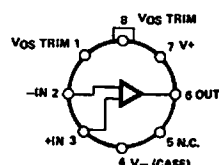
EPOXY MINI-DIP (P-Suffix)

8-PIN HERMETIC DIP

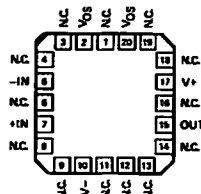
(Z-Suffix)

8-PIN SO

(S-Suffix)



TO-99 (J-Suffix)

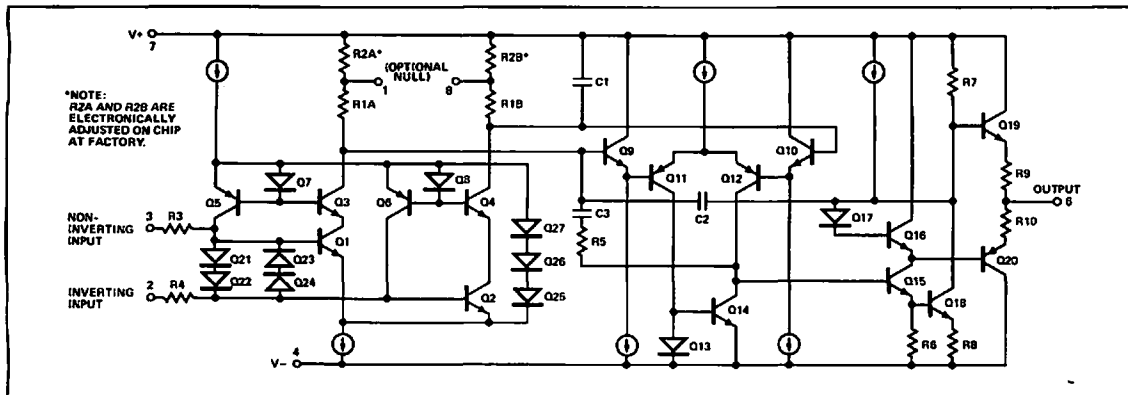


OP-77BRC/883

LCC

(RC-Suffix)

SIMPLIFIED SCHEMATIC





This product is available in five standard grades and four standard packages: the TO-99 can, the 8-pin mini-dip in ceramic or epoxy, and the 20-pin LCC.

The OP-77 is a direct or upgrade replacement for the OP-07, 05, 725, or 108A op amps. 741-types can be replaced by eliminating the V_{OS} adjust pot.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
J, Z, and RC Packages	-65°C to +150°C
P Package	-65°C to +125°C
Operating Temperature Range	
OP-77A, OP-77B (J, Z, RC)	-55°C to +125°C

OP-77E, OP-77F (J, Z)	-25°C to +85°C
OP-77E, OP-77F, OP-77G (P or S)	0°C to 70°C
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_J)	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
LCC	80°C	7.8mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77A			OP-77B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	10	25	—	20	60	μV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)	—	0.2	—	—	0.2	—	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	2.8	nA
Input Bias Current	I_B		-0.2	1.2	2.0	-0.2	1.2	2.8	nA
Input Noise Voltage	e_{n-p-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 2)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000\text{Hz}$ (Note 2)	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i_{n-p-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$ (Note 2)	—	0.32	0.80	—	0.32	0.60	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000\text{Hz}$ (Note 2)	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	26	45	—	18.5	45	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	G Ω
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	1.6	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.7	3	—	0.7	3	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	5000	12000	—	2000	8000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±13.5	±14.0	—	±13.5	±14.0	—	V
		$R_L \geq 2k\Omega$	±12.5	±13.0	—	±12.5	±13.0	—	
		$R_L \geq 1k\Omega$	±12.0	±12.5	—	±12.0	±12.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	—	0.1	0.3	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 2)	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O		—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	50	60	—	50	60	mW
		$V_S = \pm 3V$, No Load	—	3.5	4.5	—	3.5	4.5	
Offset Adjustment Range		$R_P = 20k\Omega$	—	±3	—	—	±3	—	mV

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV .

2. Sample tested.

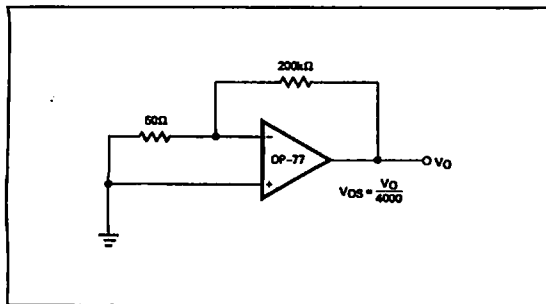
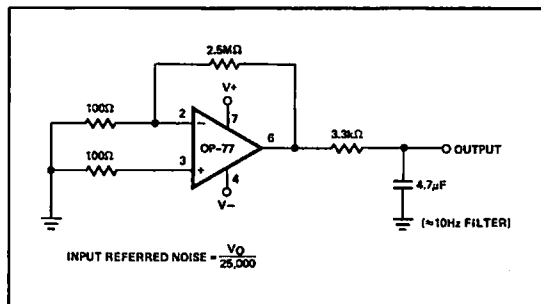
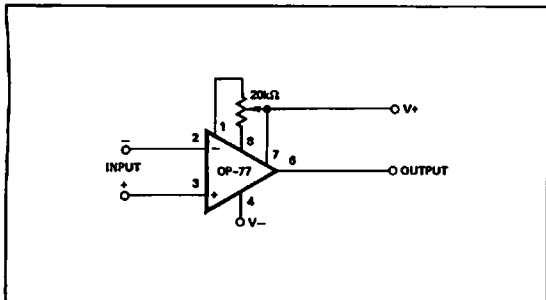
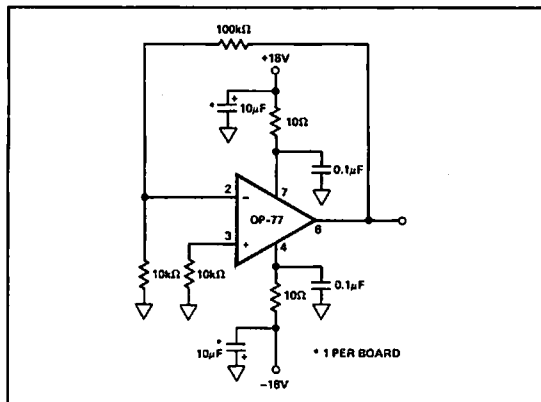
3. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77A			OP-77B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	25	60	—	45	120	μV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.1	0.3	—	0.2	0.6	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.5	2.2	—	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	1.5	25	—	1.5	50	$pA/^\circ C$
Input Bias Current	I_B		-0.2	2.4	4	-0.2	2.4	6	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	25	—	15	35	$pA/^\circ C$
Input Voltage Range	IVR		± 13	± 13.5	—	± 13	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	3	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	1	3	—	1	5	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	2000	6000	—	1000	4000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13.0	—	± 12	± 13.0	—	V
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	60	75	—	60	75	mW

NOTES:

- OP-77A: TCV_{OS} is 100% tested.
- Guaranteed by end-point limits.

TYPICAL OFFSET VOLTAGE TEST CIRCUIT

TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT

OPTIONAL OFFSET NULLING CIRCUIT

BURN-IN CIRCUIT


**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77E			OP-77F			OP-77G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	10	25	—	20	60	—	50	100	μV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 1)	—	0.3	—	—	0.4	—	—	0.4	—	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	2.8	—	0.3	2.8	nA
Input Bias Current	I_B		-0.2	1.2	2.0	-0.2	1.2	2.8	-0.2	1.2	2.8	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.38	0.65	—	0.38	0.65	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.5	20.0	—	10.5	20.0	$nV/\sqrt{Hz}$
		$f_O = 100\text{Hz}$ (Note 2)	—	10.0	13.0	—	10.2	13.5	—	10.2	13.5	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.8	11.5	—	9.8	11.5	
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	15	35	—	15	35	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.35	0.90	—	0.35	0.90	$pA/\sqrt{Hz}$
		$f_O = 100\text{Hz}$ (Note 2)	—	0.14	0.23	—	0.15	0.27	—	0.15	0.27	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.13	0.18	—	0.13	0.18	
Input Resistance — Differential-Mode	R_{IN}	(Note 3)	26	45	—	18.5	45	—	18.5	45	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	200	—	—	200	—	—	200	—	G Ω
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	1.6	—	0.1	1.6	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.7	3.0	—	0.7	3.0	—	0.7	3.0	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	5000	12000	—	2000	6000	—	2000	6000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 13.5	± 14.0	—	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
		$R_L \geq 2k\Omega$	± 12.5	± 13.0	—	± 12.5	± 13.0	—	± 12.5	± 13.0	—	
		$R_L \geq 1k\Omega$	± 12.0	± 12.5	—	± 12.0	± 12.5	—	± 12.0	± 12.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3	—	0.1	0.3	—	0.1	0.3	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$ (Note 2)	0.4	0.6	—	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	R_O		—	60	—	—	60	—	—	60	—	Ω
Power Consumption	P_d	$V_S = \pm 15V$, No Load	—	50	60	—	50	60	—	50	60	mW
		$V_S = \pm 3V$, No Load	—	3.5	4.5	—	3.5	4.5	—	3.5	4.5	
Offset Adjustment Range		$R_P = 20k\Omega$	—	± 3	—	—	± 3	—	—	± 3	—	mV

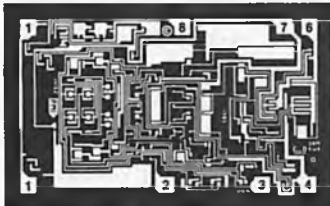
NOTES:

- Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$.
- Sample tested.
- Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-77E/FJ and OP-77E/FZ, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-77E/F/GP/GS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-77E			OP-77F			OP-77G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	J, Z Packages P Package	—	10	45	—	20	100	—	—	—	μV
Average Input Offset Voltage Drift	TCV_{OS}	J, Z Packages P Package (Note 1)	—	0.1	0.3	—	0.2	0.6	—	—	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	0.5	2.2	—	0.5	4.5	—	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	1.5	40	—	1.5	85	—	1.5	85	$pA/^\circ C$
Input Bias Current	I_B		-0.2	2.4	4.0	-0.2	2.4	6.0	-0.2	2.4	6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	—	8	40	—	15	60	—	15	60	$pA/^\circ C$
Input Voltage Range	IVR		± 13.0	± 13.5	—	± 13.0	± 13.5	—	± 13.0	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	—	0.1	1.0	—	0.1	3.0	—	0.1	3.0	$\mu V/V$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	1.0	3.0	—	1.0	5.0	—	1.0	5.0	$\mu V/V$

DICE CHARACTERISTICS



DIE SIZE 0.093×0.057 inch, 5301 sq. mils
(2.36×1.45 mm, 3.42 sq. mm)

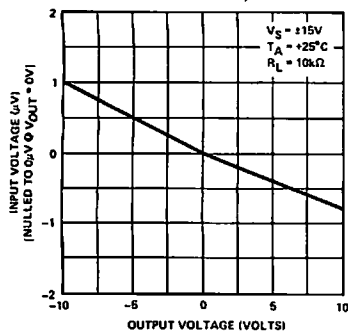
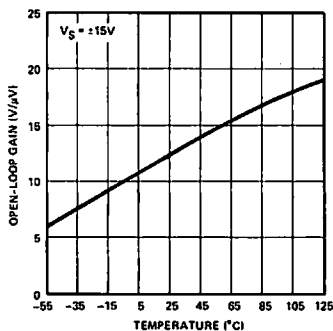
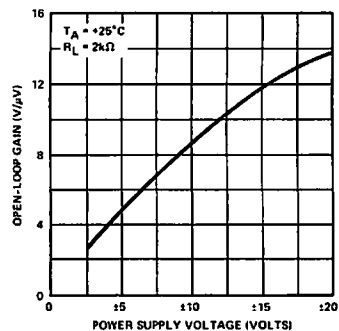
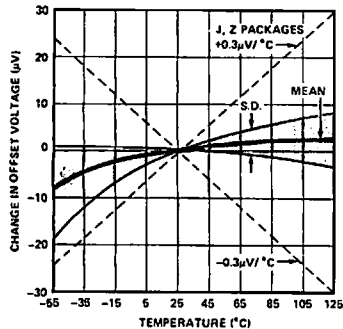
1. BALANCE
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V^-
6. OUTPUT
7. V^+
8. BALANCE

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

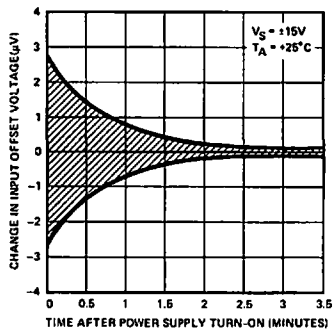
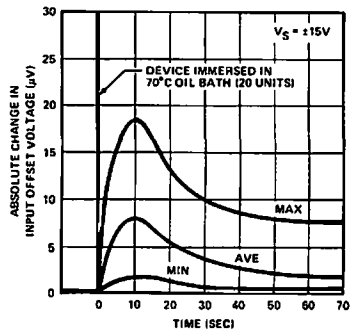
WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for OP-77N/G devices.

PARAMETER	SYMBOL	CONDITIONS	OP-77N LIMIT	OP-77G LIMIT	UNITS
Input Offset Voltage	V_{OS}		40	75	μV MAX
Input Offset Current	I_{OS}		2.0	2.8	nA MAX
Input Bias Current	I_B		± 2	± 2.8	nA MAX
Input Resistance Differential-Mode	R_{IN}	(Note 1)	26	17	M Ω MIN
Input Voltage Range	IVR		± 13	± 13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	1	1.6	$\mu V/V$ MAX
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	3	3	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 13.5	± 13.5	V MIN
		$R_L = 2k\Omega$	± 12.5	± 12.5	
		$R_L = 1k\Omega$	± 12.0	± 12.0	
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	2000	1000	V/mV MIN
Differential Input Voltage			± 30	± 30	V MAX

TYPICAL PERFORMANCE CHARACTERISTICS

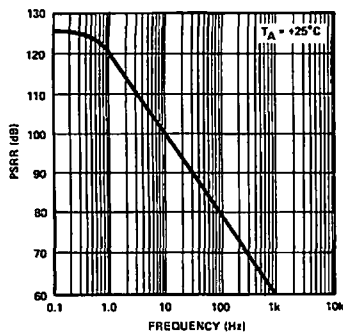
GAIN LINEARITY (INPUT
VOLTAGE vs OUTPUT
VOLTAGE)OPEN-LOOP GAIN
vs TEMPERATUREOPEN-LOOP GAIN vs POWER
SUPPLY VOLTAGEUNTRIMMED OFFSET
VOLTAGE vs TEMPERATURE

WARM-UP DRIFT

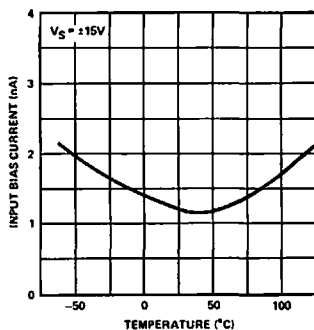
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DUE TO THERMAL SHOCKCLOSED-LOOP RESPONSE
FOR VARIOUS GAIN
CONFIGURATIONS

TYPICAL PERFORMANCE CHARACTERISTICS

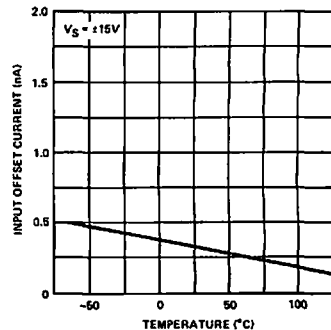
PSRR vs FREQUENCY



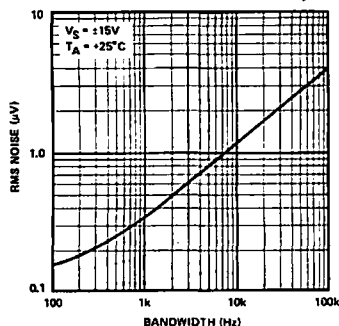
INPUT BIAS CURRENT vs TEMPERATURE



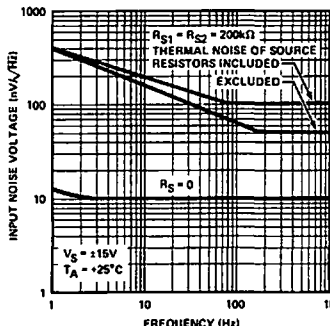
INPUT OFFSET CURRENT vs TEMPERATURE



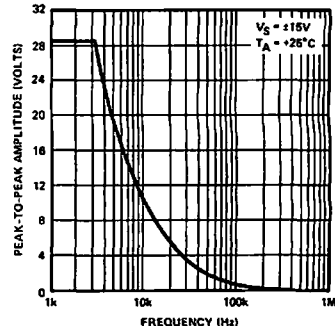
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



TOTAL INPUT NOISE VOLTAGE vs FREQUENCY

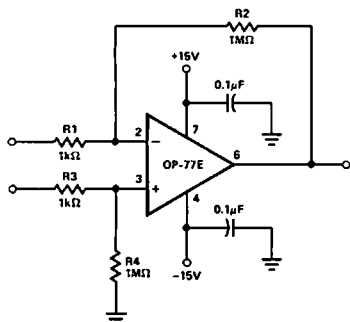


MAXIMUM OUTPUT SWING vs FREQUENCY



APPLICATIONS INFORMATION

PRECISION HIGH-GAIN DIFFERENTIAL AMPLIFIER



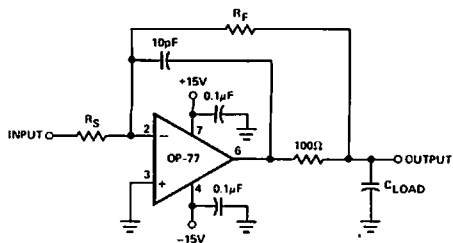
The high gain, gain linearity, CMRR, and low TCV_{OS} of the OP-77 make it possible to obtain performance not previously available in single stage very high-gain amplifier applications.

For best CMR, $\frac{R_1}{R_2}$ must equal $\frac{R_3}{R_4}$. In this example,

with a 10mV differential signal, the maximum errors are as listed.

TYPE	AMOUNT
COMMON-MODE VOLTAGE	0.01%/V
GAIN LINEARITY, WORST CASE	0.02%
TCV_{OS}	0.003%/°C
TCI_{OS}	0.008%/°C

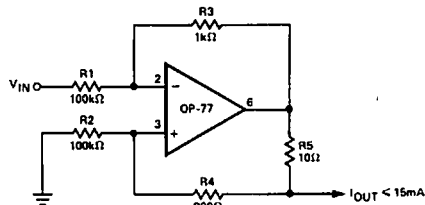
ISOLATING LARGE CAPACITIVE LOADS



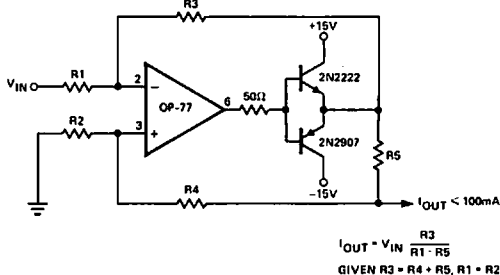
This circuit reduces maximum slew-rate but allows driving capacitive loads of any size without instability. Because the 100Ω resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open-loop gain of the OP-77.

BILATERAL CURRENT SOURCE

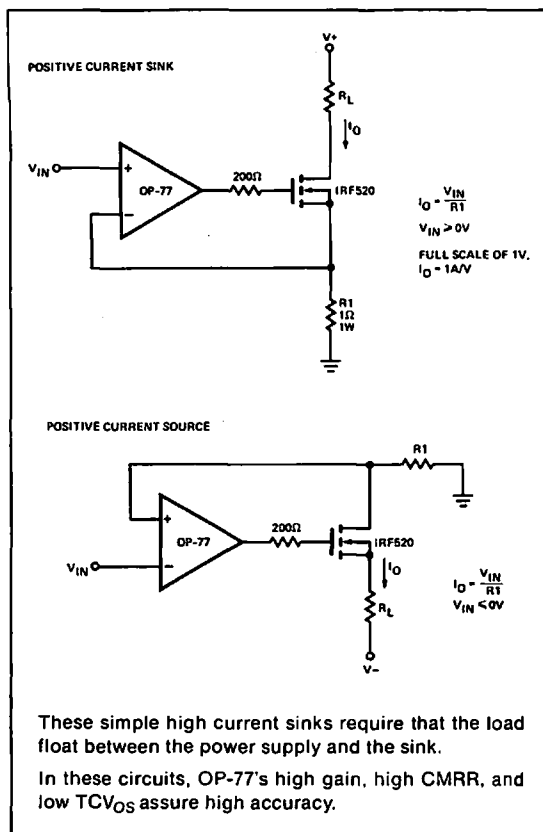
BASIC CURRENT SOURCE



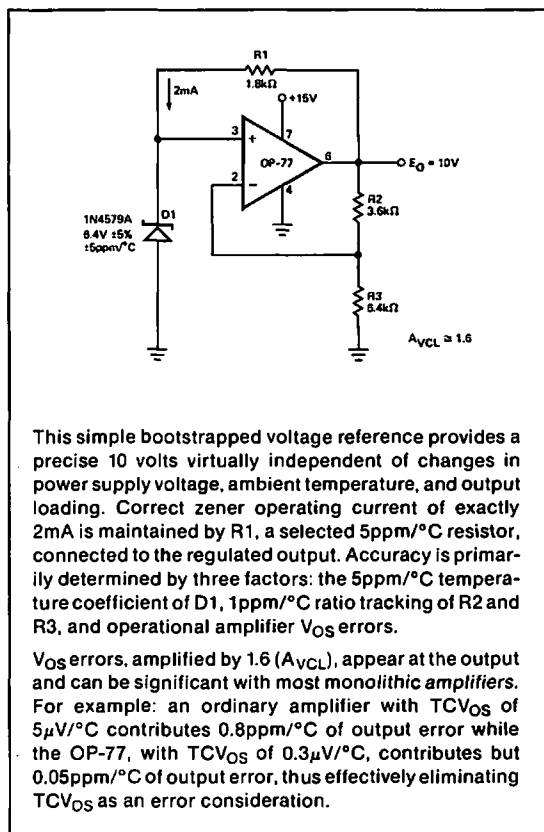
100mA CURRENT SOURCE



PRECISION CURRENT SINKS

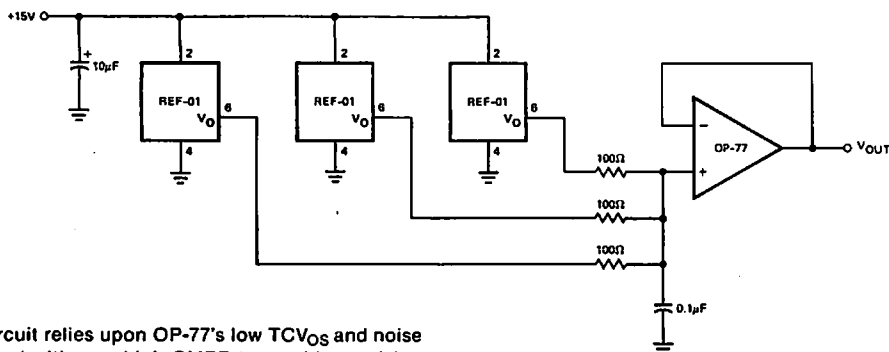


HIGH STABILITY VOLTAGE REFERENCE



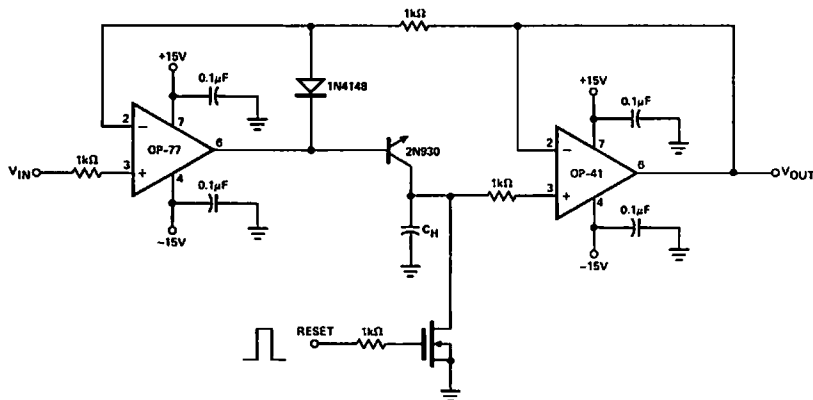
This simple bootstrapped voltage reference provides a precise 10 volts virtually independent of changes in power supply voltage, ambient temperature, and output loading. Correct zener operating current of exactly 2mA is maintained by R1, a selected 5ppm/°C resistor, connected to the regulated output. Accuracy is primarily determined by three factors: the 5ppm/°C temperature coefficient of D1, 1ppm/°C ratio tracking of R2 and R3, and operational amplifier V_{OS} errors.

LOW NOISE PRECISION REFERENCE



This circuit relies upon OP-77's low TCV_{OS} and noise combined with very high CMRR to provide precision buffering of the averaged REF-01 voltage outputs.

PRECISION POSITIVE PEAK DETECTOR

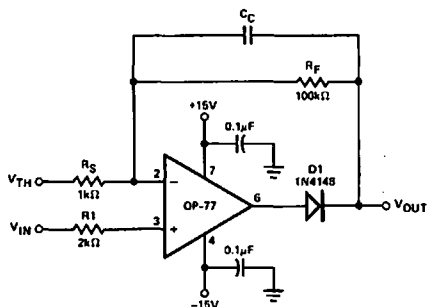


C_H must be of polystyrene, Teflon*, or polyethylene to minimize dielectric absorption and leakage. The droop

rate is determined by the size of C_H and the bias current of the OP-41.

*Teflon is a registered trademark of the Dupont Company.

PRECISION THRESHOLD DETECTOR/ AMPLIFIER

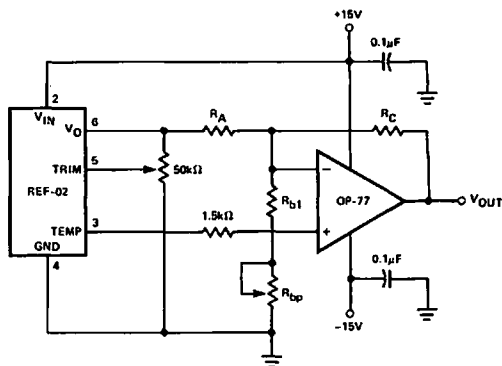


When $V_{IN} < V_{TH}$, amplifier output swings negative, reverse biasing diode D1. $V_{OUT} = V_{TH}$ if $R_L = \infty$.
When $V_{IN} \geq V_{TH}$, the loop closes,

$$V_{OUT} = V_{TH} + (V_{IN} - V_{TH}) \left(1 + \frac{R_F}{R_S} \right)$$

C_C is selected to smooth the response of the loop.

PRECISION TEMPERATURE SENSOR



RESISTOR VALUES

TCV _{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	-55°C to +125°C	-55°C to +125°C	-67°F to +257°F
OUTPUT VOLTAGE RANGE	-0.55V to +1.25V	-5.5V to +12.5V	-0.67V to +2.57V
ZERO-SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
R_A (±1% Resistor)	9.09kΩ	15kΩ	7.5kΩ
R_{B1} (±1% Resistor)	1.5kΩ	1.82kΩ	1.21kΩ
R_{BP} (Potentiometer)	200Ω	500Ω	200Ω
R_C (±1% Resistor)	5.11kΩ	84.5kΩ	8.25kΩ



OP-80

ULTRA-LOW BIAS CURRENT OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Ultra-Low Bias Current (25°C) 60fA Max
- High-Temp Bias Current (125°C) 20pA Max
- Low Supply Current 300μA Max
- True Single-Supply Operation
 - Common-Mode Range Includes Ground
 - Output Swings to Within 400μV of Ground
- Extended Industrial Temp Range -40°C to +85°C

ORDERING INFORMATION†

I _b (pA)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-99	PLASTIC	
0.150	OP80AJ*	—	MIL
0.060	OP80EJ	—	XIND
0.300	OP80FJ	—	XIND
2.5	OP80GJ	OP80GP	XIND
2.5	—	OP80GST††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

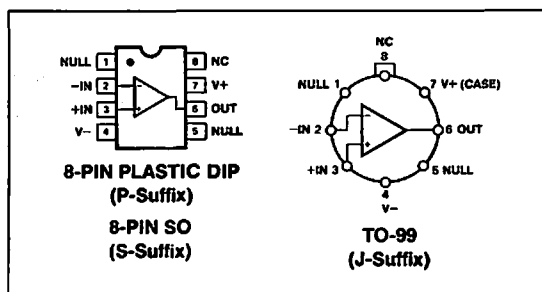
GENERAL DESCRIPTION

The OP-80 CMOS operational amplifier offers exceptionally low bias currents over its entire operating temperature range. At

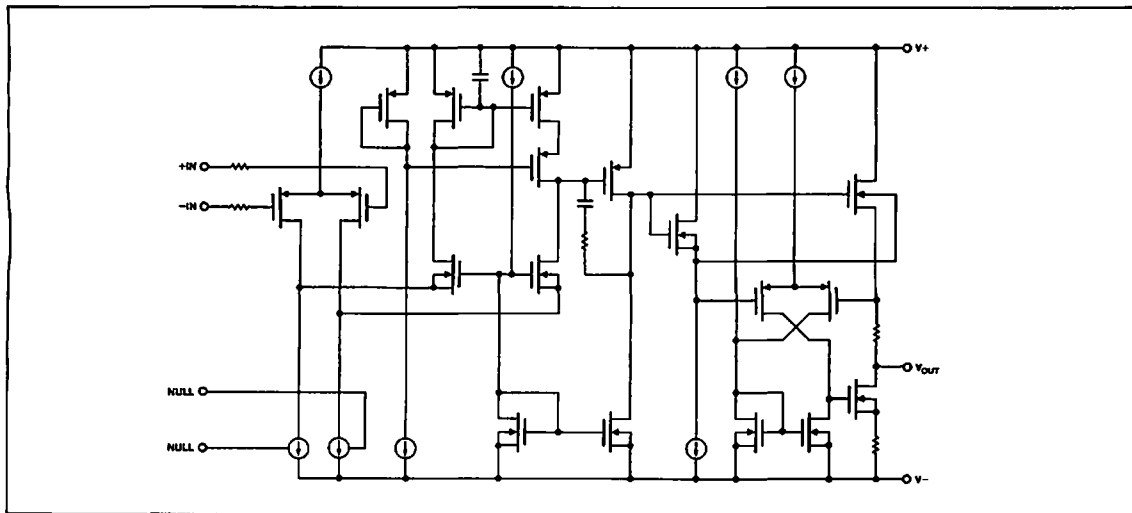
125°C, the OP-80 typically has a bias current of only 10pA. During room-temperature operation, the OP-80's bias current is equivalent to a mere 125 electrons per millisecond, only 20fA typical. The OP-80 is capable of operation with either single or dual supplies. Its low cost makes it attractive as a general-purpose amplifier for low-voltage systems, as well as systems demanding the highest level of precision in current-to-voltage conversion.

The low supply current minimizes thermal power dissipation, virtually eliminating the effects of chip self-heating. System power-supply demand is reduced as well, resulting in lower overall costs. The OP-80's CMOS design gives a good speed/power ratio, permitting a 0.2V/μs minimum slew rate and a 300kHz gain-bandwidth product with unity-gain stability.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Manufactured under U.S. Patent Number: 4,675,561.

This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



With single 5V supply operation, the OP-80 has a full-power bandwidth of 10kHz.

Capable of driving reasonable loads, the OP-80 offers greater than 100dB of gain into a 2k Ω load. Its output will source or sink more than 16mA of current. In single supply applications, the OP-80's input range and output swing both include ground. No pull-down resistor is required for the output to actively swing to ground.

Applications for the OP-80 include precision pH, conductivity and ion measurement systems, low-level light and infrared detectors, barcode readers, and magnetic and electric field detectors. Its exceptional value makes it suitable for many general-purpose applications, especially those using a single 5V supply.

The OP-80 conforms to the industry-standard 741 pinout, with the nulling potentiometer between pins 1 and 5, and the wiper to V₋.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	$\pm 8V$
Internal Power Dissipation (Note 2)	500mW

Input Voltage (Note 3)	+8V, -8.2V
Differential Input Voltage (Note 3)	16V
Output Short-Circuit Duration (Note 4)	Indefinite
Operating Temperature Range	
OP-80A (J)	-55°C to +125°C
OP-80E, F, G (J, P, S)	-40°C to +85°C
Storage Temperature Range	-65°C to 175°C
Junction Temperature Range	-65°C to 175°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. See table for maximum ambient temperature and rating.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

3. For supply voltages less than $\pm 8V$, the absolute maximum input voltage is equal to (V₊) and (V₋ - 0.2V).
4. The output may be shorted to ground indefinitely, but current must be externally limited to 25mA if the output is shorted to V₊.

ELECTRICAL CHARACTERISTICS at V_S = $\pm 5V$, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-80E			OP-80F			OP-80G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}		—	0.4	1	—	0.6	2	—	0.6	2	mV
Input Offset Current	I _{OS}		—	10	—	—	20	—	—	50	—	IA
Input Bias Current	I _B		—	20	60	—	40	300	—	200	2500	IA
Input Voltage Range	IVR	Lower Limit Upper Limit			(V ₋ - 0.2V) (V ₊ - 1.3V)			(V ₋ - 0.2V) (V ₊ - 1.3V)			(V ₋ - 0.2V) (V ₊ - 1.3V)	V
Common-Mode Rejection	CMR	V _{CM} = -5V, 3.7V	60	75	—	60	75	—	60	75	—	dB
Power-Supply Rejection	PSR	V _S = $\pm 2.25V$ to $\pm 8V$	60	75	—	60	75	—	60	75	—	dB
Large-Signal Voltage Gain	A _{VO}	V _O = -4.5V to +3.5V R _L = 10k Ω	100	400	—	80	350	—	80	350	—	V/mV
		R _L = 2k Ω	80	350	—	75	300	—	75	300	—	
		V _S = 0V, +5V; R _L = 10k Ω	+3.7 +0.0004	+4.0 —	— —	+3.7 +0.0004	+4.0 —	— —	+3.7 +0.0004	+4.0 —	— —	
Output Voltage Swing	V _O	V _S = $\pm 5V$ R _L = 10k Ω	+3.7 -4.8	+3.9 -4.9	— —	+3.7 -4.8	+3.9 -4.9	— —	+3.7 -4.8	+3.9 -4.9	— —	V
		V _S = $\pm 5V$ R _L = 2k Ω	+3.4 -4.7	+3.6 -4.8	— —	+3.4 -4.7	+3.6 -4.8	— —	+3.4 -4.7	+3.6 -4.8	— —	
Supply Current	I _{SV}	No Load	—	170	300	—	170	300	—	170	300	μA
Input Noise Voltage Density	e _n	f _O = 1000Hz	—	70	—	—	70	—	—	70	—	nV/ $\sqrt{Hz}$
Output Current	I _{OUT}	Source	25	40	—	25	40	—	25	40	—	mA
		Sink	15	22	—	15	22	—	15	22	—	
Slew Rate	SR	A _V = +1	0.2	0.4	—	0.2	0.4	—	0.2	0.4	—	V/ μs
Gain-Bandwidth Product	GBW	f _O = 10kHz	100	300	—	100	300	—	100	300	—	kHz
Input Resistance		Common-Mode	—	10 ¹⁶	—	—	10 ¹⁶	—	—	10 ¹⁶	—	Ω
		Differential	—	10 ¹³	—	—	10 ¹³	—	—	10 ¹³	—	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 5V$, $V_{CM} = 0V$, $T_A = 25^\circ C$ unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	OP-80A TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.4	1	mV
Input Offset Current	I_{OS}		—	20	—	IA
Input Bias Current	I_B		—	30	150	IA
Input Voltage Range	IVR	Lower Limit Upper Limit		(V - 0.2V) (V + 1.3V)		V
Common-Mode Rejection	CMR	$V_{CM} = -5V, 3.7V$	60	75	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2.25V$ to $\pm 8V$	60	75	—	dB
Large-Signal Voltage Gain	A_{VO}	$V_O = -4.5V$ to $+3.5V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	100 80	400 350	—	V/mV
Output Voltage Swing	V_O	$V_S = 0V, +5V$; $R_L = 10k\Omega$	+3.7 +0.0004	+4.0 —	—	V
		$V_S = \pm 5V$ $R_L = 10k\Omega$	+3.7 -4.8	+3.9 -4.9	—	
		$V_S = \pm 5V$ $R_L = 2k\Omega$	+3.4 -4.7	+3.6 -4.8	—	
Supply Current	I_{SY}	No Load	—	170	300	μA
Input Noise Voltage Density	e_n	$f_O = 1000Hz$	—	70	—	$nV/\sqrt{Hz}$
Output Current	I_{OUT}	Source Sink	25 15	40 22	—	mA
Slew Rate	SR	$A_V = +1$	0.2	0.4	—	V/ μs
Gain-Bandwidth Product	GBW	$f_O = 10kHz$	100	300	—	kHz
Input Resistance		Common-Mode	—	10^{16}	—	Ω
		Differential	—	10^{13}	—	



OP-90

PRECISION LOW-VOLTAGE MICROPOWER OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Single/Dual Supply Operation +1.6V to +36V
..... $\pm 0.8V$ to $\pm 18V$
- True Single-Supply Operation; Input and Output Voltage Ranges Include Ground
- Low Supply Current 20 μA Max
- High Output Drive 5mA Min
- Low Input Offset Voltage 150 μV Max
- High Open-Loop Gain 700V/mV Min
- Outstanding PSRR 5.6 $\mu V/V$ Max
- Standard 741 Pinout With Nulling to V-

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC DIP 8-PIN	PLASTIC 8-PIN	
150	OP90AZ*	—	MIL
150	OP90EZ	—	IND
250	OP90FZ	—	IND
450	—	OP90GP	COM
450	—	OP90GS††	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

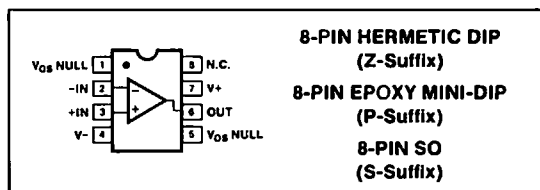
GENERAL DESCRIPTION

The OP-90 is a high performance micropower op amp that operates from a single supply of +1.6V to +36V or from dual supplies of ± 0.8 to $\pm 18V$. Input voltage range includes the negative rail allowing the OP-90 to accommodate input signals down to ground in single supply operation. The OP-90's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

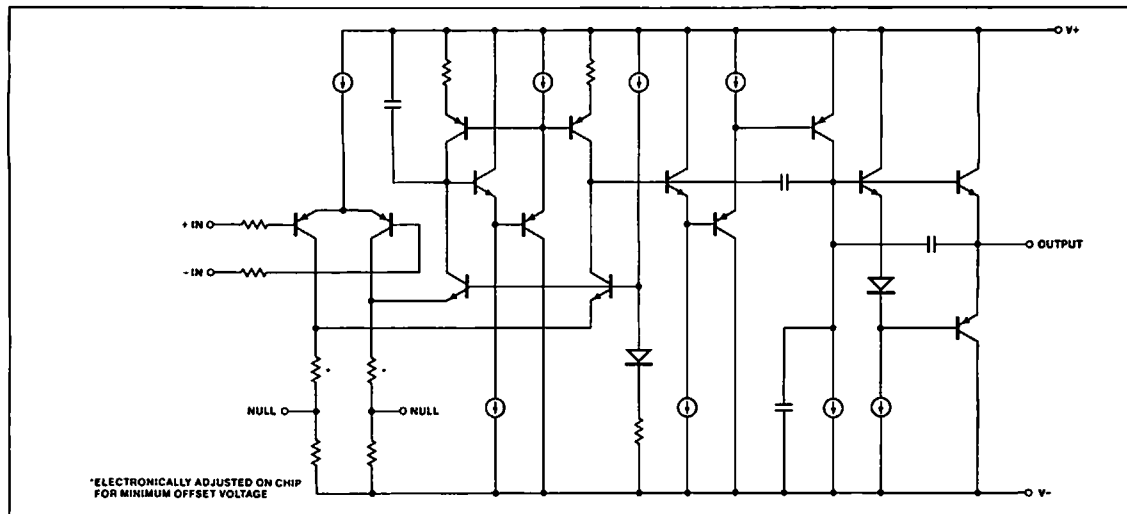
The OP-90 draws less than 20 μA of quiescent supply current, while able to deliver over 5mA of output current to a load. Input offset voltage is below 150 μV eliminating the need for external nulling. Gain exceeds 700,000 and common-mode rejection is better than 100dB. The power supply-rejection ratio of under 5.6 $\mu V/V$ minimizes offset voltage changes experienced in battery powered systems.

The low offset voltage and high gain offered by the OP-90 bring precision performance to micropower applications. The minimal voltage and current requirements of the OP-90 suit it for battery and solar powered applications, such as portable instruments, remote sensors, and satellites.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	$\pm 18\text{V}$
Power Dissipation (Note 1)	500mW
Differential Input Voltage	$[(V-) - 20\text{V}]$ to $[(V+) + 20\text{V}]$
Common-Mode Input Voltage	$[(V-) - 20\text{V}]$ to $[(V+) + 20\text{V}]$
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	
Z Package	-65°C to $+150^{\circ}\text{C}$
P Package	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	
OP-90A	-55°C to $+125^{\circ}\text{C}$
OP-90E, OP-90F	-25°C to $+85^{\circ}\text{C}$
OP-90G	0°C to $+70^{\circ}\text{C}$

DICE Junction Temperature (T_j) -65°C to $+150^{\circ}\text{C}$
 Lead Temperature Range (Soldering, 60 sec) 300°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.
- Absolute maximum ratings apply to both packaged parts and DiCE, unless otherwise noted.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
8-Pin Plastic DIP (P)	36°C	$5.6\text{mW}/^{\circ}\text{C}$
8-Pin Hermetic DIP (Z)	75°C	$6.7\text{mW}/^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5\text{V}$ to $\pm 15\text{V}$, $T_A = +25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-90A/E			OP-90F			OP-90G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	50	150	—	75	250	—	125	450	μV
Input Offset Current	I_{OS}	$V_{CM} = 0\text{V}$	—	0.4	3	—	0.4	5	—	0.4	5	nA
Input Bias Current	I_B	$V_{CM} = 0\text{V}$	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$										
		$R_L = 100\text{k}\Omega$	700	1200	—	500	1000	—	400	800	—	
		$R_L = 10\text{k}\Omega$	350	600	—	250	500	—	200	400	—	
		$R_L = 2\text{k}\Omega$	125	250	—	100	200	—	100	200	—	
		$V+ = 5\text{V}$, $V- = 0\text{V}$, $1\text{V} < V_O < 4\text{V}$										V/mV
		$R_L = 100\text{k}\Omega$	200	400	—	125	300	—	100	250	—	
		$R_L = 10\text{k}\Omega$	100	180	—	75	140	—	70	140	—	
Input Voltage Range	IVR	$V+ = 5\text{V}$, $V- = 0\text{V}$ $V_S = \pm 15\text{V}$ (Note 2)	0/4	—	—	0/4	—	—	0/4	—	—	V
Output Voltage Swing	V_O	$V_S = \pm 15\text{V}$										
		$R_L = 10\text{k}\Omega$	± 14	± 14.2	—	± 14	± 14.2	—	± 14	± 14.2	—	V
		$R_L = 2\text{k}\Omega$	± 11	± 12	—	± 11	± 12	—	± 11	± 12	—	
	V_{OH}	$V+ = 5\text{V}$, $V- = 0\text{V}$ $R_L = 2\text{k}\Omega$	4.0	4.2	—	4.0	4.2	—	4.0	4.2	—	V
Common Mode Rejection	CMR	$V+ = 5\text{V}$, $V- = 0\text{V}$, $0\text{V} < V_{CM} < 4\text{V}$	90	110	—	80	100	—	80	100	—	dB
		$V_S = \pm 15\text{V}$, $-15\text{V} < V_{CM} < 13.5\text{V}$	100	130	—	90	120	—	90	120	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	1.0	5.6	—	3.2	10	$\mu\text{V}/\text{V}$
Slew Rate	SR	$V_S = \pm 15\text{V}$	5	12	—	5	12	—	5	12	—	V/ms
Supply Current	I_{SV}	$V_S = \pm 1.5\text{V}$	—	9	15	—	9	15	—	9	15	μA
		$V_S = \pm 15\text{V}$	—	14	20	—	14	20	—	14	20	
Capacitive Load Stability		$A_V = -1$ No Oscillations (Note 1)	250	650	—	250	650	—	250	650	—	pF
Input Noise Voltage	e_{np-p}	$f_O = 0.1\text{Hz}$ to 10Hz $V_S = \pm 15\text{V}$	—	3	—	—	3	—	—	3	—	μV_{p-p}
Input Resistance Differential Mode	R_{IN}	$V_S = \pm 15\text{V}$	—	30	—	—	30	—	—	30	—	M Ω
Input Resistance Common Mode	R_{INCM}	$V_S = \pm 15\text{V}$	—	20	—	—	20	—	—	20	—	G Ω

NOTES:

- Guaranteed but not 100% tested.
- Guaranteed by CMR test.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 1.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

			OP-90A			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	80	400	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	2.5	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	1.5	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.0	20	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_O = \pm 10V$				
		$R_L = 100k\Omega$	225	400	—	
		$R_L = 10k\Omega$	125	240	—	
		$R_L = 2k\Omega$	50	110	—	
		$V_+ = 5V, V_- = 0V,$ $1V < V_O < 4V$				V/mV
		$R_L = 100k\Omega$	100	200	—	
		$R_L = 10k\Omega$	50	110	—	
Input Voltage Range	IVR	$V_+ = 5V, V_- = 0V$ $V_S = \pm 15V$ (Note 1)	0/3.5 -15/13.5	— —	— —	V
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 13.5 ± 10.5	± 13.7 ± 11.5	— —	V
	V_{OH}	$V_+ = 5V, V_- = 0V$ $R_L = 2k\Omega$	3.9	4.1	—	V
	V_{OL}	$V_+ = 5V, V_- = 0V$ $R_L = 10k\Omega$	—	100	500	μV
	Common Mode Rejection	CMR	$V_+ = 5V, V_- = 0V, 0V < V_{CM} < 3.5V$ $V_S = \pm 15V, -15V < V_{CM} < 13.5V$	85 95	105 115	— —
Power Supply Rejection Ratio	PSRR		—	3.2	10	$\mu V/V$
Supply Current	I_{SY}	$V_S = \pm 1.5V$	—	15	25	
		$V_S = \pm 15V$	—	19	30	μA

NOTE:

1. Guaranteed by CMR test.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$ for OP-90E/F, $0^\circ C \leq T_A \leq 70^\circ C$ for OP-90G, unless otherwise noted.

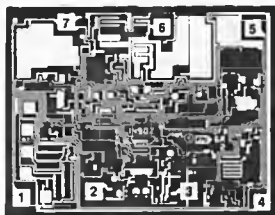
PARAMETER	SYMBOL	CONDITIONS	OP-90E			OP-90F			OP-90G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	70	270	—	110	550	—	180	675	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	2	—	0.6	5	—	1.2	5	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.8	3	—	1.0	5	—	1.3	7	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_O = \pm 10V$										V/mV
		$R_L = 100k\Omega$	500	800	—	350	700	—	300	600	—	
		$R_L = 10k\Omega$	250	400	—	175	350	—	150	250	—	
		$R_L = 2k\Omega$	100	200	—	75	150	—	75	125	—	
		$V_+ = 5V, V_- = 0V,$ $1V < V_O < 4V$										
		$R_L = 100k\Omega$	150	280	—	100	220	—	80	160	—	
		$R_L = 10k\Omega$	75	140	—	50	110	—	40	90	—	
Input Voltage Range	IVR	$V_+ = 5V, V_- = 0V$	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15\dot{V}$ (Note 1)	-15/13.5	—	—	-15/13.5	—	—	-15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm 15V$										V
		$R_L = 10k\Omega$	± 13.5	± 14	—	± 13.5	± 14	—	± 13.5	± 14	—	
		$R_L = 2k\Omega$	± 10.5	± 11.8	—	± 10.5	± 11.8	—	± 10.5	± 11.8	—	
	V_{OH}	$V_+ = 5V, V_- = 0V$										
		$R_L = 2k\Omega$	3.9	4.1	—	3.9	4.1	—	3.9	4.1	—	
	V_{OL}	$V_+ = 5V, V_- = 0V$									μV	
		$R_L = 10k\Omega$	—	100	500	—	100	500	—	100	500	
Common Mode Rejection	CMR	$V_+ = 5V, V_- = 0V,$ $0V < V_{CM} < 3.5V$	90	110	—	80	100	—	80	100	—	dB
		$V_S = \pm 15V,$ $-15V < V_{CM} < 13.5V$	100	120	—	90	110	—	90	110	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	3.2	10	—	5.6	17.8	$\mu V/V$
Supply Current	I_{SV}	$V_S = \pm 1.5V$	—	13	25	—	13	25	—	12	25	μA
		$V_S = \pm 15V$	—	17	30	—	17	30	—	16	30	

NOTE:

1. Guaranteed by CMR test.



DICE CHARACTERISTICS



1. V_{OS} NULL
2. -IN
3. +IN
4. V_-
5. V_{OS} NULL
6. OUT
7. V_+

DIE SIZE 0.086×0.067 Inch, 5762 sq. mils
(2.18×1.70 mm, 3.71 sq. mm)

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

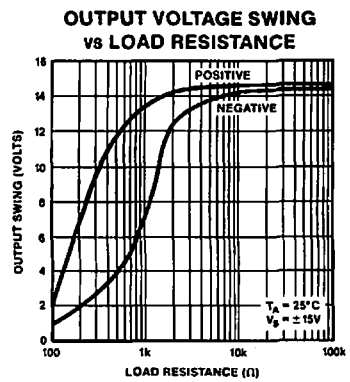
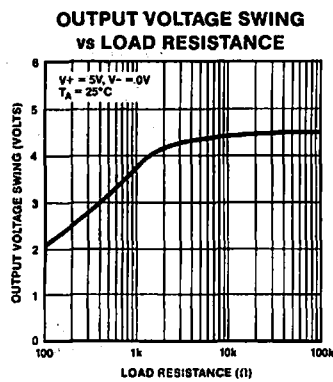
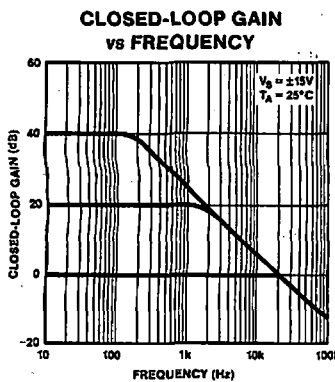
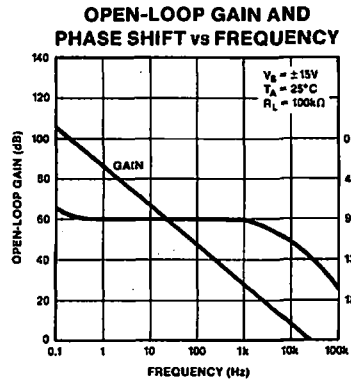
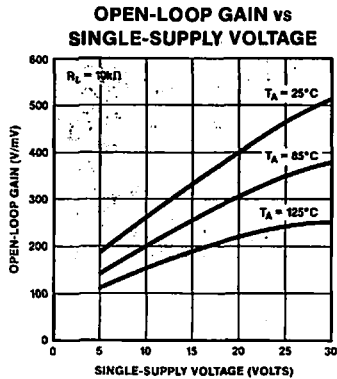
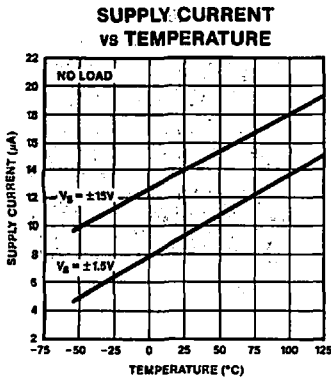
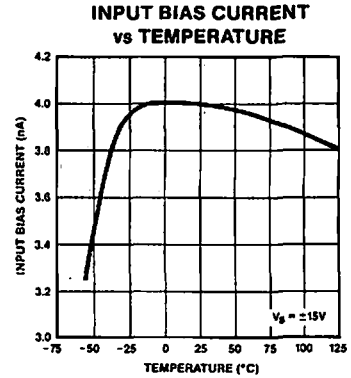
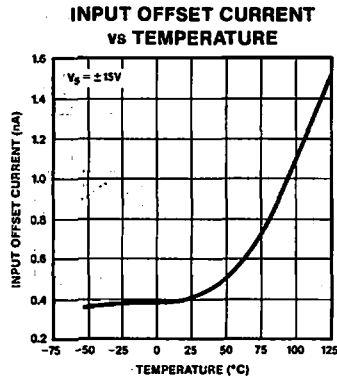
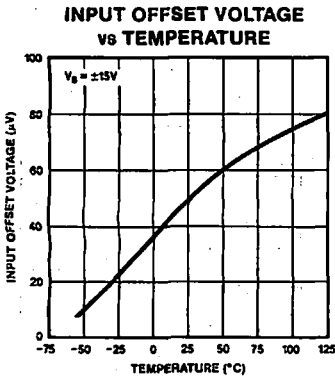
PARAMETER	SYMBOL	CONDITIONS	OP-90GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		250	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	5	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	20	nA MAX
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$	500 250	V/mV MIN
		$V_+ = 5V$, $V_- = 0V$, $1V < V_O < 4V$ $R_L = 100k\Omega$	125	V/mV MIN
Input Voltage Range	IVR	$V_+ = 5V$, $V_- = 0V$ $V_S = \pm 15V$ (Note 1)	0/4 -15/13.5	V MIN
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 14 ± 11	V MIN
	V_{OH}	$V_+ = 5V$, $V_- = 0V$ $R_L = 2k\Omega$	4.0	V MIN
	V_{OL}	$V_+ = 5V$, $V_- = 0V$ $R_L = 10k\Omega$	500	μV MAX
Common Mode Rejection	CMR	$V_+ = 5V$, $V_- = 0V$, $0V < V_{CM} < 4V$ $V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	80 90	dB MIN
Power Supply Rejection Ratio	PSRR		10	$\mu V/V$ MAX
Supply Current	I_{SY}	$V_S = \pm 15V$	20	μA MAX

NOTES:

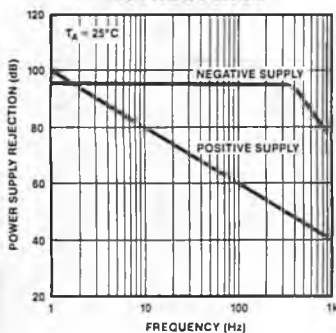
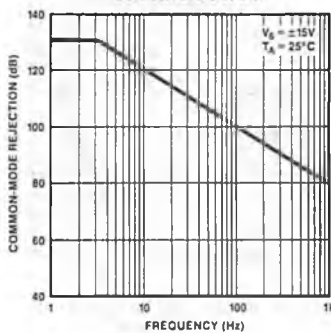
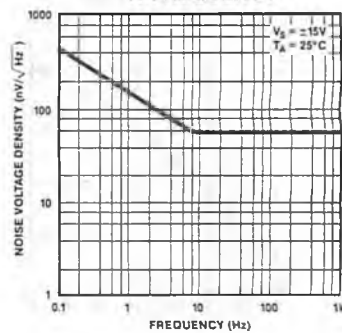
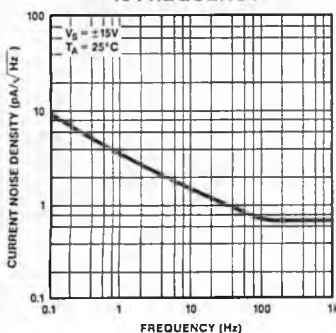
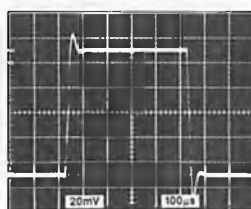
1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

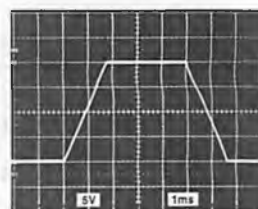
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS

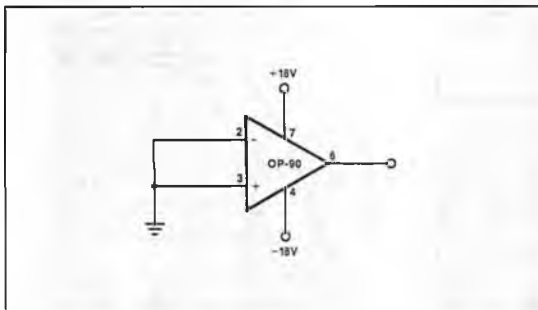
POWER SUPPLY REJECTION
vs FREQUENCYCOMMON-MODE REJECTION
vs FREQUENCYNOISE VOLTAGE DENSITY
vs FREQUENCYCURRENT NOISE DENSITY
vs FREQUENCYSMALL-SIGNAL
TRANSIENT RESPONSE

$T_A = 25^\circ\text{C}$
 $V_S = \pm 15\text{V}$
 $A_V = +1$
 $R_L = 10\text{k}\Omega$
 $C_L = 500\text{pF}$

LARGE-SIGNAL
TRANSIENT RESPONSE

$T_A = 25^\circ\text{C}$
 $V_S = \pm 15\text{V}$
 $A_V = +1$
 $R_L = 10\text{k}\Omega$
 $C_L = 500\text{pF}$

BURN-IN CIRCUIT



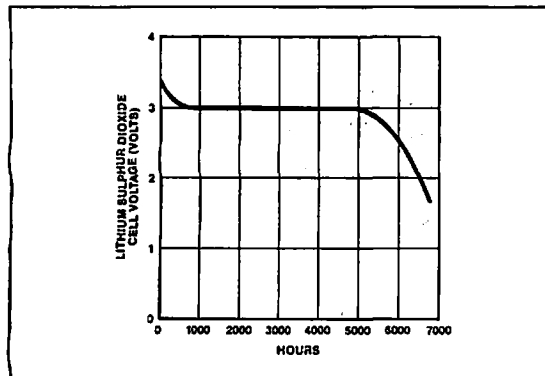
APPLICATIONS INFORMATION

BATTERY-POWERED APPLICATIONS

The OP-90 can be operated on a minimum supply voltage of +1.6V, or with dual supplies $\pm 0.8\text{V}$, and draws only $14\mu\text{A}$ of supply current. In many battery-powered circuits, the OP-90 can be continuously operated for thousands of hours before requiring battery replacement, reducing equipment downtime and operating cost.

High-performance portable equipment and instruments frequently use lithium cells because of their long shelf-life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3V and are noted for a flat discharge characteristic. The low supply voltage requirement of the OP-90, combined with the flat discharge characteristic of the lithium cell, indicates that the OP-90 can be operated over the entire useful life of the cell. Figure 1 shows the typical discharge characteristic of a 1Ah lithium cell powering an OP-90 which, in turn, is driving full output swing into a $100\text{k}\Omega$ load.

FIGURE 1: Lithium Sulphur Dioxide Cell Discharge Characteristic With OP-90 and 100k Ω Load



INPUT VOLTAGE PROTECTION

The OP-90 uses a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors coupled with the protection resistors provides a large amount of input protection, allowing the inputs to be taken 20V beyond either supply without damaging the amplifier.

OFFSET NULLING

The offset null circuit of Figure 2 provides 6mV of offset adjustment range. A 100k Ω resistor placed in series with the wiper of the offset null potentiometer, as shown in Figure 3,

FIGURE 2: Offset Nulling Circuit

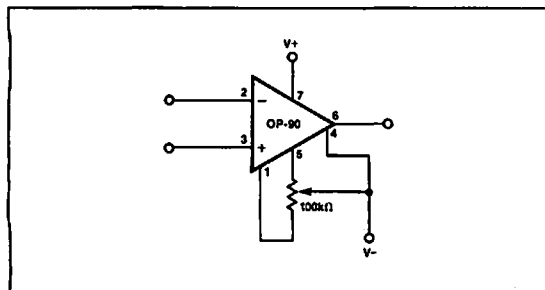
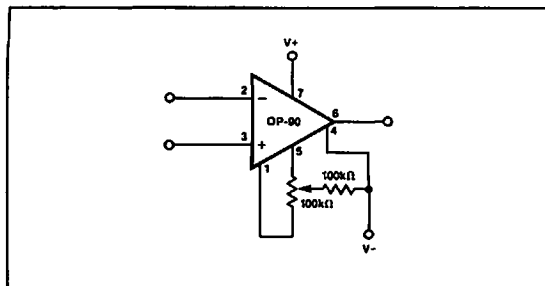


FIGURE 3: High Resolution Offset Nulling Circuit



reduces the offset adjustment range to 400 μ V and is recommended for applications requiring high null resolution. Offset nulling does not affect TCV_{OS} performance.

SINGLE-SUPPLY OUTPUT VOLTAGE RANGE

In single-supply operation the OP-90's input and output ranges include ground. This allows true "zero-in, zero-out" operation. The output stage provides an active pull-down to around 0.8V above ground. Below this level, a load resistance of up to 1M Ω to ground is required to pull the output down to zero.

In the region from ground to 0.8V the OP-90 has voltage gain equal to the data sheet specification. Output current source capability is maintained over the entire voltage range including ground.

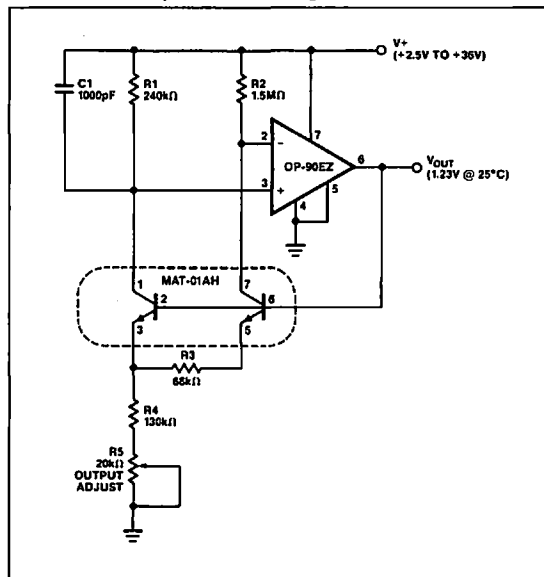
APPLICATIONS

BATTERY-POWERED VOLTAGE REFERENCE

The circuit of Figure 4 is a battery-powered voltage reference that draws only 17 μ A of supply current. At this level, two AA cells can power this reference over 18 months. At an output voltage of 1.23V @ 25°C, drift of the reference is only 5.5 μ V/°C over the industrial temperature range. Load regulation is 85 μ V/mA with line regulation at 120 μ V/V.

Design of the reference is based on the bandgap technique. Scaling of resistors R1 and R2 produces unequal currents in Q1 and Q2. The resulting V_{BE} mismatch creates a temperature-proportional voltage across R3 which, in turn, produces a larger temperature-proportional voltage across R4 and R5. This voltage appears at the output added to the V_{BE} of Q1, which has an opposite temperature coefficient. Adjusting the

FIGURE 4: Battery Powered Voltage Reference



output to 1.23V at 25°C produces minimum drift over temperature. Bandgap references can have start-up problems. With no current in R1 and R2, the OP-90 is beyond its positive input range limit and has an undefined output state. Shorting Pin 5 (an offset adjust pin) to ground forces the output high under these conditions and insures reliable start-up without significantly degrading the OP-90's offset drift.

SINGLE OP AMP FULL-WAVE RECTIFIER

Figure 5 shows a full-wave rectifier circuit that provides the absolute value of input signals up to $\pm 2.5\text{V}$ even though operated from a single 5V supply. For negative inputs, the amplifier acts as an unity gain inverter. Positive signals force the op amp output to ground. The 1N914 diode becomes reversed-biased and the signal passes through R1 and R2 to the output. Since output impedance is dependent on input polarity, load impedances cause an asymmetric output. For constant load impedances, this can be corrected by reducing R2. Varying or heavy loads can be buffered by a second OP-90. Figure 6 shows the output of the full-wave rectifier with a 4V_{p-p}, 10Hz input signal.

FIGURE 5: Single Op-Amp Full Wave Rectifier

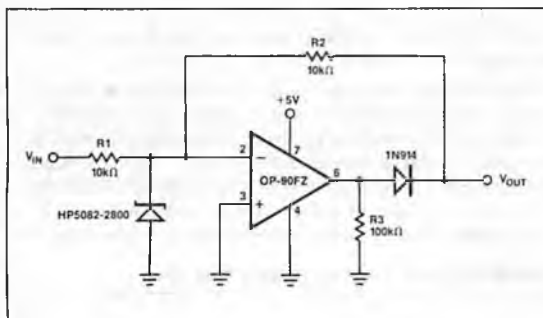


FIGURE 7: Two Wire 4-20mA Transmitter

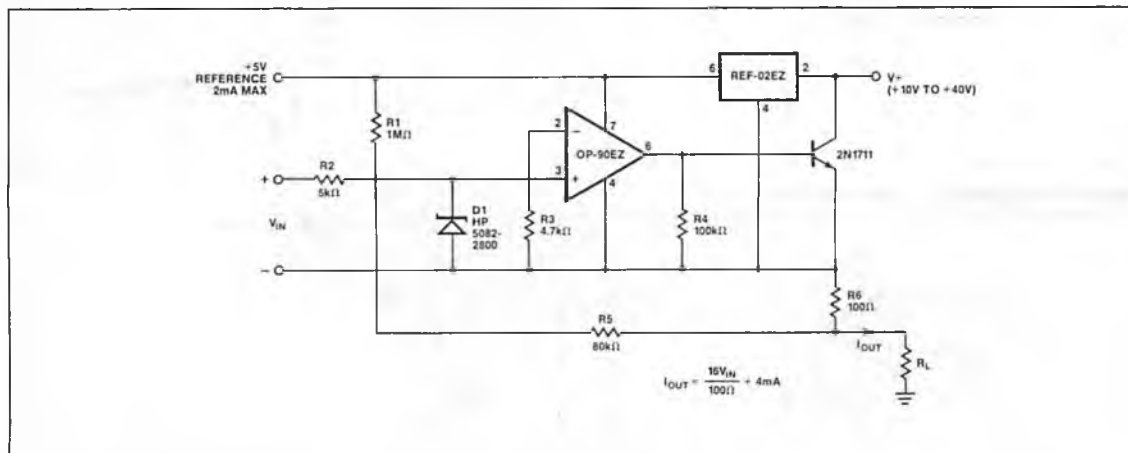
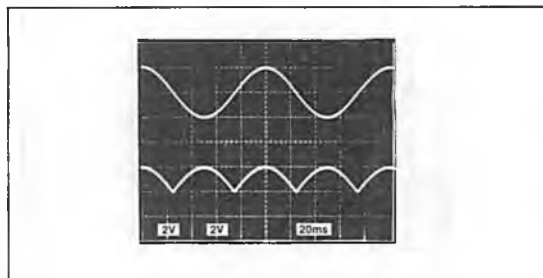


FIGURE 6: Output of Full-Wave Rectifier With 4V_{p-p}, 10Hz Input



TWO WIRE 4-20mA CURRENT TRANSMITTER

The current transmitter of Figure 7 provides an output of 4mA to 20mA that is linearly proportional to the input voltage. Linearity of the transmitter exceeds 0.004% and line rejection is 0.0005%/volt.

Biasing for the current transmitter is provided by the REF-02EZ. The OP-90EZ regulates the output current to satisfy the current summation at the noninverting node:

$$I_{OUT} = \frac{1}{R_6} \left(\frac{V_{IN} R_5}{R_2} + \frac{5V R_5}{R_1} \right)$$

For the values shown in Figure 7,

$$I_{OUT} = \left(\frac{16}{100\Omega} \right) V_{IN} + 4\text{mA}$$

giving a full-scale output of 20mA with a 100mV input. Adjustment of R2 will provide an offset trim and adjustment of R1 will provide a gain trim. These trims do not interact since the noninverting input of the OP-90 is at virtual ground. The Schottky diode, D1, prevents input voltage spikes from pull-

ing the noninverting input more than 300mV below the inverting input. Without the diode, such spikes could cause phase reversal of the OP-90 and possible latch-up of the transmitter. Compliance of this circuit is from 10V to 40V. The voltage reference output can provide up to 2mA for transducer excitation.

MICROPOWER VOLTAGE-CONTROLLED OSCILLATOR

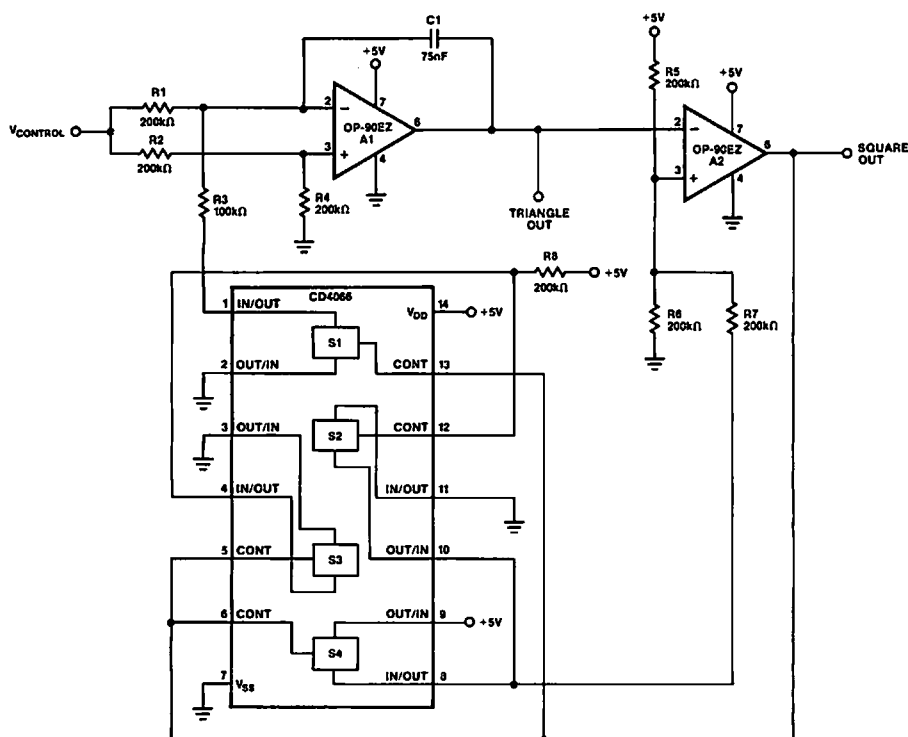
Two OP-90s in combination with an inexpensive quad CMOS switch comprise the precision VCO of Figure 8. This circuit provides triangle and square wave outputs and draws only 50μA from a single 5V supply. A1 acts as an integrator; S1 switches the charging current symmetrically to yield positive

and negative ramps. The integrator is bounded by A2 which acts as a Schmitt trigger with a precise hysteresis of 1.67 volts, set by resistors R5, R6, and R7, and associated CMOS switches. The resulting output of A1 is a triangle wave with upper and lower levels of 3.33 and 1.67 volts. The output of A2 is a square wave with almost rail-to-rail swing. With the components shown, frequency of operation is given by the equation:

$$f_{OUT} = V_{CONTROL} \text{ (volts)} \times 10\text{Hz/V}$$

but this is easily changed by varying C1. The circuit operates well up to a few hundred hertz.

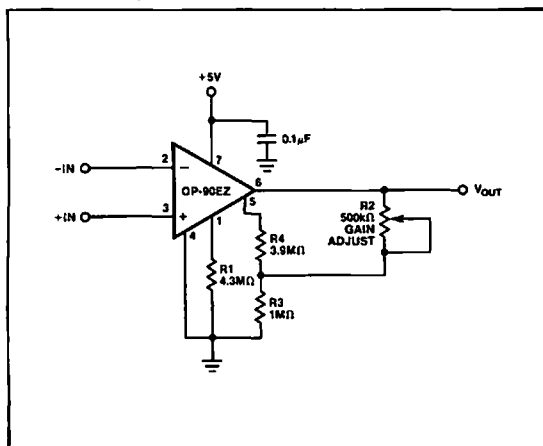
FIGURE 8: Micropower Voltage Controlled Oscillator



MICROPOWER SINGLE-SUPPLY INSTRUMENTATION AMPLIFIER

The simple instrumentation amplifier of Figure 9 provides over 110dB of common-mode rejection and draws only 15 μ A of supply current. Feedback is to the trim pins rather than to the inverting input. This enables a single amplifier to provide differential to single-ended conversion with excellent common-mode rejection. Distortion of the instrumentation amplifier is that of a differential pair, so the circuit is restricted to high gain applications. Nonlinearity is less than 0.1% for gains of 500 to 1000 over a 2.5V output range. Resistors R3 and R4 set the voltage gain and, with the values shown, yield a gain of 1000. Gain tempco of the instrumentation amplifier is only 50ppm/ $^{\circ}$ C. Offset voltage is under 150 μ V with drift below 2 μ V/ $^{\circ}$ C. The OP-90's input and output voltage ranges include the negative rail which allows the instrumentation amplifier to provide true "zero-in, zero-out" operation.

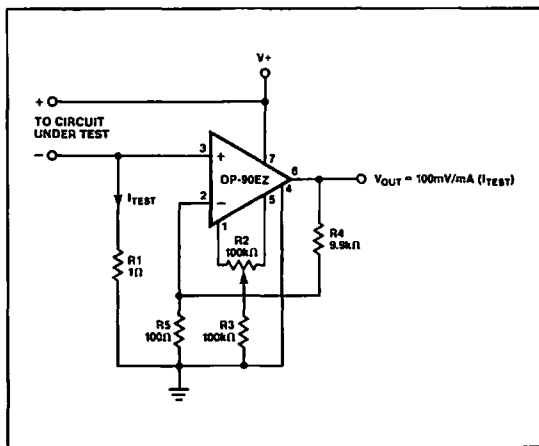
FIGURE 9: Micropower Single-Supply Instrumentation Amplifier



SINGLE-SUPPLY CURRENT MONITOR

Current monitoring essentially consists of amplifying the voltage drop across a resistor placed in series with the current to be measured. The difficulty is that only small voltage drops can be tolerated and with low precision op amps this greatly limits the overall resolution. The single-supply current monitor of Figure 10 has a resolution of 10 μ A and is capable of monitoring 30mA of current. This range can be adjusted by changing the current sense resistor R1. When measuring total system current, it may be necessary to include the supply current of the current monitor, which bypasses the current sense resistor, in the final result. This current can be measured and calibrated (together with the residual offset) by adjustment of the offset trim potentiometer, R2. This produces a deliberate offset that is temperature dependent. However, the supply current of the OP-90 is also proportional to temperature and the two effects tend to track. Current in R4 and R5, which also bypasses R1, can be accounted for by a gain trim.

FIGURE 10: Single-Supply Current Monitor





OP-97

LOW-POWER, HIGH-PRECISION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Supply Current 600 μ A Max
- OP-07 Type Performance
 - Offset Voltage 25 μ V Max
 - Offset Voltage Drift 0.6 μ V/ $^{\circ}$ C Max
- Very Low Bias Current
 - 25 $^{\circ}$ C 100pA Max
 - 55 $^{\circ}$ C to +125 $^{\circ}$ C 250pA Max
- High Common-Mode Rejection 114dB Min
- Extended Industrial Temp. Range -40 $^{\circ}$ C to +85 $^{\circ}$ C

ORDERING INFORMATION†

TO-99	PACKAGE		OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	
OP97AJ*	OP97AZ*	—	MIL
OP97EJ	OP97EZ	OP97EP	XIND
OP97FJ	OP97FZ	OP97FP	XIND
—	—	OP97FS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

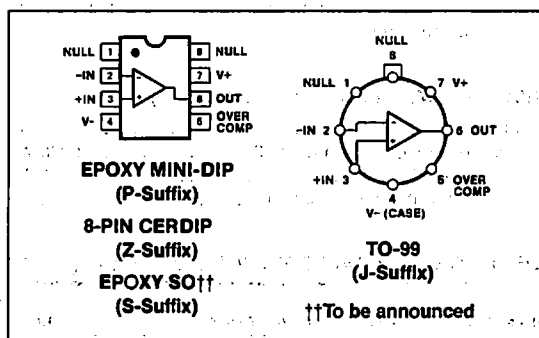
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

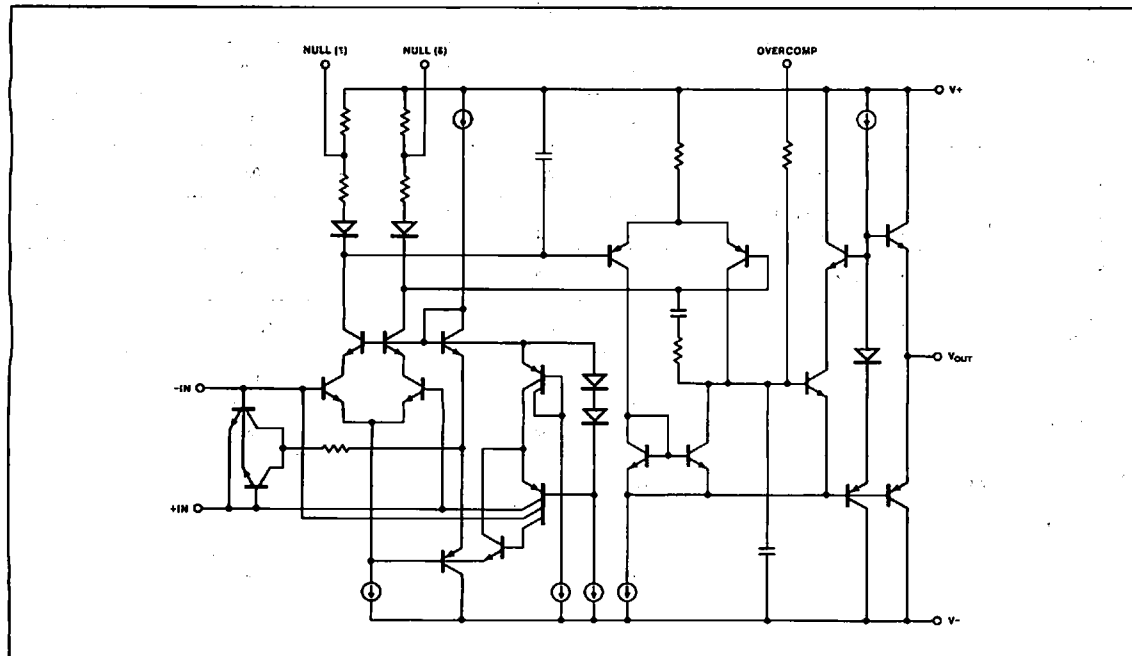
GENERAL DESCRIPTION

The OP-97 is a low-power alternative to the industry-standard OP-07 precision amplifier. The OP-97 maintains the standards of performance set by the OP-07 while utilizing only 600 μ A supply current, less than 1/6 that of an OP-07. Offset voltage is an ultra-low 25 μ V, and drift over temperature is below 0.6 μ V/ $^{\circ}$ C. External offset trimming is not required in the majority of circuits.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





Improvements have been made over OP-07 specifications in several areas. Notable is bias current, which remains below 250pA over the full military temperature range. The OP-97 is ideal for use in precision long-term integrators or sample-and-hold circuits that must operate at elevated temperatures.

Common-mode rejection and power-supply rejection are also improved with the OP-97, at 114dB minimum over wider ranges of common-mode or supply voltage. Outstanding PSR, a supply range specified from $\pm 2.25V$ to $\pm 20V$ and the OP-97's minimal power requirements combine to make the OP-97 a preferred device for portable and battery-powered instruments.

The OP-97 conforms to the OP-07 pinout, with the null potentiometer connected between pins 1 and 8 with the wiper to V+. The OP-97 will upgrade circuit designs using 725, OP05, OP07, OP12, and 1012 type amplifiers. It may replace 741-type amplifiers in circuits without nulling or where the nulling circuitry has been removed.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	$\pm 20V$
Internal Power Dissipation (Note 2)	500mW
Input Voltage (Note 3)	$\pm 20V$
Differential Input Voltage (Note 4)	$\pm 1V$

Differential Input Current (Note 4)	$\pm 10mA$
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
OP-97 (J, Z)	$-55^{\circ}C$ to $+125^{\circ}C$
OP-97 (J, Z, P, S)	$-40^{\circ}C$ to $+85^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Junction Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. See table for maximum ambient temperature and rating.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	$80^{\circ}C$	$7.1mW/^{\circ}C$
8-Pin Cerdip (Z)	$75^{\circ}C$	$6.7mW/^{\circ}C$
8-Pin Plastic DIP (P)	$82^{\circ}C$	$5.6mW/^{\circ}C$

3. For supply voltages less than $\pm 20V$, the absolute maximum input voltage is equal to the supply voltage.
4. The OP-97's inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = +25^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-97A/E			OP-97F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	10	25	—	30	75	μV
Long-Term Offset Voltage Stability	$\Delta V_{OS}/Time$		—	0.3	—	—	0.3	—	$\mu V/Month$
Input Offset Current	I_{OS}		—	30	100	—	30	150	pA
Input Bias Current	I_B		—	± 30	± 100	—	± 30	± 150	pA
Input Noise Voltage	$e_{n\ p-p}$	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 2)	—	17	30	—	17	30	$nV/\sqrt{Hz}$
		$f_O = 1000Hz$ (Note 3)	—	14	22	—	14	22	$nV/\sqrt{Hz}$
Input Noise Current Density	I_N	$f_O = 10Hz$	—	20	—	—	20	—	$tA/\sqrt{Hz}$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$; $R_L = 2k\Omega$	300	2000	—	200	2000	—	V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	114	132	—	110	132	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2V$ to $\pm 20V$	114	132	—	110	132	—	dB
Input Voltage Range	IVR	(Note 1)	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 13	± 14	—	± 13	± 14	—	V
Slew Rate	SR		0.1	0.2	—	0.1	0.2	—	V/ μs

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = +25^\circ C$, unless otherwise noted. (Continued.)

PARAMETER	SYMBOL	CONDITIONS	OP-97A/E			OP-97F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input Resistance	R_{IN}	(Note 4)	30	—	—	30	—	—	M Ω
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.4	0.9	—	0.4	0.9	—	MHz
Supply Current	I_{SY}		—	380	600	—	380	600	μA
Supply Voltage	V_S	Operating Range	± 2	± 15	± 20	± 2	± 15	± 20	V

NOTES:

1. Guaranteed by CMR test.
2. 10Hz noise voltage density is sample tested. Devices 100% tested for noise are available on request.
3. Sample tested.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $-40^\circ C \leq T_A \leq +85^\circ C$ for the OP-97E/F and $-55^\circ C \leq T_A \leq +125^\circ C$ for the OP-97A, unless otherwise noted.

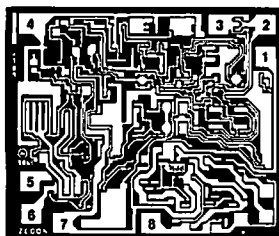
PARAMETER	SYMBOL	CONDITIONS	OP-97A/E			OP-97F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	25	60	—	60	200	μV
Average Temperature Coefficient of V_{OS}	TCV_{OS}		—	0.2	0.6	—	0.3	2.0	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	60	250	—	80	750	pA
Average Temperature Coefficient of I_{OS}	TCI_{OS}		—	0.4	2.5	—	0.6	7.5	$pA/^\circ C$
Input Bias Current	I_B		—	± 60	± 250	—	± 80	± 750	pA
Average Temperature Coefficient of I_B	TCI_B		—	0.4	2.5	—	0.6	7.5	$pA/^\circ C$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$; $R_L = 2k\Omega$	200	1000	—	150	1000	—	V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	108	128	—	108	128	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2.5V$ to $\pm 20V$	108	126	—	108	126	—	dB
Input Voltage Range	IVR	(Note 1)	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 13	± 14	—	± 13	± 14	—	V
Slew Rate	SR		0.05	0.15	—	0.05	0.15	—	V/ μs
Supply Current	I_{SY}		—	400	800	—	400	800	μA
Supply Voltage	V_S	Operating Range	± 2.5	± 15	± 20	± 2.5	± 15	± 20	V

NOTE:

1. Guaranteed by CMR test.



DICE CHARACTERISTICS



DIE SIZE 0.063×0.074 inch, 4,662 sq. mils
(1.60 $\times$ 1.88 mm, 3.01 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V^-
5. OVERCOMPENSATION
6. OUTPUT
7. V^+
8. NULL

For additional DICE ordering information, refer to
1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-97N LIMITS	UNITS
Input Offset Voltage	V_{OS}		250	μV MAX
Input Offset Current	I_{OS}		150	pA MAX
Input Bias Current	I_B		± 150	pA MAX
Large-Signal Voltage Gain	A_{VO}	$V_{OUT} = \pm 10V$, $R_L = 2k\Omega$	120	V/mV MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5$	110	dB MIN
Power-Supply Rejection	PSR	$V_S = \pm 2V$ to $\pm 20V$	110	dB MIN
Input-Voltage Range	IVR	(Note 1)	± 13.5	V MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 13	V MIN
Slew Rate	SR		0.1	V/ μs MIN
Supply Current	I_{SY}	No Load	600	μA MAX

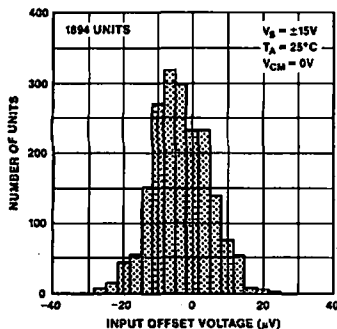
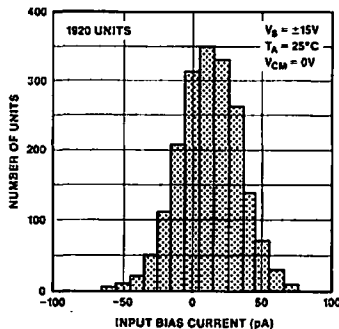
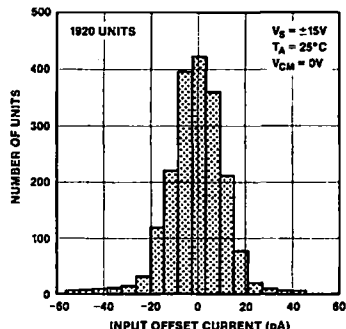
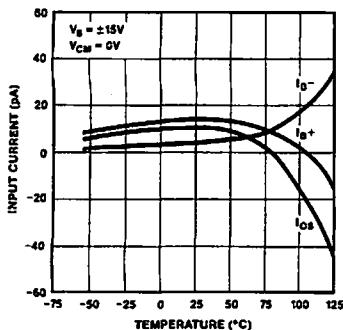
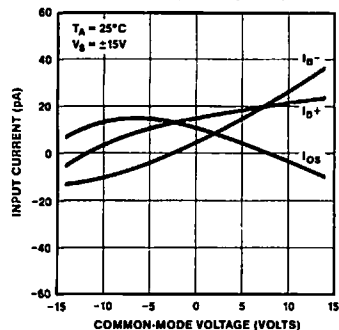
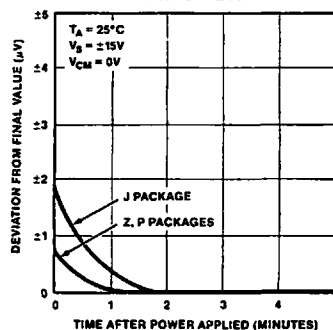
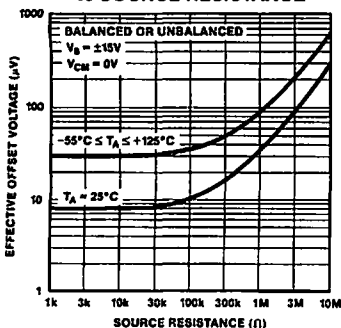
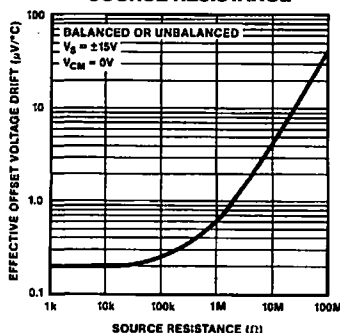
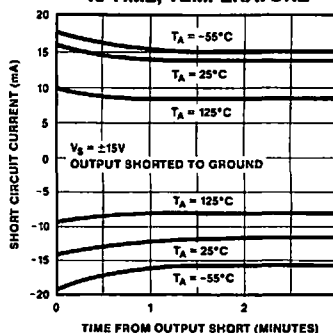
NOTES:

1. Guaranteed by CMR test.

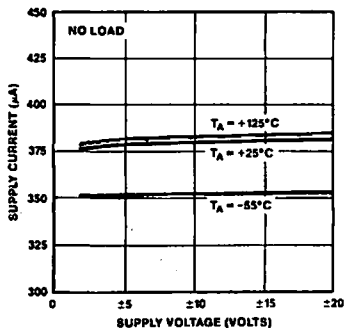
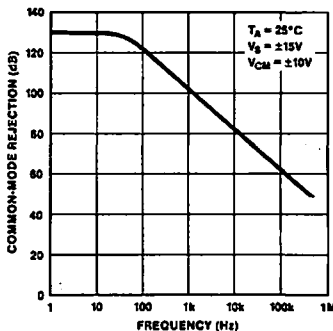
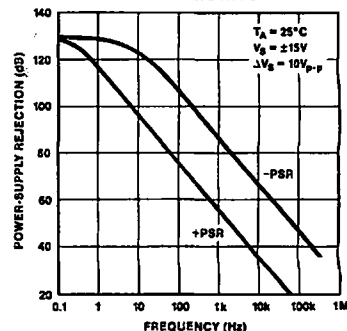
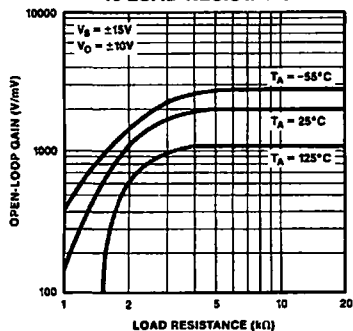
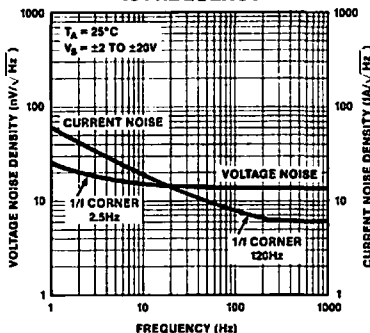
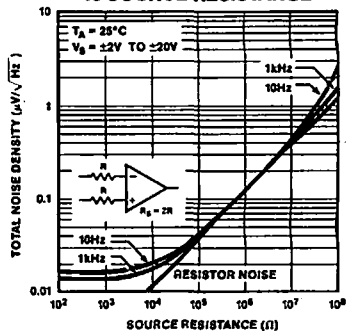
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



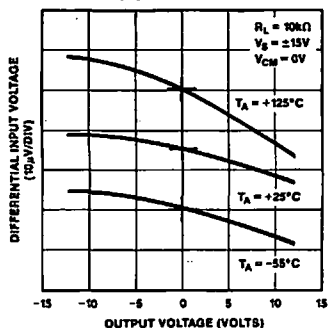
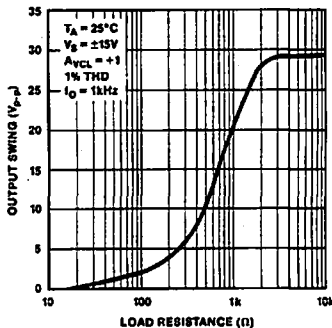
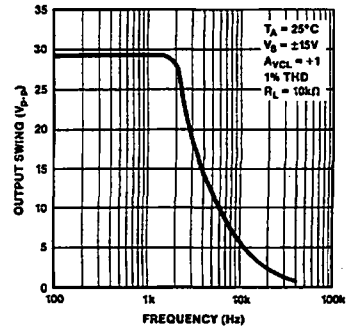
TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL DISTRIBUTION
OF INPUT OFFSET VOLTAGETYPICAL DISTRIBUTION
OF INPUT BIAS CURRENTTYPICAL DISTRIBUTION
OF INPUT OFFSET CURRENTINPUT BIAS, OFFSET
CURRENT vs TEMPERATUREINPUT BIAS, OFFSET
CURRENT vs
COMMON-MODE VOLTAGEINPUT OFFSET VOLTAGE
WARM-UP DRIFTEFFECTIVE OFFSET VOLTAGE
vs SOURCE RESISTANCEEFFECTIVE TCV_{OS} vs
SOURCE RESISTANCESHORT CIRCUIT CURRENT
vs TIME, TEMPERATURE

TYPICAL PERFORMANCE CHARACTERISTICS

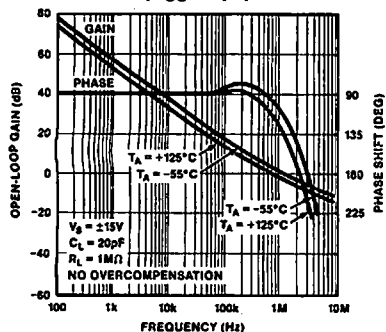
 SUPPLY CURRENT vs
SUPPLY VOLTAGE

 COMMON-MODE REJECTION
vs FREQUENCY

 POWER-SUPPLY REJECTION
vs FREQUENCY

 OPEN-LOOP GAIN
vs LOAD RESISTANCE

 NOISE DENSITY
vs FREQUENCY

 TOTAL NOISE DENSITY
vs SOURCE RESISTANCE


OPEN-LOOP GAIN LINEARITY

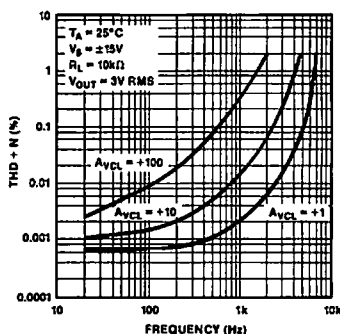

 MAXIMUM OUTPUT SWING
vs LOAD RESISTANCE

 MAXIMUM OUTPUT SWING
vs FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS

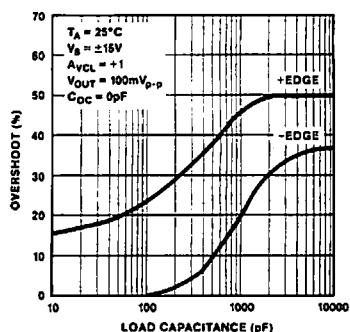
OPEN-LOOP GAIN,
PHASE vs FREQUENCY
($C_{OC} = 0\text{pF}$)



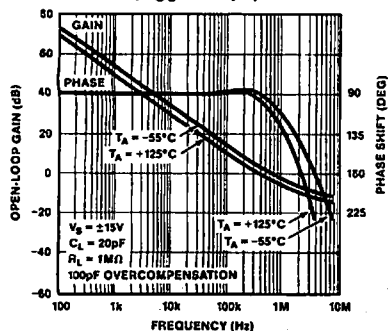
TOTAL HARMONIC
DISTORTION
PLUS NOISE vs FREQUENCY



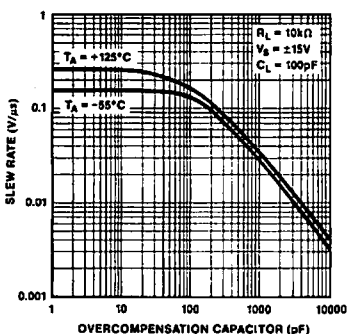
SMALL-SIGNAL OVERSHOOT
vs CAPACITIVE LOAD



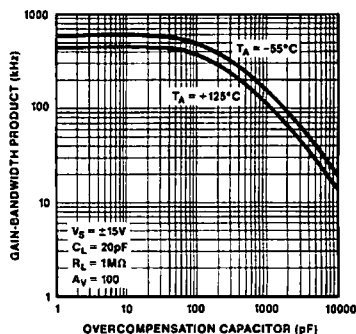
OPEN-LOOP GAIN,
PHASE vs FREQUENCY
($C_{OC} = 100\text{pF}$)



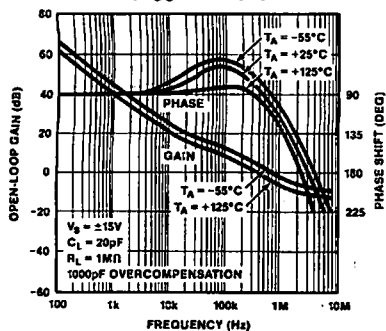
SLEW RATE vs
OVERCOMPENSATION



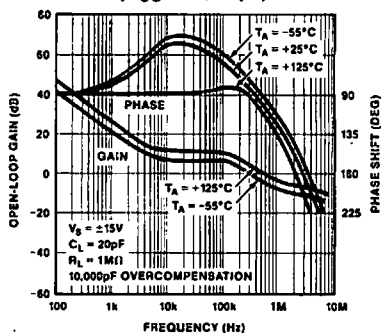
GAIN-BANDWIDTH PRODUCT
vs OVERCOMPENSATION



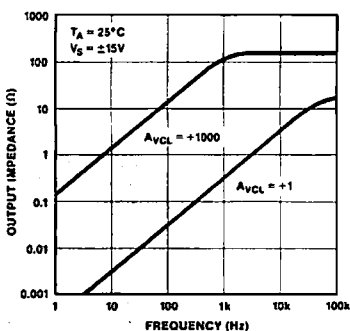
OPEN-LOOP GAIN,
PHASE vs FREQUENCY
($C_{OC} = 1000\text{pF}$)



OPEN-LOOP GAIN,
PHASE vs FREQUENCY
($C_{OC} = 10,000\text{pF}$)



CLOSED-LOOP OUTPUT
RESISTANCE vs FREQUENCY



APPLICATIONS INFORMATION

The OP-97 is a low-power alternative to the industry standard precision op amp, the OP-07. The OP-97 may be substituted directly into OP-07, OP-77, 725, OP-05, 112/312, and 1012 sockets with improved performance and/or less power dissipation, and may be inserted into sockets conforming to the 741 pinout if nulling circuitry is not used. Generally, nulling circuitry used with earlier generation amplifiers is rendered superfluous by the OP-97's extremely low offset voltage, and may be removed without compromising circuit performance.

Extremely low bias current over the full military temperature range makes the OP-97 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is not necessary with the OP-97. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the OP-97 are protected against large differential voltage by back-to-back diodes. Current-limiting resistors are not used so that low-noise performance is maintained. If differential voltages above $\pm 1V$ are expected at the inputs, series resistors must be used to limit the current flow to a maximum of 10mA. Common-mode voltages at the inputs are not restricted, and may vary over the full range of the supply voltages used.

The OP-97 requires very little operating headroom about the supply rails, and is specified for operation with supplies as low

as $\pm 2V$. Typically, the common-mode range extends to within one volt of either rail. The output typically swings to within one volt of the rails when using a 10k Ω load.

Offset nulling is achieved utilizing the same circuitry as an OP-07. A potentiometer between 5k Ω and 100k Ω is connected between pins 1 and 8 with the wiper connected to the positive supply. The trim range is between 300 μV and 850 μV , depending upon the internal trimming of the device.

AC PERFORMANCE

The OP-97's AC characteristics are highly stable over its full operating temperature range. Unity-gain small signal response is shown in Figure 2. Extremely tolerant of capacitive loading on the output, the OP-97 displays excellent response even with 1000pF loads (Figure 3). In large-signal applications, the input protection diodes effectively short the input to the output during the transients if the amplifier is connected in the usual unity-gain configuration. The output enters short-circuit current limit, with the flow going through the protection diodes. Improved large-signal transient response is obtained by using a feedback resistor between the output and the inverting input. Figure 4 shows the large-signal response of the OP-97 in unity-gain with a 10k Ω feedback resistor. The unity gain follower circuit is shown in Figure 5.

The overcompensation pin may be used to increase the phase margin of the OP-97, or to decrease gain-bandwidth product at gains greater than 10.

FIGURE 1: Optional Input Offset Voltage Nulling and Over-compensation Circuits

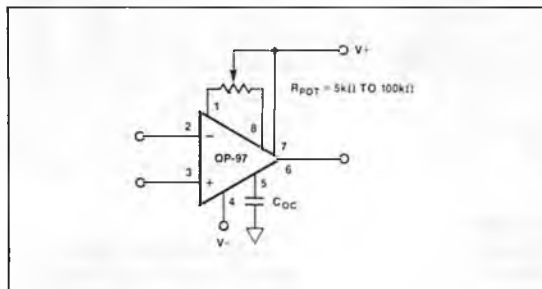


FIGURE 2: Small Signal Transient Response
($C_{LOAD} = 100pF$, $A_{VCL} = +1$)

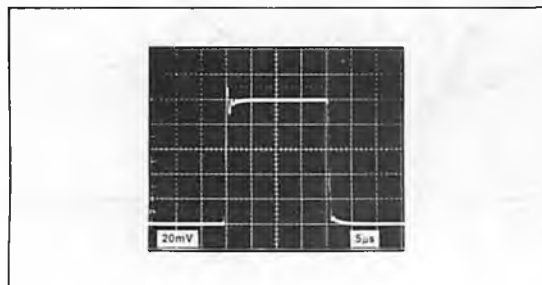


FIGURE 3: Small-Signal Transient Response
($C_{LOAD} = 1000pF$, $A_{VCL} = +1$)

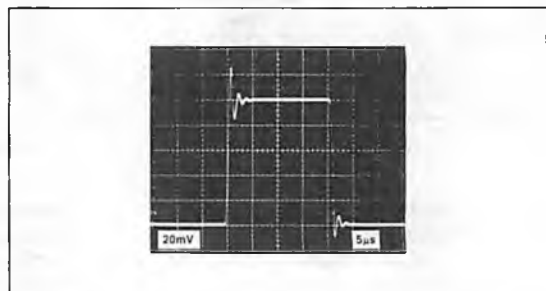


FIGURE 4: Large Signal Transient Response ($A_{VCL} = +1$)

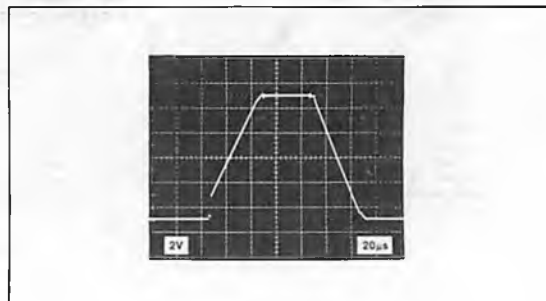
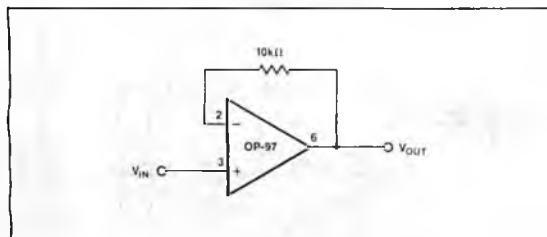
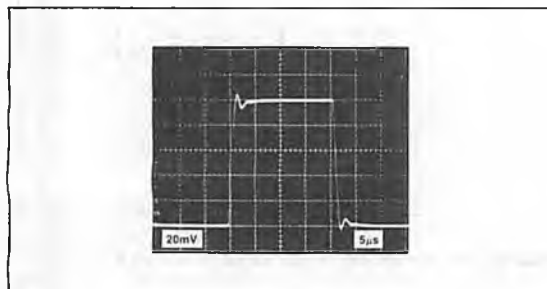


FIGURE 5: Unity-gain Follower


FIGURE 6: Small Signal Transient Response with Overcompensation ($C_{LOAD} = 1000pF$, $A_{VCL} = +1$, $C_{OC} = 220pF$)


GUARDING AND SHIELDING

To maintain the extremely high input impedances of the OP-97, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100pA of leakage currents between adjacent traces, so that guard rings

should be used around the inputs. Guard traces are operated at a voltage close to that on the inputs, so that leakage currents become minimal. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input (pin 2). In inverting applications, both inputs remain at ground, so that the guard trace should be grounded. Guard traces should be made on both sides of the circuit board.

FIGURE 8: DAC Output Amplifier

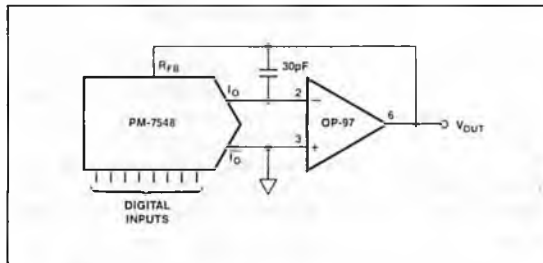


FIGURE 9: Current Monitor

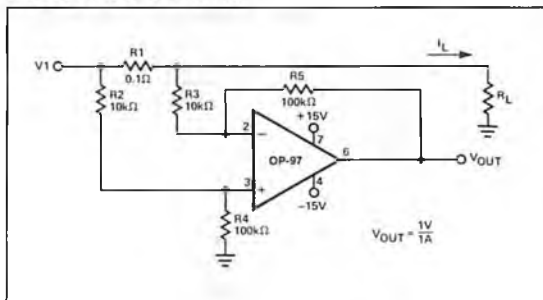
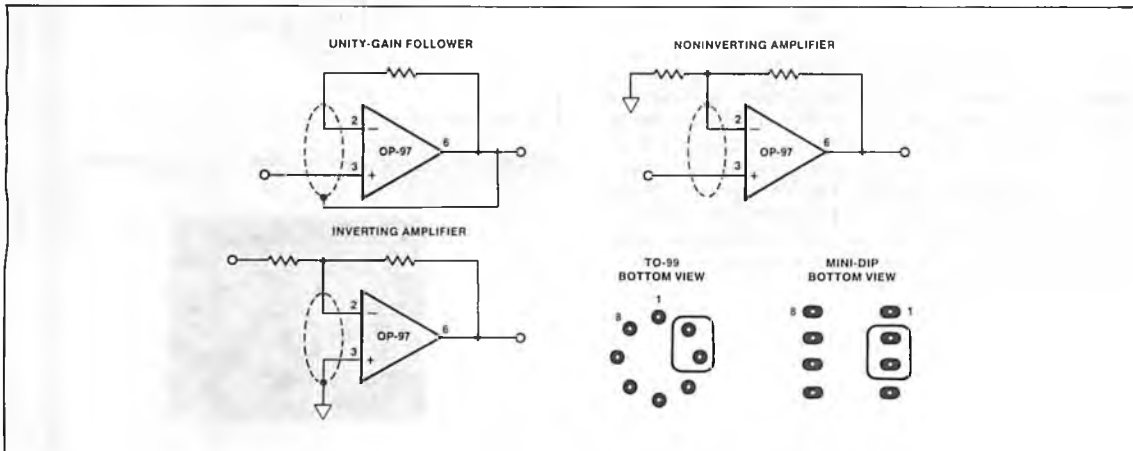


FIGURE 7: Guard Ring Layout and Connections



High impedance circuitry is extremely susceptible to RF pickup, line-frequency hum, and radiated noise from switching power-supplies. Enclosing sensitive analog sections within grounded shields is generally necessary to prevent excessive noise pickup. Twisted-pair cable will aid in rejection of line-frequency hum.

The OP-97 is an excellent choice as an output amplifier for higher resolution CMOS DACs. Its tightly trimmed offset voltage and minimal bias current result in virtually no degradation of linearity, even over wide temperature ranges.

Figure 9 shows a versatile monitor circuit that can typically sense current at any point between the $\pm 15\text{V}$ supplies. This makes it ideal for sensing current in applications such as full bridge drivers where bi-directional current is associated with large common-mode voltage changes. The 114dB CMRR of the OP-97 makes the amplifier's contribution to common-mode error negligible, leaving only the error due to the resistor ratio inequality. Ideally, $R_2/R_4 = R_3/R_5$. This is best trimmed via R_4 .

The digitally programmable gain amplifier shown in Figure 10 has 12-bit gain resolution with 10-bit gain linearity over the range of -1 to -1024 . The low bias current of the OP-97 maintains this linearity, while C_1 limits the noise voltage bandwidth allowing accurate measurement down to microvolt levels.

DIGITAL IN	GAIN (A_V)
4095	-1.00024
2048	-2
1024	-4
512	-8
256	-16
128	-32
64	-64
32	-128
16	-256
8	-512
4	-1024
2	-2048
1	-4096
0	OPEN LOOP

Many high-speed amplifiers suffer from less-than-perfect low-frequency performance. A combination amplifier consisting of a high precision, slow device like the OP-97 and a faster device such as the OP-44 results in uniformly accurate performance from DC to the high-frequency limit of the OP-44, which has a gain-bandwidth product of 23MHz. The circuit shown in Figure 11 accomplishes this, with the OP-44 providing high-frequency amplification and the OP-97 operating on low-frequency signals and providing offset correction. Offset voltage and drift of the circuit are controlled by the OP-97.

FIGURE 10: Precision Programmable Gain Amplifier

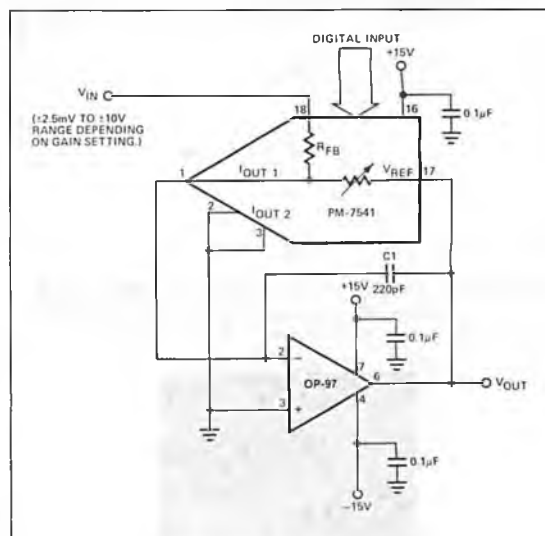


FIGURE 11: Combination High-Speed, Precision Amplifier

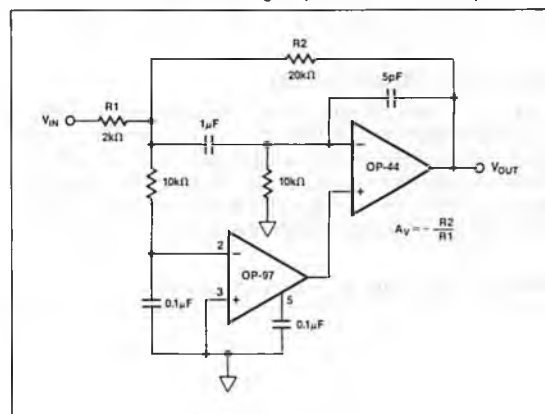
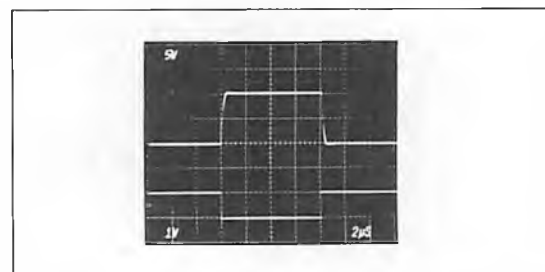


FIGURE 12: Combination Amplifier Transient Response





Precision Monolithics Inc.

OP-200

DUAL LOW-OFFSET, LOW-POWER
OPERATIONAL AMPLIFIER

FEATURES

- Low Input Offset Voltage $75\mu\text{V}$ Max
- Low Offset Voltage Drift,
Over $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $0.5\mu\text{V}/^\circ\text{C}$ Max
- Low Supply Current (Per Amplifier) $725\mu\text{A}$ Max
- High Open-Loop Gain $5000\text{V}/\text{mV}$ Min
- Low Input Bias Current 2nA Max
- Low Noise Voltage Density $11\text{nV}/\sqrt{\text{Hz}}$ at 1kHz
- Stable With Large Capacitive Loads 10nF Typ
- Pin Compatible to OP-14, OP-221, LM158, MC1458/1558,
and LT1013 With Improved Performance

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC	
75	OP200AZ*	—	OP200ARC*	MIL
75	OP200EZ	—	—	IND
150	OP200FZ	—	—	IND
200	—	OP200GP	—	COM
200	—	OP200GS††	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

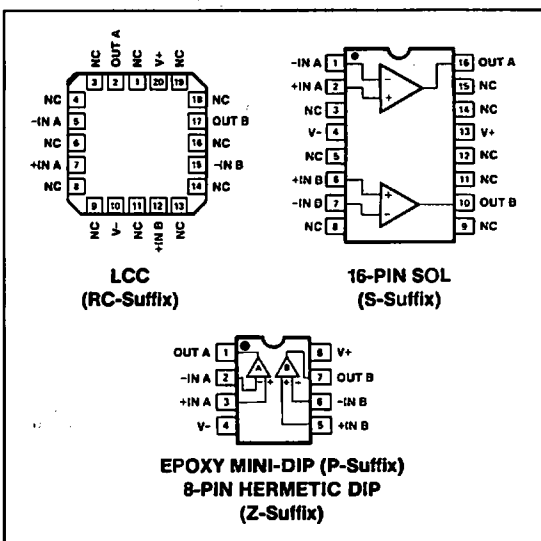
GENERAL DESCRIPTION

The OP-200 is the first monolithic dual operational amplifier to offer OP-77 type precision performance. Available in the

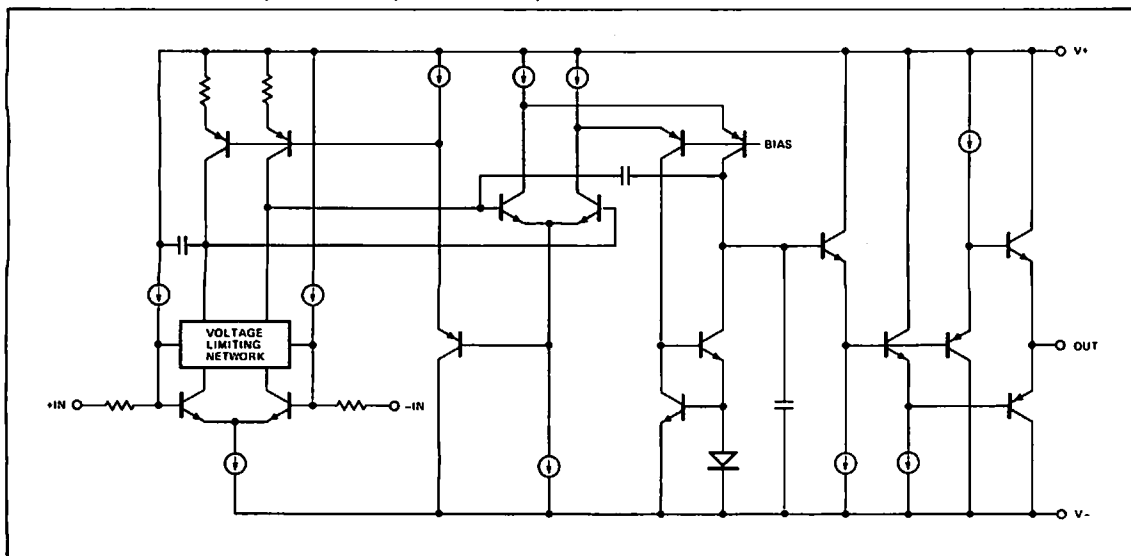
industry standard 8-pin pinout, the OP-200 combines precision performance with the space and cost savings offered by a dual amplifier.

The OP-200 features an extremely low input offset voltage of less than $75\mu\text{V}$ with a drift below $0.5\mu\text{V}/^\circ\text{C}$, guaranteed over the

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)





full military temperature range. Open-loop gain of the OP-200 exceeds 5,000,000 into a 10k Ω load; input bias current is under 2nA; CMR is over 120dB and PSRR below 1.8 μ V/V. On-chip zener-zap trimming is used to achieve the extremely low input offset voltage of the OP-200 and eliminates the need for offset nulling.

Power consumption of the OP-200 is very low, with each amplifier drawing less than 725 μ A of supply current. The total current drawn by the dual OP-200 is less than one-half that of a single OP-07, yet the OP-200 offers significant improvements over this industry standard op amp. The voltage noise density of the OP-200, 11nV/ $\sqrt{\text{Hz}}$ at 1kHz, is half that of most competitive devices.

The OP-200 is pin compatible with the OP-14, OP-221, LM158, MC1458/1558, and LT1013 and can be used to upgrade systems using these devices. The OP-200 is an ideal choice for applications requiring multiple precision op amps and where low power consumption is critical.

For a quad precision op amp, see the OP-400.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	$\pm 20\text{V}$
Internal Power Dissipation (Note 1)	
P, RC, S, Z-Package	500mW
Differential Input Voltage	$\pm 30\text{V}$
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
P, RC, S, Z-Package	-65°C to $+150^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_j)	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	
OP-200A	-55°C to $+125^{\circ}\text{C}$
OP-200E, OP-200F	-25°C to $+85^{\circ}\text{C}$
OP-200G	0°C to $+70^{\circ}\text{C}$

NOTES:

- See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
8-Pin Hermetic DIP (Z)	75°C	6.7mW/ $^{\circ}\text{C}$
8-Pin Plastic DIP (P)	62°C	5.6mW/ $^{\circ}\text{C}$
20-Pin LCC (RC)	80°C	7.8mW/ $^{\circ}\text{C}$

- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = +25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-200A/E			OP-200F			OP-200G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	25	75	—	50	150	—	80	200	μV
Long Term Input Voltage Stability			—	0.1	—	—	0.1	—	—	0.1	—	$\mu\text{V}/\text{mo}$
Input Offset Current	I_{OS}	$V_{CM} = 0\text{V}$	—	0.05	1.0	—	0.05	2.0	—	0.05	3.5	nA
Input Bias Current	I_B	$V_{CM} = 0\text{V}$	—	0.1	2.0	—	0.1	4.0	—	0.1	5.0	nA
Input Noise Voltage	$e_{n\text{ p-p}}$	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	—	0.5	—	$\mu\text{V}_{\text{p-p}}$
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	22	36	—	22	36	—	22	—	nV/ $\sqrt{\text{Hz}}$
		$f_O = 1000\text{Hz}$ (Note 1)	—	11	18	—	11	18	—	11	—	
Input Noise Current	$i_{n\text{ p-p}}$	0.1Hz to 10Hz	—	15	—	—	15	—	—	15	—	$\text{pA}_{\text{p-p}}$
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	0.4	—	—	0.4	—	—	0.4	—	$\text{pA}/\sqrt{\text{Hz}}$
Input Resistance Differential Mode	R_{IN}		—	10	—	—	10	—	—	10	—	M Ω
Input Resistance Common Mode	R_{INCM}		—	125	—	—	125	—	—	125	—	G Ω
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{V}$	5000	12000	—	3000	7000	—	3000	7000	—	V/mV
		$R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$	2000	3700	—	1500	3200	—	1500	3200	—	

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-200A/E			OP-200F			OP-200G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range	IVR	(Note 3)	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	120	135	—	115	135	—	110	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.4	1.8	—	0.4	3.2	—	0.6	5.6	$\mu V/V$
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 12	± 12.6	—	± 12	± 12.6	—	± 12	± 12.6	—	V
		$R_L = 2k\Omega$	± 11	± 12.2	—	± 11	± 12.2	—	± 11	± 12.2	—	
Supply Current Per Amplifier	I_{SY}	No Load	—	570	725	—	570	725	—	570	725	μA
Slow Rate	SR		0.1	0.15	—	0.1	0.15	—	0.1	0.15	—	V/ μs
Gain Bandwidth Product	GBWP	$A_V = +1$	—	500	—	—	500	—	—	500	—	kHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 2)	123	145	—	123	145	—	123	145	—	dB
Input Capacitance	C_{IN}		—	3.2	—	—	3.2	—	—	3.2	—	pF
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	10	—	—	10	—	—	10	—	nF

NOTES:

1. Sample tested.
2. Guaranteed but not 100% tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = +15V$, $-55^\circ C \leq T_A \leq 125^\circ C$ for OP-200A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-200A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	45	125	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.2	0.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.15	2.5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	0.9	5.0	nA
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$				V/mV
		$R_L = 10\Omega$ $R_L = 2k\Omega$	3000 1000	9000 2700	— —	
Input Voltage Range	IVR	(Note 1)	± 12	± 12.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.2	3.2	$\mu V/V$
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 12	± 12.4	—	V
		$R_L = 2k\Omega$	± 11	± 12	—	
Supply Current Per Amplifier	I_{SY}	No Load	—	600	775	μA
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	8	—	nF

NOTES:

1. Guaranteed by CMR test.

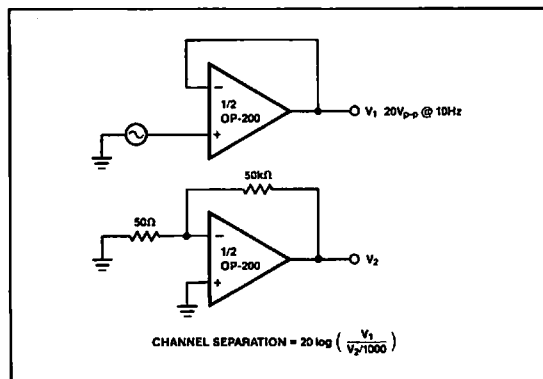
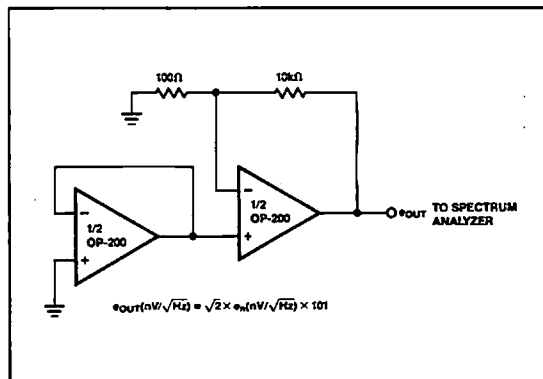


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-200E/F, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-200G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-200E			OP-200F			OP-200G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	35	100	—	80	250	—	110	300	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.2	0.5	—	0.5	1.5	—	0.6	2.0	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.08	2.5	—	0.08	3.5	—	0.1	6.0	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	0.3	5.0	—	0.3	7.0	—	0.5	10.0	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$										V/mV
		$R_L = 10k\Omega$	3000	10000	—	2000	5000	—	2000	5000	—	
		$R_L = 2k\Omega$	1500	3200	—	1000	2500	—	1000	2500	—	
Input Voltage Range	IVR	(Note 1)	± 12	± 12.5	—	± 12	± 12.5	—	± 12	± 12.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	130	—	110	130	—	105	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.15	3.2	—	0.15	5.6	—	0.3	10.0	$\mu V/V$
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 12	± 12.4	—	± 12	± 12.4	—	± 12	± 12.4	—	V
		$R_L = 2k\Omega$	± 11	± 12	—	± 11	± 12	—	± 11	± 12.2	—	
Supply Current Per Amplifier	I_{SY}	No Load	—	600	775	—	600	775	—	600	775	μA
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	10	—	—	10	—	—	10	—	nF

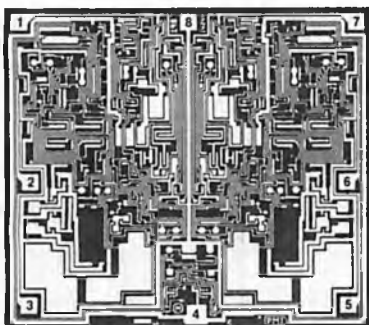
NOTES:

1. Guaranteed by CMR test.

CHANNEL SEPARATION TEST CIRCUIT**NOISE TEST SCHEMATIC**



DICE CHARACTERISTICS



DIE SIZE 0.120 × 0.106 inch, 12,720 sq. mils
(3.05 × 2.69 mm, 8.21 sq. mm)

1. OUT A
2. -IN A
3. +IN A
4. V-
5. +IN B
6. -IN B
7. OUT B
8. V+

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-200GBC	
			LIMIT	UNITS
Input Offset Voltage	V_{OS}		150	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	2	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	4	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$		
		$R_L = 10k\Omega$	3000	V/mV MIN
		$R_L = 2k\Omega$	1500	
Input Voltage Range	IVR	(Note 1)	± 12	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	3.2	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 12	
		$R_L = 2k\Omega$	± 11	V MIN
Supply Current Per Amplifier	I_{SV}	No Load	725	μA MAX

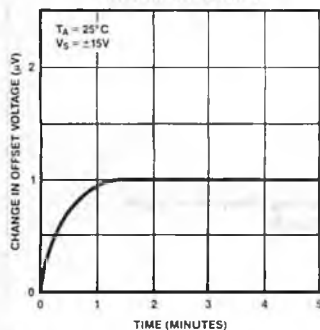
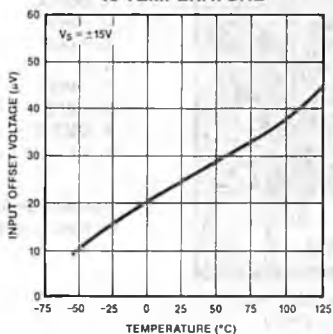
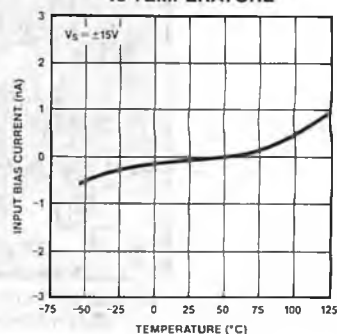
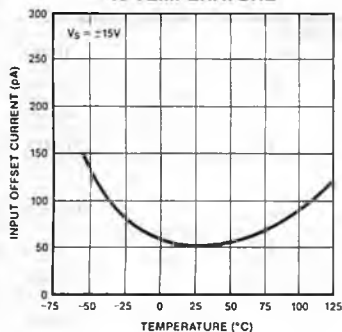
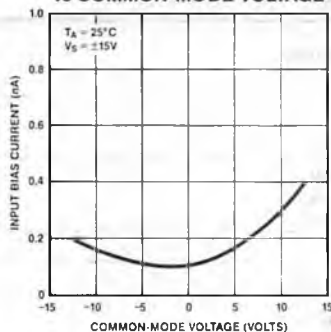
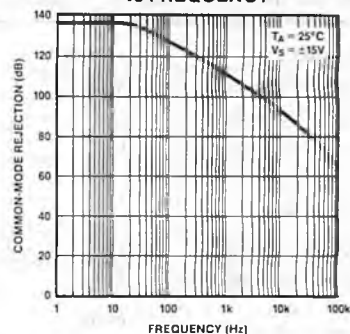
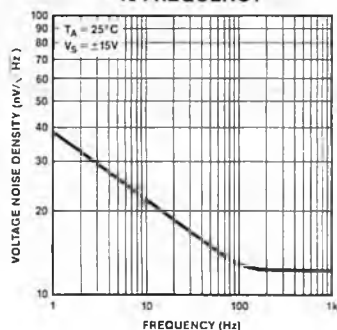
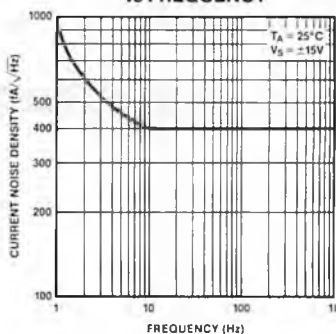
NOTES:

1. Guaranteed by CMR test.

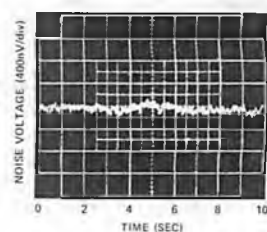
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

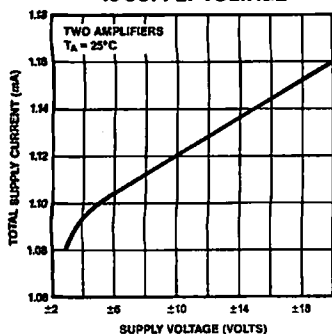
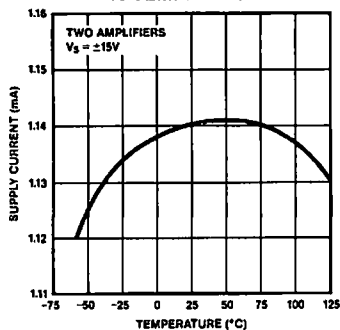
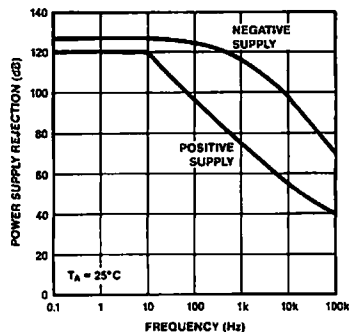
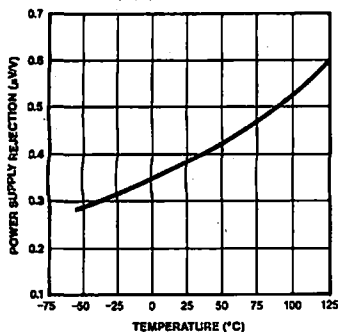
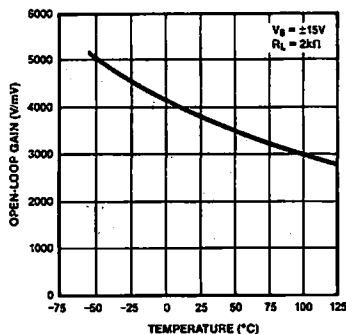
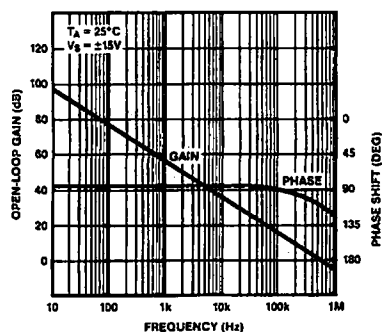
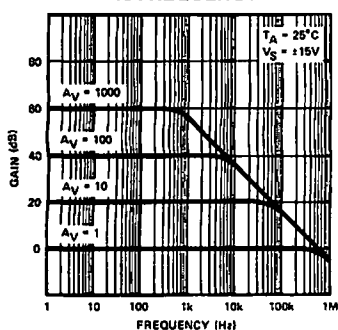
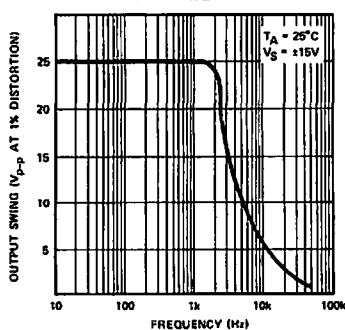
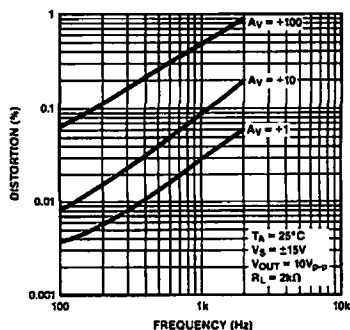
WARM-UP DRIFT

INPUT OFFSET VOLTAGE
vs TEMPERATUREINPUT BIAS CURRENT
vs TEMPERATUREINPUT OFFSET CURRENT
vs TEMPERATUREINPUT BIAS CURRENT
vs COMMON-MODE VOLTAGECOMMON-MODE REJECTION
vs FREQUENCYVOLTAGE NOISE DENSITY
vs FREQUENCYCURRENT NOISE DENSITY
vs FREQUENCY

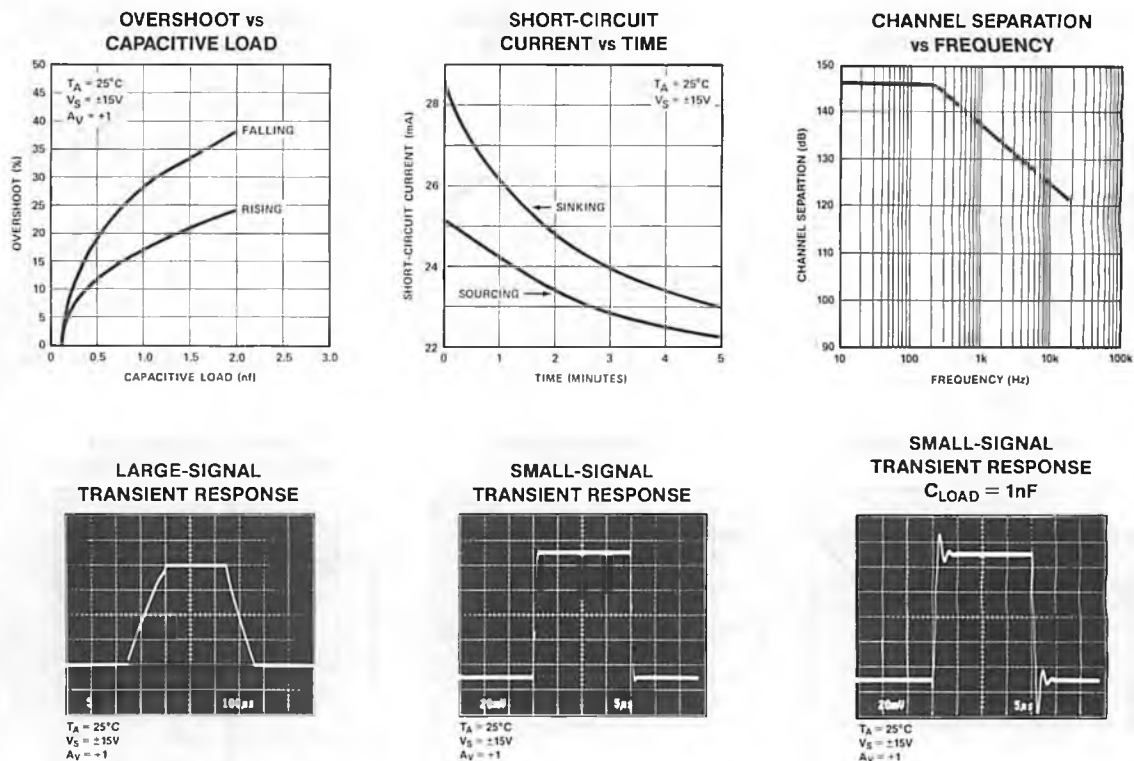
0.1Hz TO 10Hz NOISE



TYPICAL PERFORMANCE CHARACTERISTICS

 TOTAL SUPPLY CURRENT
vs SUPPLY VOLTAGE

 TOTAL SUPPLY CURRENT
vs TEMPERATURE

 POWER SUPPLY REJECTION
vs FREQUENCY

 POWER SUPPLY REJECTION
vs TEMPERATURE

 OPEN-LOOP GAIN
vs TEMPERATURE

 OPEN-LOOP GAIN AND
PHASE SHIFT vs FREQUENCY

 CLOSED-LOOP GAIN
vs FREQUENCY

 MAXIMUM OUTPUT SWING
vs FREQUENCY

 TOTAL HARMONIC
DISTORTION vs FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

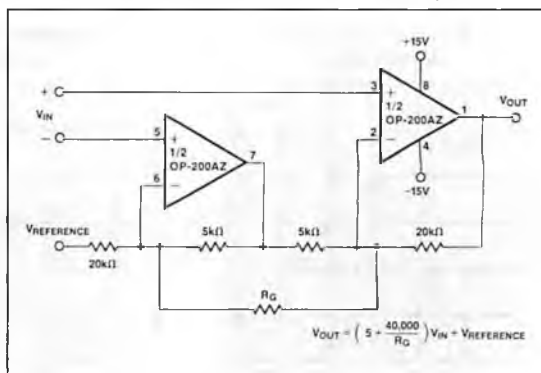
The OP-200 is inherently stable at all gains and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply decoupling is highly recommended. Proper supply decoupling reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-200.

APPLICATIONS

DUAL LOW-POWER INSTRUMENTATION AMPLIFIER

A dual instrumentation amplifier that consumes less than 33mW of power per channel is shown in Figure 1. The linearity of the instrumentation amplifier exceeds 16 bits in gains of 5 to 200 and is better than 14 bits in gains from 200 to 1000. CMRR is above 115dB (Gain = 1000). Offset voltage drift is typically $0.2\mu\text{V}/^\circ\text{C}$ over the military temperature range which is comparable to the best monolithic instrumentation amplifiers. The

FIGURE 1: Dual Low-Power Instrumentation Amplifier



bandwidth of the low-power instrumentation amplifier is a function of gain and is shown below:

GAIN	BANDWIDTH
5	150kHz
10	67kHz
100	7.5kHz
1000	500Hz

The output signal is specified with respect to the reference input, which is normally connected to analog ground. The reference input can be used to offset the output from -10V to $+10\text{V}$ if required.

PRECISION ABSOLUTE VALUE AMPLIFIER

The circuit of Figure 2 is a precision absolute value amplifier with an input impedance of $10\text{M}\Omega$. The high gain and low TCV_{OS} of the OP-200 insure accurate operation with microvolt

FIGURE 2. Precision Absolute Value Amplifier

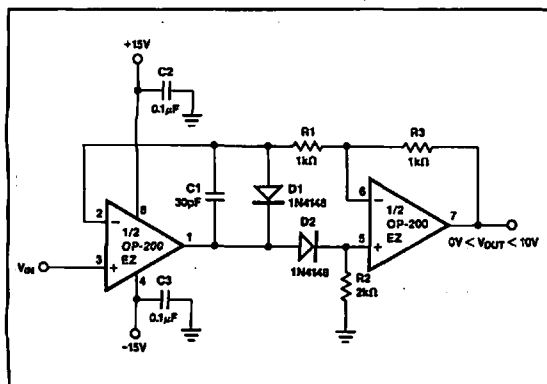
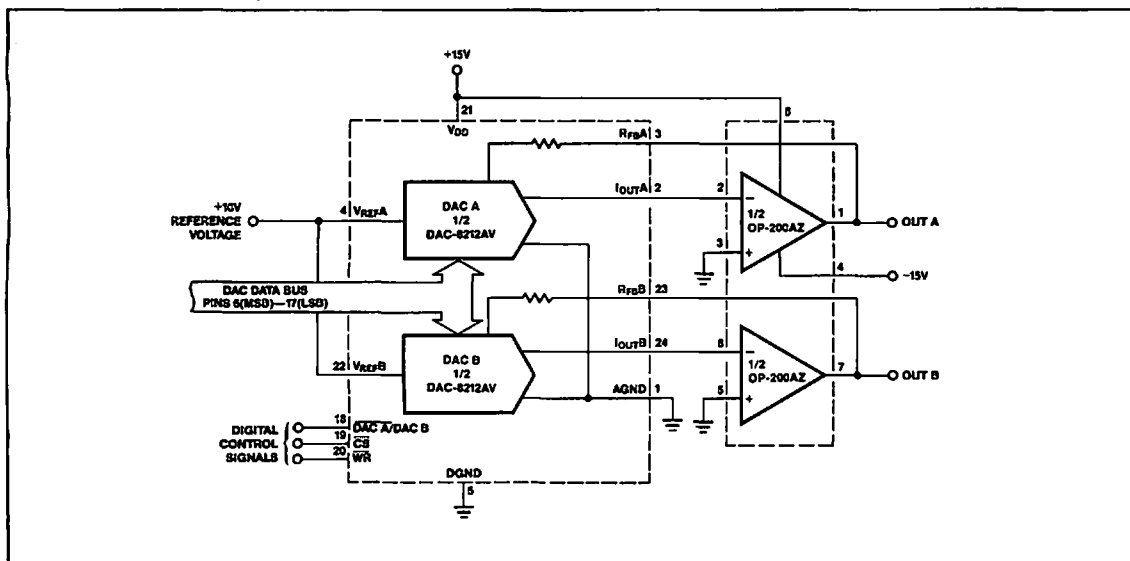


FIGURE 4. Dual 12-Bit Voltage Output DAC

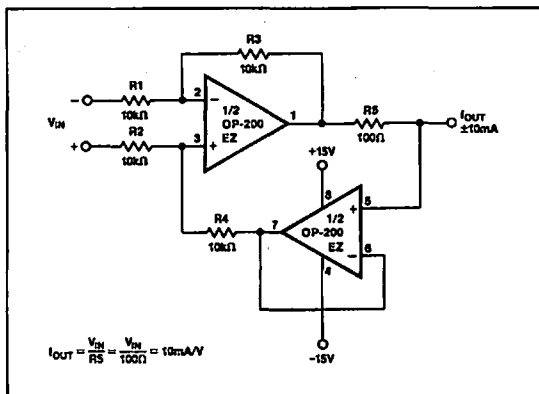


input signals. In this circuit, the input always appears as a common-mode signal to the op amps. The CMR of the OP-200 exceeds 120dB , yielding an error of less than 2ppm .

PRECISION CURRENT PUMP

Maximum output current of the precision current pump shown in Figure 3 is $\pm 10\text{mA}$. Voltage compliance is $\pm 10\text{V}$ with $\pm 15\text{V}$ supplies. Output impedance of the current transmitter exceeds $3\text{M}\Omega$ with linearity better than 16 bits.

FIGURE 3. Precision Current Pump



DUAL 12-BIT VOLTAGE OUTPUT DAC

The dual output DAC shown in Figure 4 is capable of providing untrimmed 12-bit accurate operation over the entire military temperature range. Offset voltage, bias current and gain errors of the OP-200 contribute less than $1/10$ of an LSB error at 12 bits over the military temperature range.

DUAL PRECISION VOLTAGE REFERENCE

A dual OP-200 and a REF-43, a 2.5V voltage reference, can be used to build a $\pm 2.5\text{V}$ precision voltage reference. Maximum output current from each reference is $\pm 10\text{mA}$ with load regulation under $25\mu\text{V}/\text{mA}$. Line regulation is better than $15\mu\text{V}/\text{V}$ and output voltage drift is under $20\mu\text{V}/^\circ\text{C}$. Output voltage noise from 0.1Hz to 10Hz is typically $75\mu\text{V}_{\text{p-p}}$. R1 and D1 insure correct start-up.

PROGRAMMABLE HIGH RESOLUTION WINDOW COMPARATOR

The programmable window comparator shown in Figure 6 is easily capable of 12-bit accuracy over the full military temperature range. A dual CMOS 12-bit DAC, the DAC-8212, is used in the voltage switching mode to set the upper and lower thresholds (DAC A and DAC B, respectively).

FIGURE 5. Dual Precision Voltage Reference

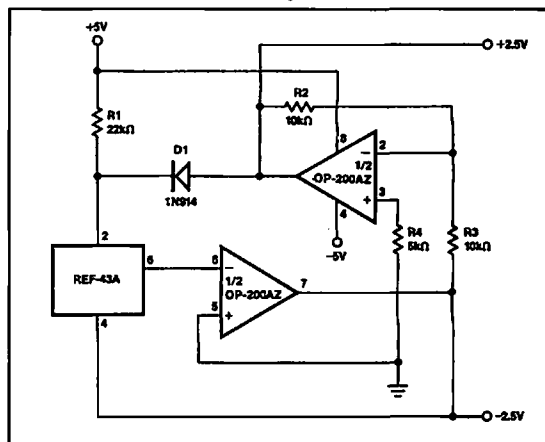
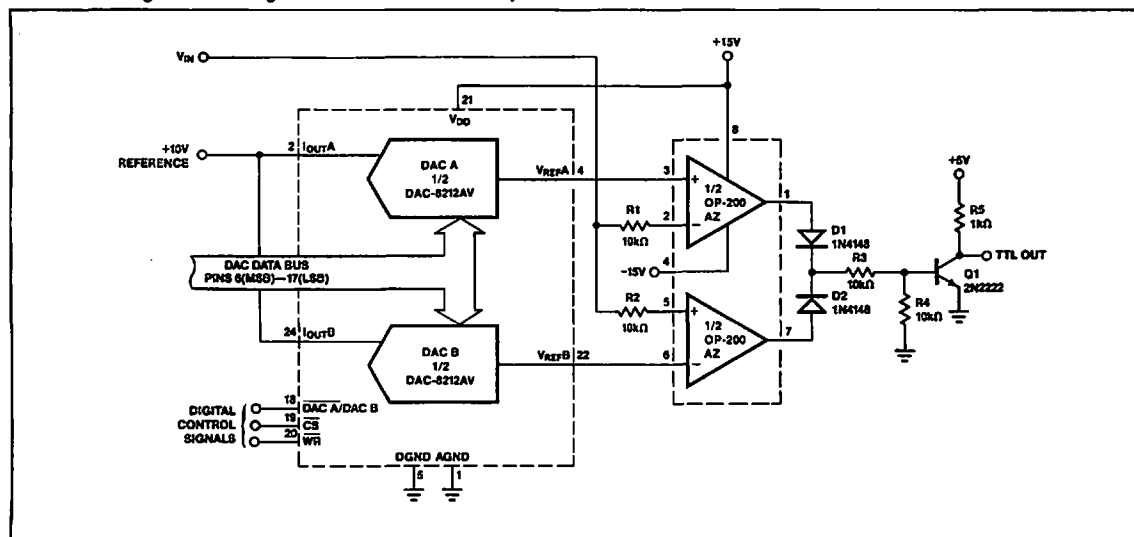


FIGURE 6. Programmable High Resolution Window Comparator



Precision Monolithics Inc.

FEATURES

- Low V_{OS} 100 μ V Max
- Offset Voltage Match 90 μ V Max
- Offset Voltage Match vs. Temp. 1.0 μ V/ $^{\circ}$ C Max
- Common-Mode Rejection Match 103dB Min
- Bias Current Match 3.5nA Max
- Low Noise 0.6 μ V $_{p-p}$ Max
- Low Bias Current 3.0nA Max
- High Channel Separation 128dB Min

ORDERING INFORMATION†

$T_A = 25^{\circ}$ C V_{OS} MAX (μ V)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
100	OP207AY*	MIL
100	OP207EY	COM
200	OP207FY	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1888 Data Book, Section 2.

GENERAL DESCRIPTION

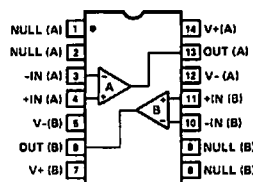
The OP-207 series of dual matched operational amplifiers consists of two independent OP-07 high performance operational amplifiers in a single 14-pin dual-in-line package. Exceptionally low offset voltage and tight matching of critical

parameters is provided between the channels of this dual operational amplifier.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. Each amplifier is fully compensated and protected.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode rejection.

PIN CONNECTIONS

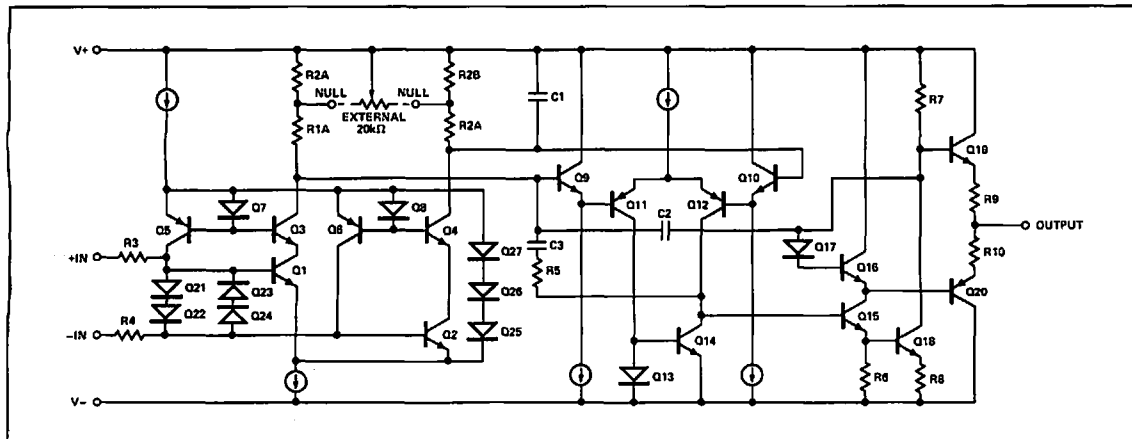


14-PIN HERMETIC DIP
(Y-Suffix)

NOTES:

1. Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B.
2. V-(A) and V-(B) are internally connected via substrate resistance.

SIMPLIFIED SCHEMATIC (1/2 OP-207)



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	$\pm 22V$
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	$\pm 30V$
Input Voltage (Note 2)	$\pm 22V$
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Operating Temperature Range	
OP-207A	$-55^{\circ}C$ to $+125^{\circ}C$
OP-207E, OP-207F	$0^{\circ}C$ to $+70^{\circ}C$
Lead Temperature (Soldering, 60 sec)	$300^{\circ}C$

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP	$108^{\circ}C$	$11.3mW/^{\circ}C$

2. For supply voltages less than $\pm 22V$, the absolute maximum input voltage is equal to the supply voltage.**MATCHING CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A/E			OP-207F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	30	90	—	50	280	μV
Average Noninverting Bias Current	I_{B+}		—	± 1.5	± 3.5	—	± 1.5	± 6.0	nA
Noninverting Offset Current	I_{OS+}		—	± 0.7	± 3.5	—	± 1.0	± 6.0	nA
Inverting Offset Current	I_{OS-}		—	± 0.7	± 3.5	—	± 1.0	± 6.0	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	103	120	—	96	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Channel Separation			126	140	—	126	140	—	dB

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}	$R_S = 100\Omega$	—	70	180	μV
Input Offset Voltage Tracking						
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	$\mu V/^{\circ}C$
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 1)	—	0.3	1.0	
Average Noninverting Bias Current	I_{B+}		—	± 2	± 6	nA
Average Drift of Non-inverting Bias Current	TCI_{B+}		—	10	—	$pA/^{\circ}C$
Noninverting Offset Current	I_{OS+}		—	2	6.5	nA
Average Drift of Non-inverting Offset Current	TCI_{OS+}		—	12	—	$pA/^{\circ}C$
Inverting Offset Current	I_{OS-}		—	2	6.5	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	100	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	$\mu V/V$

NOTE:

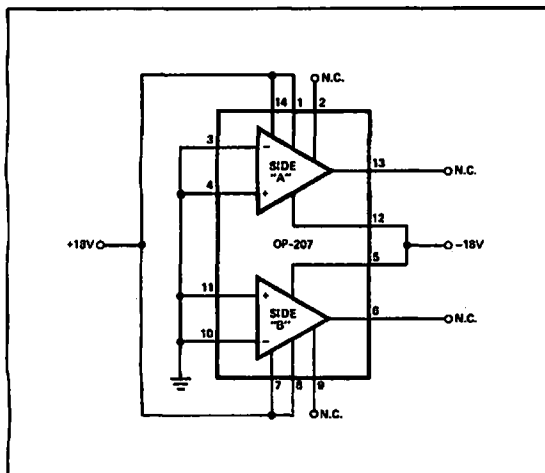
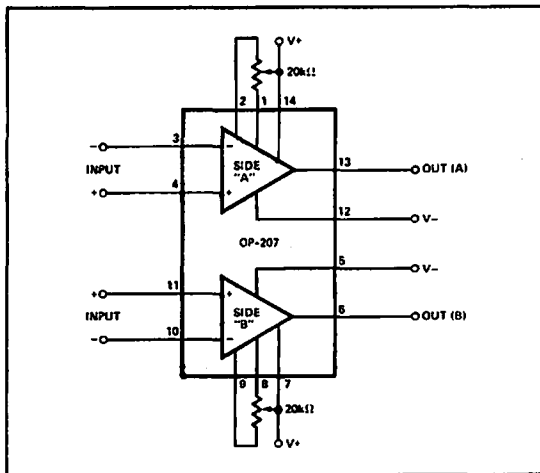
1. Sample tested.

**MATCHING CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207E			OP-207F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}	$R_B = 100\Omega$	—	60	150	—	120	350	μV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.5	1.0	—	0.9	1.5	$\mu V/^\circ C$
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 1)	—	0.3	1.0	—	0.4	1.3	$\mu V/^\circ C$
Average Noninverting Bias Current	I_{B+}		—	± 2	± 5	—	± 3	± 10	nA
Average Drift of Non-Inverting Bias Current	TCI_{B+}		—	10	—	—	12	—	$pA/^\circ C$
Noninverting Offset Current	I_{OS+}		—	2	5	—	3	10	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS+}		—	12	—	—	15	—	$pA/^\circ C$
Inverting Offset Current	I_{OS-}		—	2	5	—	3	10	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	100	117	—	94	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	10	51	—	16	100	$\mu V/V$

NOTE:

1. Sample tested.

BURN-IN CIRCUIT**OFFSET NULLING CIRCUIT**

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A/E			OP-207F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_g = 100\Omega$	—	35	100	—	60	200	μV
Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)	—	0.3	1.5	—	0.4	2.0	$\mu V/\text{Mo}$
Input Offset Current	I_{OS}		—	0.9	2.8	—	1.5	6.0	nA
Input Bias Current	I_B		—	± 1	± 3	—	± 2	± 7	nA
Input Noise Voltage	e_{n-p-p}	0.1Hz to 10Hz (Note 2)	—	0.35	0.6	—	0.35	0.6	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 2)	—	10.3	18.0	—	10.3	18.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	10.0	13.0	—	10.0	13.0	
		$f_O = 1000\text{Hz}$ (Note 2)	—	9.6	—	—	9.6	—	
Input Noise Current	i_{n-p-p}	0.1Hz to 10Hz (Note 2)	—	14	30	—	14	30	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$ (Note 2)	—	0.32	0.60	—	0.32	0.60	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 2)	—	0.14	0.23	—	0.14	0.23	
		$f_O = 1000\text{Hz}$ (Note 2)	—	0.12	—	—	0.12	—	
Input Resistance — Differential Mode	R_{IN}	(Note 3)	20	60	—	8	30	—	M Ω
Input Resistance — Common-Mode	$R_{IN CM}$		—	200	—	—	120	—	G Ω
Input Voltage Range	IVR		± 13	± 14	—	± 13	± 14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	200	500	—	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12.5	± 13.0	—	± 12.5	± 13.0	—	V
		$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 12.0	± 12.8	—	
		$R_L \geq 1k\Omega$	± 10.0	± 12.0	—	± 10.0	± 12.0	—	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.2	—	—	0.2	—	V/ μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	60	—	—	60	—	Ω
Power Consumption	P_d	No Load, Both Amplifiers	—	180	240	—	200	300	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	± 4	—	—	± 4	—	mV
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically $2.5\mu V$. Parameter is sample tested.
2. Sample tested.
3. Guaranteed by design.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	75	230	μV
Average Input Offset Voltage Drift						
Without External Trim	TCV_{OS}	$R_P = 20k\Omega$ (Notes 1, 2)	—	0.4	1.3	$\mu V/^\circ C$
With External Trim	TCV_{OSn}		—	0.4	—	
Input Offset Current	I_{OS}		—	1.8	5.6	nA
Average Input Offset Current Drift	TCI_{OS}		—	10	—	$pA/^\circ C$
Input Bias Current	I_B		—	± 3.0	± 5.6	nA
Average Input Bias Current Drift	TCI_B		—	12	—	$pA/^\circ C$
Input Voltage Range	IVR		± 13	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	400	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	V

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-207E			OP-207F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 100\Omega$	—	60	200	—	90	350	μV
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_P = 20k\Omega$ (Notes 1, 2)	—	0.4	1.3	—	0.7	1.8	$\mu V/^\circ C$
With External Trim	TCV_{OSn}		—	0.4	—	—	0.7	—	
Input Offset Current	I_{OS}		—	1.4	5	—	2.5	10	nA
Average Input Offset Current Drift	TCI_{OS}		—	10	—	—	12	—	$pA/^\circ C$
Input Bias Current	I_B		—	± 2	± 5	—	± 3	± 11	nA
Average Input Bias Current Drift	TCI_B		—	12	—	—	18	—	$pA/^\circ C$
Input Voltage Range	IVR		± 13	± 13.5	—	± 13	± 13.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	120	—	97	117	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	150	400	—	120	350	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12.0	± 12.8	—	± 12.0	± 12.8	—	V

NOTES:

- Exclude first hour of operation to allow for stabilization of external circuitry.
- Sample tested.

APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide a powerful tool for the solution of some difficult circuit design problems. Circuits include true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references, and many other demanding applications. These designs all require good matching between two operational amplifiers.

The circuit below, a differential-in, differential-out amplifier, shows how errors can be reduced. Assuming the resistors used are matched, the gain of each side will be identical; if the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* between the amplifiers' offset voltages. This error-cancellation principle holds for a number of input-referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents,

common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made exceptionally high; this is very important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than errors due to noise or drift with temperature. For example, consider the case of two op amps, each with 80dB (100 μ V/V) CMRR. If the CMRR of one device is +100 μ V/V CMRR and the other is -100 μ V/V, then the net CMRR will be 200 μ V/V, a 6dB degradation. The matching of CMRR increases the effective CMRR when used as an instrumentation input stage.

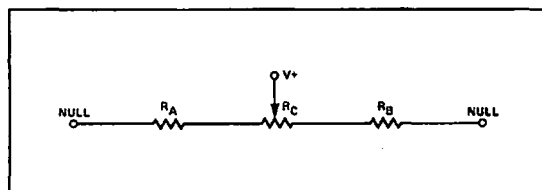
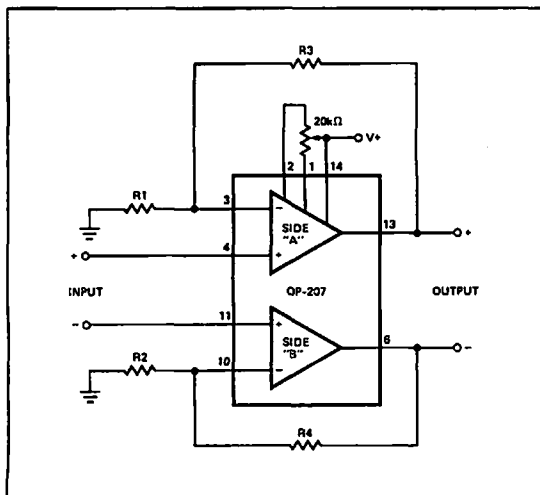
POWER SUPPLIES

The $V+$ supply terminals are completely independent and may be powered by separate supplies if desired. However, this approach would sacrifice the advantages of the power-supply-rejection-ratio matching. The $V-$ supply terminals are both connected to the common substrate and must be tied to the same voltage.

OFFSET TRIMMING

Offset voltage trimming is provided for each amplifier. Guaranteed performance over temperature is obtained by trimming one side (side A) to match the offset of the other. A net differential offset of zero results. This procedure is used during factory testing of the devices. The same results are obtained by trimming side B to match side A or by nulling each side individually.

The OP-207 is designed to provide best drift performance when trimmed with a 20k Ω potentiometer; this value provides about ± 4 mV of adjustment range which is adequate for most applications. Trimming resolution can be increased by use of the circuit shown below.



Precision Monolithics Inc.

FEATURES

- High Slew Rate 10V/ μ s Min
- Fast Settling Time 0.9 μ s to 0.1% Typ
- Low Input Offset Voltage Drift 10 μ V/ $^{\circ}$ C Max
- Wide Bandwidth 3.5MHz Min
- Temperature-Compensated Input Bias Currents
- Guaranteed Input Bias Current 18nA Max (125 $^{\circ}$ C)
- Bias Current Specified Warm-Up Over Temperature
- Low Input Noise Current 0.01pA/ $\sqrt{\text{Hz}}$ Typ
- High Common-Mode Rejection Ratio 86dB Min
- Pin Compatible With Standard Dual Pinouts
- 125 $^{\circ}$ C Temperature Tested DICE
- Models With MIL-STD-883 Class B Processing Available

ORDERING INFORMATION†

T _A = 25 $^{\circ}$ C V _{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	LCC 20-PIN	
1.0	OP215AJ*	OP215AZ*	—	MIL
1.0	OP215EJ	OP215EZ	—	COM
2.0	OP215BJ*	OP215BZ*	OP215BRC/883	MIL
2.0	OP215FJ	OP215FZ	—	COM
4.0	OP215CJ/883	OP215CZ/883	—	MIL
6.0	—	OP215GZ	—	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-215 offers the proven JFET-input performance advantages of high speed and low input bias current with the

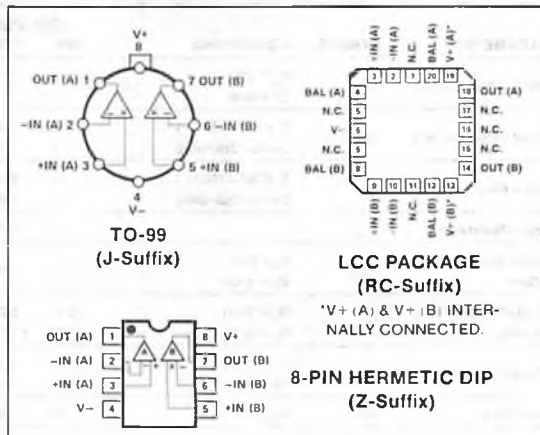
tracking and convenience advantages of a dual op-amp configuration.

Low input offset voltages, low input currents, and low drift are featured in these high-speed amplifiers.

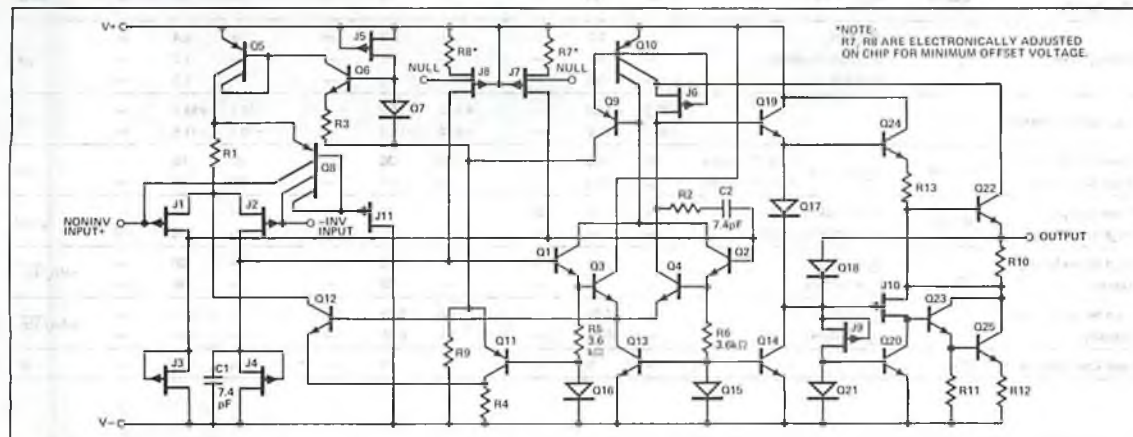
On-chip zener-zap trimming is used to achieve low V_{OS} while a bias-current compensation scheme gives a low input bias current at elevated temperatures. Thus the OP-215 features an input bias current of 18nA at 125 $^{\circ}$ C ambient (not junction) temperature which greatly extends the application usefulness of this device.

Applications include high-speed amplifiers for current output DACs, active filters, sample-and-hold buffers, and photocell amplifiers. For additional precision JFET op amps, see the OP-15/16/17 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/2 OP-215)



**ABSOLUTE MAXIMUM RATINGS** (Note 2)**Supply Voltage**

OP-215A, OP-215B, OP-215E, OP-215F

(All DICE except GR) $\pm 22\text{V}$ OP-215C, OP-215G (GR DICE only) $\pm 18\text{V}$ **Internal Power Dissipation** (Note 1) 500mW**Operating Temperature Range**OP-215A, OP-215B, OP-215C -55°C to $+125^{\circ}\text{C}$ OP-215E, OP-215F, OP-215G 0°C to $+70^{\circ}\text{C}$ **Maximum Junction Temperature** (T_J) $+150^{\circ}\text{C}$ **Differential Input Voltage**OP-215A, OP-215B, (All DICE except GR) $\pm 40\text{V}$ OP-215E, OP-215F, (All DICE except GR) $\pm 20\text{V}$ OP-215C, OP-215G (GR DICE only) $\pm 30\text{V}$ **Input Voltage**OP-215A, OP-215B, (All DICE except GR) $\pm 20\text{V}$ OP-215E, OP-215F, (All DICE except GR) $\pm 20\text{V}$ OP-215C, OP-215G (GR DICE only) $\pm 18\text{V}$

(Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.)

Output Short-Circuit Duration Indefinite**Storage Temperature Range** -65°C to $+150^{\circ}\text{C}$ **Lead Temperature (Soldering, 60 sec)** 300°C **DICE Junction Temperature** (T_J) -65°C to $+150^{\circ}\text{C}$ **NOTES:**

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
20-Pin LCC (RC)	80°C	$7.5\text{mW}/^{\circ}\text{C}$
TO-99 (J)	80°C	$7.1\text{mW}/^{\circ}\text{C}$
9-Pin Hermetic DIP (Z)	75°C	$6.7\text{mW}/^{\circ}\text{C}$

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215A/E			OP-215B/F			OP-215C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 60\Omega$ 'G' Grade	—	0.2	1.0	—	0.8	2.0	—	2.0	4.0	mV
Input Offset Current	I_{OS}	$T_J = 25^{\circ}\text{C}$ (Note 1)	—	3	50	—	3	50	—	3	100	μA
		Device Operating	—	5	100	—	5	100	—	5	200	
Input Bias Current	I_B	$T_J = 25^{\circ}\text{C}$ (Note 1)	—	± 15	± 100	—	± 15	± 200	—	± 15	± 300	μA
		Device Operating	—	± 18	± 300	—	± 18	± 400	—	± 18	± 600	
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10\text{V}$	150	500	—	75	220	—	50	200	—	V/mV
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
		$R_L = 2k\Omega$	± 11	± 12.7	—	± 11	± 12.7	—	± 11	± 12.7	—	
Supply Current	I_{SY}	'G' Grade	—	6.0	8.5	—	6.0	8.5	—	7.0	10.0	mA
			—	—	—	—	—	—	—	7.0	12.0	
Slew Rate	SR	$A_{VCL} = +1$	10	18	—	7.5	18	—	5	15	—	V/ μs
Gain Bandwidth Product	GBW	(Note 3)	3.5	5.7	—	3.5	5.7	—	3.0	5.4	—	MHz
Closed-Loop Bandwidth	CLBW	$A_{VCL} = +1$	—	13	—	—	13	—	—	12	—	MHz
Settling Time	t_s	to 0.01%	—	2.3	—	—	2.3	—	—	2.4	—	μs
		to 0.05% (Note 2)	—	1.1	—	—	1.1	—	—	1.2	—	
		to 0.10%	—	0.9	—	—	0.9	—	—	1.0	—	
Input Voltage Range	IVR		$+10.2$	$+14.8$	—	$+10.2$	$+14.8$	—	$+10.1$	$+14.8$	—	V
			-10.2	-11.5	—	-10.2	-11.5	—	-10.1	-11.5	—	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 1\text{VR}$	88	100	—	88	100	—	82	96	—	dB
		A, B, C Grades E, F, G Grades	82	100	—	82	100	—	80	96	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10\text{V}$ to $\pm 18\text{V}$ $V_S = \pm 10\text{V}$ to $\pm 15\text{V}$	—	10	51	—	10	80	—	18	100	$\mu\text{V/V}$
Input Noise Voltage Density	e_n	$f_O = 100\text{Hz}$	—	20	—	—	20	—	—	20	—	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 1000\text{Hz}$	—	15	—	—	15	—	—	15	—	
Input Noise Current Density	i_n	$f_O = 100\text{Hz}$	—	0.01	—	—	0.01	—	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
		$f_O = 1000\text{Hz}$	—	0.01	—	—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}		—	3	—	—	3	—	—	3	—	pF

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215A			OP-215B			OP-215C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.5	2.0	—	1.5	3.0	—	3.0	6.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	—	3	10	—	3	10	—	6	—	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	3	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = +125^\circ C$ $T_A = +125^\circ C$, Device Operating	—	0.8	8	—	0.8	8	—	1.0	12	nA
Input Bias Current (Note 1)	I_B	$T_J = +125^\circ C$ $T_A = +125^\circ C$, Device Operating	—	± 1.5	± 10	—	± 1.5	± 10	—	± 1.8	± 15	nA
Input Voltage Range	IVR		+10.2 -10.2	+14.6 -11.3	—	+10.2 -10.2	+14.6 -11.3	—	+10.1 -10.1	+14.6 -11.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	62	97	—	62	97	—	60	93	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$ $V_S = \pm 10V$ to $\pm 15V$	—	10	100	—	15	100	—	—	—	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	30	110	—	30	110	—	25	100	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

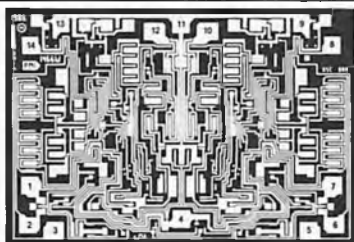
PARAMETER	SYMBOL	CONDITIONS	OP-215E			OP-215F			OP-215G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.4	1.65	—	1.4	2.65	—	3.5	6.0	mV
Average Input Offset Voltage Drift												
Without External Trim	TCV_{OS}	(Note 3)	—	3	15	—	3	15	—	6	—	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_P = 100k\Omega$	—	3	—	—	3	—	—	4	—	
Input Offset Current (Note 1)	I_{OS}	$T_J = +70^\circ C$ $T_A = +70^\circ C$, Device Operating	—	0.06	0.45	—	0.06	0.45	—	0.08	0.65	nA
Input Bias Current (Note 1)	I_B	$T_J = +70^\circ C$ $T_A = +70^\circ C$, Device Operating	—	± 0.12	± 0.70	—	± 0.12	± 0.70	—	± 0.14	± 0.9	nA
Input Voltage Range	IVR		+10.2 -10.2	+14.7 -11.4	—	+10.2 -10.2	+14.7 -11.4	—	+10.1 -10.1	+14.7 -11.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	60	96	—	60	96	—	76	94	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$ $V_S = \pm 10V$ to $\pm 15V$	—	13	100	—	13	100	—	—	—	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$ $V_O = \pm 10V$	50	180	—	50	180	—	35	130	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V

NOTES:

- Input bias current is specified for two different conditions. The $T_J = 25^\circ C$ specification is with the junction at ambient temperature; the Device Operating specification is with the device operating in a warmed-up condition at $25^\circ C$ ambient. The warmed-up bias current value is correlated to the junction temperature value via the curves of I_B vs. T_J and I_B vs. T_A . PMI has a bias current compensation circuit which gives improved bias current and bias current over temperature vs. standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Settling time is defined here for a unity gain inverter connection using $2k\Omega$ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within a specified percent of its final value from the time a $10V$ step input is applied to the inverter. See settling time test circuit.
- Sample tested.



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



- | | |
|---------------------------|------------------------|
| 1. INVERTING INPUT (A) | 8. NULL (B) |
| 2. NONINVERTING INPUT (A) | 9. V ⁺ |
| 3. NULL (A) | 10. V _O (B) |
| 4. V ⁻ | 11. V ⁺ |
| 5. NULL (B) | 12. V _O (A) |
| 6. NONINVERTING INPUT (B) | 13. V ⁺ |
| 7. INVERTING INPUT (B) | 14. NULL (A) |

ALL V⁺ PADS ARE INTERNALLY CONNECTED.

DIE SIZE 0.110 × 0.075 inch, 8250 sq. mils (2.79 × 1.91 mm, 5.33 sq. mm)

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at V_S = ±15V, T_A = 25° C for OP-215N, OP-215G and OP-215GR devices; T_A = 125° C for OP-215NT and OP-215GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215NT LIMIT	OP-215N LIMIT	OP-215GT LIMIT	OP-215G LIMIT	OP-215GR LIMIT	UNITS
Input Offset Voltage	V _{OS}	R _S = 50Ω	2	1	3	2	6	mV MAX
Input Bias Current	I _B		±18	—	±18	—	—	nA MAX
Input Offset Current	I _{OS}		14	—	14	—	—	nA MAX
Large-Signal Voltage Gain	A _{VO}	V _O = ±10V, R _L = 2kΩ	30	150	30	75	50	V/mV MIN
Input Voltage Range	IVR		±10.2	±10.2	±10.2	±10.2	±10.1	V MIN
Common-Mode Rejection Ratio	CMRR	V _{CM} = ±IVR	82	86	82	86	82	dB MIN
Power Supply Rejection Ratio	PSRR	V _S = ±10 to ±16V V _S = ±10 to ±15V	100 —	51 —	100 —	80 —	— 100	μV/V MAX
Output Voltage Swing	V _O	R _L = 10kΩ R _L = 2kΩ	±12 —	±12 ±11	±12 —	±12 ±11	±12 ±11	V MIN
Supply Current	I _{SY}		—	8.5	—	8.5	12.0	mA MAX

NOTES:

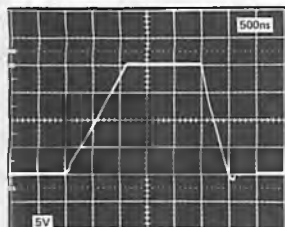
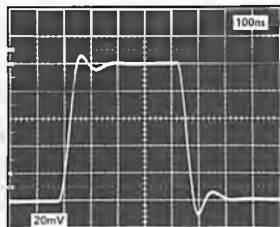
For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

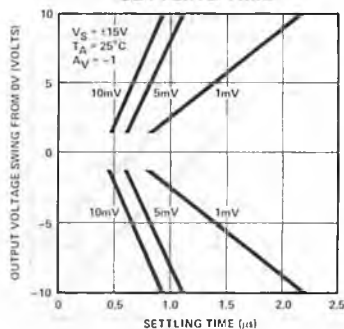
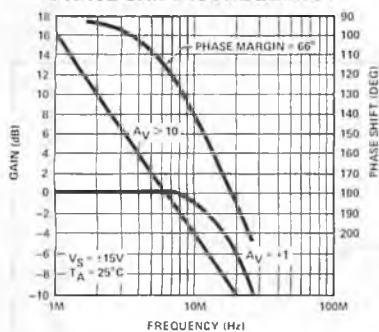
TYPICAL ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25° C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-215NT TYPICAL	OP-215N TYPICAL	OP-215GT TYPICAL	OP-215G TYPICAL	OP-215GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV _{OS}	Unnulled R _P = 100kΩ	2	2	3	3	4	μV/° C
Average Input Offset Voltage Drift	TCV _{OSn}	Nulled R _P = 100kΩ	0.5	0.5	1	1	2	μV/° C
Input Offset Current	I _{OS}		3	3	3	3	3	pA
Input Bias Current	I _B		±15	±15	±15	±15	±15	pA
Slew Rate	SR	A _{VCL} = +1	17	17	16	16	15	V/μs
Settling Time	t _S	to 0.01%	2.2	2.2	2.3	2.3	2.4	μs
		to 0.05%	1.1	1.1	1.1	1.1	1.2	
		to 0.10%	0.9	0.9	0.9	0.9	1.0	
Gain Bandwidth Product	GBW		6.0	6.0	5.7	5.7	5.4	MHz
Closed-Loop Bandwidth	CLBW	A _{VCL} = +1	14	14	13	13	12	MHz
Input Noise Voltage Density	e _n	f _O = 100Hz	20	20	20	20	20	nV/√Hz
		f _O = 1000Hz	15	15	15	15	15	
Input Noise Current Density	i _n	f _O = 100Hz	0.01	0.01	0.01	0.01	0.01	pA/√Hz
		f _O = 1000Hz	0.01	0.01	0.01	0.01	0.01	
Input Capacitance	C _{IN}		3	3	3	3	3	pF

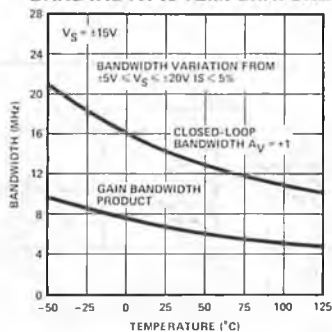
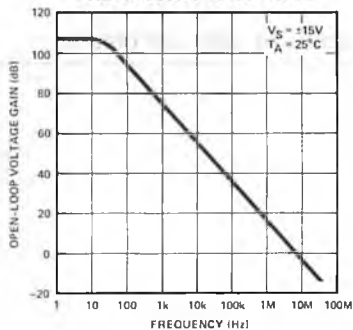
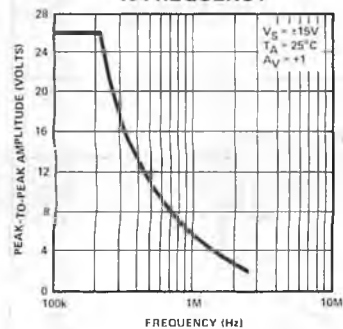
TYPICAL PERFORMANCE CHARACTERISTICS

LARGE-SIGNAL
TRANSIENT RESPONSESMALL-SIGNAL
TRANSIENT RESPONSE

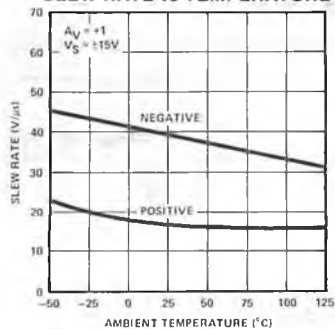
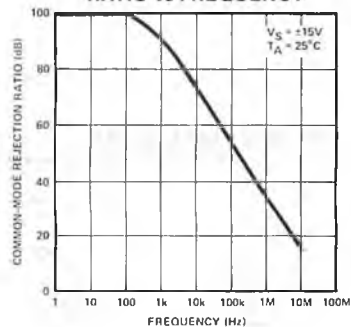
SETTLING TIME

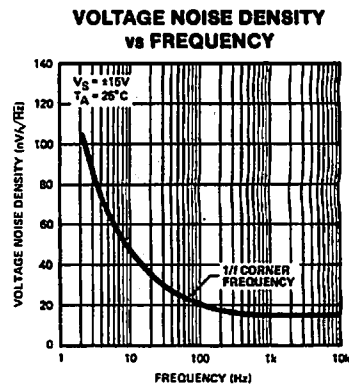
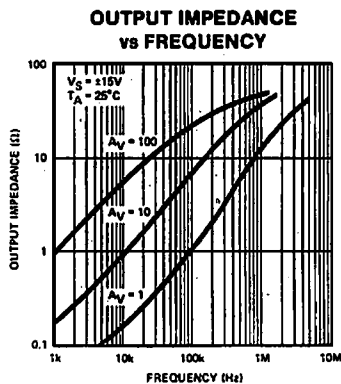
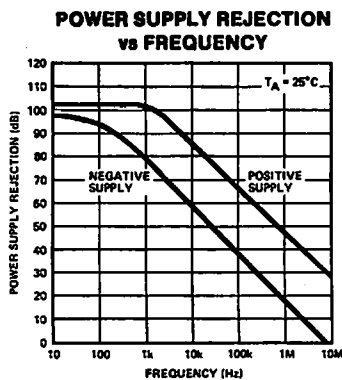
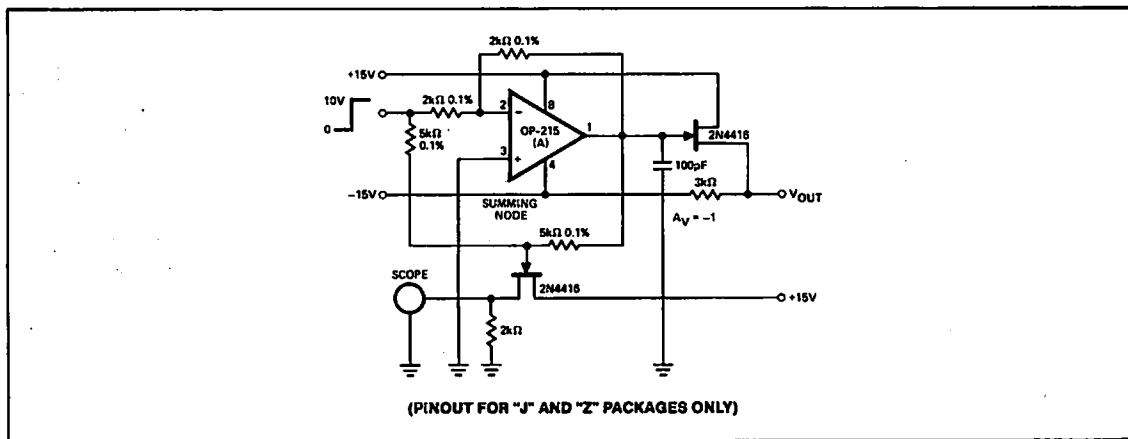
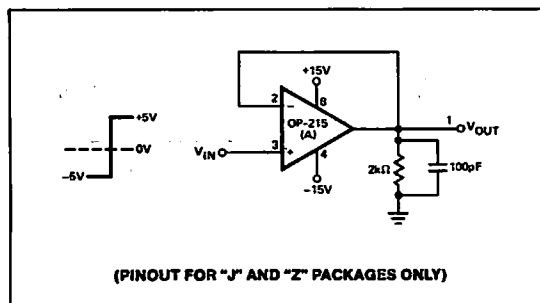
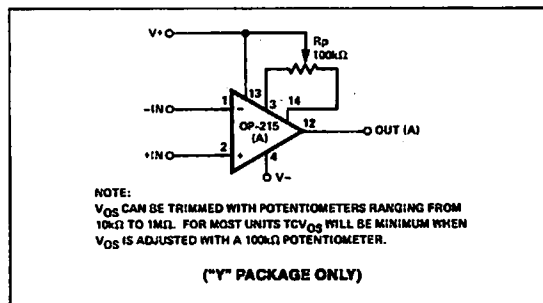
CLOSED-LOOP
BANDWIDTH AND
PHASE SHIFT vs FREQUENCY

BANDWIDTH vs TEMPERATURE

OPEN-LOOP
FREQUENCY RESPONSEMAXIMUM OUTPUT SWING
vs FREQUENCY

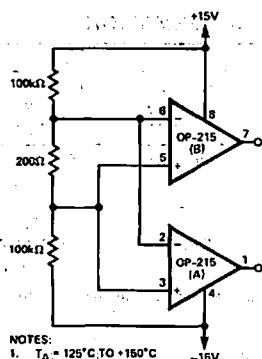
SLEW RATE vs TEMPERATURE

COMMON-MODE REJECTION
RATIO vs FREQUENCY

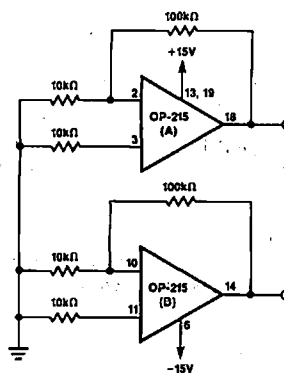
TYPICAL PERFORMANCE CHARACTERISTICS

BASIC CONNECTIONS
SETTLING TIME TEST CIRCUIT

SLEW RATE TEST CIRCUIT

INPUT OFFSET VOLTAGE NULLING


BASIC CONNECTIONS

BURN-IN CIRCUIT



("J" AND "Z" PACKAGES ONLY)



("RC" PACKAGE)

APPLICATIONS INFORMATION

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to

AC ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the negative input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than, or equal to, the original feedback-pole time constant.



OP-220

DUAL MICROPOWER OPERATIONAL AMPLIFIER (SINGLE OR DUAL SUPPLY)

Precision Monolithics Inc.

FEATURES

- Excellent TCV_{OS} Match $2\mu V/^{\circ}C$ Max
- Low Input Offset Voltage $150\mu V$ Max
- Low Supply Current $100\mu A$
- Single-Supply Operation $+5V$ to $+30V$
- Low Input Offset Voltage Drift $0.75\mu V/^{\circ}C$
- High Open-Loop Gain $2000V/mV$
- High PSRR $3\mu V/V$
- Low Input Bias Current $12nA$
- Wide Common-Mode Voltage Range $V-$ to within $1.5V$ of $V+$
- Pin Compatible with 1458, LM158, LM2904

GENERAL DESCRIPTION

The OP-220 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The low offset voltage, and input offset voltage tracking as low as $1.0\mu V/^{\circ}C$, make this the first micropower precision dual operational amplifier.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provides high performance in instrumentation amplifier designs. The individual amplifiers feature extremely low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection ratios.

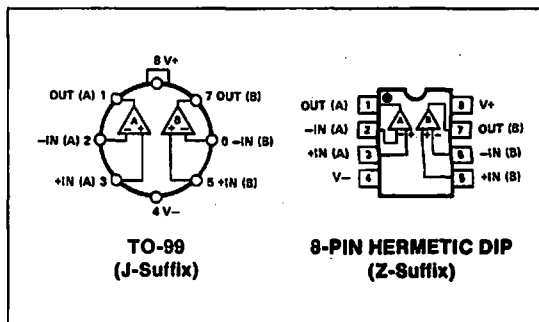
ORDERING INFORMATION†

$T_A = 25^{\circ}C$ V_{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	
150	OP220AJ*	OP220AZ	MIL
150	—	OP220EZ	IND
300	OP220BJ	—	MIL
300	—	OP220FZ	IND
750	OP220CJ*	OP220CZ	MIL
750	OP220GJ	OP220GZ	IND

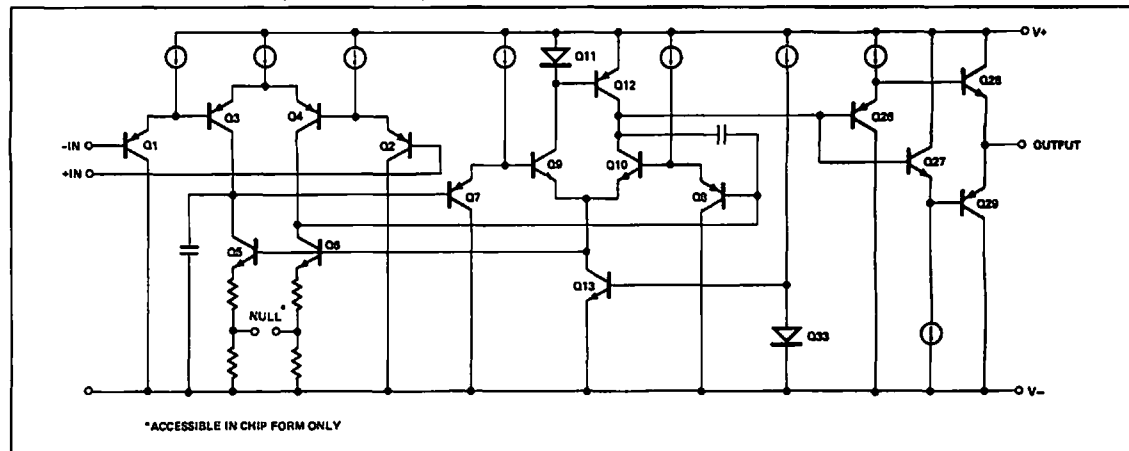
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (Each Amplifier)



**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage	±18V
Power Dissipation	500mW
Differential Input Voltage	30V or Supply Voltage
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-220A, B, C	-55°C to +125°C
OP-220E, F, G	-25°C to +85°C

Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_J)	-65°C to +150°C

NOTE:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E			OP-220B/F			OP-220C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	120	150	—	250	300	—	500	750	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.15	1.5	—	0.2	2	—	0.2	3.5	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	20	—	13	25	—	14	30	nA
Input Voltage Range	IVR	$V^+ = 5V, V^- = 0V$, $V_S = \pm 15V$	0/3.5 -15/13.5	—	—	0/3.5 -15/13.5	—	—	0/3.5 -15/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V^+ = 5V, V^- = 0V$, $0V \leq V_{CM} \leq 3.5V$	90	100	—	85	90	—	75	85	—	dB
		$V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.5V$	95	100	—	90	95	—	80	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	3	10	—	10	32	—	32	100	$\mu V/V$
		$V^- = 0V, V^+ = 5V$ to 30V	—	6	18	—	18	57	—	57	180	
Large-Signal Voltage Gain	A_{VO}	$V^+ = 5V, V^- = 0V, R_L = 100k\Omega$ $1V \leq V_O \leq 3.5V$	500	1000	—	500	800	—	300	500	—	V/mV
		$V_S = \pm 15V, R_L = 25k\Omega$	1000	2000	—	1000	2000	—	800	1600	—	
		$V_O = \pm 10V$	—	—	—	—	—	—	—	—	—	
Output Voltage Swing	V_O	$V^+ = 5V, V^- = 0V$, $R_L = 10k\Omega$	0.7/4	—	—	0.7/4	—	—	0.8/4	—	—	V
		$V_S = \pm 15V, R_L = 25k\Omega$	±14	—	—	±14	—	—	±14	—	—	
Slew Rate	SR	$R_L = 25k\Omega$, (Note 1)	—	0.05	—	—	0.05	—	—	0.05	—	V/ μs
Bandwidth	BW	$A_{VCL} = +1, R_L = 25k\Omega$	—	200	—	—	200	—	—	200	—	kHz
Supply Current (Both Amplifiers)	I_{SV}	$V_S = \pm 2.5V$, No Load	—	100	115	—	115	125	—	125	135	μA
		$V_S = \pm 15V$, No Load	—	140	170	—	150	190	—	205	220	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-220A, B, and C, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-220 E, F, and G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E			OP-220B/F			OP-220C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	$V_S = \pm 15V$	—	0.75	1.5	—	1.2	2	—	2	3	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	200	300	—	400	500	—	1000	1300	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	2	—	0.6	2.5	—	0.8	5	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	12	25	—	13	30	—	14	40	nA
Input Voltage Range	IVR	$V^+ = 5V, V^- = 0V$, $V_S = \pm 15V$	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	$V^+ = 5V, V^- = 0V$, $0V \leq V_{CM} \leq 3.2V$	85	90	—	80	85	—	70	80	—	dB
		$V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.2V$	90	95	—	85	90	—	75	85	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	6	18	—	18	57	—	57	180	$\mu V/V$
		$V^- = 0V, V^+ = 5V$ to 30V	—	10	32	—	32	100	—	100	320	

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-220A, B, and C, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-220 E, F, and G, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E			OP-220B/F			OP-220C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 50k\Omega$ $V_O = \pm 10V$	500	1000	—	500	800	—	400	500	—	V/mV
Output Voltage Swing	V_O	$V_+ = 5V$, $V_- = 0V$, $R_L = 20k\Omega$ $V_S = \pm 15V$, $R_L = 50k\Omega$	0.9/3.8	—	—	0.9/3.8	—	—	1/3.8	—	—	V
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	—	135	170	—	155	185	—	170	210	μA
			—	190	250	—	200	260	—	275	330	

NOTE: 1. Sample tested.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220A/E			OP-220B/F			OP-220C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	150	300	—	250	500	—	300	600	μV
Average Noninverting Bias Current	I_{B^+}	$V_{CM} = 0$	—	10	20	—	15	25	—	20	30	nA
Noninverting Offset Current	I_{OS^+}	$V_{CM} = 0$	—	0.7	1.5	—	1	2	—	1.4	2.5	nA
Common-Mode Rejection Ratio Match (Note 1)	$\Delta CMRR$	$V_{CM} = -15V$ to $+13.5V$	92	100	—	87	95	—	72	85	—	dB
Power Supply Rejection Ratio Match (Note 2)	$\Delta PSRR$	$V_S = \pm 2.5V$ to $\pm 15V$	—	6	14	—	18	44	—	57	140	$\mu V/V$

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-220A, B and C; $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-220 E, F and G, unless otherwise noted. Grades E, F, and G are sample tested.

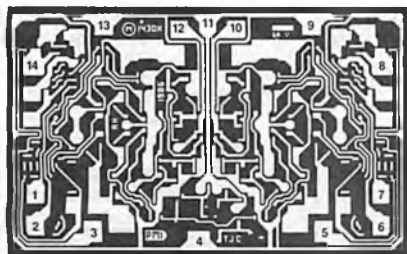
PARAMETER	SYMBOL	CONDITIONS	OP-220A/E			OP-220B/F			OP-220C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	250	500	—	400	800	—	800	1600	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	(Note 3)	—	1	2	—	1.5	3	—	1.5	5	$\mu V/^\circ C$
Average Noninverting Bias Current	I_{B^+}	$V_{CM} = 0$	—	10	25	—	15	30	—	22	40	nA
Average Drift of Noninverting Bias Current	TCI_{B^+}	$V_{CM} = 0$ (Note 3)	—	15	25	—	15	30	—	30	50	$pA/^\circ C$
Noninverting Offset Current	I_{OS^+}	$V_{CM} = 0$	—	0.7	2	—	1	2.5	—	2.5	5	nA
Average Drift of Noninverting Offset Current	TCI_{OS^+}	$V_{CM} = 0$ (Note 3)	—	7	15	—	12	22.5	—	15	30	$pA/^\circ C$
Common-Mode Rejection Ratio Match (Note 1)	$\Delta CMRR$	$V_{CM} = -15V$ to $+13V$	87	98	—	82	96	—	72	80	—	dB
Power Supply Rejection Ratio Match (Note 2)	$\Delta PSRR$	$V_S = \pm 2.5V$ to $\pm 15V$	—	10	26	—	30	78	—	57	250	$\mu V/V$

NOTES:

- $\Delta CMRR$ is $20 \log_{10} V_{CM}/\Delta CME$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
- $\Delta PSRR$ is:
$$\frac{\text{Input-referred differential error}}{\Delta V_S}$$
- Sample tested.



DICE CHARACTERISTICS



DIE SIZE 0.097 × 0.063 inch, 6111 sq. mils
(2.464 × 1.600 mm, 3.94 sq. mm)

NOTE: All V+ PADS ARE INTERNALLY CONNECTED.

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V-
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUT (B)
11. V+
12. OUT (A)
13. V+
14. BALANCE (A)

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25^\circ C$ for OP-220N, OP-220G and OP-220GR devices; $T_A = 125^\circ C$ for OP-221NT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-220NT LIMIT	OP-220N LIMIT	OP-220G LIMIT	OP-220GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		350	200	500	1000	μV MAX
Input Offset Voltage Match	ΔV_{OS}		500	300	500	600	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	2.5	2	3.5	5	nA MAX
Input Bias Current	I_B	$V_{CM} = 0$	30	25	30	40	nA MAX
Input Voltage Range	IVR	$V_S = \pm 15V$	-15/13.5	-15/13.5	-15/13.5	-15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_- = 0V, V_+ = 5V, 0V \leq V_{CM} \leq 3.5V$	83	88	83	75	dB MIN
		$-15V \leq V_{CM} \leq 13.5V, V_S = \pm 15V$	88	93	88	80	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	22	12.5	40	100	$\mu V/V$ MAX
		$V_- = 0V, V_+ = 5V$ to $30V$	36	22.5	70	180	
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega, V_S = \pm 15V$ $V_O = \pm 10V$	—	1000	800	500	V/mV MIN
		$V_S = \pm 15V, R_L = 50k\Omega$ $V_O = \pm 10V$	500	—	—	—	
		$V_+ = 5V, V_- = 0V, R_L = 10k\Omega$ $V_S = \pm 15V, R_L = 25k\Omega$	—	0.7/4 ± 14	0.8/4 ± 14	0.8/3.8 ± 13.8	
Output Voltage Swing	V_O	$V_+ = 5V, V_- = 0V, R_L = 20k\Omega$ $V_S = \pm 15V, R_L = 50k\Omega$	0.9/3.8 ± 13.8	—	—	—	V MIN
Supply Current (Both Amplifiers)	I_{SV}	$V_S = \pm 2.5V$, No Load	170	125	135	170	μA MAX
		$V_S = \pm 15V$, No Load	250	190	220	300	

NOTE:

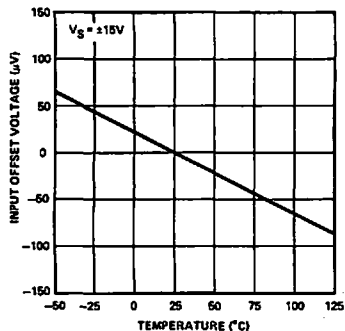
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

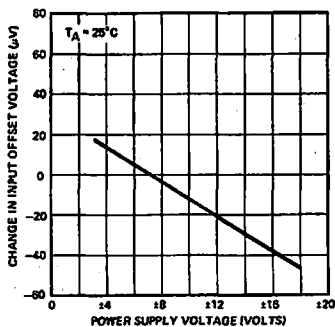
PARAMETER	SYMBOL	CONDITIONS	OP-220NT TYPICAL	OP-220N TYPICAL	OP-220G TYPICAL	OP-220GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		1.5	1.5	2	3	$\mu V/^\circ C$
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$	2000	2000	1600	800	V/mV

TYPICAL PERFORMANCE CHARACTERISTICS

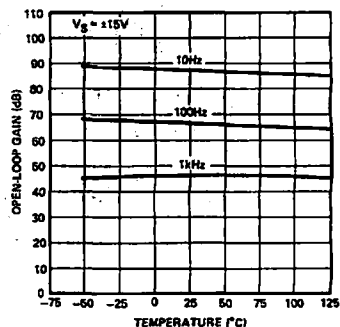
NORMALIZED OFFSET VOLTAGE vs TEMPERATURE



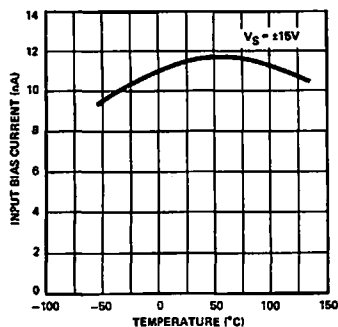
INPUT OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE



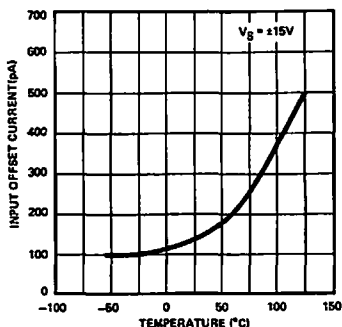
OPEN-LOOP GAIN vs TEMPERATURE



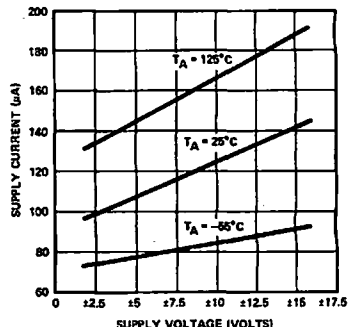
INPUT BIAS CURRENT vs TEMPERATURE



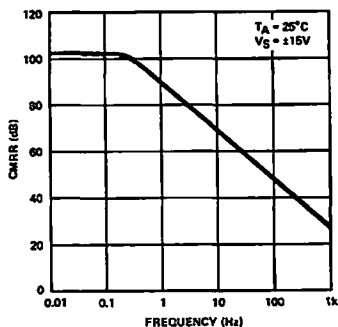
INPUT OFFSET CURRENT vs TEMPERATURE



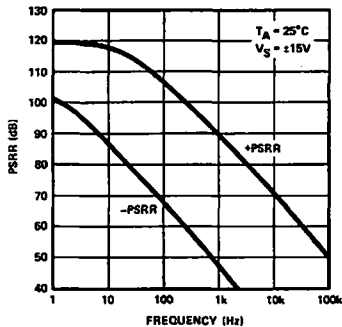
SUPPLY CURRENT vs SUPPLY VOLTAGE



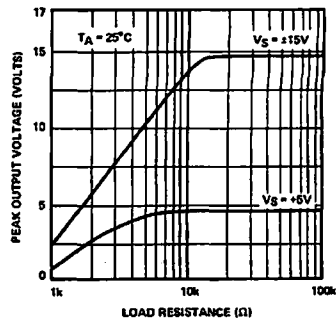
CMMR vs FREQUENCY



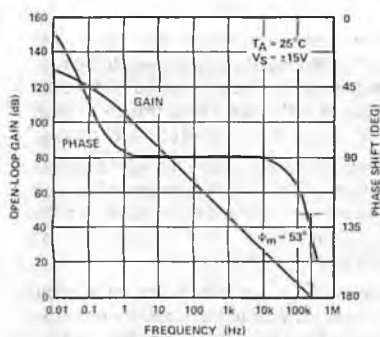
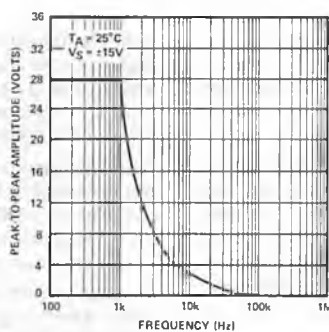
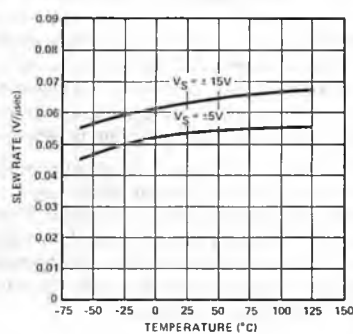
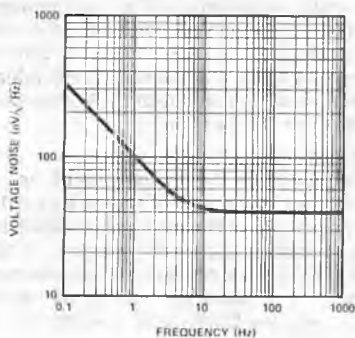
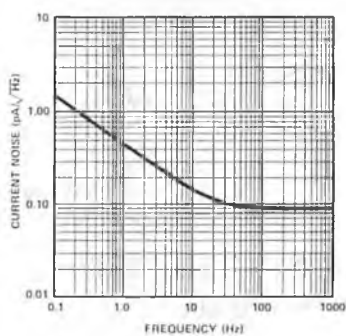
PSRR vs FREQUENCY



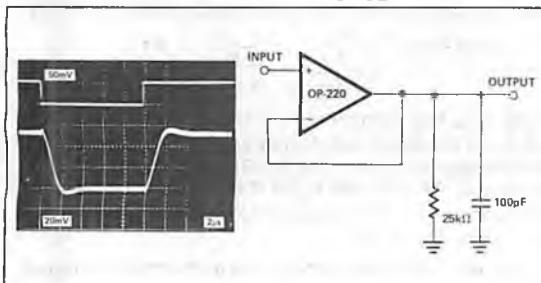
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



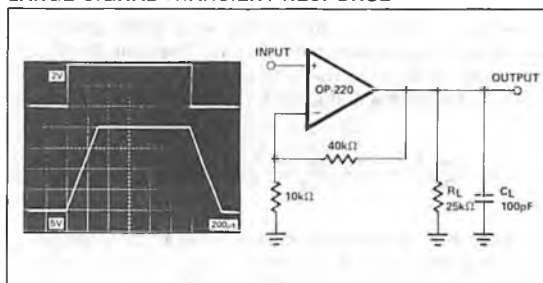
TYPICAL PERFORMANCE CHARACTERISTICS

OPEN-LOOP VOLTAGE GAIN
AND PHASE vs FREQUENCYMAXIMUM OUTPUT SWING
vs FREQUENCYSLEW RATE vs
TEMPERATUREVOLTAGE NOISE DENSITY (e_n)
vs FREQUENCYCURRENT NOISE DENSITY (i_n)
vs FREQUENCY

SMALL-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE



INSTRUMENTATION AMPLIFIER APPLICATIONS OF THE OP-220

TWO-OP-AMP CONFIGURATION

The excellent input characteristics of the OP-220 make it ideal for use in instrumentation amplifier configurations where low-level differential signals are to be amplified. The low-noise, low input offsets, low drift, and high gain combined with excellent CMRR provide the characteristics needed for high-performance instrumentation amplifiers. In addition, the power supply current drain is very low.

The circuit of Figure 1 is recommended for applications where the common-mode input range is relatively low and differential gain will be in the range of 10 to 1000. This two-op-amp instrumentation amplifier features independent adjustment of common-mode rejection and differential gain. Input impedance is very high since both inputs are applied to noninverting op amp inputs.

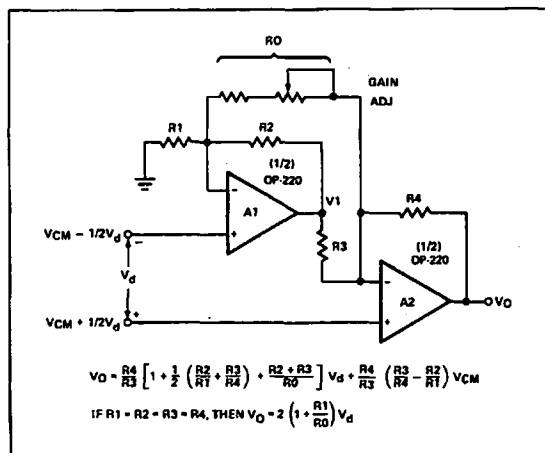


Figure 1. Two-Op-Amp Instrumentation Amplifier Configuration

The input voltages are represented as a common-mode input V_{CM} plus a differential input V_d . The ratio R_3/R_4 is made equal to the ratio R_2/R_1 to reject the common-mode input V_{CM} . The differential signal V_d is then amplified according to:

$$V_O = \frac{R_4}{R_3} \left(1 + \frac{R_3}{R_4} + \frac{R_2 + R_3}{R_O} \right) V_d, \text{ where } \frac{R_3}{R_4} = \frac{R_2}{R_1}$$

Note that gain can be independently varied by adjusting R_O . From considerations of dynamic range, resistor tempco matching, and matching of amplifier response, it is generally best to make R_1 , R_2 , R_3 , and R_4 approximately equal. Designating R_1 , R_2 , R_3 , and R_4 as R_N allows the output equation to be further simplified:

$$V_O = 2 \left(1 + \frac{R_N}{R_O} \right) V_d, \text{ where } R_N = R_1 = R_2 = R_3 = R_4$$

Dynamic range is limited by A1 as well as A2; the output of A1 is:

$$V_1 = - \left(1 + \frac{R_N}{R_O} \right) V_d + 2 V_{CM}$$

If the instrumentation amplifier were designed for a gain of 10 and maximum V_d of $\pm 1V$, then R_N/R_O would need to be four and V_O would be a maximum of $\pm 10V$. Amplifier A1 would have a maximum output of $\pm 5V$ plus $2V_{CM}$, thus a limit of $\pm 10V$ on the output of A1 would imply a limit of $\pm 2.5V$ on V_{CM} .

A nominal value of $100k\Omega$ for R_N is suitable for most applications. A range of 200Ω to $25k\Omega$ for R_O will then provide a gain range of 10 to 1000. The current through R_O is V_d/R_O , so the amplifiers must supply $\pm 10mV/200\Omega$ when the gain is at the maximum value of 1000 and V_d is at $\pm 10mV$.

Rejecting common-mode inputs is most important in accurately amplifying low-level differential signals. Two factors determine the CMR of this instrumentation amplifier configuration (assuming infinite gain):

- (1) CMRR of the op amps
- (2) Matching of the resistor network ($R_3/R_4 = R_2/R_1$)

In this instrumentation amplifier configuration, error due to CMRR effect is directly proportional to the differential CMRR of the op amps. For the OP-220A/E, this combined CMRR is a minimum of 98dB. A combined CMRR value of 100dB and common-mode input range of $\pm 2.5V$ indicates a peak input-referred error of only $\pm 25\mu V$.

Resistor matching is the other factor affecting CMRR. Defining A_d as the differential gain of the instrumentation amplifier and assuming that R_1 , R_2 , R_3 and R_4 are approximately equal (R_N will be the nominal value), then CMRR will be approximately A_d divided by $4\Delta R/R_N$. CMRR at differential gain of 100 would be 88dB with resistor matching of 0.1%. Trimming R_1 to make the ratio R_3/R_4 equal to R_2/R_1 will directly raise the CMRR until it is limited by linearity and resistor stability considerations.

The high open-loop gain of the OP-220 is very important in achieving high accuracy in the two-op-amp instrumentation amplifier configuration. Gain error can be approximated by:

$$\text{Gain Error} \sim \frac{1}{1 + \frac{A_d}{A_{O2}}} \cdot \frac{A_d}{2 A_{O1} A_{O2}} \ll 1$$

where A_d is the instrumentation amplifier differential gain and A_{O2} is the open-loop gain of op amp A2. This analysis assumes equal values of R_1 , R_2 , R_3 , and R_4 . For example, consider an OP-220 with A_{O2} of 700V/mV. If the differential gain A_d were set to 700, the gain error would be $1/1.001$ which is approximately 0.1%.

Another effect of finite op amp gain is undesired feedthrough of common-mode input. Defining A_{O1} as the open-loop gain of op amp A1, then the common-mode error (CME) at the output due to this effect will be approximately

$$\text{CME} \sim \frac{2 A_d}{1 + \frac{A_d}{A_{O1}}} \cdot \frac{1}{A_{O1}} V_{CM}$$

For $A_d/A_{01} \ll 1$, this simplifies to $(2A_d/A_{01}) \times V_{CM}$. If the op amp gain is 700V/mV, V_{CM} is 2.5V, and A_d is set to 700, then the error at the output due to this effect will be approximately 5mV.

The OP-220 offers a unique combination of excellent dc performance, wide input range, and low supply current drain that is particularly attractive for instrumentation amplifier design.

THREE-OP-AMP CONFIGURATION

A three-op-amp instrumentation amplifier configuration using the OP-220 and OP-22 is recommended for applications requiring high accuracy over a wide gain range. This

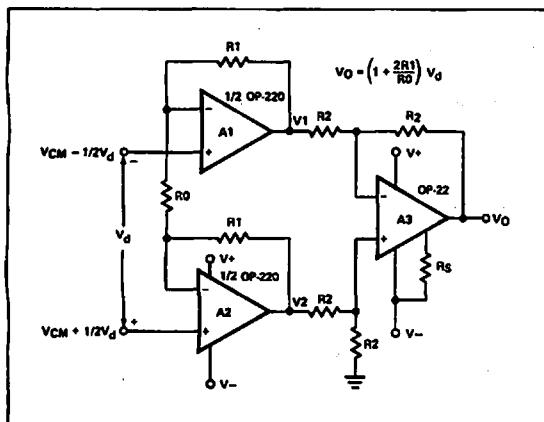


Figure 2. Three-Op-Amp Instrumentation Amplifier Using OP-220 and OP-22

circuit provides excellent CMR over a wide input range. As with the two-op-amp instrumentation amplifier circuits, tight matching of the two op amps provides a real boost in performance. The OP-22 is a micropower op-amp featuring programmable supply current.

A simplified schematic is shown in Figure 2. The input stage (A1 and A2) serves to amplify the differential input V_d without amplifying the common-mode voltage V_{CM} . The output stage then rejects the common-mode input. With ideal op-amps and no resistor matching errors, the outputs of each amplifier will be:

$$V_1 = -\left(1 + \frac{2R_1}{R_O}\right) \frac{V_d}{2} + V_{CM}$$

$$V_2 = \left(1 + \frac{2R_1}{R_O}\right) \frac{V_d}{2} + V_{CM}$$

$$V_O = V_2 - V_1 = \left(1 + \frac{2R_1}{R_O}\right) V_d$$

$$V_O = A_d V_d$$

The differential gain A_d is $1 + 2R_1/R_O$ and the common-mode input V_{CM} is rejected.

This three-op-amp instrumentation amplifier configuration using an OP-220 at the input and an OP-22 at the output provides excellent performance over a wide gain range with very low power consumption. A gain range of 1 to 2000 is practical and CMR of over 120dB is readily achievable.



OP-221

DUAL LOW-POWER OPERATIONAL AMPLIFIER (SINGLE OR DUAL SUPPLY)

Precision Monolithics Inc.

FEATURES

- Excellent TCV_{OS} Match $2\mu V/^{\circ}C$ Max
- Low Input Offset Voltage $150\mu V$ Max
- Low Supply Current $550\mu A$ Max
- Single Supply Operation $+5V$ to $+30V$
- Low Input Offset Voltage Drift $0.75\mu V/^{\circ}C$
- High Open-Loop Gain $1500V/mV$ Min
- High PSRR $3\mu V/V$
- Wide Common-Mode Voltage Range $V-$ to within $1.5V$ of $V+$
- Pin Compatible with 1458, LM158, LM2904

ORDERING INFORMATION†

$T_A = 25^{\circ}C$ V_{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	HERMETIC DIP 8-PIN	
150	—	OP221AZ	MIL
150	—	OP221EZ	IND
300	OP221BJ	—	MIL
500	OP221CJ	—	MIL
500	OP221GJ	OP221GZ	IND

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

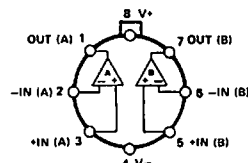
The OP-221 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The

wide supply voltage range, wide input voltage range, and low supply current drain of the OP-221 make it well-suited for operation from batteries or unregulated power supplies.

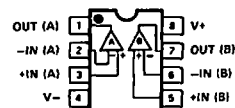
The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection.

PIN CONNECTIONS

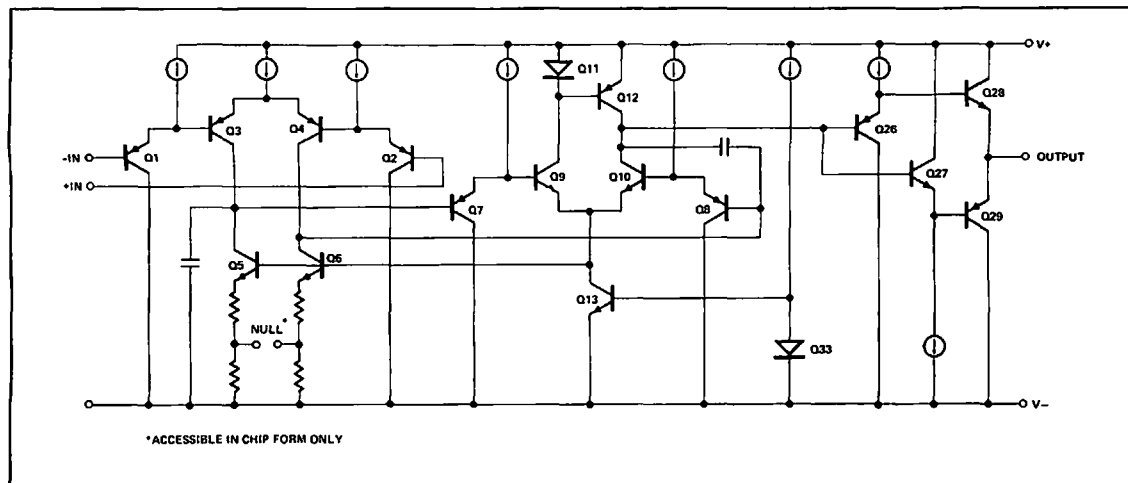


TO-99 (J-Suffix)



8-PIN HERMETIC DIP
(Z-Suffix)

SIMPLIFIED SCHEMATIC (Each Amplifier)



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	30V or Supply Voltage
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP-221A, B, C	-55°C to +125°C
OP-221E, G	-25°C to +85°C

Lead Temperature (Soldering, 60 sec.)	300°C
DICE Junction Temperature (T_j)	-65°C to +150°C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.
- Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E			OP-221B			OP-221C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	75	150	—	150	300	—	250	500	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	0.5	3	—	1	5	—	1.5	7	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	50	80	—	60	100	—	70	120	nA
Input Voltage Range	IVR	$V^+ = 5V, V^- = 0V$ $V_S = \pm 15V$ (Note 2)	0/3.5 -15/13.5	—	—	0/3.5 -15/13.5	—	—	0/3.5 -15/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V^+ = 5V, V^- = 0V$ $0V \leq V_{CM} \leq 3.5V$ $V_S = \pm 15V$	90	100	—	85	90	—	75	85	—	dB
		$-15V \leq V_{CM} \leq 13.5V$	95	100	—	90	95	—	80	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$	—	3	10	—	10	32	—	32	100	$\mu V/V$
		$V^- = 0V, V^+ = 5V$ to 30V	—	6	18	—	18	57	—	57	180	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, R_L = 10k\Omega$ $V_O = \pm 10V$	1500	—	—	1000	—	—	800	—	—	V/mV
Output Voltage Swing	V_O	$V^+ = 5V, V^- = 0V,$ $R_L = 10k\Omega$	0.7/4.1	—	—	0.7/4.1	—	—	0.8/4	—	—	V
		$V_S = \pm 15V, R_L = 10k\Omega$	± 13.8	—	—	± 13.8	—	—	± 13.5	—	—	
Slew Rate	SR	$R_L = 10k\Omega$, (Note 1)	0.2	0.3	—	0.2	0.3	—	0.2	0.3	—	V/ μs
Bandwidth	BW		—	600	—	—	600	—	—	600	—	kHz
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	450	550	—	500	600	—	550	650	μA
		$V_S = \pm 15V$, No Load	—	600	800	—	800	850	—	850	900	

NOTES:

- Sample tested.
- Guaranteed by CMRR test limits.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-221A, B and C; $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-221E and G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E			OP-221B			OP-221C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		—	0.75	1.5	—	1.2	2	—	2	3	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}		—	150	300	—	250	450	—	400	700	μV
Input Offset Current	I_{OS}	$V_{CM} = 0$	—	1	5	—	1.5	7	—	2	10	nA
Input Bias Current	I_B	$V_{CM} = 0$	—	55	100	—	65	120	—	80	140	nA
Input Voltage Range	IVR	$V^+ = 5V, V^- = 0V$ $V_S = \pm 15V$ (Note 2)	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	0/3.2 -15/13.2	—	—	V
Common-Mode Rejection Ratio	CMRR	$V^+ = 5V, V^- = 0V$ $0V \leq V_{CM} \leq 3.2V$ $V_S = \pm 15V$	85	90	—	80	85	—	70	80	—	dB
		$-15V \leq V_{CM} \leq 13.2V$	90	95	—	85	90	—	75	85	—	



ELECTRICAL CHARACTERISTICS at $V_S = \pm 2.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-221A, B and C; $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-221E and G, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E			OP-221B			OP-221C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ $V_- = 0V$, $V_+ = 5V$ to $30V$	—	6	18	—	18	57	—	57	180	$\mu V/V$
			—	10	32	—	32	100	—	100	320	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 10k\Omega$ $V_O = \pm 10V$	1000	—	—	800	—	—	600	—	—	V/mV
Output Voltage Swing	V_O	$V_+ = 5V$, $V_- = 0V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 10k\Omega$	0.8/3.8	—	—	0.8/3.8	—	—	0.9/3.7	—	—	V
			± 13.5	± 14	—	± 13.5	± 14	—	± 13.2	—	—	
Supply Current (Both Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	—	500	650	—	550	700	—	600	750	μA
			—	700	900	—	900	950	—	950	1000	

NOTES:

1. Sample tested.
2. Guaranteed by CMRR test limits.

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-221A/E			OP-221B			OP-221C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	50	200	—	150	400	—	250	600	μV
Average Noninverting Bias Current	I_{B+}		—	—	80	—	—	100	—	—	120	nA
Noninverting Input Offset Current	I_{OS+}		—	2	5	—	2	5	—	4	10	nA
Common-Mode Rejection Ratio Match (Note 1)	$\Delta CMRR$	$V_{CM} = -15V$ to $+13.5V$	92	—	—	87	—	—	72	—	—	dB
Power Supply Rejection Ratio Match (Note 2)	$\Delta PSRR$	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	14	—	—	44	—	—	140	$\mu V/V$

MATCHING CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-221A, B and C; $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-221E and G, unless otherwise noted. Grades E and G are sample tested.

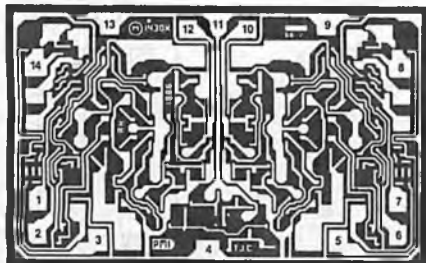
PARAMETER	SYMBOL	CONDITIONS	OP-221A/E			OP-221B			OP-221C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	100	400	—	250	600	—	400	800	μV
Average Noninverting Bias Current	I_{B+}	$V_{CM} = 0$	—	—	100	—	—	120	—	—	140	nA
Input Offset Voltage Tracking	$TC\Delta V_{OS}$		—	1	2	—	1	3	—	3	5	$\mu V/^\circ C$
Noninverting Input Offset Current	I_{OS+}	$V_{CM} = 0$	—	3	7	—	3	7	—	6	12	nA
Common-Mode Rejection Ratio Match (Note 1)	$\Delta CMRR$	$V_{CM} = -15V$ to $+13.2V$	87	90	—	82	85	—	72	80	—	dB
Power Supply Rejection Ratio Match (Note 2)	$\Delta PSRR$		—	—	26	—	—	78	—	—	250	$\mu V/V$

NOTES:

1. $\Delta CMRR$ is $20 \log_{10} V_{CM}/\Delta CME$, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
2. $\Delta PSRR$ is: $\frac{\text{Input-Referred Differential Error}}{\Delta V_S}$



DICE CHARACTERISTICS



DIE SIZE 0.097 × 0.063 inch, 6111 sq. mils
(2.464 × 1.600 mm, 3.94 sq. mm)

NOTE: All V+ PADS ARE INTERNALLY CONNECTED.

1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V-
5. BALANCE (B)
6. NONINVERTING INPUT (B)
7. INVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUT (B)
11. V+
12. OUT (A)
13. V+
14. BALANCE (A)

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

5

WAFER TEST LIMITS at $V_S = \pm 2.5V$ to $\pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

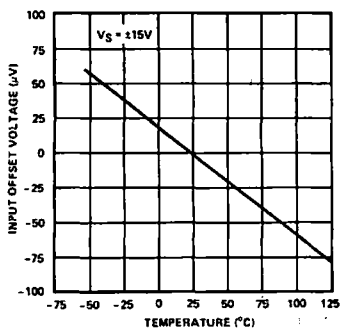
PARAMETER	SYMBOL	CONDITIONS	OP-221N LIMIT	OP-221G LIMIT	OP-221GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		200	350	500	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0$	3.5	5.5	7	nA MAX
Input Bias Current	I_B	$V_{CM} = 0$	85	105	120	nA MAX
Input Voltage Range	IVR	$V_+ = 5V$, $V_- = 0V$ $V_S = \pm 15V$	0/3.5 -15/13.5	0/3.5 -15/13.5	0/3.5 -15/13.5	V MIN/MAX V MIN
Common-Mode Rejection Ratio	CMRR	$V_- = 0V$, $V_+ = 5V$, $0V \leq V_{CM} \leq 3.5V$ $V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.5V$	88 93	83 88	75 80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ $V_- = 0V$, $V_+ = 5V$ to $30V$	12.5 22.5	40 70	100 180	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $R_L = 10k\Omega$	1500	1000	800	V/mV MIN
Output Voltage Swing	V_O	$V_+ = 5V$, $V_- = 0V$, $R_L = 10k\Omega$ $V_S = \pm 15V$, $R_L = 10k\Omega$	0.7/4.1 ± 13.8	0.7/4.1 ± 13.8	0.8/4 ± 13.5	V MIN/MAX V MIN
Supply Current (Both Amplifiers)	I_{SV}	$V_S = \pm 2.5V$, No Load $V_S = \pm 15V$, No Load	560 810	610 860	650 900	μA MAX

NOTE:

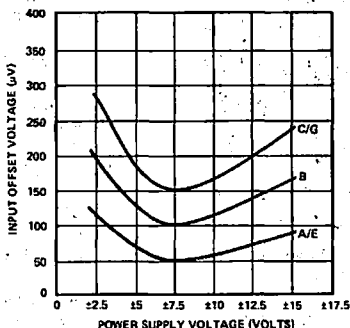
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

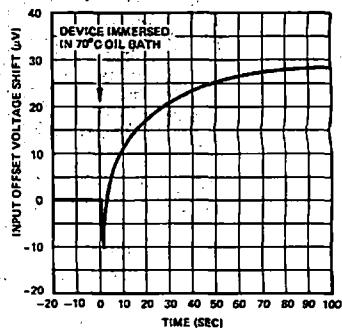
NORMALIZED INPUT OFFSET VOLTAGE vs TEMPERATURE



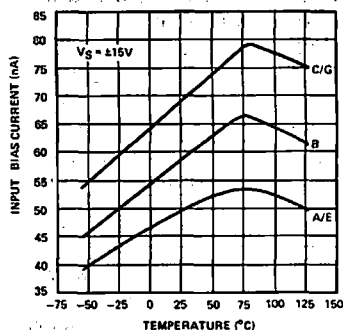
INPUT OFFSET VOLTAGE vs SUPPLY VOLTAGE



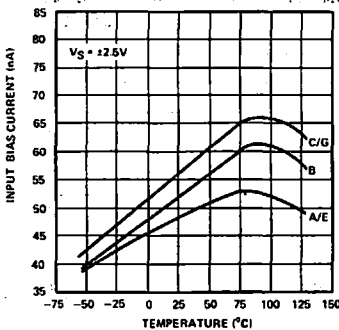
OFFSET VOLTAGE SHIFT DUE TO THERMAL SHOCK



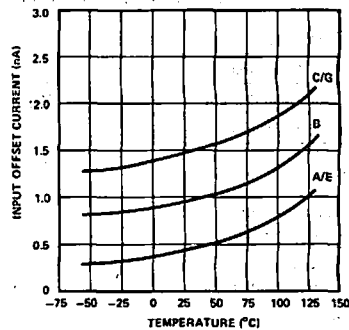
INPUT BIAS CURRENT vs TEMPERATURE



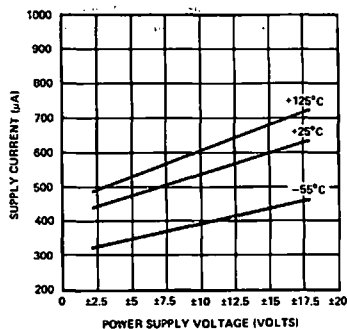
INPUT BIAS CURRENT vs TEMPERATURE



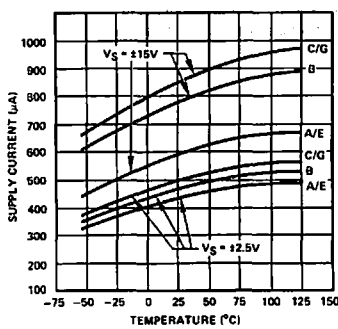
INPUT OFFSET CURRENT vs TEMPERATURE



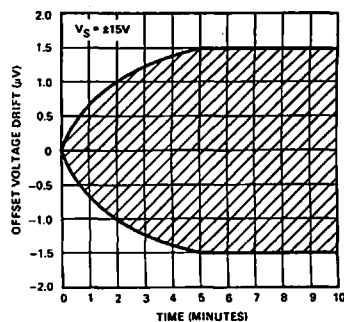
SUPPLY CURRENT vs SUPPLY VOLTAGE FOR OP-221A/E



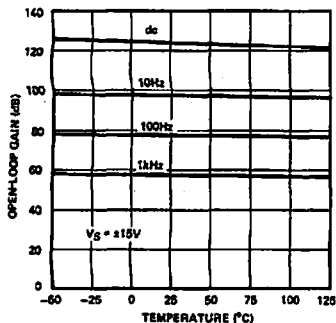
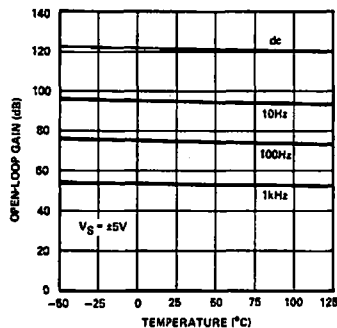
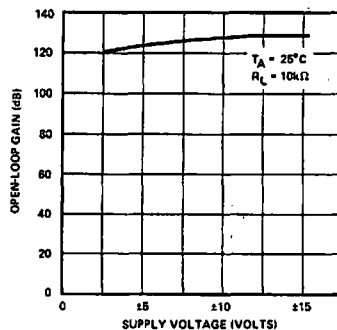
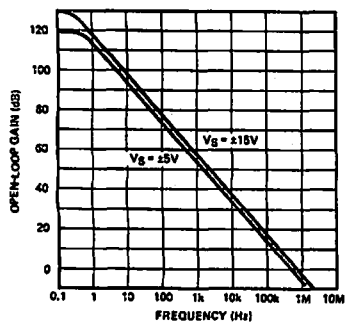
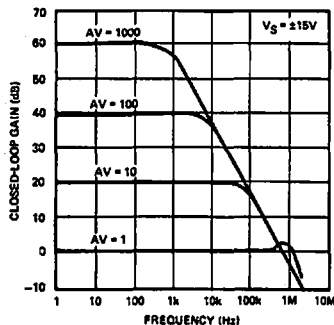
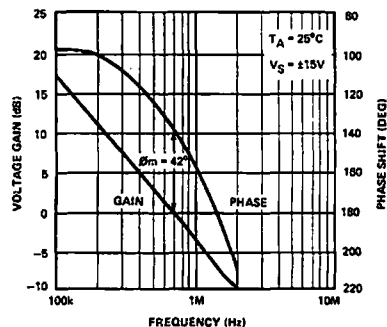
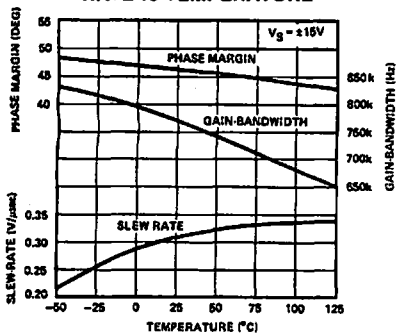
SUPPLY CURRENT vs TEMPERATURE AT V_S = ±15V AND ±2.5V



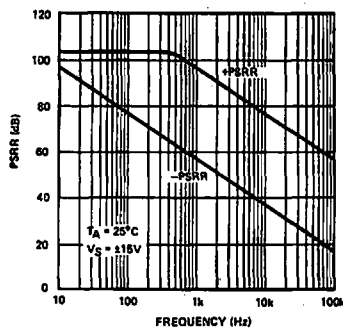
INITIAL OFFSET VOLTAGE DRIFT vs TIME



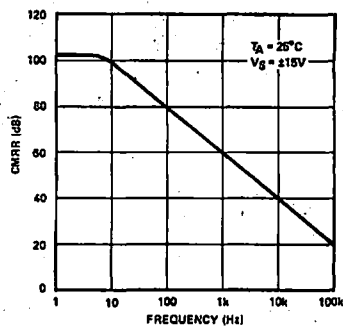
TYPICAL PERFORMANCE CHARACTERISTICS

 OPEN-LOOP GAIN AT $\pm 15V$
vs TEMPERATURE

 OPEN-LOOP GAIN AT $\pm 5V$
vs TEMPERATURE

 OPEN-LOOP GAIN
vs SUPPLY VOLTAGE

 OPEN-LOOP GAIN
vs FREQUENCY

 CLOSED-LOOP GAIN
vs FREQUENCY

 GAIN AND PHASE SHIFT
vs FREQUENCY

 PHASE MARGIN, GAIN-BANDWIDTH, AND SLEW RATE
vs TEMPERATURE


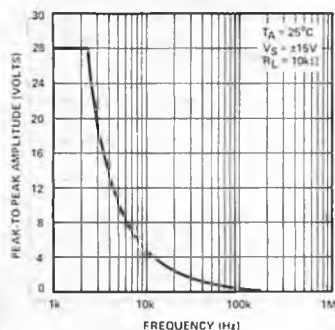
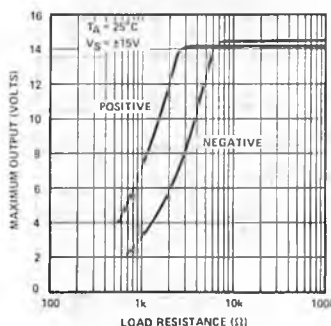
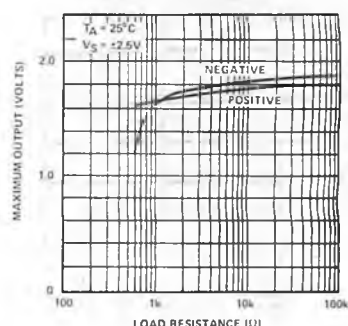
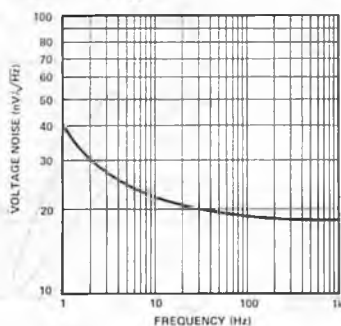
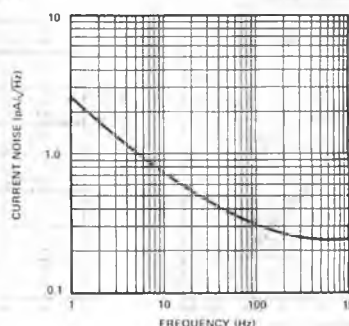
PSRR vs FREQUENCY



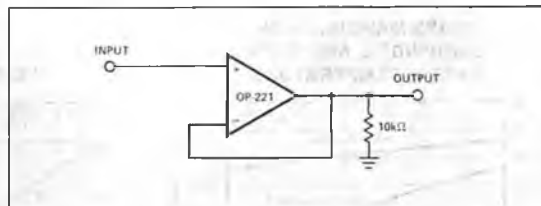
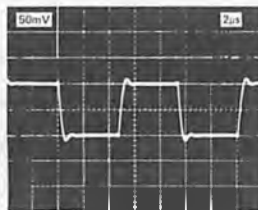
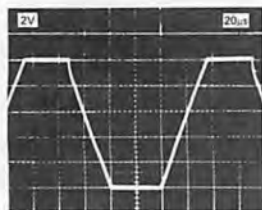
CMRR vs FREQUENCY



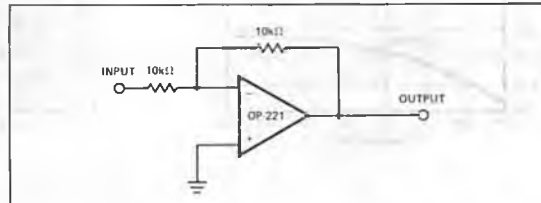
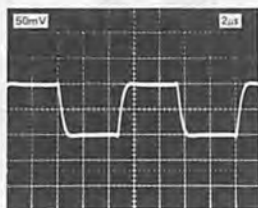
TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM OUTPUT SWING
vs FREQUENCY

MAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCE

MAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCE

VOLTAGE NOISE DENSITY (e_n)
vs FREQUENCY

CURRENT NOISE DENSITY (i_n)
vs FREQUENCY


NONINVERTING STEP RESPONSE



INVERTING STEP RESPONSE



SPECIAL NOTES ON THE APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

ADVANTAGES OF DUAL MONOLITHIC OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide the engineer with a powerful tool for designing instrumentation amplifiers and many other differential-input circuits. These designs are based on the principle that careful matching between two operational amplifiers can minimize the effect of DC errors in the individual amplifiers.

Reference to the circuit shown in Figure 1, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical. If the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifier's output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the *difference* (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are high and tightly matched, an important feature not practical with single operational amplifier circuits.

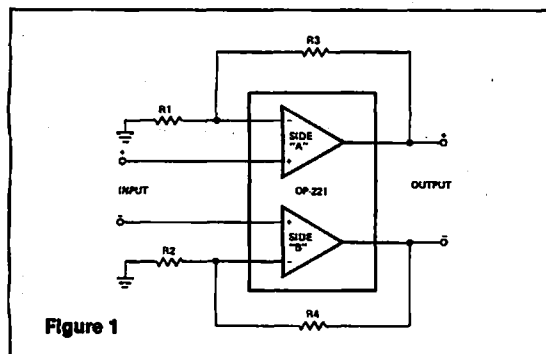


Figure 1

INSTRUMENTATION AMPLIFIER APPLICATIONS

Two-Op-Amp Configuration

The two-op-amp circuit (Figure 2), is recommended where the common-mode input voltage range is relatively limited; the common-mode and differential voltage both appear at V1.

The high open-loop gain of the OP-221 is very important in achieving good CMRR in this configuration. Finite open-loop gain of A1 (A_{01}) causes undesired feedthrough of the common-mode input. For $A_d/A_{01} \ll 1$, the common-mode error (CME) at the output due to this effect is approximately $(2 A_d/A_{01}) \times V_{CM}$. This circuit features independent adjustment of CMRR and differential gain.

Three-Op-Amp Configuration

The three-op-amp circuit (Figure 3), has increased common-mode voltage range because the common-mode voltage is not amplified as it is in Figure 2. The CMR of this amplifier is directly proportional to the match of the CMR of the input op amps. CMRR can be raised even further by trimming the output stage resistors.

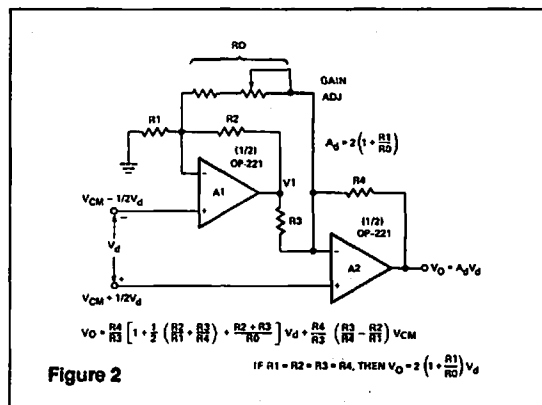


Figure 2

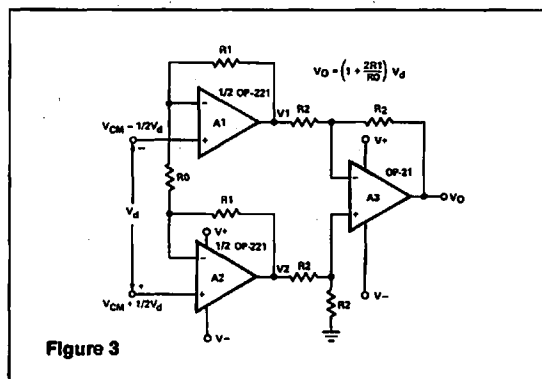


Figure 3



OP-227

DUAL LOW-NOISE LOW-OFFSET INSTRUMENTATION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Excellent Individual Amplifier Parameters
- Low V_{OS} 80 μ V Max
- Offset Voltage Match 80 μ V Max
- Offset Voltage Match vs Temperature 1 μ V/ $^{\circ}$ C Max
- Stable V_{OS} vs Time 1 μ V/Mo Max
- Low Voltage Noise 3.9nV/ $\sqrt{\text{Hz}}$ Max
- Fast 2.8V/ μ s Typ
- High Gain 1.8 Million Typ
- High Channel Separation 154dB Typ

ORDERING INFORMATION†

$T_A = 25^{\circ}\text{C}$ V_{OS} MAX (μ V)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
80	OP227AY*	MIL
80	OP227EY	IND
120	OP227BY/883	MIL
120	OP227FY	IND
180	OP227GY	IND

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The OP-227 is the first dual amplifier to offer a combination of low offset, low noise, high speed and guaranteed amplifier matching characteristics in one device. The OP-227 with a V_{OS} match of 25 μ V typical, a TCV_{OS} match of 0.3 μ V/ $^{\circ}$ C typical, and a 1/f corner of only 2.7Hz is an excellent choice for precision low noise designs. These D.C. characteristics, coupled with a slew rate of 2.8V/ μ s typical and a small-signal bandwidth of 8MHz typical, allow the designer to achieve AC performance previously unattainable with op-amp-based instrumentation designs.

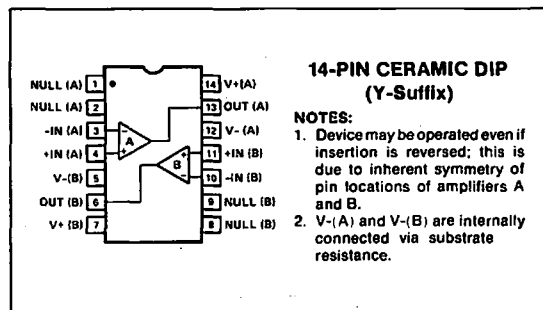
When used in a three-op-amp instrumentation amplifier configuration, the OP-227 can achieve a CMRR in excess of 100dB at 10kHz. In addition, this device has an open-loop gain of 1.5M typical with a 1k Ω load. The OP-227 also features an I_B of ± 10 nA typical, an I_{OS} of 7nA typical, and guaranteed matching of input currents between amplifiers. These outstanding input current specifications are realized through the use of a unique input current-cancellation-circuit which typically holds I_B and I_{OS} to ± 20 nA and 15nA respectively over the full military temperature range.

Other sources of input-referred errors, such as PSRR and CMRR, are reduced by factors in excess of 120dB for the individual amplifiers. D.C. stability is assured by a long-term drift specification of 1.0 μ V/month.

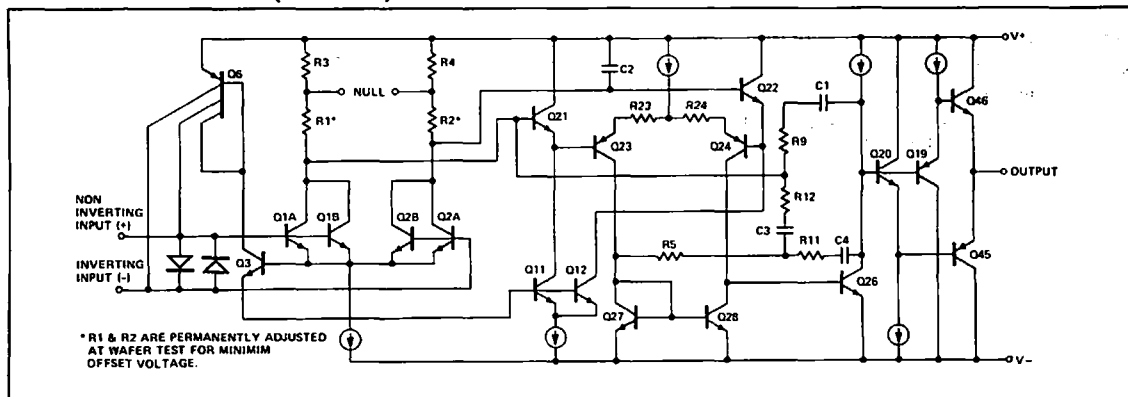
Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias current, CMRR, and power supply rejection ratio. This unique dual amplifier allows the elimination of external components for offset nulling and frequency compensation.

The OP-227 is pin compatible with the OP-10 and OP-207.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/2 OP-227)





ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Input Voltage (Note 3)	±22V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage (Note 2)	±0.7V
Differential Input Current (Note 2)	±25mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature	
OP-227A	-55°C to +125°C
OP-227E, OP-227F, OP-227G	-25°C to +85°C
Lead Temperature Range (Soldering, 60 sec)	300°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin (Y)	105°C	11.3mW/°C

2. The OP-227's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

3. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

INDIVIDUAL AMPLIFIER CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A/E			OP-227F			OP-227G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	20	80	—	40	120	—	60	180	μV
Long-Term V_{OS} Stability	$V_{OS}/Time$	(Notes 2, 4)	—	0.2	1.0	—	0.3	1.5	—	0.4	2.0	$\mu V/Mo$
Input Offset Current	I_{OS}		—	7	35	—	9	50	—	12	75	nA
Input Bias Current	I_B		—	±10	±40	—	±12	±55	—	±15	±80	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Notes 3, 5)	—	0.08	0.20	—	0.08	0.20	—	0.09	0.28	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 3)	—	3.5	6.0	—	3.5	6.0	—	3.8	9.0	$nV/\sqrt{Hz}$
		$f_O = 30Hz$ (Note 3)	—	3.1	4.7	—	3.1	4.7	—	3.3	5.9	
		$f_O = 1000Hz$ (Note 3)	—	3.0	3.9	—	3.0	3.9	—	3.2	4.6	
Input Noise Current Density	i_n	$f_O = 10Hz$ (Notes 3, 6)	—	1.7	4.5	—	1.7	4.5	—	1.7	—	$pA/\sqrt{Hz}$
		$f_O = 30Hz$ (Notes 3, 6)	—	1.0	2.5	—	1.0	2.5	—	1.0	—	
		$f_O = 1000Hz$ (Notes 3, 6)	—	0.4	0.7	—	0.4	0.7	—	0.4	0.7	
Input Resistance — Differential-Mode	R_{IN}	(Note 7)	1.3	6	—	0.94	5	—	0.7	4	—	M Ω
Input Resistance — Common-Mode	R_{INCM}		—	3	—	—	2.5	—	—	2	—	G Ω
Input Voltage Range	IVR		±11.0	±12.3	—	±11.0	±12.3	—	±11.0	±12.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$	114	126	—	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4V$ to $\pm 18V$	—	1	10	—	1	10	—	2	20	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	1000	1800	—	1000	1800	—	700	1500	—	V/mV
		$R_L \geq 600\Omega$, $V_O = \pm 10V$	800	1500	—	800	1500	—	600	1500	—	
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	±12.0	±13.8	—	±12.0	±13.8	—	±11.5	±13.5	—	V
		$R_L \geq 600\Omega$	±10.0	±11.5	—	±10.0	±11.5	—	±10.0	±11.5	—	
Slew Rate	SR	$R_L \geq 2k\Omega$ (Note 4)	1.7	2.8	—	1.7	2.8	—	1.7	2.8	—	V/ μs
Gain Bandwidth Prod.	GBW	(Note 4)	5	8	—	5	8	—	5	8	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	70	—	—	70	—	—	70	—	Ω
Power Consumption	P_d	Each Amplifier	—	90	140	—	90	140	—	100	170	mW
Offset Adjustment Range		$R_P = 10k\Omega$	—	±4	—	—	±4	—	—	±4	—	mV

NOTES:

1. Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grade specifications are guaranteed fully warmed up.

2. Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5 μV — refer to typical performance curve.

3. Sample tested.

4. Parameter is guaranteed by design.

5. See test circuit and frequency response curve for 0.1Hz to 10Hz tester.

6. See test circuit for current noise measurement.

7. Guaranteed by input bias current.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** for $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	60	180	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Notes 2, 3)	—	0.3	1.0	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	15	50	nA
Input Bias Current	I_B		—	± 20	± 60	nA
Input Voltage Range	IVR		± 10.0	± 11.5	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	108	122	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	600	1200	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.5	± 13.5	—	V

INDIVIDUAL AMPLIFIER CHARACTERISTICS for $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227E			OP-227F			OP-227G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	40	140	—	60	200	—	85	280	μV
Average Input Offset Drift	TCV_{OS} TCV_{OSn}	(Note 2)	—	0.5	1.0	—	0.4	1.5	—	0.5	1.8	$\mu V/^\circ C$
Input Offset Current	I_{OS}		—	10	50	—	14	85	—	20	135	nA
Input Bias Current	I_B		—	± 14	± 60	—	± 18	± 95	—	± 25	± 150	nA
Input Voltage Range	IVR		± 10.0	± 11.8	—	± 10.0	± 11.8	—	± 10.0	± 11.8	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10V$	110	124	—	102	121	—	96	118	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	2	32	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	750	1500	—	700	1300	—	450	1000	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 11.7	± 13.6	—	± 11.4	± 13.5	—	± 11.0	± 13.3	—	V

MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A/E			OP-227F			OP-227G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	25	80	—	35	150	—	55	300	μV
Average Noninverting Bias Current	I_{B+}	$I_{B+} = \frac{I_{B+A} + I_{B+B}}{2}$	—	± 10	± 40	—	± 12	± 55	—	± 15	± 90	nA
Noninverting Offset Current	I_{OS+}	$I_{OS+} = I_{B+A} - I_{B+B}$	—	± 12	± 60	—	± 15	± 80	—	± 20	± 130	nA
Inverting Offset Current	I_{OS-}	$I_{OS-} = I_{B-A} - I_{B-B}$	—	± 12	± 60	—	± 15	± 80	—	± 20	± 130	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 11V$	110	123	—	103	120	—	97	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 4V$ to $\pm 18V$	—	2	10	—	2	10	—	2	20	$\mu V/V$
Channel Separation	CS	(Note 1)	126	154	—	126	154	—	126	154	—	dB

NOTES:

- Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
- The TCV_{OS} performance is within the specifications unnullled or when nulled with $R_P = 8k\Omega$ to $20k\Omega$, optimum performance is obtained with $R_P = 8k\Omega$.
- Sample tested.

**MATCHING CHARACTERISTICS** for $V_S = \pm 15V$, $T_A = -55^\circ C$ to $+125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-227A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	55	180	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	Nullled or Unnullled (Note 2)	—	0.3	1.0	$\mu V/^\circ C$
Average Noninverting Bias Current	I_{B^+}	$I_{B^+} = \frac{I_{B^+A} + I_{B^+B}}{2}$	—	± 20	± 60	nA
Average Drift of Non-Inverting Bias Current	TCI_{B^+}		—	100	—	$pA/^\circ C$
Noninverting Offset Current	I_{OS^+}	$I_{OS^+} = I_{B^+A} - I_{B^+B}$	—	± 25	± 80	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS^+}		—	130	—	$pA/^\circ C$
Inverting Offset Current	I_{OS^-}	$I_{OS^-} = I_{B^-A} - I_{B^-B}$	—	± 25	± 80	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$	105	118	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	16	$\mu V/V$

MATCHING CHARACTERISTICS for $V_S = \pm 15V$, $T_A = -25^\circ C$ to $+85^\circ C$, unless otherwise noted.

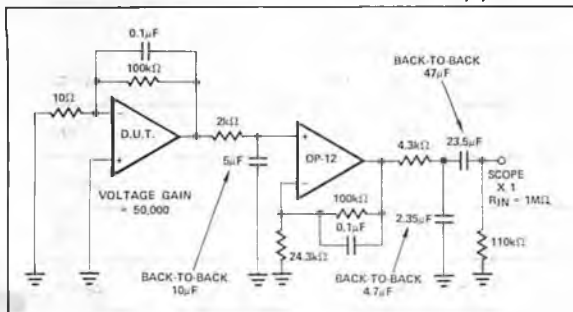
PARAMETER	SYMBOL	CONDITIONS	OP-227E			OP-227F			OP-227G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	ΔV_{OS}		—	40	140	—	65	210	—	90	400	μV
Input Offset Voltage Tracking	$TC\Delta V_{OS}$	Nullled or Unnullled (Note 1)	—	0.3	1.0	—	0.4	1.5	—	0.5	1.8	$\mu V/^\circ C$
Average Noninverting Bias Current	I_{B^+}	$I_{B^+} = \frac{I_{B^+A} + I_{B^+B}}{2}$	—	± 14	± 60	—	± 18	± 85	—	± 25	± 170	nA
Average Drift of Non-Inverting Bias Current	TCI_{B^+}		—	80	—	—	140	—	—	180	—	$pA/^\circ C$
Noninverting Offset Current	I_{OS^+}	$I_{OS^+} = I_{B^+A} - I_{B^+B}$	—	± 20	± 80	—	± 25	± 140	—	± 35	± 250	nA
Average Drift of Non-Inverting Offset Current	TCI_{OS^+}		—	130	—	—	200	—	—	250	—	$pA/^\circ C$
Inverting Offset Current	I_{OS^-}	$I_{OS^-} = I_{B^-A} - I_{B^-B}$	—	± 20	± 80	—	± 25	± 140	—	± 35	± 250	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 10V$	106	120	—	98	117	—	90	112	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 4.5V$ to $\pm 18V$	—	2	15	—	2	16	—	3	32	$\mu V/V$

NOTES:

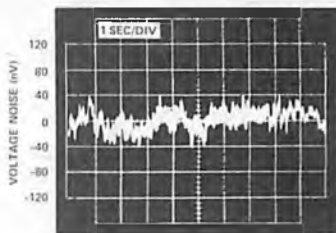
1. Sample tested.
2. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE TEST CIRCUIT (0.1Hz-TO-10Hz_{p-p})



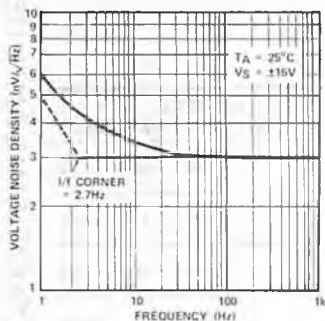
LOW-FREQUENCY NOISE



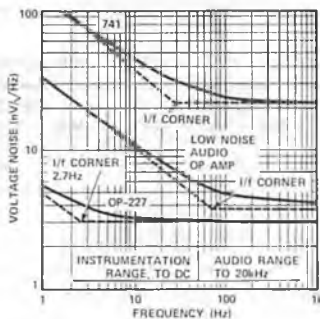
0.1Hz TO 10Hz PEAK-TO-PEAK NOISE

NOTE: OBSERVATION TIME MUST BE LIMITED TO 10 SECONDS TO ENSURE 0.1Hz CUTOFF.

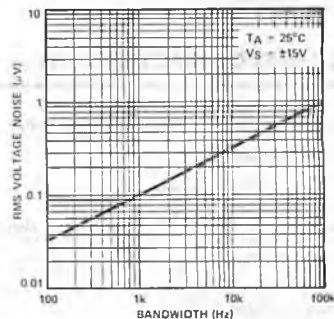
VOLTAGE NOISE DENSITY vs FREQUENCY



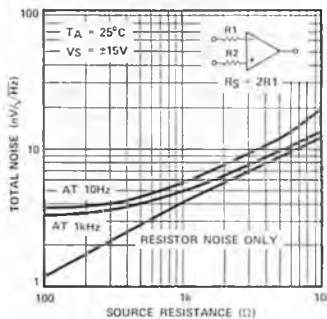
COMPARISON OF OP-AMP VOLTAGE NOISE SPECTRA



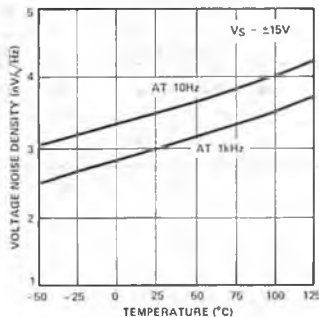
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1Hz TO FREQUENCY INDICATED)



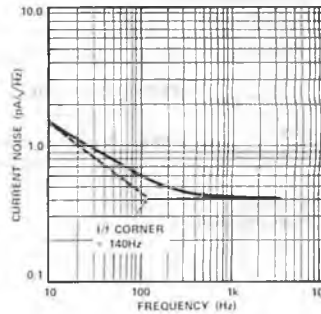
TOTAL NOISE vs SOURCE RESISTANCE



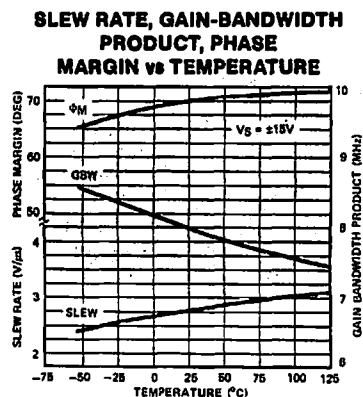
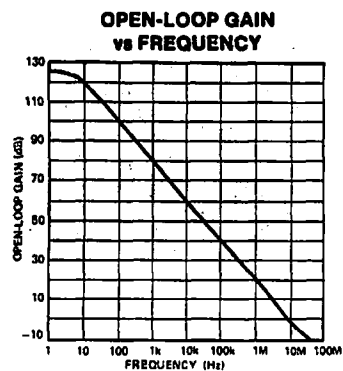
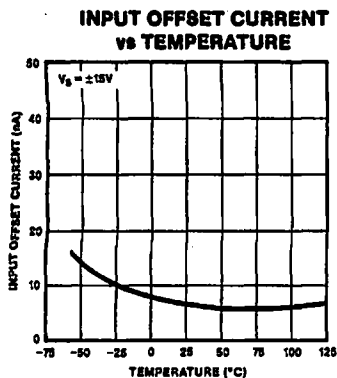
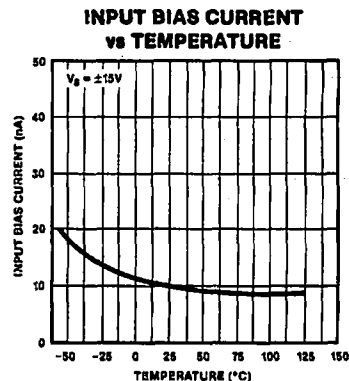
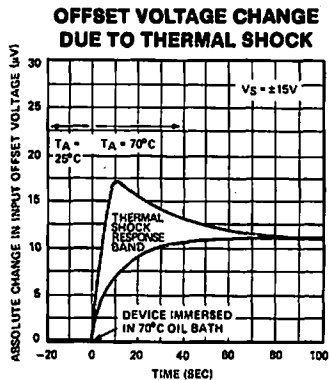
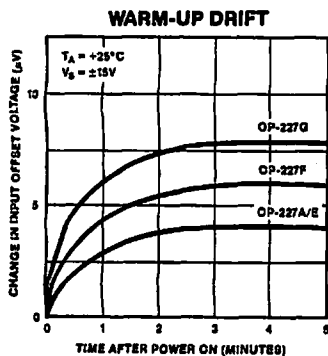
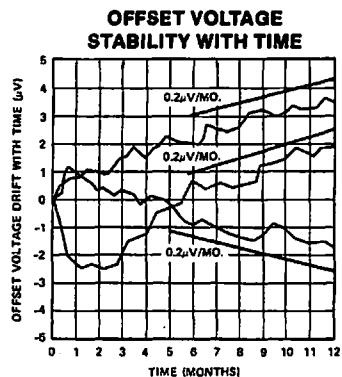
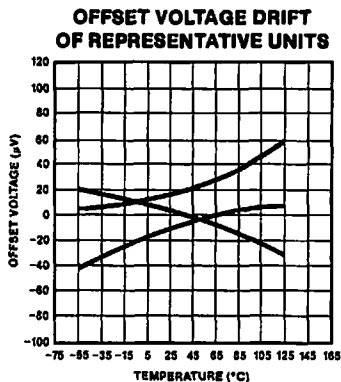
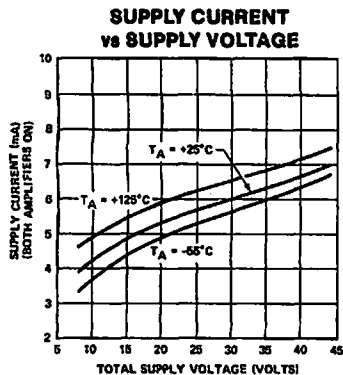
VOLTAGE NOISE DENSITY vs TEMPERATURE



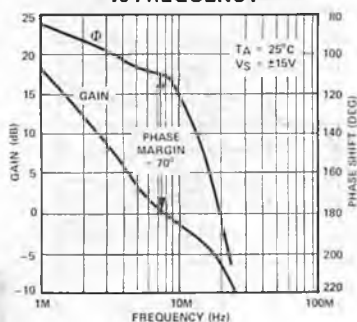
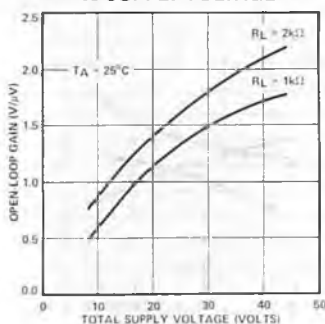
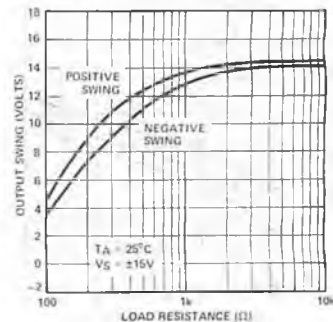
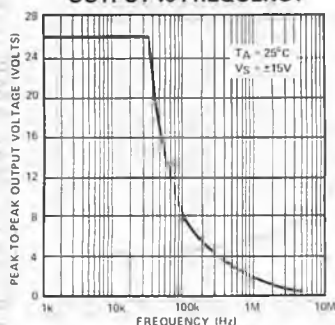
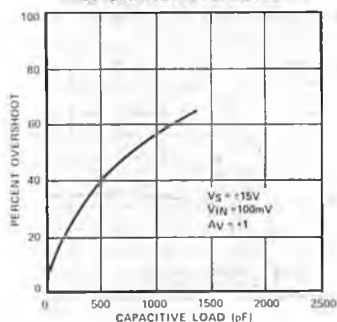
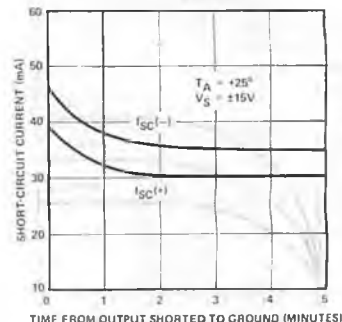
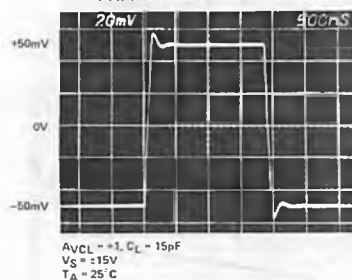
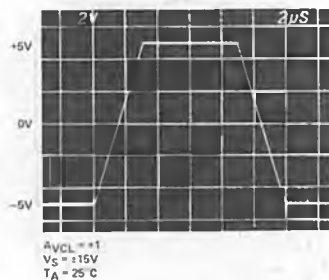
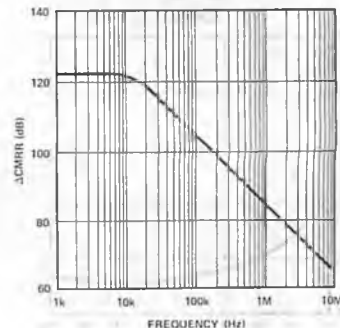
CURRENT NOISE DENSITY vs FREQUENCY



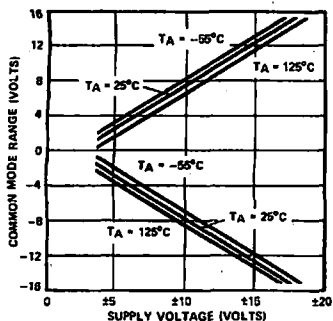
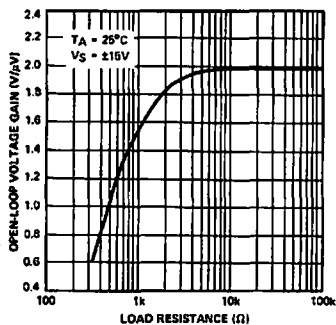
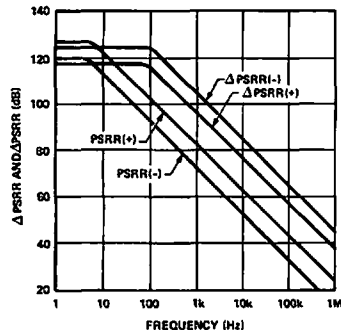
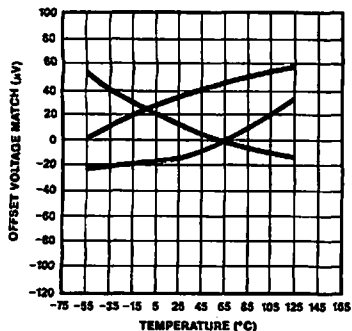
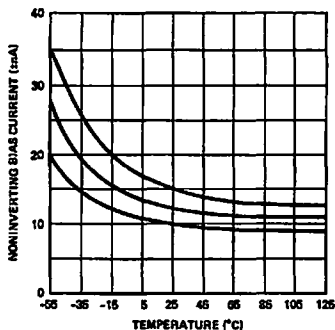
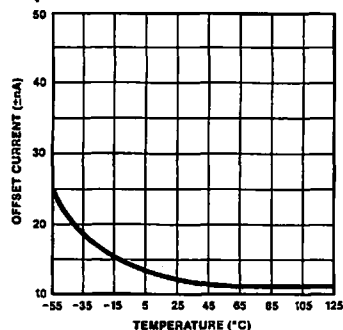
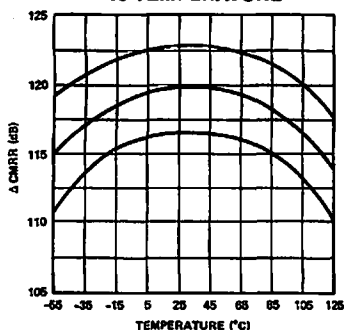
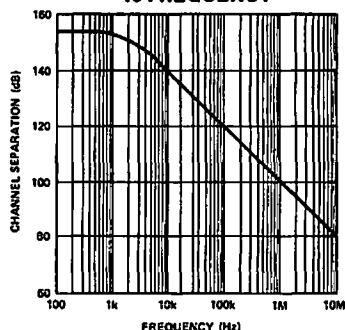
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS

 GAIN, PHASE SHIFT
vs FREQUENCY

 OPEN-LOOP GAIN
vs SUPPLY VOLTAGE

 OUTPUT SWING
vs RESISTIVE LOAD

 MAXIMUM UNDISTORTED
OUTPUT vs FREQUENCY

 SMALL-SIGNAL OVERSHOOT
vs CAPACITIVE LOAD

 SHORT-CIRCUIT
CURRENT vs TIME

 SMALL-SIGNAL
TRANSIENT RESPONSE

 LARGE-SIGNAL
TRANSIENT RESPONSE

 MATCHING CHARACTERISTIC
CMRR MATCH vs FREQUENCY


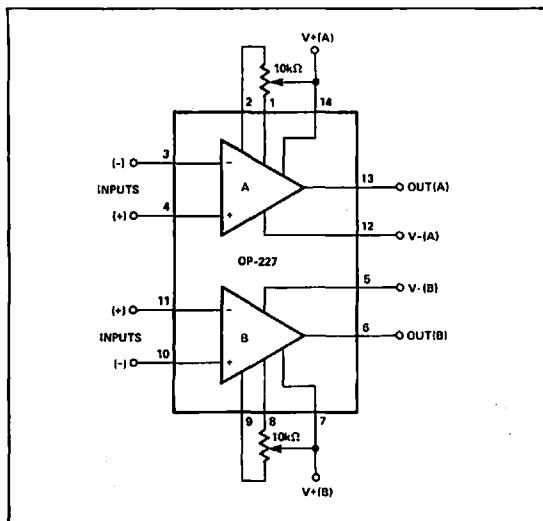
TYPICAL PERFORMANCE CHARACTERISTICS

 COMMON-MODE INPUT RANGE
vs SUPPLY VOLTAGE

 OPEN-LOOP VOLTAGE GAIN
vs LOAD RESISTANCE

 PSRR AND ΔPSRR
vs FREQUENCY

 MATCHING CHARACTERISTIC;
DRIFT OF OFFSET
VOLTAGE MATCH
OF REPRESENTATIVE UNITS

 MATCHING CHARACTERISTIC;
AVERAGE NONINVERTING
BIAS CURRENT
vs TEMPERATURE

 MATCHING CHARACTERISTIC;
AVERAGE OFFSET
CURRENT vs TEMPERATURE
(INVERTING OR NONINVERTING)

 MATCHING CHARACTERISTIC;
CMRR MATCH
vs TEMPERATURE

 CHANNEL SEPARATION
vs FREQUENCY


OPERATIONAL AMPLIFIERS

BASIC CONNECTIONS

OFFSET NULLING CIRCUIT



APPLICATIONS INFORMATION

NOISE MEASUREMENTS

To measure the 80nV peak-to-peak noise specification of the OP-227 in the 0.1Hz to 10Hz range, the following precautions must be observed:

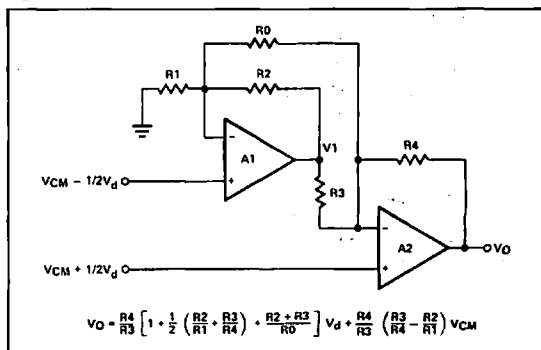
- (1) The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4μV due to increasing chip temperature after power-up. In the 10-second measurement interval these temperature-induced effects can exceed tens-of-nanovolts.
- (2) For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.
- (3) Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.
- (4) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve, the 0.1Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.
- (5) A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

INSTRUMENTATION AMPLIFIER APPLICATIONS OF THE OP-227

The excellent input characteristics of the OP-227 make it ideal for use in instrumentation amplifier configurations where low-level differential signals are to be amplified. The low-noise, low input offsets, low drift, and high gain combined with excellent CMR provides the characteristics needed for high-performance instrumentation amplifiers. In addition, CMR vs. frequency is very good due to the wide gain-bandwidth of these op amps.

The circuit of Figure 1 is recommended for applications where the common-mode input range is relatively low and differential gain will be in the range of 10 to 1000. This two-op-amp instrumentation amplifier features independent adjustment of common-mode rejection and differential gain. Input impedance is very high since both inputs are applied to non-inverting op amp inputs.

FIGURE 1: Two-Op-Amp Instrumentation Amplifier Configuration



The output voltage V_O , assuming ideal op amps, is given in Fig. 1. The input voltages are represented as a common-mode input V_{CM} plus a differential input V_d . The ratio R_3/R_4 is made equal to the ratio R_2/R_1 to reject the common-mode input V_{CM} . The differential signal V_d is then amplified according to:

$$V_O = \frac{R_4}{R_3} \left(1 + \frac{R_3}{R_4} + \frac{R_2 + R_3}{R_O} \right) V_d, \text{ where } \frac{R_3}{R_4} = \frac{R_2}{R_1}$$

Note that gain can be independently varied by adjusting R_O . From considerations of dynamic range, resistor tempco matching, and matching of amplifier response, it is generally best to make R_1 , R_2 , R_3 , and R_4 approximately equal. Designating R_1 , R_2 , R_3 , and R_4 as R_N allows the output equation to be further simplified:

$$V_O = 2 \left(1 + \frac{R_N}{R_O} \right) V_d, \text{ where } R_N = R_1 = R_2 = R_3 = R_4$$

Dynamic range is limited by A1 as well as A2; the output of A1 is:

$$V_1 = - \left(1 + \frac{R_N}{R_O} \right) V_d + 2 V_{CM}$$

The differential gain A_d is $1 + 2R_1/R_O$ and the common-mode input V_{CM} is rejected.

While output error due to input offsets and noise are easily determined, the effects of finite gain and common-mode rejection are more subtle. CMRR of the complete instrumentation amplifier is directly proportioned to the match in CMR of the input op-amps. This match varies from 97dB to 110dB minimum for the OP-227. Using 100dB, then the output response to a common-mode input V_{CM} would be:

$$[V_O]_{CM} = A_d V_{CM} \times 10^{-5}$$

CMRR of the instrumentation amplifier, which is defined as $20 \log_{10} A_d/A_{CM}$, is simply equal to the Δ CMRR of the OP-227. While this Δ CMRR is already high, overall CMRR of the complete amplifier can be raised by trimming the output stage resistor network.

Finite gain of the input op-amps causes a scale factor error and a small degradation in CMR. Designating the open-loop gain of op-amp A_1 as A_{O1} , and op-amp A_2 as A_{O2} , then the following equation approximates the output:

$$V_O \sim \frac{1}{1 + \frac{R_1}{R_O} \left(\frac{1}{A_{O1}} + \frac{1}{A_{O2}} \right)} \left(A_d V_d + \frac{2R_1}{R_O} \left(\frac{1}{A_{O1}} - \frac{1}{A_{O2}} \right) V_{CM} \right)$$

This can be simplified by defining A_O as the nominal open-loop gain and ΔA_O as the differential open-loop gain. Then

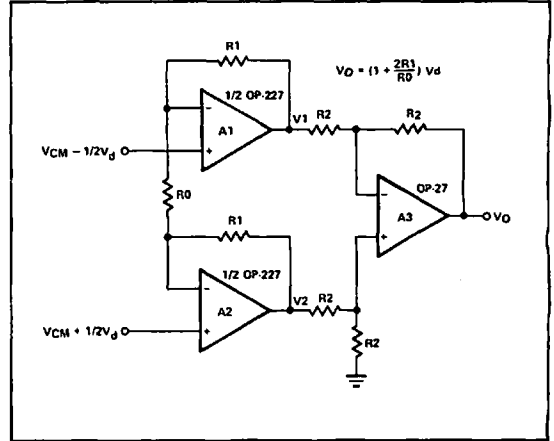
$$V_O \sim \frac{1}{1 + \frac{2R_1}{R_O} \frac{1}{A_O}} \left(A_d V_d + \frac{2R_1}{R_O} \frac{\Delta A_O}{A_O^2} V_{CM} \right)$$

The high open-loop gain of each amplifier within the OP-227 (700,000 minimum at 25°C into $R_L \geq 2k$) assures good gain accuracy even at high values of A_d . The effect of finite open-loop gain on CMR can be approximated by:

$$CMRR \sim \frac{A_O^2}{\Delta A_O}$$

If $\Delta A_O/A_O$ were 6% and A_O were 600,000, then the CMRR due to finite gain of the input op-amps would be approximately 140dB.

FIGURE 3: Three-Op-Amp Instrumentation Amplifier Using OP-227 and OP-27



The unity-gain output stage contributes negligible error to the overall amplifier. However, matching of the four-resistor R_2 -network is critical to achieving high CMR. Consider a worst-case situation where each R_2 resistor has an error of $\pm \Delta R_2$. If the resistor ratio is high on one side and low on the other, then the common-mode gain will be $2\Delta R_2/R_2$. Since the output stage gain is unity, CMRR will then be $R_2/2\Delta R_2$. It is common practice to trim the R_2 resistor connected to ground to maximize overall CMRR for the total instrumentation amplifier circuit.

This three-op-amp instrumentation amplifier configuration provides excellent performance over a wide gain range. A gain range of 1 to 2000 is practical and CMR of over 120dB is achievable.

HIGH SPEED PRECISION RECTIFIER

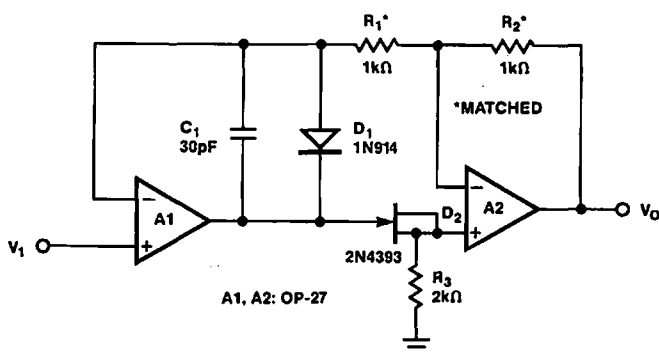
The low offsets and excellent load driving capability of the OP-27 are key advantages in this precision rectifier circuit. The summing impedances can be as low as $1\text{k}\Omega$ which helps to reduce the effects of stray capacitance.

For positive inputs, D2 conducts and D1 is biased OFF. Amplifiers A1 and A2 act as a follower with output-to-input feedback and the R1 resistors are no critical. For negative inputs, D1 conducts and D2 is biased OFF. A1 acts as a follower and A2 serves as a precision inverter. In this mode, matching of the two R1 resistors is critical to gain accuracy.

Typical component values are 30pF for C1 and $2\text{k}\Omega$ for R3. The drop across D1 must be less than the drop across the FET diode D2. A 1N914 for D1 and a 2N4393 for the JFET were used successfully.

The circuit provides full-wave rectification for inputs of up to $\pm 10\text{V}$ and up to 20kHz in frequency. To assure frequency stability, be sure to decouple the power supply inputs and minimize any capacitive loading. An OP-227, which is two OP-27 amplifiers in a single package, can be used to improve packaging density.

FIGURE 4: High Speed Precision Rectifier



Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Slew Rate 200V/ μ s Min
- -3dB Bandwidth ($A_V = 1$ to 50) 8MHz Min
- Output Current Drive 20mA Min
- Bandwidth is Independent of Gain

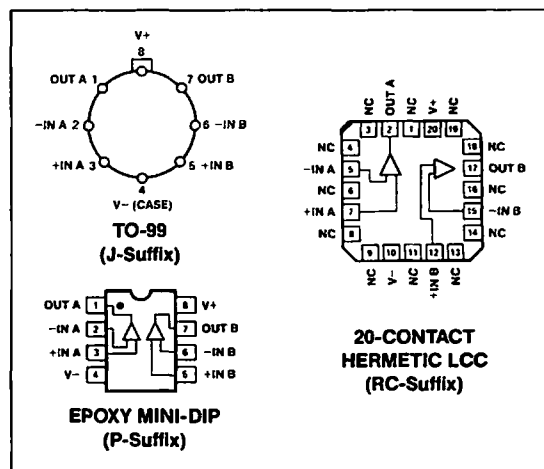
GENERAL DESCRIPTION

The OP-260 represents a new concept in high-speed monolithic operational amplifiers. A dual amplifier, the OP-260 employs current-feedback to provide consistently wideband amplification regardless of gain. A -3dB bandwidth of 8MHz minimum for gains from 1 to 50, and a bandwidth of 5MHz min in a gain of 100 combine with a 200V/ μ s min slew rate for extremely high-speed operation. Although gain-bandwidth product does not apply to current-feedback amplifiers, the OP-260 rivals op amps with GBWs of 1/2GHz!

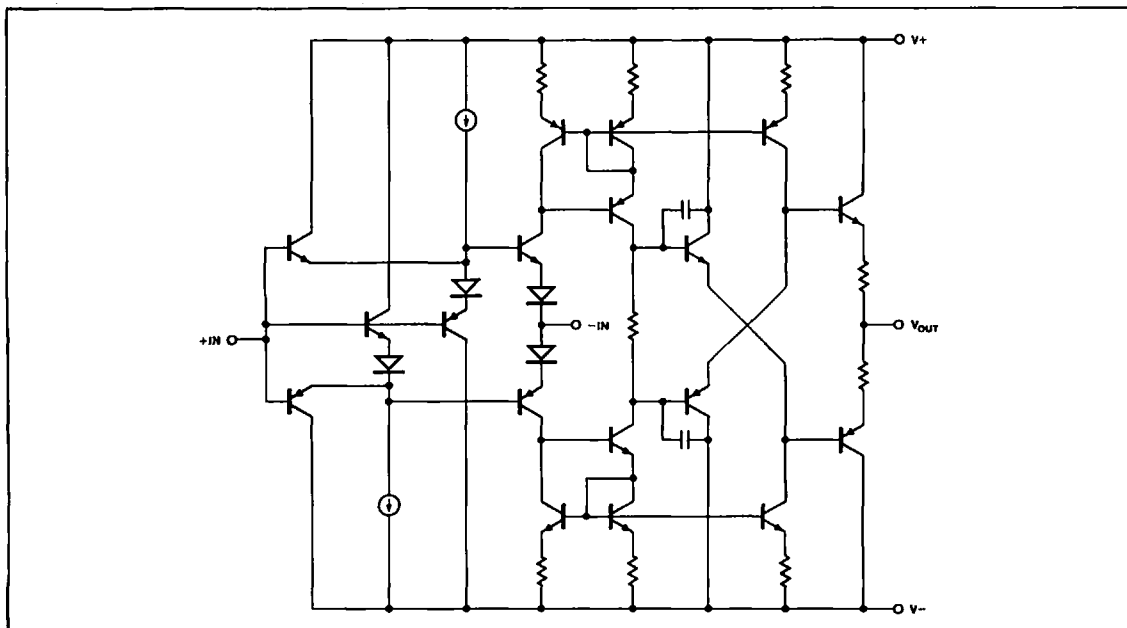
Two independent amplifiers are contained on the OP-260 chip. This allows two-channel amplification with matched AC characteristics between the two amplifiers. High-speed instrumentation front-ends are easily achieved with the OP-260 as well. The OP-260 will output substantial current. 20mA minimum current drive is available, with 40mA minimum during transients. If large loads are being driven, a clip-on heat sink is recommended.

Applications include ultrasound and sonar systems, video blocks, IF amplification and high-speed data acquisition systems.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of Two Amplifiers)



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation (Note 2)	500mW
Input Voltage (Note 3)	$\pm 18\text{V}$
Output Short-Circuit Duration	10 sec
Operating Temperature Range	
OP-260A (J, RC)	-55°C to $+125^{\circ}\text{C}$
OP-260E (J, P)	-40°C to $+85^{\circ}\text{C}$
Storage Temperature Range	-65°C to $+175^{\circ}\text{C}$
Junction Temperature Range	-65°C to $+175^{\circ}\text{C}$
Lead Temperature (Soldering, 10 sec)	300°C

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. See table for maximum ambient temperature and rating.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
20-Contact LCC (RC)	80°C	$7.8\text{mW}/^{\circ}\text{C}$
TO-99 (J)	80°C	$7.1\text{mW}/^{\circ}\text{C}$
8-Pin Plastic DIP (P)	62°C	$5.6\text{mW}/^{\circ}\text{C}$

3. For supply voltages less than $\pm 18\text{V}$, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $R_F = 5\text{k}\Omega$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	OP-260A/E		UNITS
				TYP	MAX	
Input Offset Voltage	V_{IOS}	Each Amplifier	—	—	8	mV
	ΔV_{IOS}	Matching	—	—	1	
Output Offset Voltage ($R_F = 5\text{k}\Omega$)	V_{OOS}	Each Amplifier	—	—	15	mV
	ΔV_{OOS}	Matching	—	—	2.5	
Offset Voltage Temperature Coefficient	TCV_{OS}	Each Amplifier	—	—	25	$\mu\text{V}/^{\circ}\text{C}$
	ΔTCV_{OS}	Matching	—	—	5	
Input Bias Current	I_B	+Input	—	—	0.4	μA
	I_B	-Input	—	—	3	
	ΔI_B	+Input Matching	—	—	0.2	
	ΔI_B	-Input Matching	—	—	0.5	
Input Bias Current Temperature Coefficient	TCI_B	+Input	—	—	4	nA/ $^{\circ}\text{C}$
	TCI_B	-Input	—	—	30	
	ΔTCI_B	+Input Matching	—	—	2	
	ΔTCI_B	-Input Matching	—	—	5	
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{V}$	Each Amplifier	50	—	dB
	ΔCMR		Matching	80	—	
Power-Supply Rejection	PSR	$V_S = \pm 9\text{V}$ to $\pm 18\text{V}$	Each Amplifier	60	—	dB
	ΔPSR		Matching	80	—	
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{V}$; $R_L = 1\text{k}\Omega$	25	—	—	V/mV
Output Voltage Swing	V_O	$R_L = 1\text{k}\Omega$	± 12	—	—	V
Output Current Drive	I_{OUT}		± 20	—	—	mA
Slew Rate	SR		200	—	—	V/ μs
-3dB Bandwidth	BW	$A_V = 1$ to 50	8	—	—	MHz
		$A_V = 100$	5	—	—	
Supply Current	I_{SY}		—	—	11	mA



OP-270

DUAL LOW-NOISE PRECISION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Very Low Noise $3.5\text{nV}/\sqrt{\text{Hz}}$ @ 1kHz Max
- Excellent Input Offset Voltage $50\mu\text{V}$ Max
- Low Offset Voltage Drift $0.6\mu\text{V}/^\circ\text{C}$ Max
- Very High Gain $1000\text{V}/\text{mV}$ Min
- Outstanding CMR 110dB Min
- Slew Rate $2\text{V}/\mu\text{s}$ Typ
- Gain-Bandwidth Product 6MHz Typ
- Industry Standard 8-Pin Dual Pinout

ORDERING INFORMATION†

$T_A = 25^\circ\text{O}$ V_{OS} MAX (μV)		PACKAGE		OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC	
50	OP270AZ*	—	OP270ARC/883	MIL
50	OP270EZ	—	—	XIND
100	OP270FZ	—	—	XIND
200	—	OP270GP	—	XIND
200	—	OP270GS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

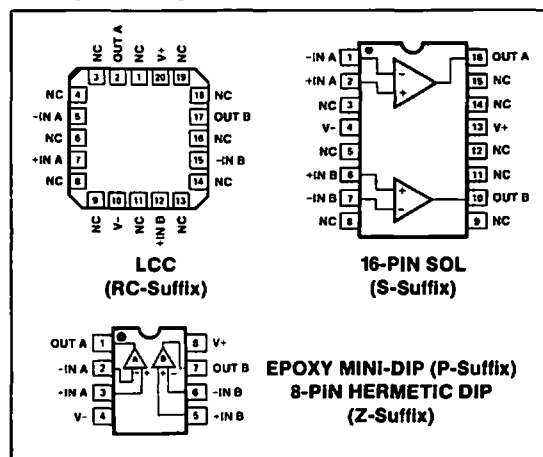
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

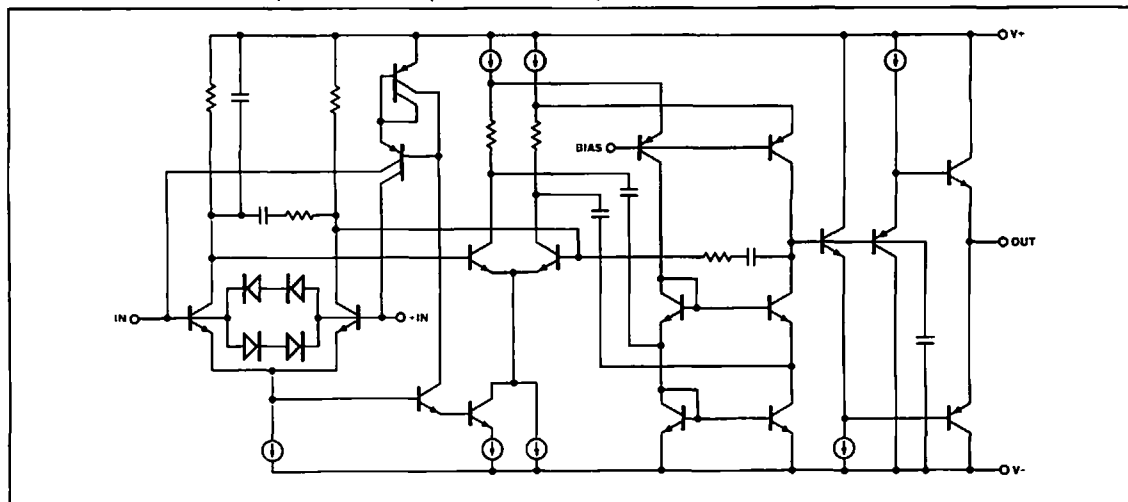
The OP-270 is a high-performance monolithic dual operational amplifier with exceptionally low voltage noise, $3.5\text{nV}/\sqrt{\text{Hz}}$ at 1kHz Max, offering comparable performance to PMI's industry standard OP-27.

The OP-270 features an input offset voltage below $50\mu\text{V}$ and an offset drift under $0.6\mu\text{V}/^\circ\text{C}$, guaranteed over the full military temperature range. Open-loop gain of the OP-270 is over 1,000,000 into a $10\text{k}\Omega$ load insuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under 10nA which reduces errors due to signal source resistance. The OP-270's CMR of over 110dB and PSRR of less than $1.8\mu\text{V}/\text{V}$ significantly reduce errors due to ground noise and power supply fluctuations. Power con-

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



sumption of the dual OP-270 equals that of a single OP-27, a significant advantage for power conscious applications. The OP-270 is unity-gain stable with a gain-bandwidth product of 6MHz and a slew rate of 2V/ μ s.

The OP-270 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, dual buffers, and low-noise active filters.

The OP-270 conforms to the industry standard 8-pin DIP pinout. It is pin compatible with the MC1458/1558, SE5532/A, RM4558 and HA5102 dual op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-271, with a slew rate of 8V/ μ s, is recommended. For a quad op amp, see the OP-470.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	$\pm 18V$
Internal Power Dissipation (Note 1)	
P, RC, S, Z-Package	500mW
Differential Input Voltage (Note 3)	$\pm 1.0V$
Differential Input Current (Note 3)	$\pm 25mA$

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-270A/E			OP-270F			OP-270G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	10	50	—	30	100	—	75	200	μV
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	3	10	—	6	15	—	12	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	3	10	—	6	15	—	12	20	nA
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	2.6	5.0	—	2.6	5.0	—	2.6	5.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$	—	2.1	4.0	—	2.1	4.0	—	2.1	4.0	
		$f_O = 1kHz$ (Note 2)	—	2.0	3.5	—	2.0	3.5	—	2.0	3.5	
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$	1000	2300	—	800	1700	—	800	1700	—	V/mV
		$R_L = 2k\Omega$	500	1200	—	400	900	—	400	900	—	
Input Voltage Range	IVR	(Note 3)	± 11	± 12	—	± 11	± 12	—	± 11	± 12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection CMR		$V_{CM} = \pm 11V$	110	125	—	100	120	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	0.56	1.8	—	1.0	5.6	—	5.6	10	$\mu V/V$
Slew Rate	SR		1.4	2	—	1.4	2	—	1.4	2	—	V/ μs
Supply Current (All Amplifiers)	I_{SV}	No Load	—	4	5	—	4	5	—	4	5	mA
Gain Bandwidth Product	GBW	$A_V = +10$	—	6	—	—	6	—	—	6	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	155	—	125	155	—	125	155	—	dB

NOTES:

- Guaranteed but not 100% tested.
- Sample tested.
- Guaranteed by CMR test.

Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
P, RC, S, Z-Package	$-65^\circ C$ to $+150^\circ C$
Lead Temperature Range (Soldering, 60 sec)	$300^\circ C$
DICE Junction Temperature (T_J)	$-65^\circ C$ to $+150^\circ C$
Operating Temperature Range	
OP-270A	$-55^\circ C$ to $+125^\circ C$
OP-270E, OP-270F, OP-270G	$-40^\circ C$ to $+85^\circ C$

NOTES:

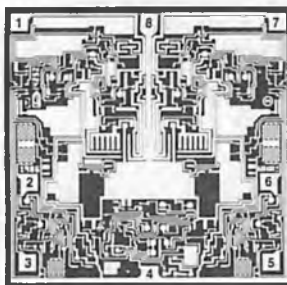
- See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
8-Pin Hermetic DIP (Z)	$75^\circ C$	$8.7mW/^\circ C$
8-Pin Plastic DIP (P)	$62^\circ C$	$5.6mW/^\circ C$
20-Pin LCC (RC)	$80^\circ C$	$7.8mW/^\circ C$

- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
- The OP-270's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds $\pm 1.0V$, the input current should be limited to $\pm 25mA$.



DICE CHARACTERISTICS



DIE SIZE 0.094×0.092 Inch, 8,648 sq. mils
(2.39×2.34 mm, 5.60 sq. mm)

1. OUT A
2. -IN A
3. +IN A
4. V-
5. +IN B
6. -IN B
7. OUT B
8. V-

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-270GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		100	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	15	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	15	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$	800	V/mV MIN
		$R_L = 10k\Omega$ $R_L = 2k\Omega$	400	
Input Voltage Range	IVR	(Note 1)	± 11	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	V MIN
Common Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	5.6	$\mu V/V$ MAX
Slew Rate	SR		1.4	V/ μs MIN
Supply Current (All Amplifiers)	I_{SY}	No Load	5	mA MAX

NOTES:

1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



Precision Monolithics Inc.

OP-271

HIGH-SPEED LOW-NOISE DUAL OPERATIONAL AMPLIFIER

PRELIMINARY

FEATURES

- Excellent Speed $8V/\mu s$ Typ
- Low Noise $10nV/\sqrt{Hz}$ @ 1kHz Max
- Unity-Gain Stable
- High Gain-Bandwidth $6.5MHz$ Typ
- Low Input Offset Voltage $300\mu V$ Max
- Low Offset Voltage Drift $2\mu V/^{\circ}C$ Max
- High Gain $500V/mV$ Min
- Outstanding CMR $105dB$ Min
- Industry Standard 8-Pin Dual Pinout

ORDERING INFORMATION†

$T_A = 25^{\circ}C$ V_{OS} MAX (μV)		PACKAGE		OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC	
300	OP271AZ*	—	OP271ARC/883	MIL
300	OP271EZ	—	—	XIND
500	OP271FZ	—	—	XIND
750	—	OP271GP	—	XIND
750	—	OP271GS††	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

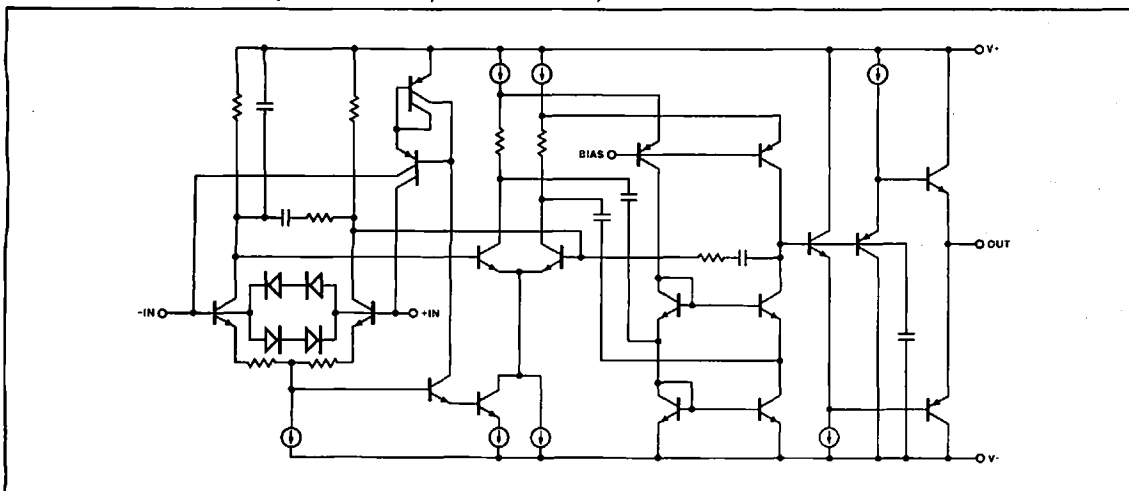
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The OP-271 is a monolithic dual op amp featuring low noise, $10nV/\sqrt{Hz}$ Max @ 1kHz, excellent speed, $8V/\mu s$ typical, a gain-bandwidth of 6.5MHz, and unity-gain stability.

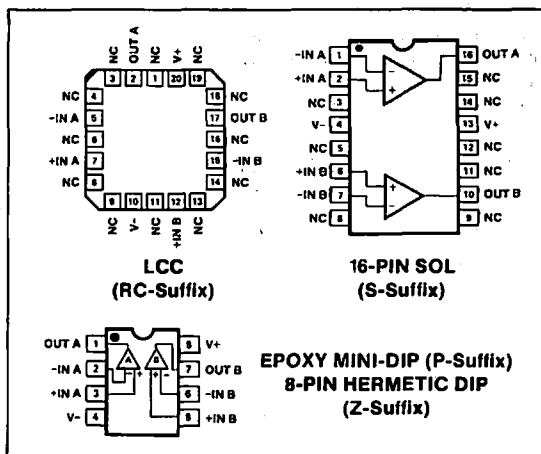
SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

The OP-271 has an input offset voltage under $300\mu V$ and an input offset voltage drift below $2\mu V/^{\circ}C$, guaranteed over the full military temperature range. Open loop gain of the OP-271 is over 500,000 into a $10k\Omega$ load insuring outstanding gain accuracy and linearity. The input bias current is under 10nA limiting errors due to signal source resistance. The OP-271's CMR of over 105dB and PSRR of under $5.6\mu V/V$ significantly reduce errors caused by ground noise and power supply fluctuations.

PIN CONNECTIONS



OPERATIONAL AMPLIFIERS

5



The OP-271 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, dual buffers and low-noise active filters.

The OP-271 conforms to the industry standard 8-pin DIP pinout. It is pin compatible with the MC1458/1558, RC4558, TL082 and TL072 dual op amps and can be used to upgrade systems using these devices.

For applications requiring even lower voltage noise the OP-270, with a voltage density of $3.5\text{nV}/\sqrt{\text{Hz}}$ Max @ 1kHz, is recommended. For a quad op amp, see the OP-471.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation (Note 1)	
P, RC, S, Z-Package	500mW
Differential Input Voltage (Note 3)	$\pm 1.0\text{V}$
Differential Input Current (Note 3)	$\pm 25\text{mA}$
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous

Storage Temperature Range

P, RC, S, Z-Package	-65°C to $+150^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_j)	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	
OP-271A	-55°C to $+125^{\circ}\text{C}$
OP-271E, OP-271F, OP-271G	-40°C to $+85^{\circ}\text{C}$

NOTES:

- See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
8-Pin Hermetic DIP (Z)	75°C	$6.7\text{mW}/^{\circ}\text{C}$
8-Pin Plastic DIP (P)	62°C	$5.6\text{mW}/^{\circ}\text{C}$
20-Pin LCC (RC)	80°C	$7.8\text{mW}/^{\circ}\text{C}$

- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
- The OP-271's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds $\pm 1.0\text{V}$, the input current should be limited to $\pm 25\text{mA}$.

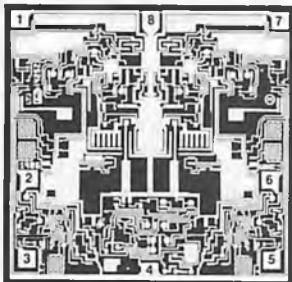
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-271A/E			OP-271F			OP-271G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	100	300	—	250	500	—	350	750	μV
Input Offset Current	I_{OS}	$V_{CM} = 0\text{V}$	—	3	10	—	6	15	—	12	20	nA
Input Bias Current	I_B	$V_{CM} = 0\text{V}$	—	3	10	—	6	15	—	12	20	nA
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	9	15	—	9	15	—	9	15	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	7	11	—	7	11	—	7	11	
		$f_O = 1\text{kHz}$	—	6	10	—	6	10	—	6	10	
		(Note 2)										
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{V}$	500	700	—	300	500	—	300	500	—	V/mV
		$R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$	350	550	—	175	275	—	175	275	—	
Input Voltage Range	IVR	(Note 3)	± 11	± 12	—	± 11	± 12	—	± 11	± 12	—	V
Output Voltage Swing	V_O	$R_L \geq 2\text{k}\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection CMR		$V_{CM} = \pm 11\text{V}$	105	120	—	95	115	—	95	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$	—	1	5.6	—	5.6	17.8	—	5.6	17.8	$\mu\text{V}/\text{V}$
Slew Rate	SR		6.5	8	—	6.5	8	—	6.5	8	—	$\text{V}/\mu\text{s}$
Supply Current (All Amplifiers)	I_{SY}	No Load	—	4	5	—	4	5	—	4	5	mA
Gain-Bandwidth Product	GBW	$A_V = +10$	—	6.5	—	—	6.5	—	—	6.5	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10\text{Hz}$ (Note 1)	125	150	—	125	150	—	125	150	—	dB

NOTES:

- Guaranteed but not 100% tested.
- Sample tested.
- Guaranteed by CMR test.

DICE CHARACTERISTICS



1. OUT A
2. -IN A
3. +IN A
4. V-
5. +IN B
6. -IN B
7. OUT B
8. V+

DIE SIZE 0.094×0.092 inch, 8,648 sq. mils
(2.39×2.34 mm, 5.60 sq. mm)

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-271GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		500	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	15	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	15	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$		
		$R_L = 10k\Omega$	300	V/mV MIN
		$R_L = 2k\Omega$	175	
Input Voltage Range	IVR	(Note 1)	± 11	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	17.8	$\mu V/V$ MAX
Slew Rate	SR		6.5	V/ μs MIN
Supply Current (All Amplifiers)	I_{SY}	No Load	5	mA MAX

NOTES:

1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



OP-290

PRECISION LOW-VOLTAGE MICROPOWER
DUAL OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- **Single/Dual Supply Operation** +1.6V to +36V
..... $\pm 0.8V$ to $\pm 18V$
- **True Single-Supply Operation; Input and Output Voltage Ranges Include Ground**
- **Low Supply Current (per amplifier)** 20 μA Max
- **High Output Drive** 5mA Min
- **Low Input Offset Voltage** 150 μV Max
- **High Open-Loop Gain** 700V/mV Min
- **Outstanding PSRR** 5.6 $\mu V/V$ Max
- **Industry Standard 8-Pin Dual Pinout**

ORDERING INFORMATION†

$T_A = 25^{\circ}\text{C}$ V_{OS} MAX		PACKAGE		OPERATING TEMPERATURE RANGE	
(μV)		CERDIP	PLASTIC		LCC
150	OP290AZ*	—		OP290ARC*	MIL
150	OP290EZ	—		—	IND
250	OP290FZ	—		—	IND
450	—		OP290GP	—	COM
450	—		OP290GS††	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

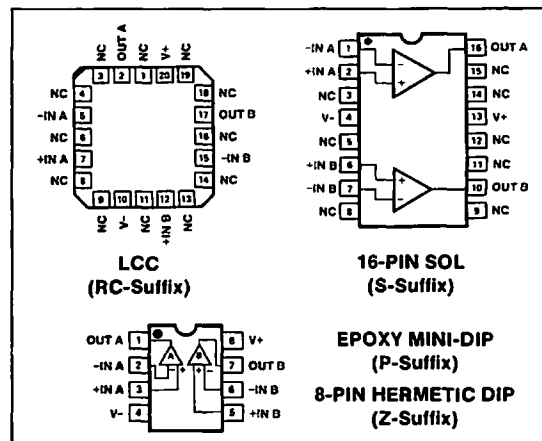
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

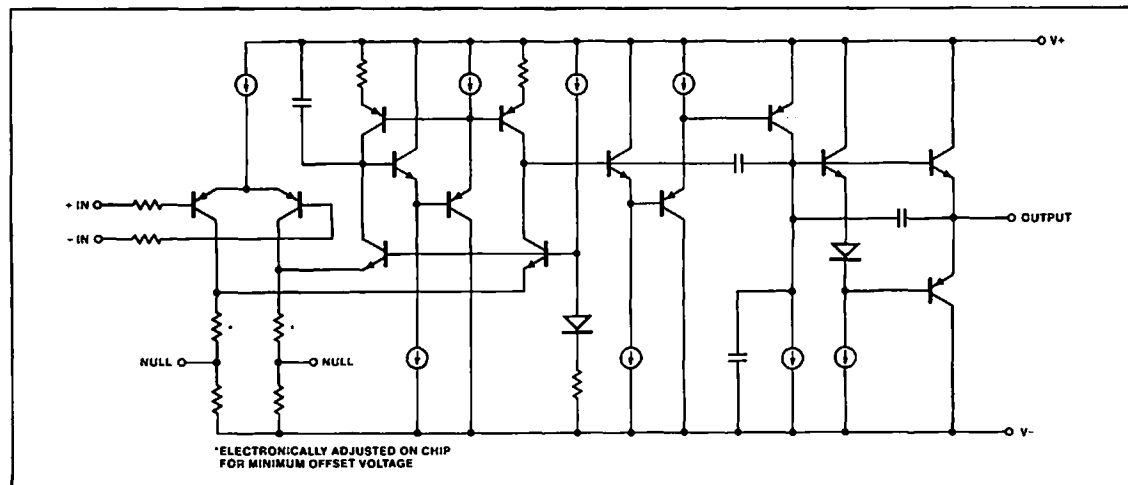
GENERAL DESCRIPTION

The OP-290 is a high performance micropower dual op amp that operates from a single supply of +1.6V to +36V or from dual supplies of ± 0.8 to $\pm 18V$. Input voltage range includes the negative rail allowing the OP-290 to accommodate input signals down to ground in single supply operation. The OP-290's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of two amplifiers is shown.)



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



The OP-290 draws less than 20 μ A of quiescent supply current per amplifier, while able to deliver over 5mA of output current to a load. Input offset voltage is below 150 μ V eliminating the need for external nulling. Gain exceeds 700,000 and common-mode rejection is better than 100dB. The power supply rejection ratio of under 5.6 μ V/V minimizes offset voltage changes experienced in battery powered systems.

The low offset voltage and high gain offered by the OP-290 bring precision performance to micropower applications. The minimal voltage and current requirements of the OP-290 suit it for battery and solar powered applications, such as portable instruments, remote sensors, and satellites. For a single op amp, see the OP-90; for a quad, see the OP-490.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	± 18 V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	[(V ₋) - 20V] to [(V ₊) + 20V]
Common-Mode Input Voltage	[(V ₋) - 20V] to [(V ₊) + 20V]

Output Short-Circuit DurationIndefinite
Storage Temperature Range

P, RC, S, Z Package -65°C to +150°C
Operating Temperature Range

OP-290A -55°C to +125°C

OP-290E, OP-290F -40°C to +85°C

OP-290G 0°C to +70°C

DICE Junction Temperature (T_J) -65°C to +150°C

Lead Temperature Range (Soldering, 60 sec) 300°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.
- Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
8-Pin Plastic DIP (P)	36°C	5.6mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
20-Pin LCC (RC)	80°C	7.8mW/°C

ELECTRICAL CHARACTERISTICS at V_S = ± 1.5 V to ± 15 V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-290A/E			OP-290F			OP-290G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}		—	50	150	—	75	250	—	125	450	μ V
Input Offset Current	I _{OS}	V _{CM} = 0V	—	0.4	3	—	0.4	5	—	0.4	5	nA
Input Bias Current	I _B	V _{CM} = 0V	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A _{VO}	V _S = ± 15 V, V _O = ± 10 V R _L = 100k Ω	700	1200	—	500	1000	—	400	800	—	V/mV
		R _L = 10k Ω	350	600	—	250	500	—	200	400	—	
		R _L = 2k Ω	125	250	—	100	200	—	100	200	—	
		V ₊ = 5V, V ₋ = 0V, 1V < V _O < 4V R _L = 100k Ω	200	400	—	125	300	—	100	250	—	
		R _L = 10k Ω	100	180	—	75	140	—	70	140	—	
Input Voltage Range	IVR	V ₊ = 5V, V ₋ = 0V	0/4	—	—	0/4	—	—	0/4	—	—	V
		V _S = ± 15 V (Note 1)	-15/13.5	—	—	-15/13.5	—	—	-15/13.5	—	—	
Output Voltage Swing	V _O	V _S = ± 15 V R _L = 10k Ω	± 14	± 14.2	—	± 14	± 14.2	—	± 14	± 14.2	—	V
		R _L = 2k Ω	± 11	± 12	—	± 11	± 12	—	± 11	± 12	—	
	V _{OH}	V ₊ = 5V, V ₋ = 0V R _L = 2k Ω	4.0	4.2	—	4.0	4.2	—	4.0	4.2	—	V
		V ₊ = 5V, V ₋ = 0V R _L = 10k Ω	—	100	500	—	100	500	—	100	500	μ V
Common-Mode Rejection	CMR	V ₊ = 5V, V ₋ = 0V, 0V < V _{CM} < 4V V _S = ± 15 V, -15V < V _{CM} < 13.5V	90	110	—	80	100	—	80	100	—	dB
			100	130	—	90	120	—	90	120	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	1.0	5.6	—	3.2	10	μ V/V
Supply Current (All Amplifiers)	I _{SV}	V _S = ± 1.5 V	—	18	30	—	18	30	—	18	30	μ A
		V _S = ± 15 V	—	28	40	—	28	40	—	28	40	
Capacitive Load Stability		A _V = +1 No Oscillations	—	650	—	—	650	—	—	650	—	pF
Input Noise Voltage	e _{np-p}	f _O = 0.1Hz to 10Hz V _S = ± 15 V	—	3	—	—	3	—	—	3	—	μ V _{p-p}

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 1.5\text{V}$ to $\pm 15\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-290A/E			OP-290F			OP-290G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Resistance Differential Mode	R_{IN}	$V_S = \pm 15\text{V}$	—	30	—	—	30	—	—	30	—	M Ω
Input Resistance Common Mode	R_{INCM}	$V_S = \pm 15\text{V}$	—	20	—	—	20	—	—	20	—	G Ω
Slew Rate	SR	$V_S = \pm 15\text{V}$	5	12	—	5	12	—	5	12	—	V/ms
Gain Bandwidth Product	GBWP	$A_V = +1$	—	20	—	—	20	—	—	20	—	kHz
Channel Separation	CS	$f_O = 10\text{Hz}$ $V_O = 20\text{V}_{p-p}$ $V_S = \pm 15\text{V}$ (Note 2)	120	150	—	120	150	—	120	150	—	dB

NOTES:

1. Guaranteed by CMR test.
2. Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5\text{V}$ to $\pm 15\text{V}$, $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-290A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	80	400	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	2.5	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}	$V_{CM} = 0\text{V}$	—	1.5	5	nA
Input Bias Current	I_B	$V_{CM} = 0\text{V}$	—	4.0	20	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$ $R_L = 100\text{k}\Omega$	225	400	—	V/mV
		$R_L = 10\text{k}\Omega$	125	240	—	
		$R_L = 2\text{k}\Omega$	50	110	—	
		$V^+ = 5\text{V}$, $V^- = 0\text{V}$, $1\text{V} < V_O < 4\text{V}$ $R_L = 100\text{k}\Omega$	100	200	—	
		$R_L = 10\text{k}\Omega$	50	110	—	
Input Voltage Range	IVR	$V^+ = 5\text{V}$, $V^- = 0\text{V}$ (Note 1) $V_S = \pm 15\text{V}$	0/3.5 -15/13.5	— —	— —	V
Output Voltage Swing	V_O	$V_S = \pm 15\text{V}$ $R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$	± 13.5 ± 10.5	± 13.7 ± 11.5	— —	V
	V_{OH}	$V^+ = 5\text{V}$, $V^- = 0\text{V}$ $R_L = 2\text{k}\Omega$	3.9	4.1	—	V
	V_{OL}	$V^+ = 5\text{V}$, $V^- = 0\text{V}$ $R_L = 10\text{k}\Omega$	—	100	500	μV
Common-Mode Rejection	CMR	$V^+ = 5\text{V}$, $V^- = 0\text{V}$, $0\text{V} < V_{CM} < 3.5\text{V}$ $V_S = \pm 15\text{V}$, $-15\text{V} < V_{CM} < 13.5\text{V}$	85 95	105 115	— —	dB
Power Supply Rejection Ratio	PSRR		—	3.2	10	$\mu\text{V}/\text{V}$
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 1.5\text{V}$ $V_S = \pm 15\text{V}$	— —	30 38	50 60	μA

NOTE:

1. Guaranteed by CMR test.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $-40^\circ C \leq T_A \leq 85^\circ C$ for OP-290E/F, $0^\circ C \leq T_A \leq 70^\circ C$ for OP-290G, unless otherwise noted.

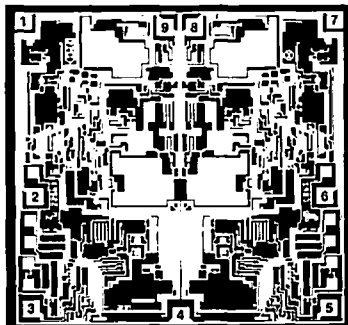
PARAMETER	SYMBOL	CONDITIONS	OP-290E			OP-290F			OP-290G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	70	270	—	110	550	—	180	675	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	2	—	0.6	5	—	1.2	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.8	3	—	1.0	5	—	1.3	7	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.0	15	—	4.0	20	—	4.0	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100k\Omega$	500	800	—	350	700	—	300	600	—	V/mV
		$R_L = 10k\Omega$	250	400	—	175	350	—	150	250	—	
		$R_L = 2k\Omega$	100	200	—	75	150	—	75	125	—	
		$V^+ = 5V$, $V^- = 0V$, $1V < V_O < 4V$ $R_L = 100k\Omega$	150	280	—	100	220	—	80	160	—	
		$R_L = 10k\Omega$	75	140	—	50	110	—	40	90	—	
Input Voltage Range	IVR	$V^+ = 5V$, $V^- = 0V$	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$ (Note 1)	-15/13.5	—	—	-15/13.5	—	—	-15/13.5	—	—	
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$	± 13.5	± 14	—	± 13.5	± 14	—	± 13.5	± 14	—	V
		$R_L = 2k\Omega$	± 10.5	± 11.8	—	± 10.5	± 11.8	—	± 10.5	± 11.8	—	
	V_{OH}	$V^+ = 5V$, $V^- = 0V$ $R_L = 2k\Omega$	3.9	4.1	—	3.9	4.1	—	3.9	4.1	—	V
Common-Mode Rejection	CMR	$V^+ = 5V$, $V^- = 0V$, $0V < V_{CM} < 3.5V$	90	110	—	80	100	—	80	100	—	dB
		$V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	100	120	—	90	110	—	90	110	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	3.2	10	—	5.6	17.8	$\mu V/V$
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 1.5V$	—	26	50	—	26	50	—	24	50	μA
		$V_S = \pm 15V$	—	34	60	—	34	60	—	32	60	

NOTE:

1. Guaranteed by CMR test.



DICE CHARACTERISTICS

DIE SIZE 0.109×0.104 inch, 11,336 sq. mils
(2.77×1.70 mm, 4.71 sq. mm)

1. OUT A
2. -IN A
3. +IN A
4. V-
5. +IN B
6. -IN B
7. OUT B
8. V+ B
9. V+ A

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$ to $\pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-290GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		250	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	5	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	20	nA MAX
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100k\Omega$	500	V/mV MIN
		$R_L = 10k\Omega$	250	
		$V+ = 5V$, $V- = 0V$, $1V < V_O < 4V$ $R_L = 100k\Omega$	125	V/mV MIN
Input Voltage Range	IVR	$V+ = 5V$, $V- = 0V$ (Note 1) $V_S = \pm 15V$	0/4 -15/13.5	V MIN
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 14 ± 11	V MIN
	V_{OH}	$V+ = 5V$, $V- = 0V$ $R_L = 2k\Omega$	4.0	V MIN
	V_{OL}	$V+ = 5V$, $V- = 0V$ $R_L = 10k\Omega$	500	μV MAX
Common-Mode Rejection	CMR	$V+ = 5V$, $V- = 0V$, $0V < V_{CM} < 4V$	80	dB MIN
		$V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	90	
Power Supply Rejection Ratio	PSRR		10	$\mu V/V$ MAX
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 15V$	40	μA MAX

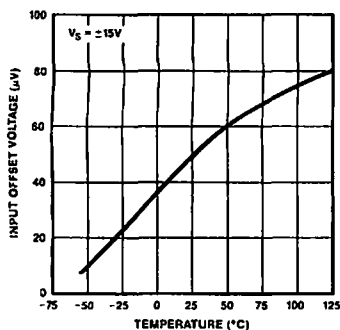
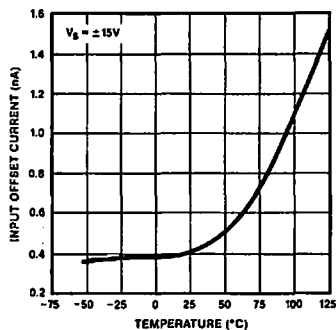
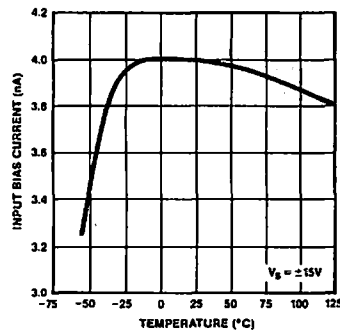
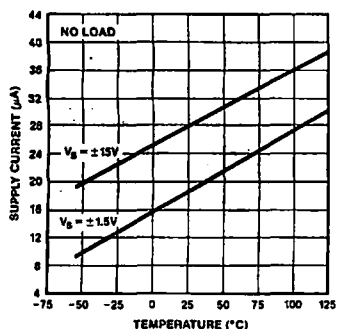
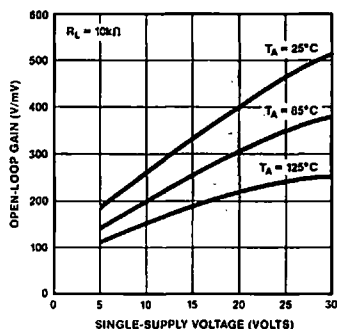
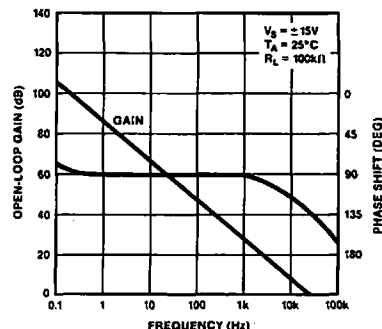
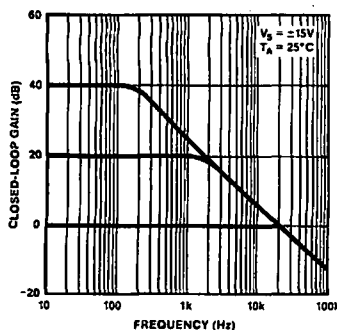
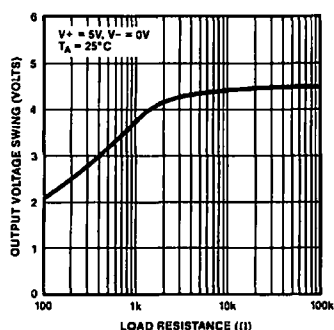
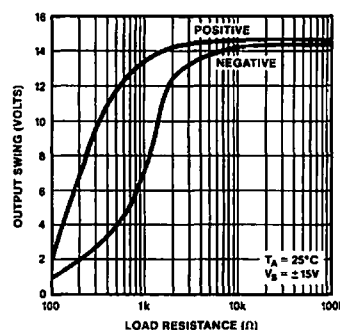
NOTES:

1. Guaranteed by CMR test.

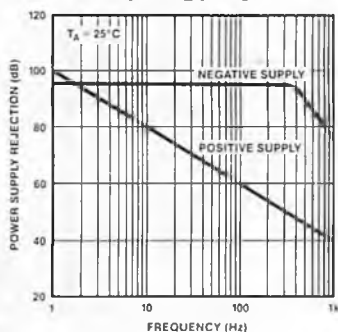
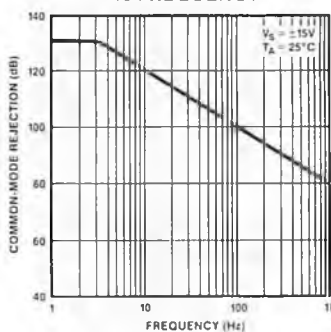
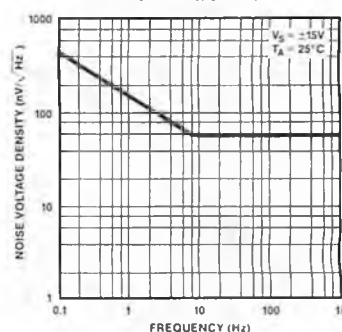
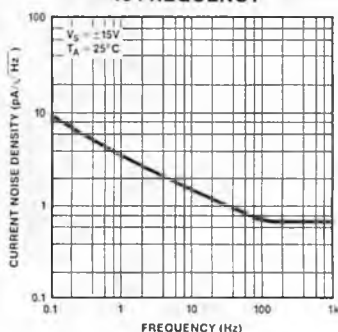
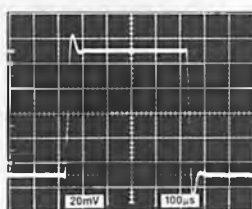
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



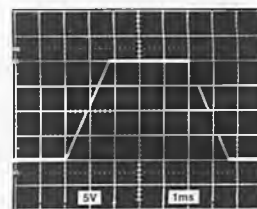
TYPICAL PERFORMANCE CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs TEMPERATUREINPUT OFFSET CURRENT
vs TEMPERATUREINPUT BIAS CURRENT
vs TEMPERATURESUPPLY CURRENT
vs TEMPERATUREOPEN-LOOP GAIN vs
SINGLE-SUPPLY VOLTAGEOPEN-LOOP GAIN AND
PHASE SHIFT vs FREQUENCYCLOSED-LOOP GAIN
vs FREQUENCYOUTPUT VOLTAGE SWING
vs LOAD RESISTANCEOUTPUT VOLTAGE SWING
vs LOAD RESISTANCE

TYPICAL PERFORMANCE CHARACTERISTICS

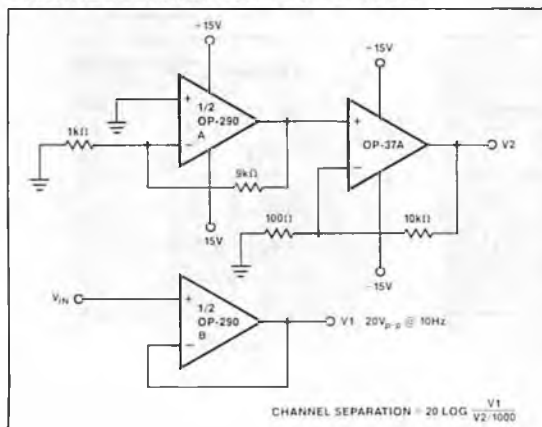
 POWER SUPPLY REJECTION
vs FREQUENCY

 COMMON-MODE REJECTION
vs FREQUENCY

 NOISE VOLTAGE DENSITY
vs FREQUENCY

 CURRENT NOISE DENSITY
vs FREQUENCY

 SMALL-SIGNAL
TRANSIENT RESPONSE


$T_A = 25^\circ\text{C}$
 $V_S = \pm 15\text{V}$
 $A_V = -1$
 $R_L = 10\text{k}\Omega$
 $C_L = 500\text{pF}$

 LARGE-SIGNAL
TRANSIENT RESPONSE


$T_A = 25^\circ\text{C}$
 $V_S = \pm 15\text{V}$
 $A_V = -1$
 $R_L = 10\text{k}\Omega$
 $C_L = 500\text{pF}$

CHANNEL SEPARATION TEST CIRCUIT



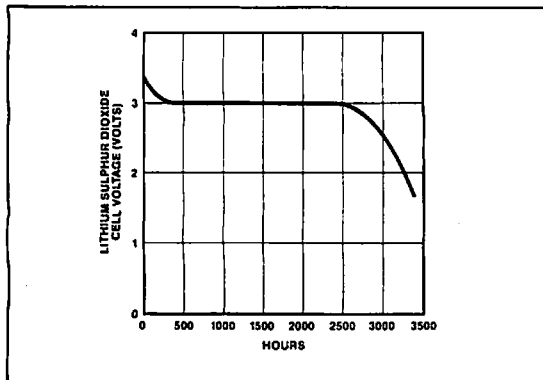
APPLICATIONS INFORMATION

BATTERY-POWERED APPLICATIONS

The OP-290 can be operated on a minimum supply voltage of $\pm 1.6\text{V}$, or with dual supplies $\pm 0.8\text{V}$, and draws only $18\mu\text{A}$ of supply current. In many battery-powered circuits, the OP-290 can be continuously operated for thousands of hours before requiring battery replacement, reducing equipment downtime and operating cost.

High-performance portable equipment and instruments frequently use lithium cells because of their long shelf-life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3V and are noted for a flat discharge characteristic. The low supply voltage requirement of the OP-290, combined with the flat discharge characteristic of the lithium cell, indicates that the OP-290 can be operated over the entire useful life of the cell. Figure 1 shows the typical discharge characteristic of a 1Ah lithium cell powering an OP-290 with each amplifier, in turn, driving full output swing into a $100\text{k}\Omega$ load.

**FIGURE 1: Lithium Sulphur Dioxide Cell Discharge
Characteristic With OP-290 and 100k Ω Loads**



INPUT VOLTAGE PROTECTION

The OP-290 uses a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors coupled with the protection resistors provides a large amount of input protection, allowing the inputs to be taken 20V beyond either supply without damaging the amplifier.

SINGLE-SUPPLY OUTPUT VOLTAGE RANGE

In single-supply operation the OP-290's input and output ranges include ground. This allows true "zero-in, zero-out" operation. The output stage provides an active pull-down to around 0.8V above ground. Below this level, a load resistance of up to 1M Ω to ground is required to pull the output down to zero.

In the region from ground to 0.8V the OP-290 has voltage gain equal to the data sheet specification. Output current source capability is maintained over the entire voltage range including ground.



OP-400

QUAD LOW-OFFSET, LOW-POWER OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Input Offset Voltage 150 μ V Max
- Low Offset Voltage Drift,
Over -55°C to +125°C 1.2 μ V/°C Max
- Low Supply Current (Per Amplifier) 725 μ A Max
- High Open-Loop Gain 5000V/mV Min
- Input Bias Current 3nA Max
- Low Noise Voltage Density 11nV/ $\sqrt{\text{Hz}}$ at 1kHz
- Stable With Large Capacitive Loads 10nF Typ
- Pin Compatible to OP-11, LM148, HA4741, RM4156, and
LT1014 With Improved Performance

ORDERING INFORMATION†

T _A = 25°C V _{OS} MAX (μ V)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC	
150	OP400AY*	—	OP400ATC/883	MIL
150	OP400EY	—	—	IND
230	OP400FY	—	—	IND
300	—	OP400GP	—	COM
300	—	OP400GS††	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

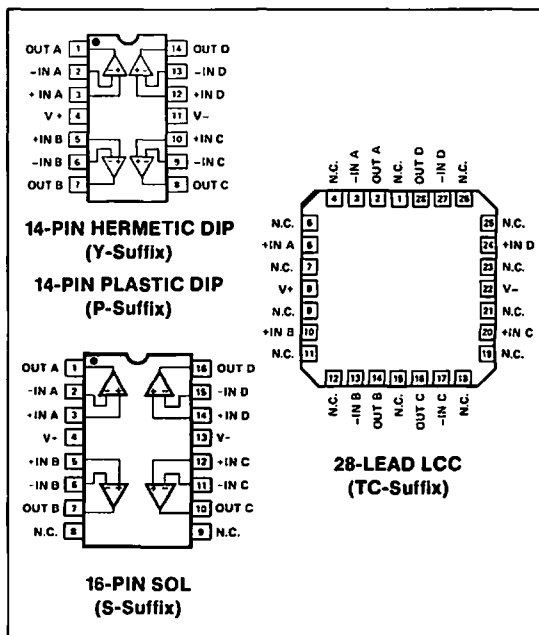
GENERAL DESCRIPTION

The OP-400 is the first monolithic quad operational amplifier that features OP-77 type performance. Precision performance no longer has to be sacrificed to obtain the space and

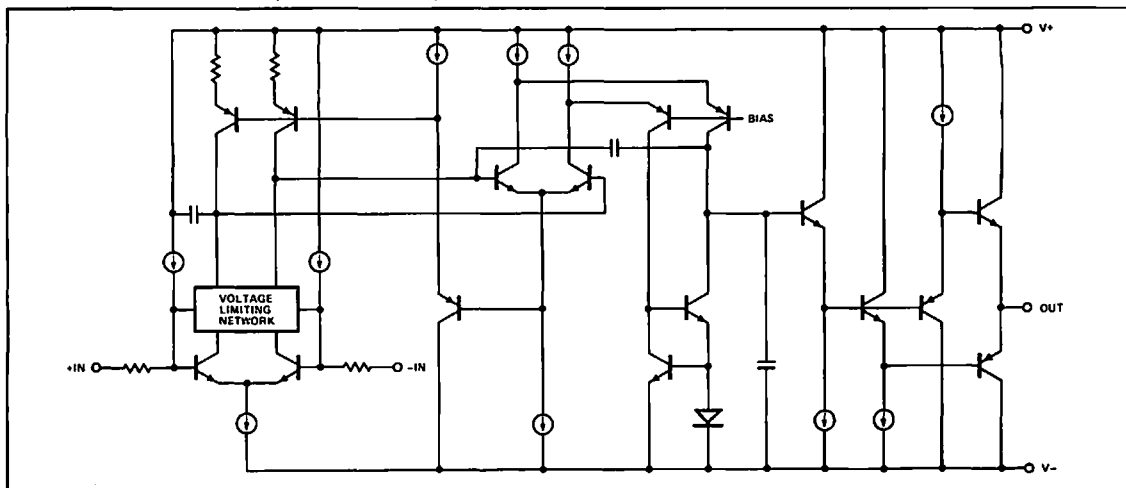
cost savings offered by quad amplifiers.

The OP-400 features an extremely low input offset voltage of less than 150 μ V with a drift of under 1.2 μ V/°C, guaranteed

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)





over the full military temperature range. Open-loop gain of the OP-400 is over 5,000,000 into a 10k Ω load; input bias current is under 3nA; CMR is above 120dB and PSRR below 1.8 μ V/V. On-chip zener-zap trimming is used to achieve the low input offset voltage of the OP-400 and eliminates the need for offset nulling. (The OP-400 conforms to the industry-standard quad pinout which does not have null terminals.)

The OP-400 features low power consumption, drawing less than 725 μ A per amplifier. The total current drawn by this quad amplifier is less than that of a single OP-07, yet the OP-400 offers significant improvements over this industry-standard op amp. Voltage noise density of the OP-400 is a low 11nV/ $\sqrt{\text{Hz}}$ at 10Hz which is half that of most competitive devices.

The OP-400 is pin compatible with the OP-11, LM148, HA4741, RM4156, and LT1014 operational amplifiers and can be used to upgrade systems using these devices. The OP-400 is an ideal choice for applications requiring multiple precision operational amplifiers and where low power consumption is critical.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	$\pm 20\text{V}$
Internal Power Dissipation (Note 1)	
Y-Package	800mW
P, TC-Package	500mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-400A/E			OP-400F			OP-400G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	40	150	—	60	230	—	80	300	μV
Long Term Input Voltage Stability			—	0.1	—	—	0.1	—	—	0.1	—	$\mu\text{V}/\text{mo}$
Input Offset Current	I_{OS}	$V_{CM} = 0\text{V}$	—	0.1	1.0	—	0.1	2.0	—	0.1	3.5	nA
Input Bias Current	I_B	$V_{CM} = 0\text{V}$	—	0.75	3.0	—	0.75	6.0	—	0.75	7.0	nA
Input Noise Voltage	$e_{n\text{ p-p}}$	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	—	0.5	—	$\mu\text{V}_{\text{p-p}}$
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	22	36	—	22	36	—	22	—	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 1000\text{Hz}$ (Note 1)	—	11	18	—	11	18	—	11	—	
Input Noise Current	$i_{n\text{ p-p}}$	0.1Hz to 10Hz	—	15	—	—	15	—	—	15	—	$\text{pA}_{\text{p-p}}$
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	0.6	—	—	0.6	—	—	0.6	—	$\text{pA}/\sqrt{\text{Hz}}$
Input Resistance Differential Mode	R_{IN}		—	10	—	—	10	—	—	10	—	M Ω
Input Resistance Common Mode	R_{INCM}		—	200	—	—	200	—	—	200	—	G Ω
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{V}$ $R_L = 10\text{k}\Omega$	5000	12000	—	3000	7000	—	3000	7000	—	V/mV
		$R_L = 2\text{k}\Omega$	2000	3500	—	1500	3000	—	1500	3000	—	

Differential Input Voltage	$\pm 30\text{V}$
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
P, TC, Y-Package	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_J)	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	
OP-400A	-55°C to $+125^\circ\text{C}$
OP-400E, OP-400F	-25°C to $+85^\circ\text{C}$
OP-400G	0°C to $+70^\circ\text{C}$

NOTES:

1. See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	70°C	10.0mW/ $^\circ\text{C}$
14-Pin Plastic DIP (P)	70°C	9.1mW/ $^\circ\text{C}$
28-Pin Lead LCC (TC)	100°C	10.0mW/ $^\circ\text{C}$

2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-400A/E			OP-400F			OP-400G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range	IVR	Note 3	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common Mode Rejection	CMR	$V_{CM} = \pm 12V$	120	140	—	115	140	—	110	135	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.1	1.8	—	0.1	3.2	—	0.2	5.6	$\mu V/V$
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	± 12 ± 11	± 12.6 ± 12.2	—	± 12 ± 11	± 12.6 ± 12.2	—	± 12 ± 11	± 12.6 ± 12.2	—	V
Supply Current Per Amplifier	I_{SY}	No Load	—	600	725	—	600	725	—	600	725	μA
Slew Rate	SR		0.1	0.15	—	0.1	0.15	—	0.1	0.15	—	V/ μs
Gain Bandwidth Product	GBWP	$A_V = +1$	—	500	—	—	500	—	—	500	—	kHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 2)	123	135	—	123	135	—	123	135	—	dB
Input Capacitance	C_{IN}		—	3.2	—	—	3.2	—	—	3.2	—	pF
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	10	—	—	10	—	—	10	—	nF

NOTES:

1. Sample tested.
2. Guaranteed but not 100% tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$ for OP-400A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-400A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	70	270	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	1.2	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.1	2.5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	1.3	5.0	nA
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	3000 1000	9000 2300	—	V/mV
Input Voltage Range	IVR	Note 1	± 12	± 12.5	—	V
Common Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.2	3.2	$\mu V/V$
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	± 12 ± 11	± 12.4 ± 12	—	V
Supply Current Per Amplifier	I_{SY}	No Load	—	600	775	μA
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	8	—	nF

NOTE:

1. Guaranteed by CMR test.



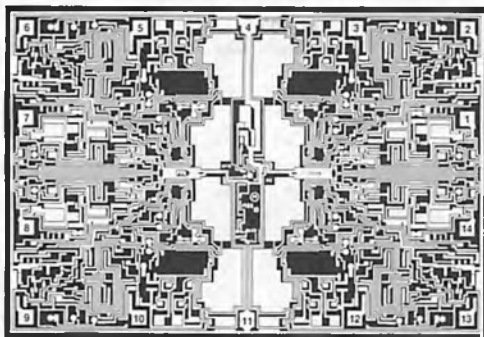
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-400E/F, $0^\circ C \leq T_A \leq +70^\circ C$ for OP-400G, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-400E			OP-400F			OP-400G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	60	220	—	80	350	—	110	400	μV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.3	1.2	—	0.3	2.0	—	0.6	2.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.1	2.5	—	0.1	3.5	—	0.2	6.0	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	0.9	5.0	—	0.9	10.0	—	1.0	12.0	nA
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$	3000	10000	—	2000	5000	—	2000	5000	—	V/mV
		$R_L = 2k\Omega$	1500	2700	—	1000	2000	—	1000	2000	—	
Input Voltage Range	IVR	Note 1	± 12	± 12.5	—	± 12	± 12.5	—	± 12	± 12.5	—	V
Common Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	135	—	110	135	—	105	130	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	0.15	3.2	—	0.15	5.6	—	0.3	10.0	$\mu V/V$
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 12	± 12.4	—	± 12	± 12.4	—	± 12	± 12.6	—	V
		$R_L = 2k\Omega$	± 11	± 12	—	± 11	± 12	—	± 11	± 12.2	—	
Supply Current Per Amplifier	I_{SY}	No Load	—	600	775	—	600	775	—	600	775	μA
Capacitive Load Stability		$A_V = +1$ No Oscillations	—	10	—	—	10	—	—	10	—	nF

NOTE:

1. Guaranteed by CMR test.

DICE CHARACTERISTICS



DIE SIZE 0.181×0.123 Inch, 22,263 sq. mils
(4.60×3.12 mm, 14.35 sq. mm)

- | | |
|----------|-----------|
| 1. OUT A | 8. OUT C |
| 2. -IN A | 9. -IN C |
| 3. +IN A | 10. +IN C |
| 4. V+ | 11. V- |
| 5. +IN B | 12. +IN D |
| 6. -IN B | 13. -IN D |
| 7. OUT B | 14. OUT D |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-400GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		230	μV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	2	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	6	nA MAX
Large Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	3000 1500	V/mV MIN
Input Voltage Range	IVR	Note 1	± 12	V MIN
Common Mode Rejection	CMR	$V_{CM} = \pm 12V$	115	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	3.2	$\mu V/V$ MAX
Output Voltage Swing	V_O	$R_L = 10k\Omega$ $R_L = 2k\Omega$	± 12 ± 11	V MIN
Supply Current Per Amplifier	I_{SY}	No Load	725	μA MAX

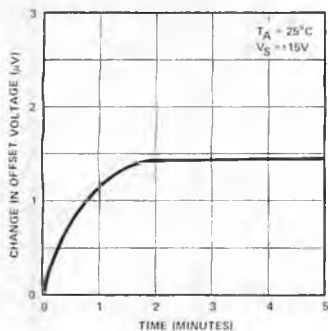
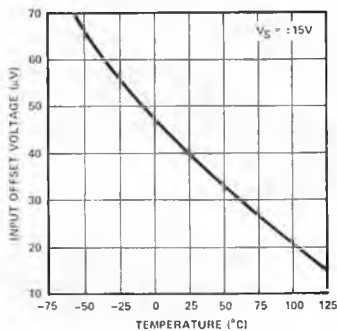
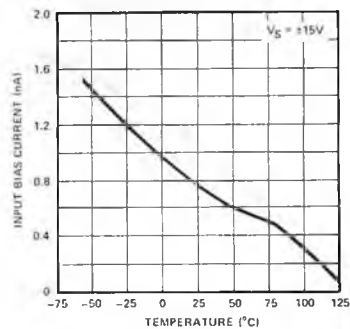
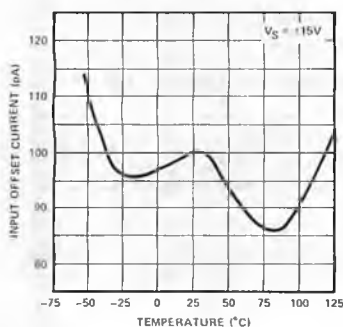
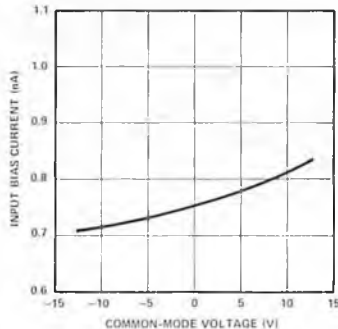
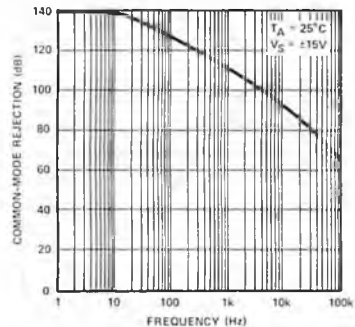
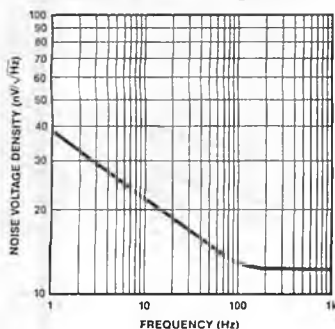
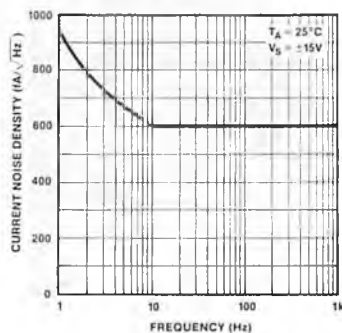
NOTES:

1. Guaranteed by CMR test.

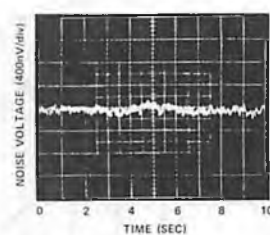
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

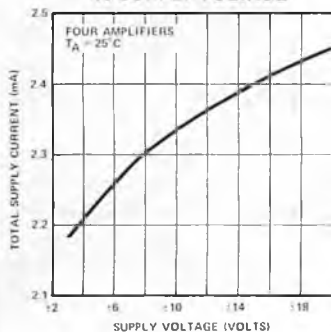
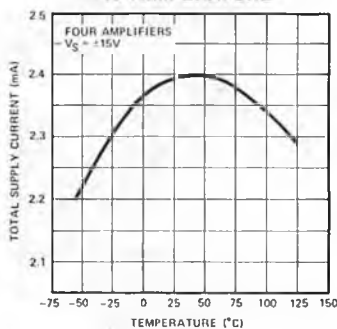
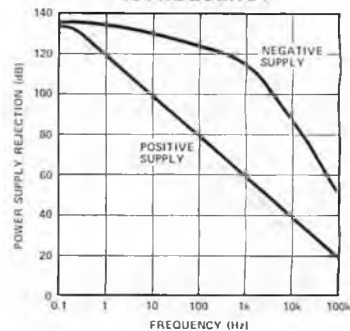
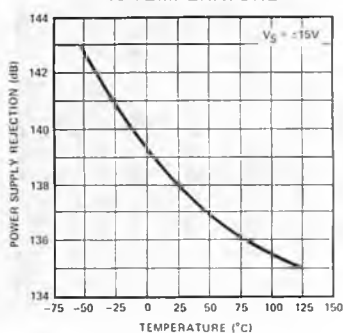
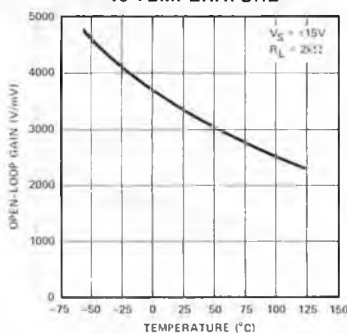
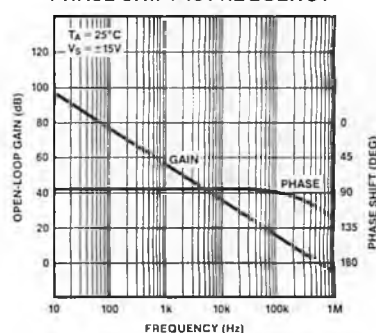
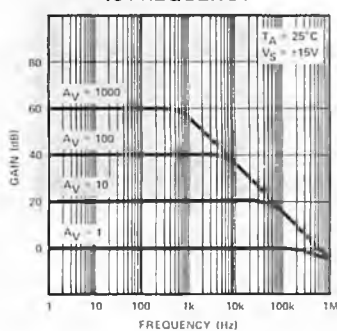
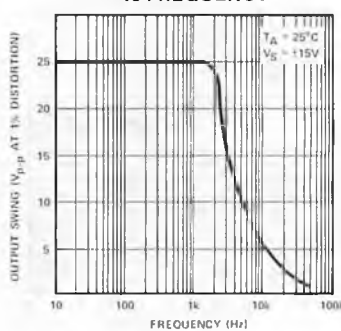
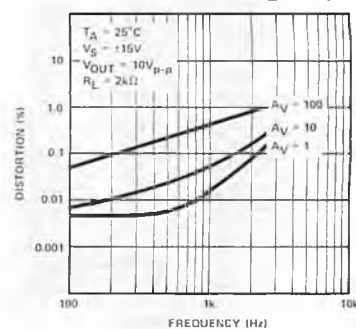
WARM-UP DRIFT


INPUT OFFSET VOLTAGE
vs TEMPERATURE

INPUT BIAS CURRENT
vs TEMPERATURE

INPUT OFFSET CURRENT
vs TEMPERATURE

INPUT BIAS CURRENT vs
COMMON-MODE VOLTAGE

COMMON-MODE REJECTION
vs FREQUENCY

NOISE VOLTAGE DENSITY
vs FREQUENCY

CURRENT NOISE DENSITY
vs FREQUENCY


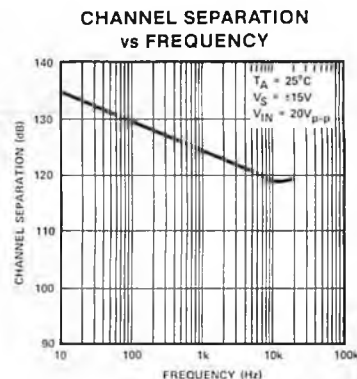
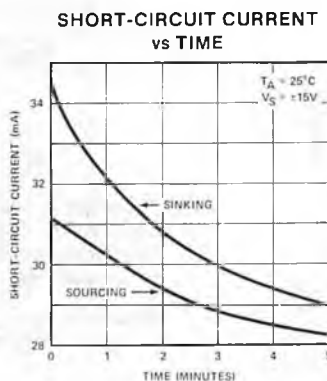
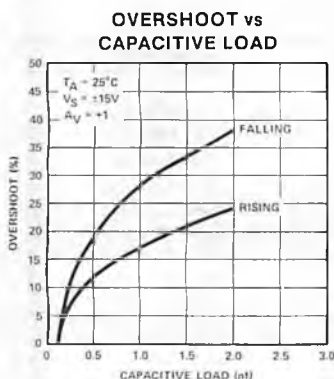
0.1Hz TO 10Hz NOISE



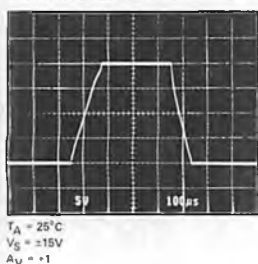
TYPICAL PERFORMANCE CHARACTERISTICS

TOTAL SUPPLY CURRENT
vs SUPPLY VOLTAGETOTAL SUPPLY CURRENT
vs TEMPERATUREPOWER SUPPLY REJECTION
vs FREQUENCYPOWER SUPPLY REJECTION
vs TEMPERATUREOPEN-LOOP GAIN
vs TEMPERATUREOPEN-LOOP GAIN AND
PHASE SHIFT vs FREQUENCYCLOSED-LOOP GAIN
vs FREQUENCYMAXIMUM OUTPUT SWING
vs FREQUENCYTOTAL HARMONIC
DISTORTION vs FREQUENCY

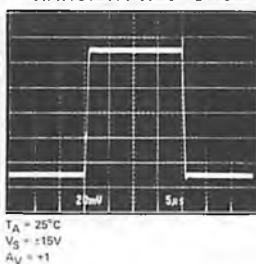
TYPICAL PERFORMANCE CHARACTERISTICS



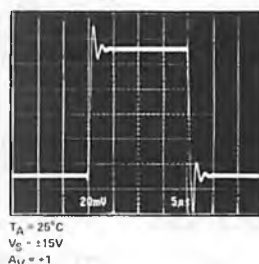
LARGE-SIGNAL TRANSIENT RESPONSE



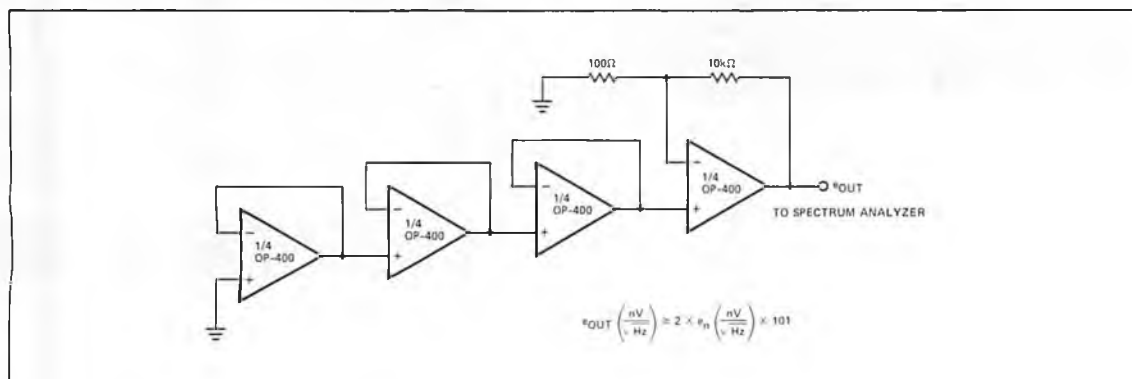
SMALL-SIGNAL TRANSIENT RESPONSE



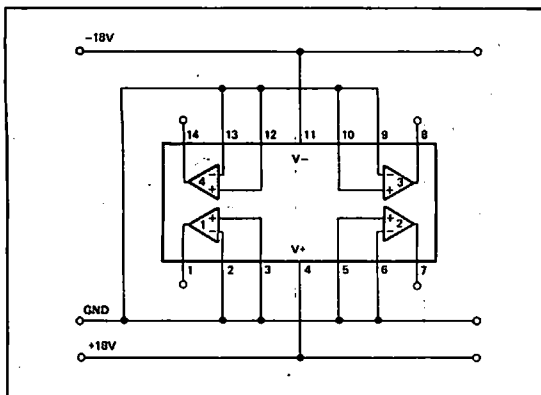
SMALL-SIGNAL TRANSIENT RESPONSE
 $C_{LOAD} = 1\text{nF}$



NOISE TEST SCHEMATIC



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The OP-400 is inherently stable at all gains and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply decoupling is highly recommended. Proper supply decoupling reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-400.

Total supply current can be reduced by connecting the inputs of an unused amplifier to V^- . This turns the amplifier off, lowering the total supply current.

APPLICATIONS

DUAL LOW-POWER INSTRUMENTATION AMPLIFIER

A dual instrumentation amplifier that consumes less than 33mW of power per channel is shown in Figure 1. The linearity of the instrumentation amplifier exceeds 16 bits in gains of 5 to 200 and is better than 14 bits in gains from 200 to 1000. CMRR is above 115dB (Gain = 1000). Offset voltage drift is typically $0.4\mu\text{V}/^\circ\text{C}$ over the military temperature range

which is comparable to the best monolithic instrumentation amplifiers. The bandwidth of the low-power instrumentation amplifier is a function of gain and is shown below:

GAIN	BANDWIDTH
5	150kHz
10	67kHz
100	7.5kHz
1000	500Hz

The output signal is specified with respect to the reference input, which is normally connected to analog ground. The reference input can be used to offset the output from -10V to $+10\text{V}$ if required.

FIGURE 1: Dual Low-Power Instrumentation Amplifier

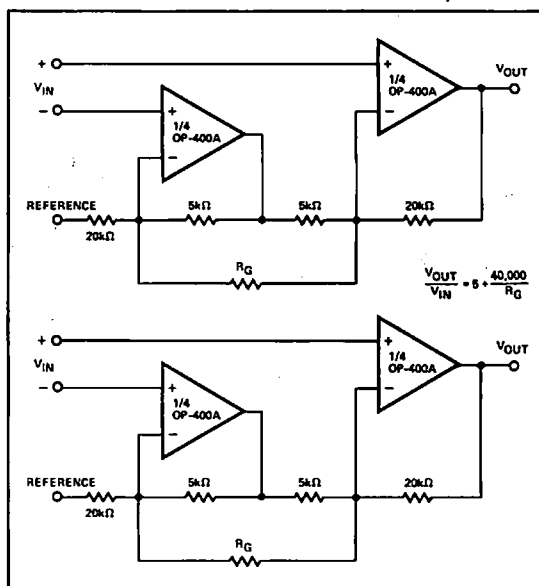
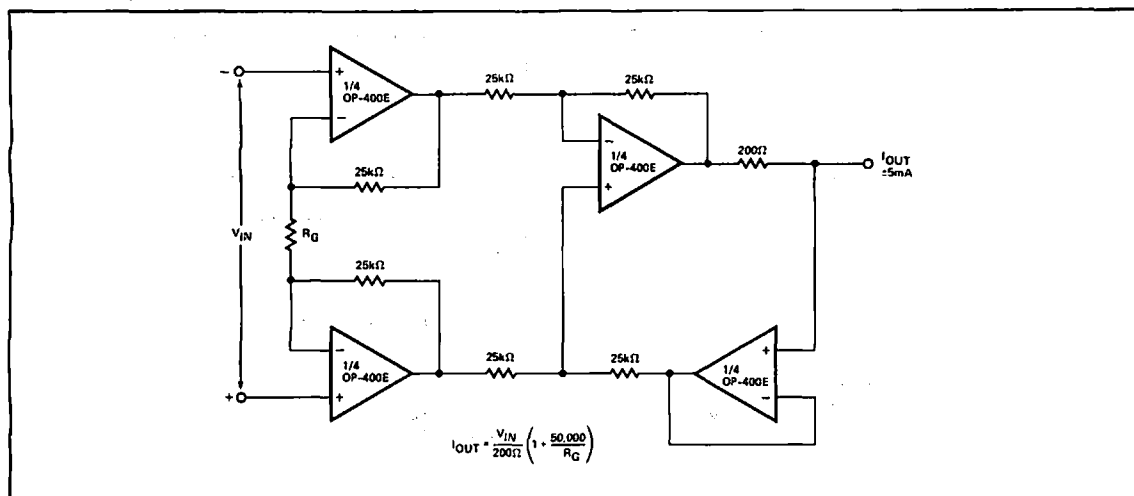


FIGURE 2: Bipolar Current Transmitter

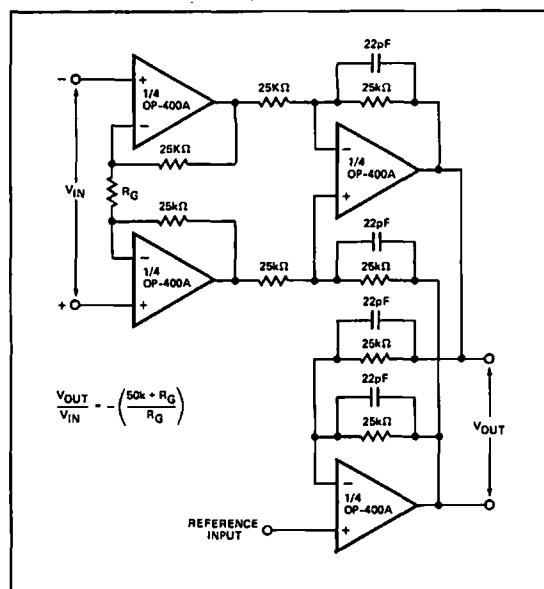
**BIPOLAR CURRENT TRANSMITTER**

In the circuit of Figure 2, which is an extension of the standard three op-amp instrumentation amplifier, the output current is proportional to the differential input voltage. Maximum output current is $\pm 5\text{mA}$ with voltage compliance equal to $\pm 10\text{V}$ when using $\pm 15\text{V}$ supplies. Output impedance of the current transmitter exceeds $3\text{M}\Omega$ and linearity is better than 16 bits with gain set for a full scale input of $\pm 100\mu\text{V}$.

DIFFERENTIAL OUTPUT INSTRUMENTATION AMPLIFIER

The output voltage swing of a single-ended instrumentation amplifier is limited by the supplies, normally at $\pm 15\text{V}$, to a maximum of 24V_{p-p} . The differential output instrumentation amplifier of Figure 3 can provide an output voltage swing of 48V_{p-p} when operated with $\pm 15\text{V}$ supplies. The extended output swing is due to the opposite polarity of the outputs. Both outputs will swing 24V_{p-p} but with opposite polarity, for a total output voltage swing of 48V_{p-p} . The reference input can be used to set a common-mode output voltage over the range $\pm 10\text{V}$. PSRR of the amplifier is less than $1\mu\text{V}/\text{V}$ with CMRR (Gain = 1000) better than 115dB. Offset voltage drift is typically $0.4\mu\text{V}/^\circ\text{C}$ over the military temperature range.

FIGURE 3: Differential Output Instrumentation Amplifier

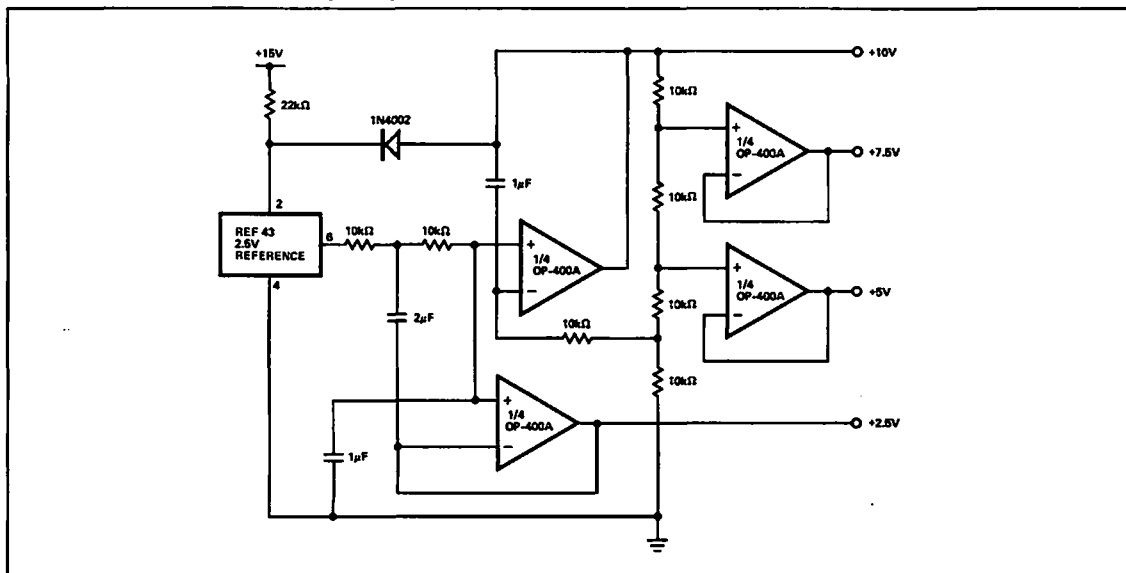


MULTIPLE OUTPUT TRACKING VOLTAGE REFERENCE

Figure 4 shows a circuit that provides outputs of 10V, 7.5V, 5V, and 2.5V for use as a system voltage reference. Maximum output current from each reference is 5mA with load regulation under $25\mu\text{V}/\text{mA}$. Line regulation is better than $15\mu\text{V}/\text{V}$

and output voltage drift is under $20\mu\text{V}/^\circ\text{C}$. Output voltage noise from 0.1Hz to 10Hz is typically $75\mu\text{V}_{\text{p-p}}$ from the 10V output and proportionately less from the 7.5V, 5V, and 2.5V outputs.

FIGURE 4: Multiple-Output Tracking Voltage Reference





Precision Monolithics Inc.

OP-420

QUAD MICROWATT OPERATIONAL AMPLIFIER

FEATURES

- Low Supply Current 200 μ A Max @ $V_S = +5V$
- Single-Supply Operation +5V to +30V
- Dual-Supply Operation $\pm 2.5V$ to $\pm 15V$
- Low Input Offset Voltage 500 μ V Typ
- Low Input Offset Voltage Drift 5 μ V/ $^{\circ}$ C Typ
- High Common-Mode Input Range ... V- to (V+ - 1.5V)
- High CMRR 100dB Typ
- High Open-Loop Gain 1100V/mV Typ
- LM 148 Pinout

ORDERING INFORMATION†

$T_A = 25^{\circ}\text{C}$ V_{OS} MAX (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC DIP 14-PIN	LCC	
2.5	OP420BY*	—	MIL
2.5	OP420FY	—	IND
4.0	OP420CY*	OP420CRC/883	MIL
4.0	OP420GY	—	IND
6.0	OP420HY	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

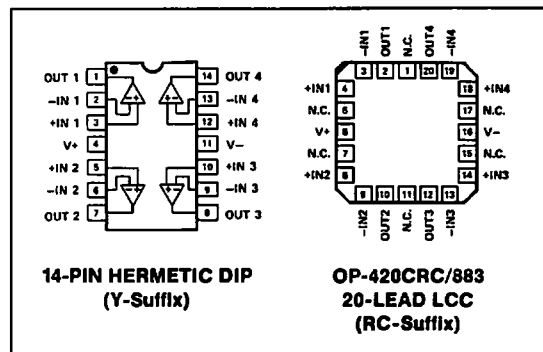
GENERAL DESCRIPTION

The OP-420 quad micropower operational amplifier is a single-chip quad patterned after the OP-20 precision micro-

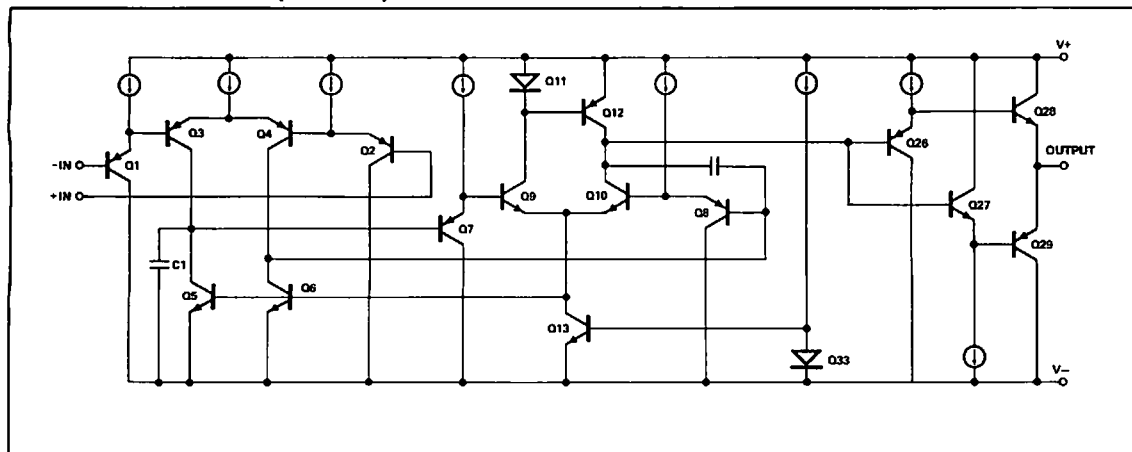
power single operational amplifier. A Darlington PNP input stage allows the input common-mode voltage to include V-. The wide input range combined with low power-supply drain ($\sim 40\mu\text{A}/\text{section}$ at 5V), provides a unique solution for designs requiring high functional density and portable operation. Applications include two-wire transmitters for process control loops, battery-operated remote-line filters, signal preconditioning amplifiers, and a variety of multiple-gain block arrays.

For micropower applications requiring offset nulling, see the OP-20, OP-21 and OP-22 data sheets.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/4 Shown)



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous (One Amplifier Only)
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	OP-420BY, OP-420CY, OP-420CRC .. -55°C to +125°C OP-420FY, OP-420GY .. -25°C to +85°C

OP-420HY	0°C to +70°C
DICE Junction Temperature (T _j)	-65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-420B OP-420F			OP-420C OP-420G			OP-420H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	V _S = ±2.5V to ±15V	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current (Note 1)	I _{OS}	V _S = ±2.5V to ±15V	—	0.5	1.5	—	0.8	2.5	—	1.2	6	nA
Input Bias Current (Note 1)	I _B	V _S = ±2.5V to ±15V	—	9	20	—	12	30	—	18	40	nA
Input Noise Voltage Density	e _n	f _O = 10Hz f _O = 100Hz	—	50	—	—	50	—	—	50	—	nV/√Hz
Input Noise Current Density	i _n	f _O = 10Hz f _O = 100Hz	—	0.12	—	—	0.12	—	—	0.12	—	pA/√Hz
Input Voltage Range	IVR	V ₊ = +5V, V ₋ = 0V V _S = ±15V	0/3.5 -15/13.5	—	—	0/3.5 -15/13.5	—	—	0/3.5 -15/13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	V ₊ = +5V, V ₋ = 0V 0V ≤ V _{CM} ≤ 3.5V	83	100	—	80	96	—	76	90	—	dB
		V _S = ±15V -15V ≤ V _{CM} ≤ 13.5V	83	100	—	80	96	—	76	90	—	
Power Supply Rejection Ratio	PSRR	V _S = ±2.5V to ±15V; & V ₋ = 0V, V ₊ = 5V to 30V	—	10	30	—	20	50	—	30	80	μV/V
Large-Signal Voltage Gain	A _{VO}	R _L = 25kΩ, V _O = ±10V	600	1100	—	400	900	—	200	800	—	V/mV
Slew Rate	SR		—	0.05	—	—	0.05	—	—	0.05	—	V/μs
Closed-Loop Bandwidth	BW	A _{VCL} = +1.0 R _L = 10kΩ	—	150	—	—	150	—	—	150	—	kHz
Output Voltage Swing	V _O	V ₊ = 5V, V ₋ = 0V, R _L = 10kΩ	0.7/4.1	—	—	0.8/4.0	—	—	0.9/3.8	—	—	V
		V _S = ±15V, R _L = 25kΩ	±14.0	—	—	±14.0	—	—	±13.8	—	—	
Supply Current (Four Amplifiers)	I _{SV}	V _S = ±2.5V, No Load	—	140	200	—	170	300	—	200	400	μA
		V _S = ±15V, No Load	—	330	360	—	360	460	—	390	600	

NOTE:1. I_B and I_{OS} are measured at V_{CM} = 0.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-420B and OP-420C, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-420F and OP-420G, and $0^\circ C \leq T_A \leq +70^\circ C$ for OP-420H, unless otherwise noted.

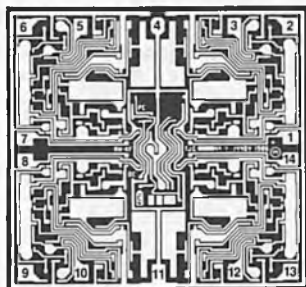
PARAMETER	SYMBOL	CONDITIONS	OP-420B OP-420F			OP-420C OP-420G			OP-420H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}	Unnullified	—	5	10	—	8	15	—	15	25	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3.5	—	—	5.5	—	—	7.5	mV
Input Offset Current (Note 2)	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	3	—	—	4	—	—	8	nA
Input Bias Current (Note 2)	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	—	30	—	—	40	—	—	60	nA
Input Voltage Range	IVR	$V+ = +5V$, $V- = 0V$	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	-15/13.2	—	—	-15/13.2	—	—	-15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	$V+ = +5V$, $V- = 0V$, $0V \leq V_{CM} \leq 3.2V$	76	96	—	73	92	—	73	86	—	dB
		$V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.2V$	76	96	—	73	92	—	73	86	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ and $V- = 0V$, $V+ = 5V$ to $30V$	—	15	50	—	25	80	—	40	100	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $R_L = 50k\Omega$, $V_O = \pm 10V$	300	800	—	200	650	—	100	400	—	V/mV
Output Voltage Swing	V_O	$V+ = 5V$, $V- = 0V$, $R_L = 20k\Omega$	0.9/3.9	—	—	1.0/3.8	—	—	1.1/3.6	—	—	V
		$V_S = \pm 15V$, $R_L = 50k\Omega$	± 13.8	—	—	± 13.8	—	—	± 13.6	—	—	
Supply Current (Four Amplifiers)	I_{SY}	$V_S = \pm 2.5V$, No Load	—	170	300	—	210	400	—	250	600	μA
		$V_S = \pm 15V$, No Load	—	390	500	—	420	640	—	500	800	

NOTES:

- Sample tested.
- I_B and I_{OS} are measured at $V_{CM} = 0$.



DICE CHARACTERISTICS



DIE SIZE 0.093×0.087 inch, 8091 sq. mils
(2.36×2.21 mm, 5.22 sq. mm)

1. OUTPUT 1
2. INVERTING INPUT 1
3. NONINVERTING INPUT 1
4. V_+
5. NONINVERTING INPUT 2
6. INVERTING INPUT 2
7. OUTPUT 2
8. OUTPUT 3
9. INVERTING INPUT 3
10. NONINVERTING INPUT 3
11. V_-
12. NONINVERTING INPUT 4
13. INVERTING INPUT 4
14. OUTPUT 4

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

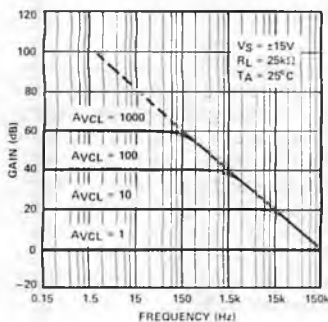
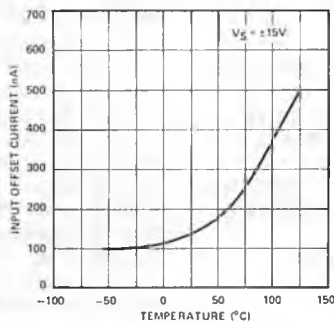
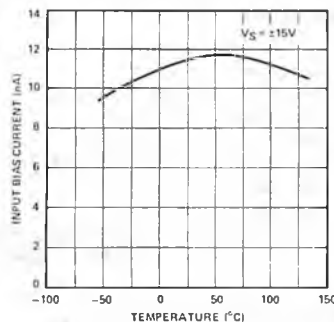
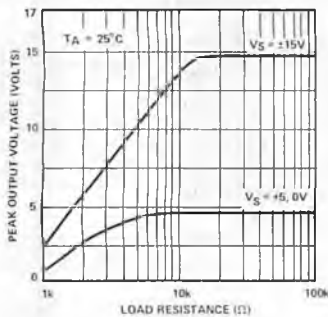
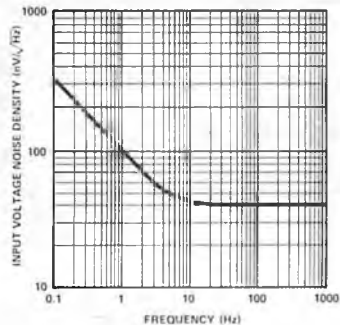
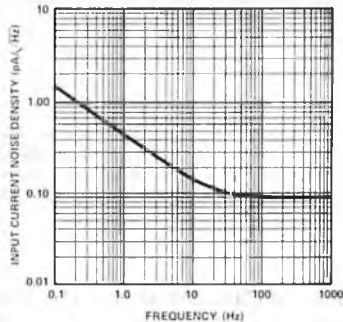
PARAMETER	SYMBOL	CONDITIONS	OP-420N LIMIT	OP-420G LIMIT	OP-420GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	2.5	4	6	mV MAX
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$, (Note 1)	1.5	2.5	6	nA MAX
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$, (Note 1)	20	30	40	nA MAX
Input Voltage Range	IVR		-15/13.5	-15/13.5	-15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_+ = +5V$, $V_- = 0V$	83	80	76	dB MIN
		$0V \leq V_{CM} \leq 3.5V$	83	80	76	
		$V_S = \pm 15V$, $-15V \leq V_{CM} \leq 13.5V$				
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$ $V_- = 0V$, $V_+ = +5V$ to $+30V$	30	50	80	$\mu V/V$ MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 25k\Omega$, $V_O = \pm 10V$	600	400	200	V/mV MIN
Output Voltage Swing	V_O	$V_+ = +5V$, $V_- = 0V$	0.7/4.1	0.8/4.0	0.9/3.8	V MAX
		$R_L = 10k\Omega$				
		$V_S = \pm 15V$ $R_L = 25k\Omega$	± 14.0	± 14.0	± 13.8	
Supply Current	I_{SY}	No Load, (Four Amplifiers)	360	460	600	μA MAX

NOTES:

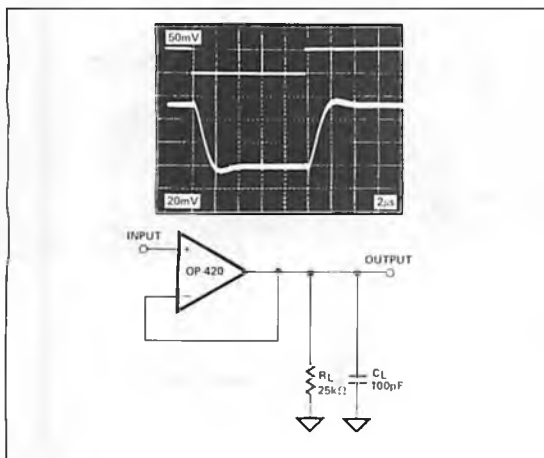
1. I_B and I_{OS} are measured at $V_{CM} = 0$.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

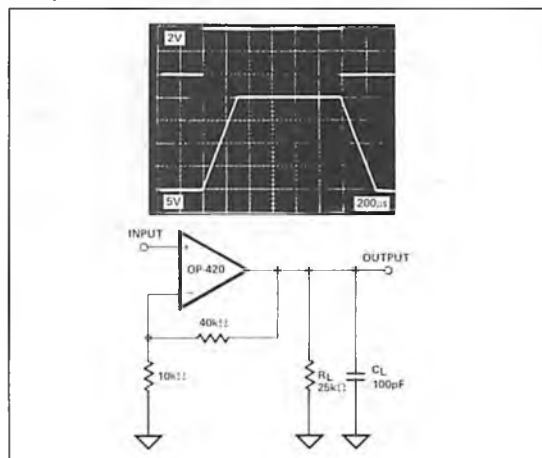
TYPICAL PERFORMANCE CHARACTERISTICS

CLOSED-LOOP GAIN
vs FREQUENCYINPUT OFFSET CURRENT
vs TEMPERATUREINPUT BIAS CURRENT
vs TEMPERATUREMAXIMUM OUTPUT VOLTAGE
vs LOAD RESISTANCEINPUT VOLTAGE NOISE
DENSITY (e_n) vs FREQUENCYINPUT CURRENT NOISE
DENSITY (i_n) vs FREQUENCY

SMALL-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE





OP-421

QUAD LOW-POWER OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Supply Current 1mA Max
- Slew Rate 0.25V/ μ s Min
- Single Supply Operation +5V to +30V
- Low Input Offset Voltage 500 μ V Typ
- Low Input Offset Voltage Drift 10 μ V/ $^{\circ}$ C Max
- High Common-Mode Input Range ... V- to V+ (-1.5V)
- High CMRR 100dB Typ
- High Open-Loop Gain 400V/mV Typ
- Single-Chip Monolithic Construction
- Pin Compatible With LM124, LM148, and OP-11

ORDERING INFORMATION†

$T_A = 25^{\circ}$ C V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
2.5	OP421BY*	MIL
2.5	OP421FY	IND
4	OP421CY*	MIL
4	OP421GY	IND
6	OP421HY	COM

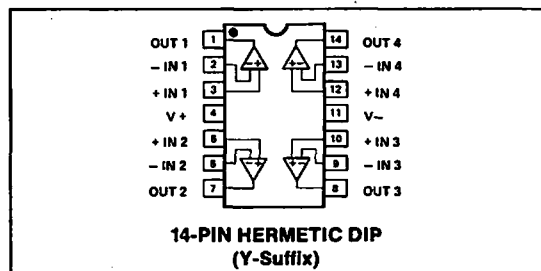
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

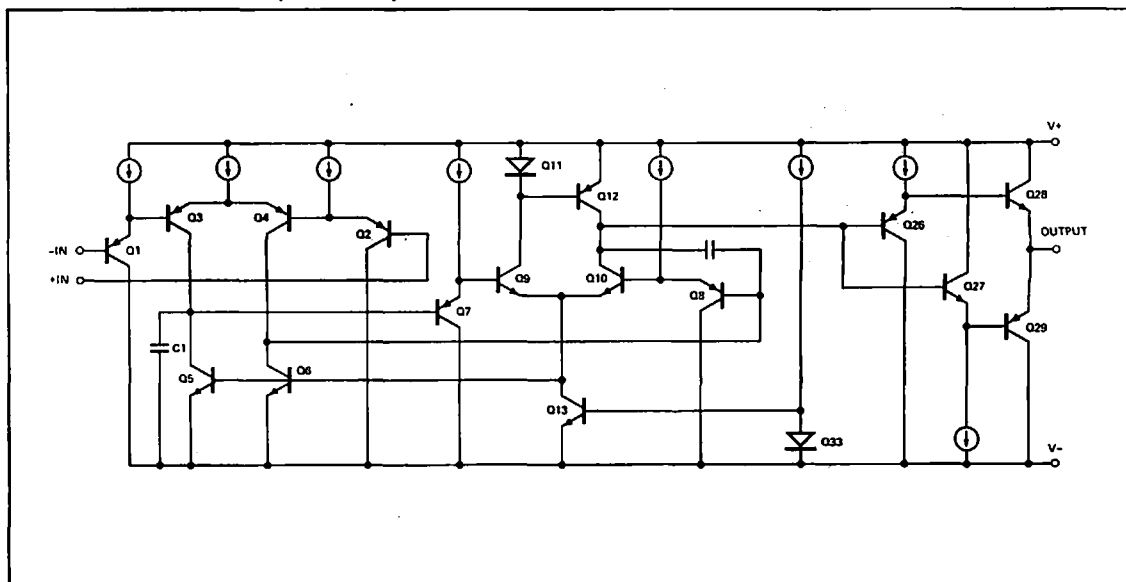
GENERAL DESCRIPTION

The OP-421 quad low-power operational amplifier is a single-chip quad patterned after the OP-21 single operational amplifier. The PNP input stage allows the input common-mode voltage to include V-. Featuring a low power-supply current (150 μ A/section typical at 5V), the OP-421 offers a unique solution for designs requiring a combination of high function density, wide bandwidth, and low-power operation. Applications for the OP-421 include low-power active filters, battery-operated remote line filters, and signal preconditioning amplifiers. In addition, the ever-present problem of crossover distortion in low-power devices is eliminated by a unique double-buffered output section.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/4 Shown)



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
(One Amplifier Only)	
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Operating Temperature Range	
OP-421BY, OP-421CY	-55°C to +125°C
OP-421FY, OP-421GY	-25°C to +85°C
OP-421HY	0°C to +70°C

DICE Junction Temperature (T_j) -65°C to +150°C**NOTES:**

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10.0mW/°C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421B OP-421F			OP-421C OP-421G			OP-421H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.5	2.5	—	1	4	—	2	6	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	0.6	5.0	—	2.0	10	—	5.0	20	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	20	50	—	50	80	—	100	150	nA
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 1)	—	20	40	—	20	40	—	20	40	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 1)	—	15	30	—	15	30	—	15	30	
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$ (Note 1)	—	0.3	0.6	—	0.3	0.6	—	0.3	0.6	$pA/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$ (Note 1)	—	0.2	0.4	—	0.2	0.4	—	0.2	0.4	
Input Voltage Range	IVR	$V^+ = +5V$, $V^- = 0V$	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
		$V_S = \pm 15V$	-15/13.5	—	—	-15/13.5	—	—	-15/13.5	—	—	
Common-Mode Rejection Ratio	CMRR	$V^+ = +5V$, $V^- = 0V$, $0V \leq V_{CM} \leq +3.5V$	83	100	—	80	96	—	76	90	—	dB
		$V_S = \pm 15V$, $-15V \leq V_{CM} \leq +13.5V$	83	100	—	80	96	—	76	90	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; & $V^- = 0V$, $V^+ = 5V$ to $30V$	—	10	30	—	20	50	—	30	80	$\mu V/V$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$	200	400	—	100	200	—	100	200	—	V/mV
Output Voltage Swing	V_O	$V^+ = 5V$, $V^- = 0V$ $R_L = 5k\Omega$	0.7/4.0	—	—	0.8/3.9	—	—	0.9/3.8	—	—	V
		$V_S = \pm 15V$, $R_L = 10k\Omega$	±14	—	—	±13.9	—	—	±13.8	—	—	
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$, $R_L = 10k\Omega$	1.0	1.9	—	1.0	1.9	—	1.0	1.9	—	MHz
Supply Current (Four Amplifiers)	I_{SV}	$V_S = \pm 2.5V$, No Load	—	0.6	1.0	—	0.7	1.5	—	0.9	2.0	mA
		$V_S = \pm 15V$, No Load	—	1.2	1.8	—	1.4	2.3	—	1.8	3.0	
Slew Rate	SR	(Note 1)	0.25	0.5	—	0.25	0.5	—	0.25	0.5	—	V/ μs
Channel Separation	CS	(Note 1)	100	120	—	100	120	—	100	120	—	dB

NOTES:

1. Sample tested.
2. Guaranteed by design.

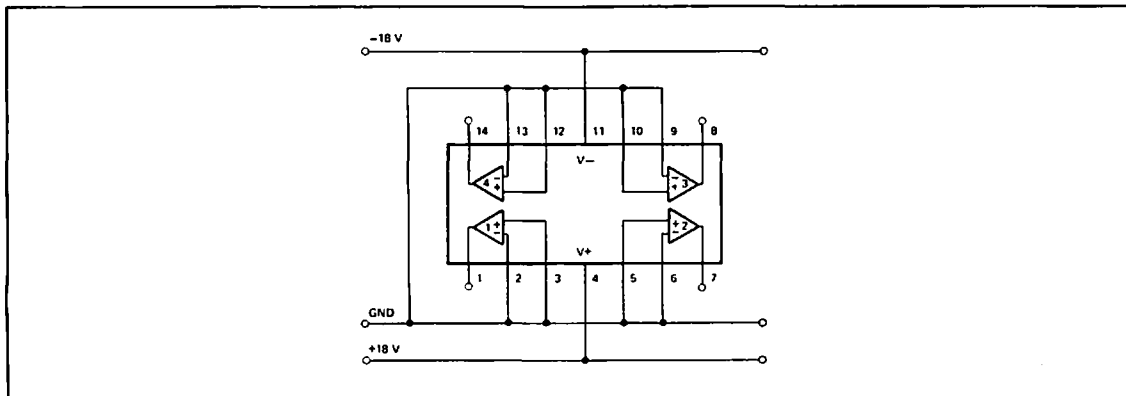


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for OP-421B and OP-421C, $-25^\circ C \leq T_A \leq +85^\circ C$ for OP-421F and OP-421G, and $0^\circ C \leq T_A \leq +70^\circ C$ for OP-421H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421B OP-421F			OP-421C OP-421G			OP-421H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Average Input Offset Voltage Drift (Note 1)	TCV_{OS}		—	5	10	—	8	15	—	10	15	$\mu V/^\circ C$
Input Offset Voltage	V_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1	3.5	—	1.8	5.5	—	3	7.5	mV
Input Offset Current	I_{OS}	$V_S = \pm 2.5V$ to $\pm 15V$	—	1.6	8	—	3.0	15	—	6.0	30	nA
Input Bias Current	I_B	$V_S = \pm 2.5V$ to $\pm 15V$	—	25	70	—	60	125	—	140	230	nA
Input Voltage Range	IVR	$V_+ = +5V, V_- = 0V$	0/3.2	—	—	0/3.2	—	—	0/3.2	—	—	V
		$V_S = \pm 15V$	-15/13.2	—	—	-15/13.2	—	—	-15/13.2	—	—	
Common-Mode Rejection Ratio	CMRR	$V_+ = +5V, V_- = 0V,$ $0V \leq V_{CM} \leq +3.2V$	78	96	—	74	94	—	73	86	—	dB
		$V_S = \pm 15V,$ $-15V \leq V_{CM} \leq +13.2V$	78	96	—	74	94	—	73	86	—	
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5V$ to $\pm 15V$; &	—	15	50	—	25	80	—	40	100	$\mu V/V$
		$V_- = 0V, V_+ = 5V$ to $30V$	—	15	50	—	25	80	—	40	100	
Large-Signal Voltage Gain	A_{VO}	$V_O = 10V$ $R_L = 20k\Omega$	100	200	—	50	100	—	50	100	—	V/mV
Output Voltage Swing	V_O	$V_+ = 5V, V_- = 0V$ $R_L = 10k\Omega$	0.8/3.9	—	—	0.9/3.8	—	—	1.0/3.7	—	—	V
		$V_S = \pm 15V,$ $R_L = 20k\Omega$	± 13.8	—	—	± 13.7	—	—	± 13.7	—	—	
Supply Current (Four Amplifiers)	I_{SV}	$V_S = \pm 2.5V$, No Load	—	1.2	1.5	—	1.5	2.0	—	2.0	3.0	mA
		$V_S = \pm 15V$, No Load	0.68	2.0	2.5	0.68	2.5	3.2	0.68	3.2	4.0	

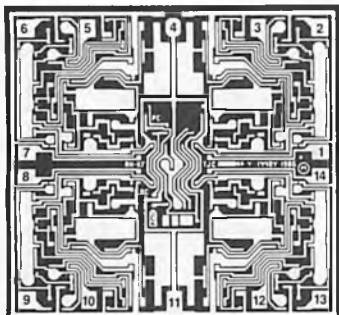
NOTE:

1. Sample tested.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.093 × 0.087 inch, 8091 sq. mils
(2.36 × 2.21 mm, 5.22 sq. mm)

1. OUTPUT 1
2. INVERTING INPUT 1
3. NONINVERTING INPUT 1
4. V⁺
5. NONINVERTING INPUT 2
6. INVERTING INPUT 2
7. OUTPUT 2
8. OUTPUT 3
9. INVERTING INPUT 3
10. NONINVERTING INPUT 3
11. V⁻
12. NONINVERTING INPUT 4
13. INVERTING INPUT 4
14. OUTPUT 4

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

5

OPERATIONAL AMPLIFIERS

WAFER TEST LIMITS at V_S = ±15V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421N LIMIT	OP-421G LIMIT	OP-421GR LIMIT	UNITS
Input Offset Voltage	V _{OS}	V _S = ±2.5V to ±15V	2.5	4	6	mV MAX
Input Offset Current	I _{OS}	V _S = ±2.5V to ±15V	5	10	20	nA MAX
Input Bias Current	I _B	V _S = ±2.5V to ±15V	50	80	150	nA MAX
Input Voltage Range	IVR		-15/13.5	-15/13.5	-15/13.5	V MIN
Common-Mode Rejection Ratio	CMRR	V ₊ = +5V, V ₋ = 0V 0V ≤ V _{CM} ≤ +3.5V V _S = ±15V, -15V ≤ V _{CM} ≤ +13.5V	83	80	76	dB MIN
Power Supply Rejection Ratio	PSRR	V _S = ±2.5V to ±15V; and V ₋ = 0V, V ₊ = +5V to 30V	30	50	80	μV/V MAX
Large-Signal Voltage Gain	A _{VO}	V _O = ±10V R _L = 20kΩ	200	200	100	V/mV MIN
Output Voltage Swing	V _O	V ₊ = +5V, V ₋ = 0V, R _L = 5kΩ V _S = ±15V, R _L = 10kΩ	0.7/4.0 ±14	0.8/3.9 ±13.9	0.9/3.8 ±13.8	V MIN
Supply Current (Four Amplifiers)	I _{SY}	V _S = ±2.5V, No Load V _S = ±15V, No Load	1.0 1.8	1.5 2.3	2.0 3.0	mA MAX

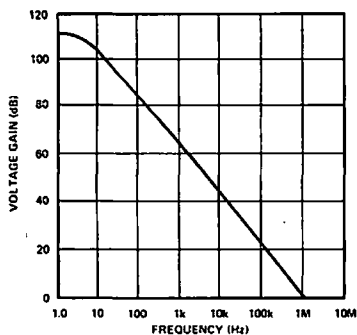
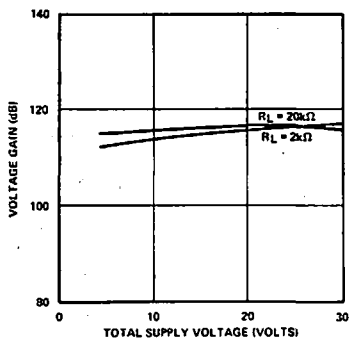
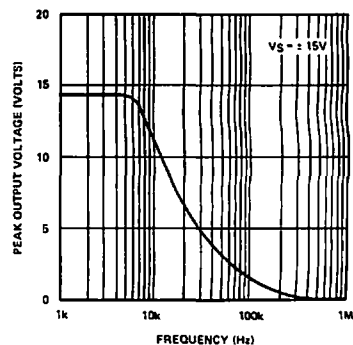
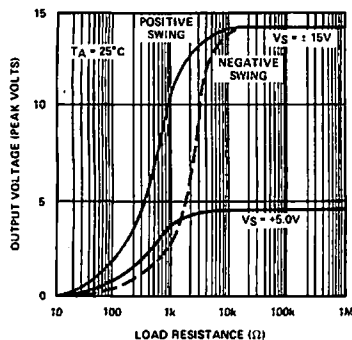
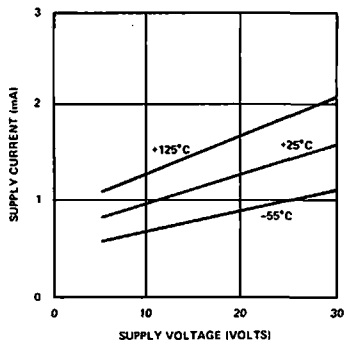
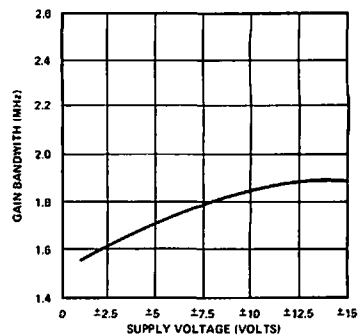
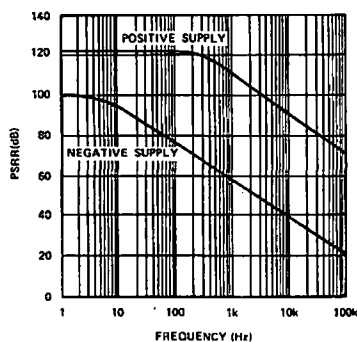
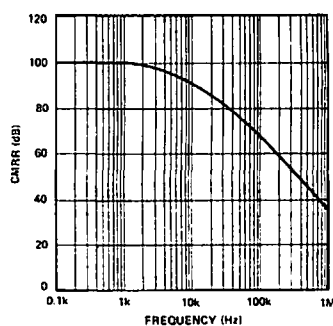
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

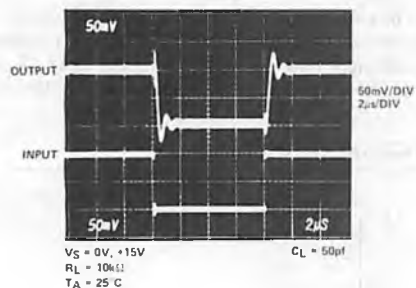
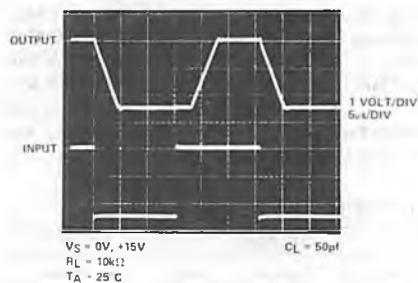
TYPICAL ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-421N TYPICAL	OP-421G TYPICAL	OP-421GR TYPICAL	UNITS
Input Noise Voltage Density	e _n	f _O = 10Hz f _O = 100Hz	20 15	20 15	20 15	nV/√Hz
Closed-Loop Bandwidth	BW	A _{VCL} = +10 R _L = 10kΩ	1.9	1.9	1.9	MHz
Slew Rate	SR		0.5	0.5	0.5	V/μs
Channel Separation	CS		120	120	120	dB

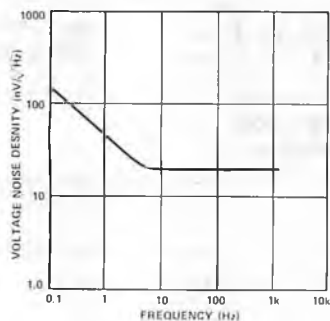
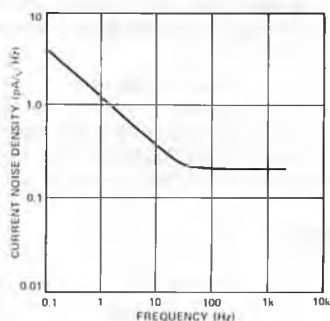
TYPICAL PERFORMANCE CHARACTERISTICS

OPEN-LOOP
FREQUENCY RESPONSEOPEN-LOOP GAIN
vs POWER SUPPLY VOLTAGEOUTPUT SWING
vs FREQUENCYOUTPUT SWING vs
OUTPUT LOADSUPPLY CURRENT vs
SUPPLY VOLTAGEGAIN BANDWIDTH vs
SUPPLY VOLTAGEPOWER SUPPLY REJECTION
RATIO vs FREQUENCYCOMMON-MODE REJECTION
RATIO vs FREQUENCY

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE FOLLOWER
SMALL-SIGNAL RESPONSEVOLTAGE FOLLOWER
LARGE-SIGNAL RESPONSE

NOISE CHARACTERISTICS

INPUT NOISE VOLTAGE
DENSITY vs FREQUENCYINPUT NOISE CURRENT
DENSITY vs FREQUENCY



OP-470

VERY LOW-NOISE QUAD
OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Very Low Noise $5\text{nV}/\sqrt{\text{Hz}}$ @ 1kHz Max
- Excellent Input Offset Voltage 0.4mV Max
- Low Offset Voltage Drift $2\mu\text{V}/^\circ\text{C}$ Max
- Very High Gain 1000V/mV Min
- Outstanding CMR 110dB Min
- Slew Rate $2\text{V}/\mu\text{s}$ Typ
- Gain-Bandwidth Product 6MHz Typ
- Industry Standard Quad Pinouts

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} MAX (μV)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC	PLASTIC	LCC	
400	OP470AY*	—	OP470ATC/883	MIL
400	OP470EY	—	—	IND
800	OP470FY	—	—	IND
1000	—	OP470GP	—	COM
1000	—	OP470GS††	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

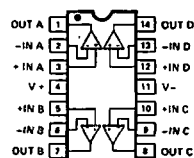
GENERAL DESCRIPTION

The OP-470 is a high-performance monolithic quad operational amplifier with exceptionally low voltage noise, $5\text{nV}/\sqrt{\text{Hz}}$ at 1kHz Max, offering comparable performance to PMI's industry standard OP-27.

The OP-470 features an input offset voltage below 0.4mV, excellent for a quad op amp, and an offset drift under $2\mu\text{V}/^\circ\text{C}$, guaranteed over the full military temperature range. Open-loop gain of the OP-470 is over 1,000,000 into a $10\text{k}\Omega$ load insuring excellent gain accuracy and linearity, even in high-

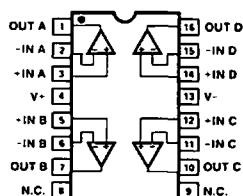
gain applications. Input bias current is under 25nA which reduces errors due to signal source resistance. The OP-470's CMR of over 110dB and PSRR of less than $1.8\mu\text{V}/\text{V}$ significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the quad OP-470 is half that of four OP-27s, a significant advantage for power con-

PIN CONNECTIONS

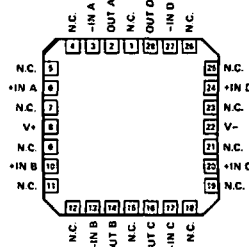


14-PIN HERMETIC DIP
(Y-Suffix)

14-PIN PLASTIC MINI-DIP
(P-Suffix)

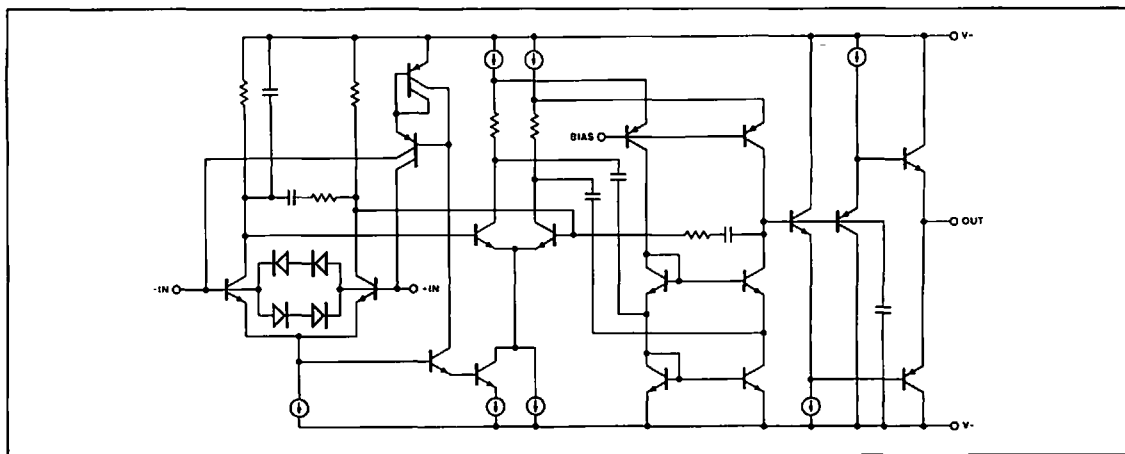


16-PIN SOL
(S-Suffix)



28-LEAD LCC
(TC-Suffix)

SIMPLIFIED SCHEMATIC





scious applications. The OP-470 is unity-gain stable with a gain-bandwidth product of 6MHz and a slew rate of 2V/ μ s.

The OP-470 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers, and low-noise active filters.

The OP-470 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, HA5104, and RM4156 quad op amps and can be used to upgrade systems using these devices.

For higher speed applications the OP-471, with a slew rate of 8V/ μ s, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	± 18 V
Internal Power Dissipation (Note 1)	
Y-Package	800mW
P, TC-Package	500mW
Differential Input Voltage (Note 3)	± 1.0 V
Differential Input Current (Note 3)	± 25 mA
Input Voltage	Supply Voltage

Output Short-Circuit Duration Continuous
Storage Temperature Range

P, TC, Y-Package -65°C to $+150^{\circ}\text{C}$

Lead Temperature Range (Soldering, 60 sec) 300°C

DICE Junction Temperature (T_J) -65°C to $+150^{\circ}\text{C}$

Operating Temperature Range

OP-470A -55°C to $+125^{\circ}\text{C}$

OP-470E, OP-470F -25°C to $+85^{\circ}\text{C}$

OP-470G 0°C to $+70^{\circ}\text{C}$

NOTES:

1. See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	70°C	$10.0\text{mW}/^{\circ}\text{C}$
14-Pin Plastic DIP	70°C	$15\text{mW}/^{\circ}\text{C}$
28-Lead LCC (TC)	100°C	$10.0\text{mW}/^{\circ}\text{C}$

2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

3. The OP-470's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds ± 1.0 V, the input current should be limited to ± 25 mA.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15$ V, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470A/E			OP-470F			OP-470G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.1	0.4	—	0.2	0.8	—	0.4	1.0	mV
Input Offset Current	I_{OS}	$V_{CM} = 0$ V	—	3	10	—	6	20	—	12	30	nA
Input Bias Current	I_B	$V_{CM} = 0$ V	—	6	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	80	200	—	80	200	—	80	200	nV _{p-p}
Input Noise Voltage Density	e_n	$f_O = 10$ Hz	—	3.8	6.5	—	3.8	6.5	—	3.8	6.5	nV/ $\sqrt{\text{Hz}}$
		$f_O = 100$ Hz	—	3.3	5.5	—	3.3	5.5	—	3.3	5.5	
		$f_O = 1$ kHz (Note 2)	—	3.2	5.0	—	3.2	5.0	—	3.2	5.0	
Input Noise Current Density	i_n	$f_O = 10$ Hz	—	1.7	—	—	1.7	—	—	1.7	—	pA/ $\sqrt{\text{Hz}}$
		$f_O = 100$ Hz	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1$ kHz	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10$ V										V/mV
		$R_L = 10$ k Ω	1000	2300	—	800	1700	—	800	1700	—	
		$R_L = 2$ k Ω	500	1200	—	400	900	—	400	900	—	
Input Voltage Range	IVR	(Note 3)	± 11	± 12	—	± 11	± 12	—	± 11	± 12	—	V
Output Voltage Swing	V_O	$R_L \geq 2$ k Ω	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection CMR		$V_{CM} = \pm 11$ V	110	125	—	100	120	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5$ V to ± 18 V	—	0.56	1.8	—	1.0	5.6	—	1.0	5.6	μ V/V
Slew Rate	SR		1.4	2	—	1.4	2	—	1.4	2	—	V/ μ s

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-470A/E			OP-470F			OP-470G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9	11	—	9	11	—	9	11	mA
Gain Bandwidth Product	GBW	$A_V = +10$	—	6	—	—	6	—	—	6	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	155	—	125	155	—	125	155	—	dB
Input Capacitance	C_{IN}		—	2	—	—	2	—	—	2	—	pF
Input Resistance Differential-Mode	R_{IN}		—	0.4	—	—	0.4	—	—	0.4	—	M Ω
Input Resistance Common-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	G Ω
Settling Time	t_s	$A_V = +1$	—	5.5	—	—	5.5	—	—	5.5	—	μs
		to 0.1% to 0.01%	—	6.0	—	—	6.0	—	—	6.0	—	

NOTES:

1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$ for OP-470A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-470A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.14	0.6	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	5	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	15	50	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$ $R_L = 10k\Omega$	750	1600	—	V/mV
		$R_L = 2k\Omega$	400	800	—	
Input Voltage Range	IVR	(Note 1)	± 11	± 12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	1.0	5.6	$\mu V/V$
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	mA

NOTE:

1. Guaranteed by CMR test.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$ for OP-470E/F, $0^\circ C \leq T_A \leq 70^\circ C$ for OP-470G, unless otherwise noted.

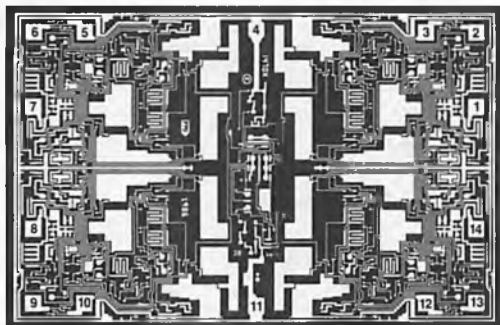
PARAMETER	SYMBOL	CONDITIONS	OP-470E			OP-470F			OP-470G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.12	0.5	—	0.24	1.0	—	0.5	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.4	2	—	0.6	4	—	2	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	4	20	—	7	40	—	20	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	11	50	—	20	70	—	40	75	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$										
		$R_L = 10k\Omega$	800	1800	—	800	1400	—	600	1500	—	V/mV
		$R_L = 2k\Omega$	400	900	—	300	700	—	300	800	—	
Input Voltage Range	IVR	(Note 1)	± 11	± 12	—	± 11	± 12	—	± 11	± 12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	120	—	90	115	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	0.7	5.6	—	1.8	10	—	1.8	10	$\mu V/V$
Supply Current (All Amplifiers)	I_{SV}	No Load	—	9.2	11	—	9.2	11	—	9.3	11	mA

NOTE:

1. Guaranteed by CMR test.



DICE CHARACTERISTICS



DIE SIZE 0.163×0.106 inch, 17,278 sq. mils
(4.14×2.69 mm, 11.14 sq. mm)

1. OUT A
2. -IN A
3. +IN A
4. V+
5. -IN B
6. -IN B
7. OUT B
8. OUT C
9. -IN C
10. +IN C
11. V-
12. +IN D
13. -IN D
14. OUT D

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

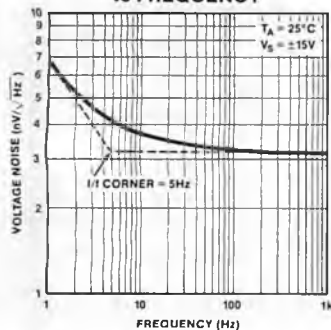
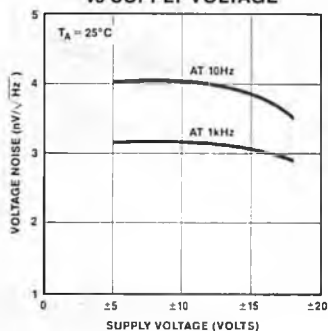
PARAMETER	SYMBOL	CONDITIONS	OP-470GBC	
			LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.8	mV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	20	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	50	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$	800	V/mV MIN
		$R_L = 10k\Omega$ $R_L = 2k\Omega$	400	
Input Voltage Range	IVR	(Note 1)	± 11	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	V MIN
Common Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	5.6	$\mu V/V$ MAX
Slew Rate	SR		1.4	V/ μs MIN
Supply Current (All Amplifiers)	I_{SY}	No Load	11	mA MAX

NOTE:

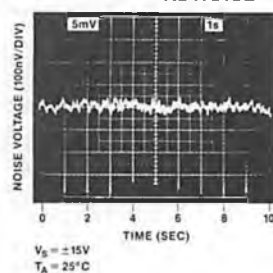
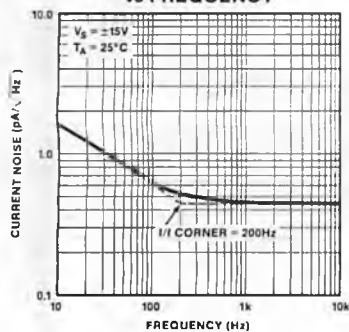
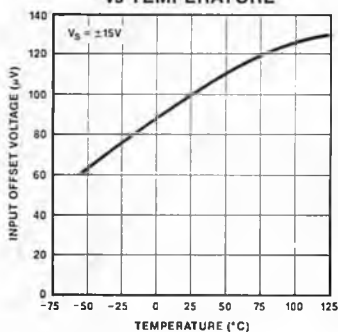
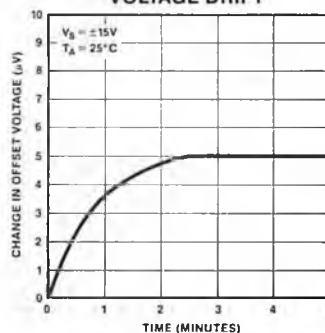
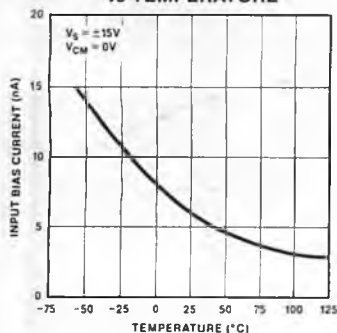
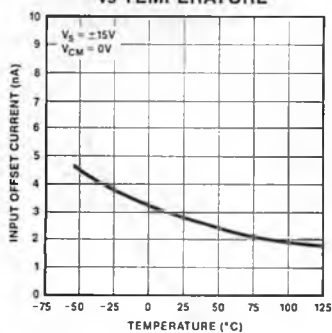
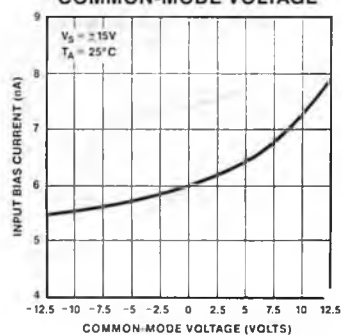
1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

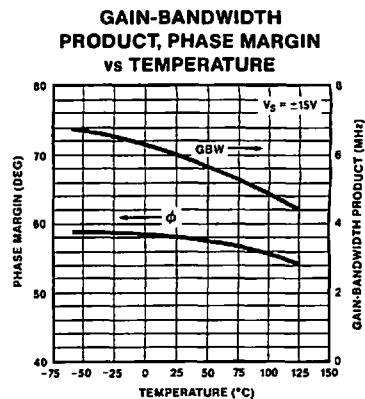
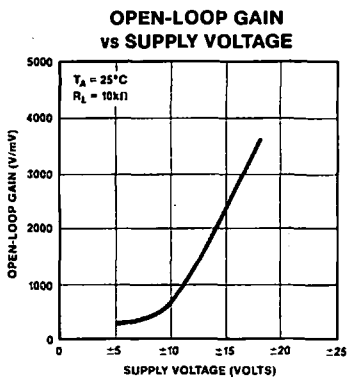
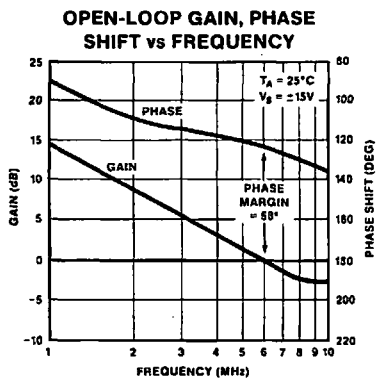
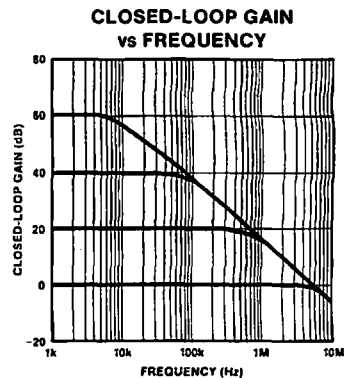
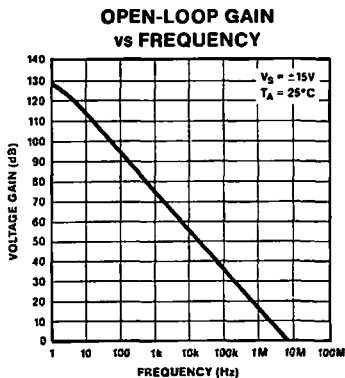
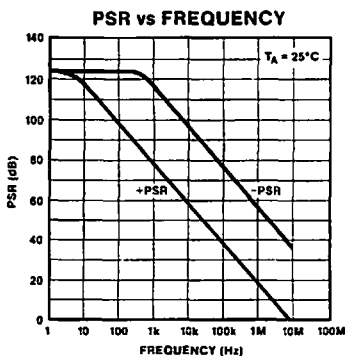
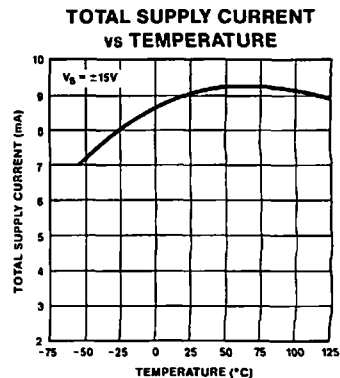
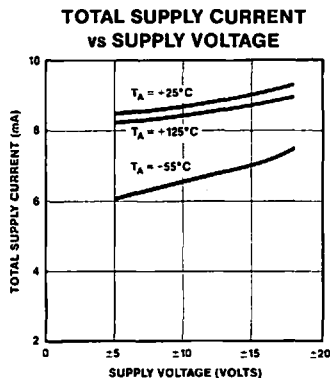
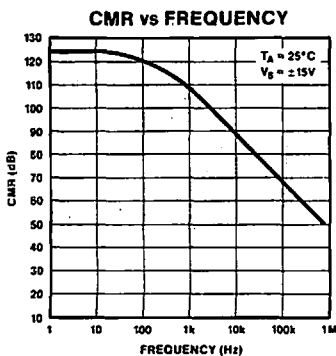
TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE DENSITY
vs FREQUENCYVOLTAGE NOISE DENSITY
vs SUPPLY VOLTAGE

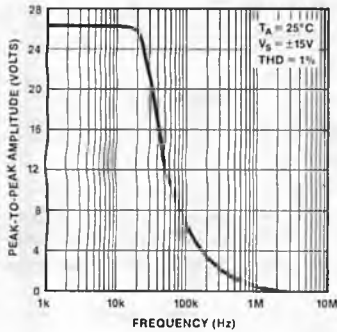
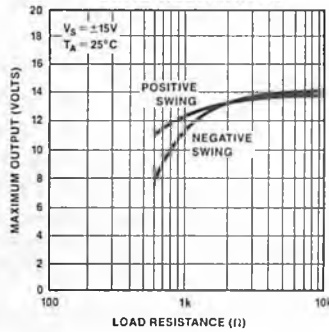
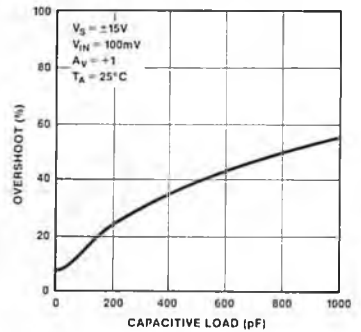
0.1Hz TO 10Hz NOISE

CURRENT NOISE DENSITY
vs FREQUENCYINPUT OFFSET VOLTAGE
vs TEMPERATUREWARM-UP OFFSET
VOLTAGE DRIFTINPUT BIAS CURRENT
vs TEMPERATUREINPUT OFFSET CURRENT
vs TEMPERATUREINPUT BIAS CURRENT vs
COMMON-MODE VOLTAGE

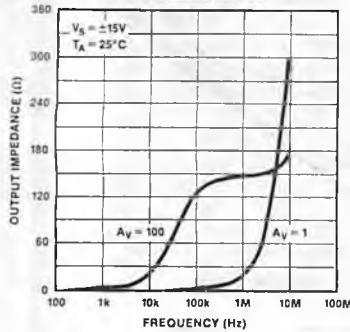
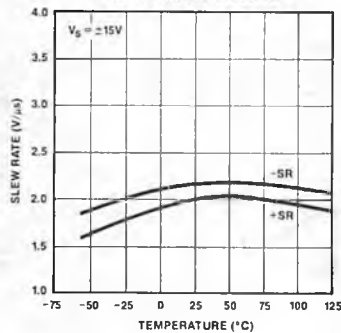
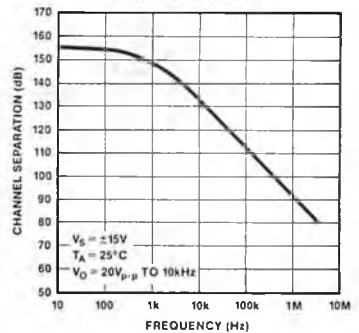
TYPICAL PERFORMANCE CHARACTERISTICS



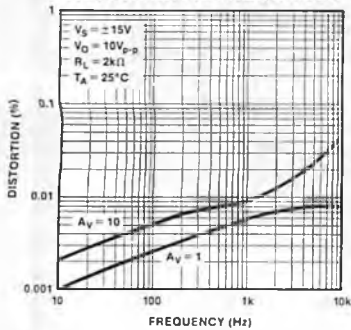
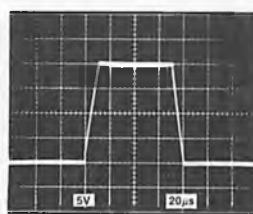
TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM OUTPUT SWING
vs FREQUENCY

MAXIMUM OUTPUT
VOLTAGE vs
LOAD RESISTANCE

SMALL-SIGNAL
OVERSHOOT vs
CAPACITIVE LOAD


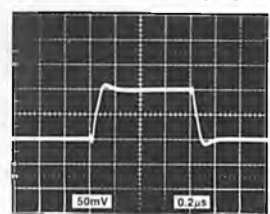
5

OUTPUT IMPEDANCE
vs FREQUENCY

SLEW RATE
vs TEMPERATURE

CHANNEL SEPARATION
vs FREQUENCY


OPERATIONAL AMPLIFIERS

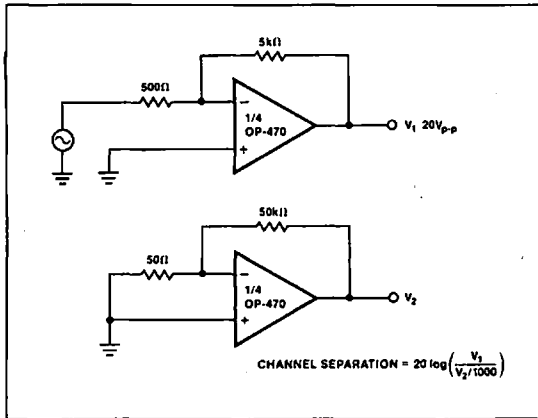
TOTAL HARMONIC
DISTORTION vs FREQUENCY

LARGE-SIGNAL
TRANSIENT RESPONSE

$T_A = 25^\circ\text{C}$
 $V_S = \pm 15\text{V}$
 $A_V = +1$

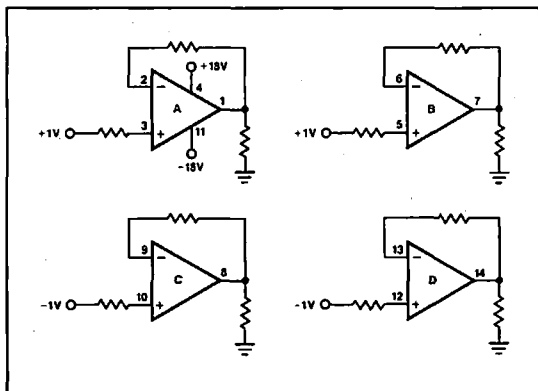
SMALL-SIGNAL
TRANSIENT RESPONSE

$T_A = 25^\circ\text{C}$
 $V_S = \pm 15\text{V}$
 $A_V = +1$

CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP-470 is a very low-noise quad op amp, exhibiting a typical voltage noise of only $3.2\text{nV}/\sqrt{\text{Hz}}$ @ 1kHz. The exceptionally low noise characteristics of the OP-470 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-470 is gained at the expense of current noise performance, which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_r).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calculated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_r)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_r = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1\text{k}\Omega$ the total noise is dominated by the voltage noise of the OP-470. As R_S rises above

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

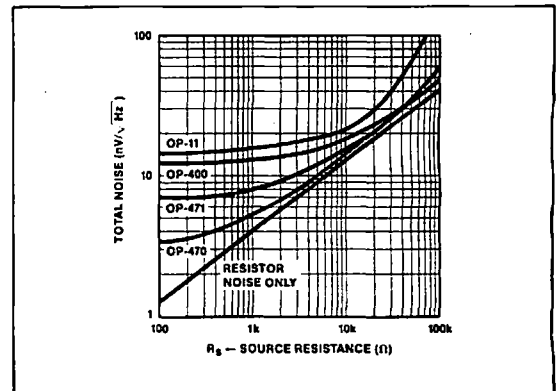
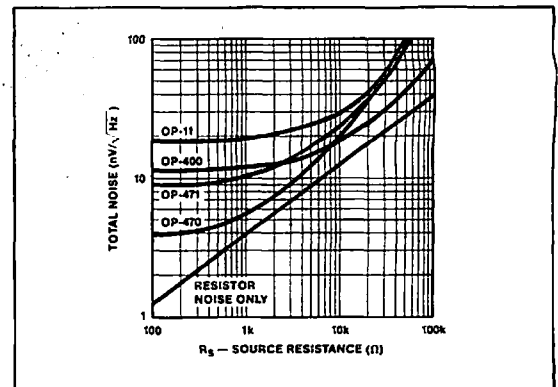


FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz



1k Ω , total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-470. When R_S exceeds 20k Ω , current noise of the OP-470 becomes the major contributor to total noise.

Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz. Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-470 dominates the total noise when $R_S > 5k\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-400, with lower current noise than the OP-470, will provide lower total noise.

Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S ,

FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)

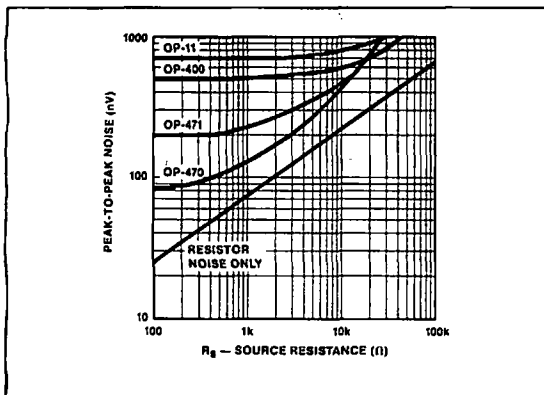
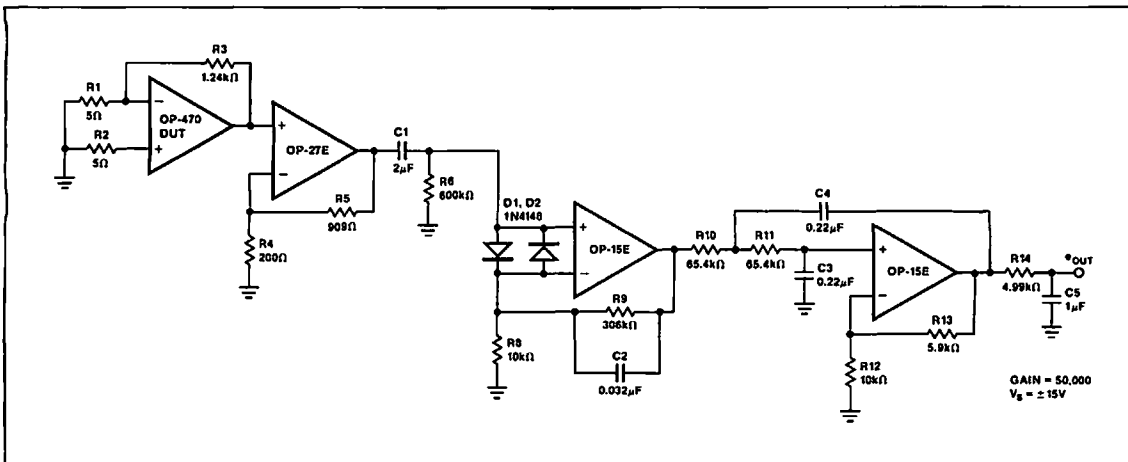


FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)



the voltage noise of the OP-470 is the major contributor to peak-to-peak noise with current noise the major contributor as R_S increases. The crossover point between the OP-470 and the OP-400 for peak-to-peak noise is at $R_S = 17k\Omega$.

The OP-471 is a higher speed version of the OP-470, with a slew rate of 8V/ μ s. Noise of the OP-471 is only slightly higher than the OP-470. Like the OP-470, the OP-471 is unity-gain stable.

For reference, typical source resistances of some signal sources are listed in Table I.

TABLE I

DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	<500 Ω	Typically used in low-frequency applications.
Magnetic tapehead	<1500 Ω	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-470 I_B can be neglected.
Magnetic phonograph cartridges	<1500 Ω	Similar need for low I_B in direct coupled applications. OP-470 will not introduce any self-magnetization problem.
Linear variable differential transformer	<1500 Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz.

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

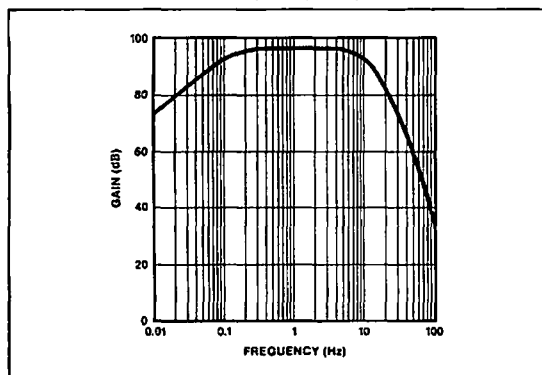
NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 200nV peak-to-peak

noise specification of the OP-470 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes $5\mu\text{V}$ due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

FIGURE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response



4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the $1/f$ corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced via the amplifier supply pins.

NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101 \left(\sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2} \right)$$

The OP-470 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101 \left(\sqrt{4e_n^2} \right) = 101 (2e_n)$$

FIGURE 6: Noise Voltage Density Test Circuit

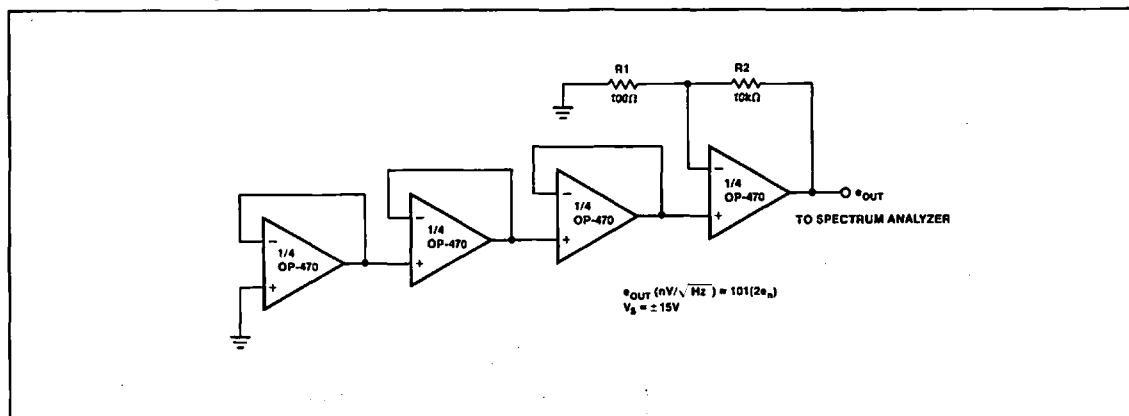
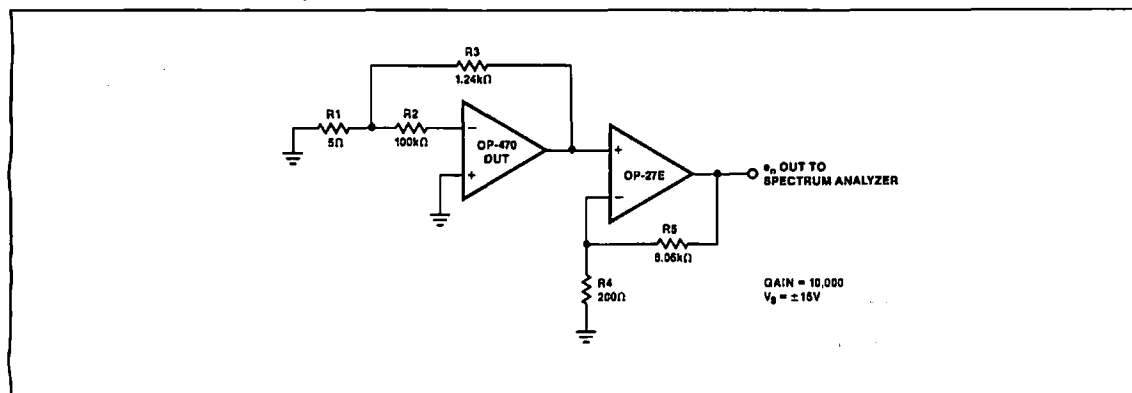


FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000

R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-470 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-470.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for a load capacitance of up to 1000pF when used with the OP-470.

In applications where the OP-470's inverting or noninverting inputs are driven by a low source impedance (under 100Ω) or connected to ground, if V+ is applied before V-, or when V- is disconnected, excessive parasitic currents will flow. Most

FIGURE 8: Driving Large Capacitive Loads

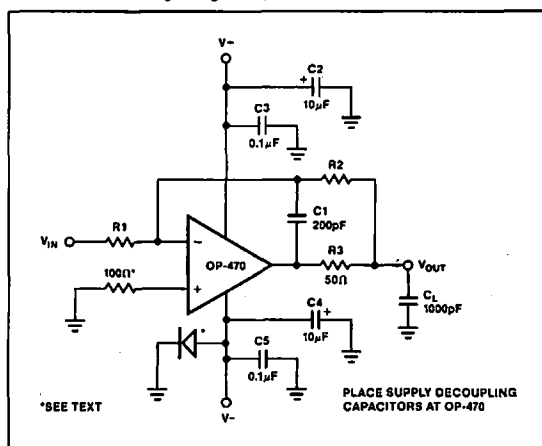
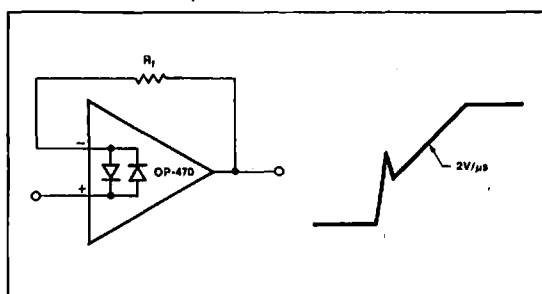


FIGURE 9: Pulsed Operation



applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100Ω in series with all inputs (Figure 8) will limit the parasitic currents to a safe level if V_- is disconnected. It should be noted that any source resistance, even 100Ω , adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V_- pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

UNITY-GAIN BUFFER APPLICATIONS

When $R_i \leq 100\Omega$ and the input is driven with a fast, large-signal pulse ($>1V$), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_i \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at $10V$); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_i > 3k\Omega$, a pole created by R_i and the amplifier's input capacitance ($2pF$) creates additional phase shift and reduces phase margin. A small capacitor (20 to $50pF$) in parallel with R_i helps eliminate this problem.

APPLICATIONS

LOW NOISE AMPLIFIER

A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 10. Amplifier noise, depicted in Figure 11, is around $2nV/\sqrt{Hz}$ @ $1kHz$ (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 1000. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω . The amplifier is stable with a $10nF$ capacitive load and can supply up to $30mA$ of output drive.

DIGITAL PANNING CONTROL

Figure 12 uses a DAC-8408, a quad 8-bit DAC, to pan a signal between two channels. The complementary DAC current outputs of two of the DAC-8408's four DACs drive current-to-voltage converters built from a single quad OP-470. The amplifiers have complementary outputs with the amplitudes dependent upon the digital code applied to the DAC. Figure 13 shows the complementary outputs for a $1kHz$ input signal and digital ramp applied to the DAC digital inputs. Distortion of the digital panning control is less than 0.01% .

Gain error due to the mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resis-

tors is eliminated by using feedback resistors internal to the DAC. Of the four DACs available in the DAC-8408, only two, DACs A and C, actually pass a signal. DACs B and D are used to provide the additional feedback resistors needed in the circuit. If the V_{REFB} and V_{REFD} inputs remain unconnected the current-to-voltage converters using R_{FB} and R_{FD} are unaffected by digital data reaching DACs B and D.

FIGURE 10: Low Noise Amplifier

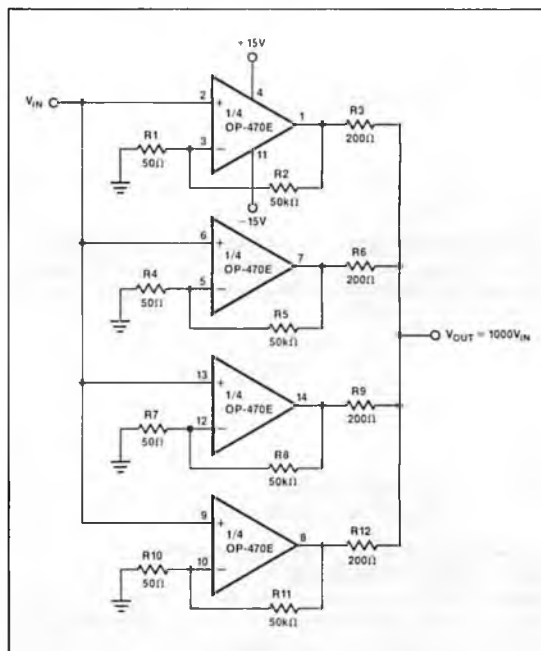


FIGURE 11: Noise Density of Low Noise Amplifier, $G = 1000$

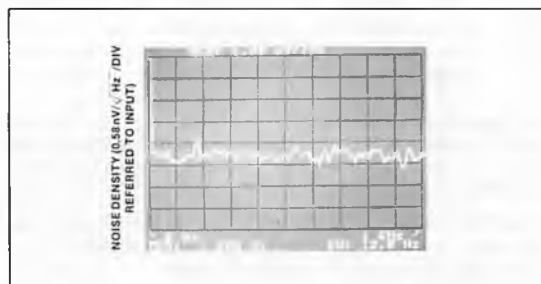


FIGURE 12: Digital Panning Control Circuit

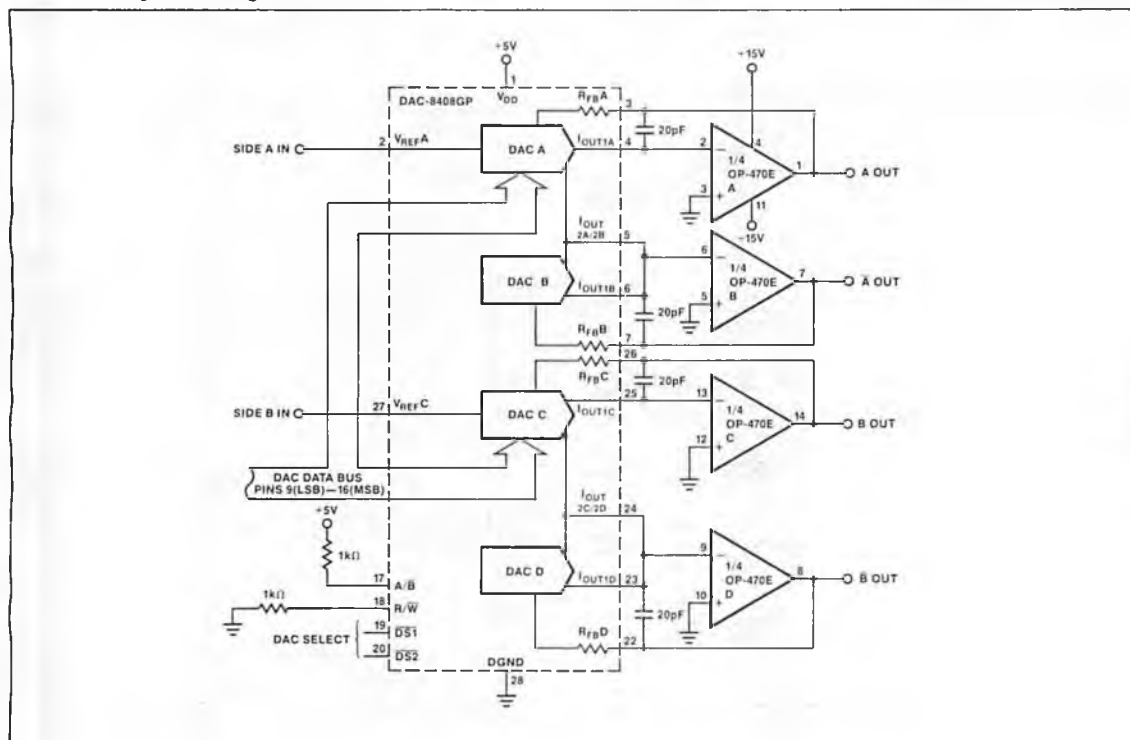
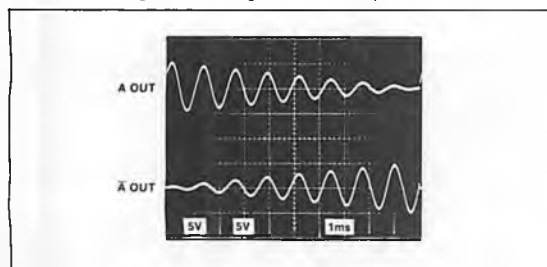


FIGURE 13: Digital Panning Control Output

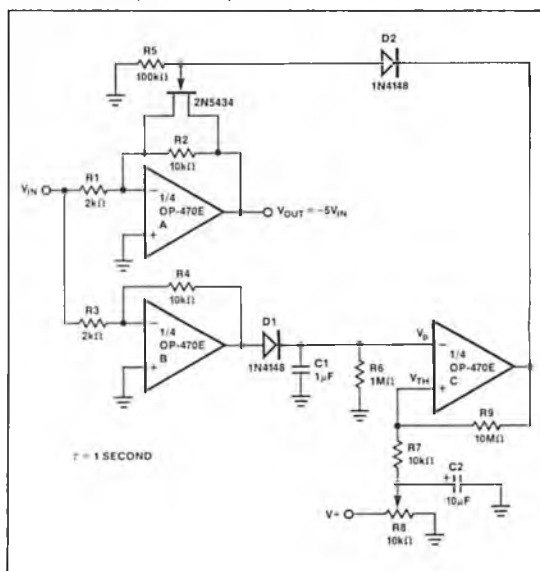


SQUELCH AMPLIFIER

The circuit of Figure 14 is a simple squelch amplifier that uses a FET switch to cut off the output when the input signal falls below a preset limit.

The input signal is sampled by a peak detector with a time constant set by C1 and R6. When the output of the peak detector, V_p , falls below the threshold voltage, V_{TH} , set by R8, the comparator formed by op amp C switches from V^- to V^+ . This drives the gate of the N-channel FET high, turning it ON, reducing the gain of the inverting amplifier formed by op amp A to zero.

FIGURE 14: Squelch Amplifier

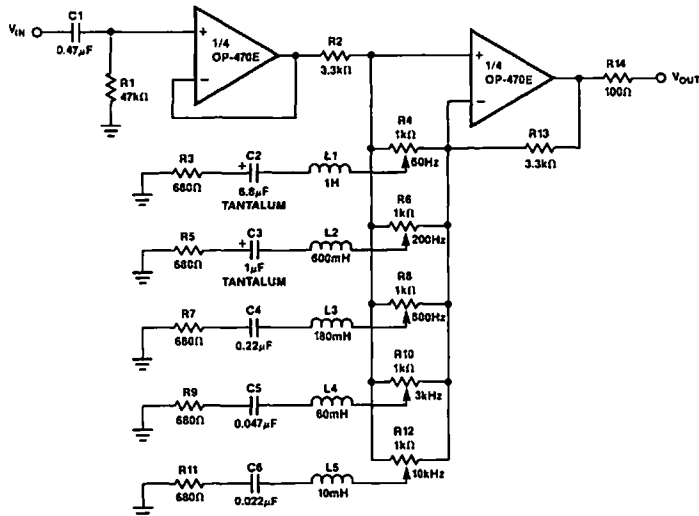


FIVE-BAND LOW NOISE STEREO GRAPHIC EQUALIZER

The graphic equalizer circuit shown in Figure 15 provides 15dB of boost or cut over a 5-band range. Signal-to-noise

ratio over a 20kHz bandwidth is better than 100dB referred to a 3V rms input. Larger inductors can be replaced by active inductors but this reduces the signal-to-noise ratio.

FIGURE 15: 5-Band Low Noise Graphic Equalizer





OP-471

HIGH-SPEED LOW-NOISE QUAD OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Excellent Speed 8V/ μ s Typ
- Low Noise 11nV/ $\sqrt{\text{Hz}}$ @ 1kHz Max
- Unity-Gain Stable
- High Gain-Bandwidth 6.5MHz Typ
- Low Input Offset Voltage 0.8mV Max
- Low Offset Voltage Drift 4 μ V/ $^{\circ}$ C Max
- High Gain 500V/mV Min
- Outstanding CMR 105 dB Min
- Industry Standard Quad Pinouts

ORDERING INFORMATION†

$T_A = 25^{\circ}\text{C}$ $V_{OS} \text{ MAX}$ (μ V)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC	PLASTIC	LCC	
800	OP471AY*	—	OP471ATC/883	MIL
800	OP471EY	—	—	IND
1500	OP471FY	—	—	IND
1800	—	OP471GP	—	COM
1800	—	OP471GS††	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

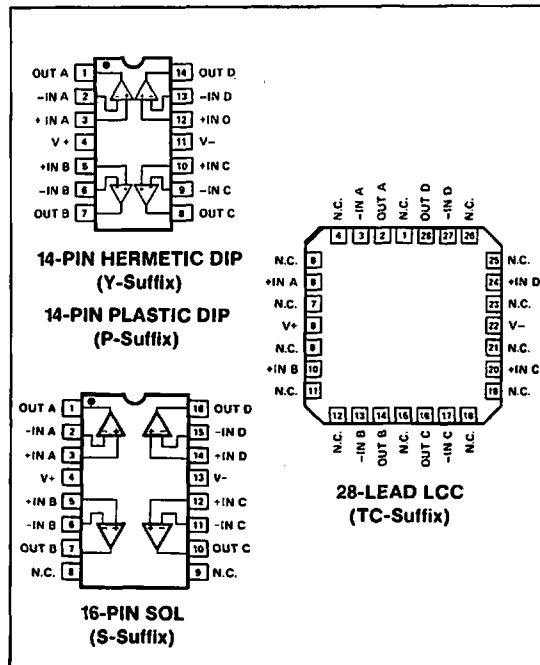
GENERAL DESCRIPTION

The OP-471 is a monolithic quad op amp featuring low noise, 11nV/ $\sqrt{\text{Hz}}$ Max @ 1kHz, excellent speed, 8V/ μ s typical, a gain-bandwidth of 6.5MHz, and unity-gain stability.

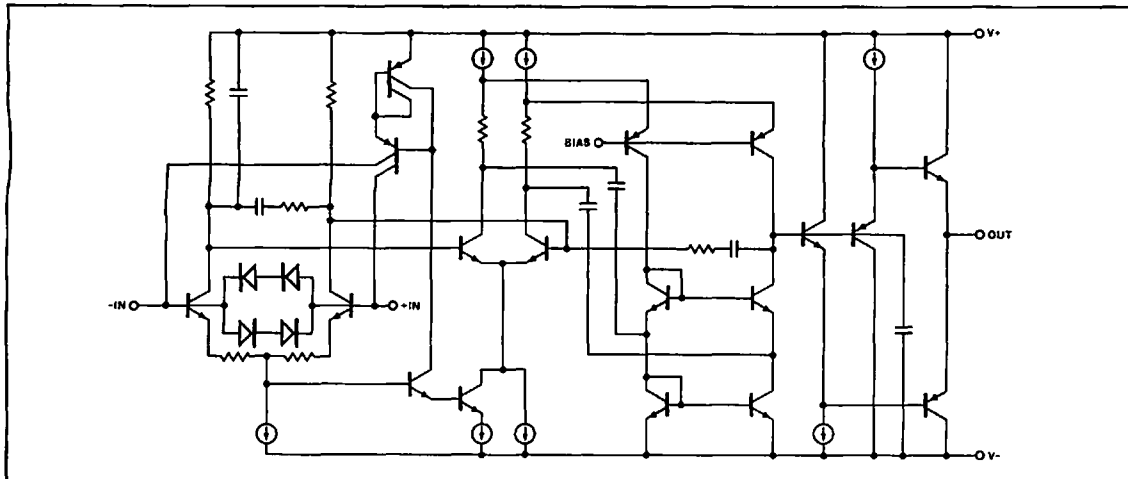
The OP-471 has an input offset voltage under 0.8mV and an input offset voltage drift below 4 μ V/ $^{\circ}$ C, guaranteed over the

full military temperature range. Open loop gain of the OP-471 is over 500,000 into a 10k Ω load insuring outstanding gain accuracy and linearity. The input bias current is under 25nA

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)



limiting errors due to signal source resistance. The OP-471's CMR of over 105dB and PSRR of under $5.6\mu\text{V/V}$ significantly reduce errors caused by ground noise and power supply fluctuations.

The OP-471 offers excellent amplifier matching which is important for applications such as multiple gain blocks, low-noise instrumentation amplifiers, quad buffers and low-noise active filters.

The OP-471 conforms to the industry standard 14-pin DIP pinout. It is pin compatible with the OP-11, LM148/149, HA4741, RM4156, MC33074, TL084 and TL074 quad op amps and can be used to upgrade systems using these devices.

For applications requiring even lower voltage noise the OP-470, with a voltage density of $5\text{nV}/\sqrt{\text{Hz}}$ Max @ 1kHz, is recommended.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	$\pm 18\text{V}$
Internal Power Dissipation (Note 1)	
Y-Package	800mW
P, TC-Package	500mW
Differential Input Voltage (Note 3)	$\pm 1.0\text{V}$
Differential Input Current (Note 3)	$\pm 25\text{mA}$

Input Voltage	Supply Voltage
Output Short-Circuit Duration	Continuous
Storage Temperature Range	
P, TC, Y-Package	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering, 60 sec)	300°C
DICE Junction Temperature (T_J)	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	
OP-471A	-55°C to $+125^\circ\text{C}$
OP-471E, OP-471F	-25°C to $+85^\circ\text{C}$
OP-471G	0°C to $+70^\circ\text{C}$

NOTES:

1. See table for maximum ambient temperature and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	70°C	$10.0\text{mW}/^\circ\text{C}$
14-Pin Plastic DIP	70°C	$15\text{mW}/^\circ\text{C}$
28-Lead LCC (TC)	100°C	$10.0\text{mW}/^\circ\text{C}$

2. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

3. The OP-471's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise performance. If differential voltage exceeds $\pm 1.0\text{V}$, the input current should be limited to $\pm 25\text{mA}$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-471A/E			OP-471F			OP-471G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.25	0.8	—	0.5	1.5	—	1.0	1.8	mV
Input Offset Current	I_{OS}	$V_{CM} = 0\text{V}$	—	4	10	—	7	20	—	12	30	nA
Input Bias Current	I_B	$V_{CM} = 0\text{V}$	—	7	25	—	15	50	—	25	60	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 1)	—	250	500	—	250	500	—	250	500	nV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$	—	9	16	—	9	16	—	9	16	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	7	12	—	7	12	—	7	12	
		$f_O = 1\text{kHz}$ (Note 2)	—	6.5	11	—	6.5	11	—	6.5	11	
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	1.7	—	—	1.7	—	—	1.7	—	$\text{pA}/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	0.7	—	—	0.7	—	—	0.7	—	
		$f_O = 1\text{kHz}$	—	0.4	—	—	0.4	—	—	0.4	—	
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10\text{V}$	—	—	—	—	—	—	—	—	—	V/mV
		$R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$	500 350	700 550	—	300 175	500 275	—	300 175	500 275	—	
Input Voltage Range	IVR	(Note 3)	± 11	± 12	—	± 11	± 12	—	± 11	± 12	—	V
Output Voltage Swing	V_O	$R_L \geq 2\text{k}\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{V}$	105	120	—	95	115	—	95	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$	—	1	5.6	—	5.6	17.8	—	5.6	17.8	$\mu\text{V/V}$
Slew Rate	SR		6.5	8	—	6.5	8	—	6.5	8	—	V/ μs

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-471A/E			OP-471F			OP-471G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.2	11	—	9.2	11	—	9.2	11	mA
Gain-Bandwidth Product	GBW	$A_V = +10$	—	6.5	—	—	6.5	—	—	6.5	—	MHz
Channel Separation	CS	$V_O = 20V_{p-p}$ $f_O = 10Hz$ (Note 1)	125	150	—	125	150	—	125	150	—	dB
Input Capacitance	C_{IN}		—	2.6	—	—	2.6	—	—	2.6	—	pF
Input Resistance Differential-Mode	R_{IN}		—	1.1	—	—	1.1	—	—	1.1	—	M Ω
Input Resistance Common-Mode	R_{INCM}		—	11	—	—	11	—	—	11	—	G Ω
Settling Time	t_s	$A_V = +1$	—	4.5	—	—	4.5	—	—	4.5	—	μs
		to 0.1%	—	4.5	—	—	4.5	—	—	4.5	—	
		to 0.01%	—	7.5	—	—	7.5	—	—	7.5	—	

NOTES:

1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$ for OP-471A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-471A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.4	1.2	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	4	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	6	20	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	16	50	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$				V/mV
		$R_L = 10k\Omega$ $R_L = 2k\Omega$	375 250	500 350	— —	
Input Voltage Range	IVR	(Note 1)	± 11	± 12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	5.6	10	$\mu V/V$
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.3	11	mA

NOTE:

1. Guaranteed by CMR test.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$ for OP-471E/F, $0^\circ C \leq T_A \leq 70^\circ C$ for OP-471G, unless otherwise noted.

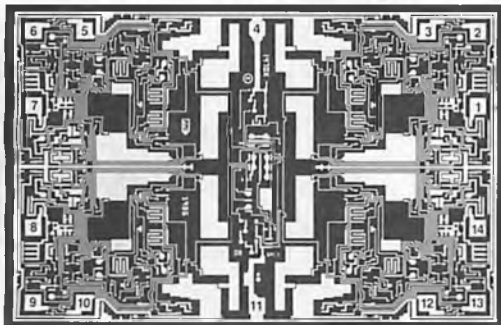
PARAMETER	SYMBOL	CONDITIONS	OP-471E			OP-471F			OP-471G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.3	1.1	—	0.6	2.0	—	1.2	2.5	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	1	4	—	2	7	—	4	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	5	20	—	8	40	—	20	50	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	13	50	—	25	70	—	40	75	nA
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$										
		$R_L = 10k\Omega$	375	600	—	200	400	—	200	400	—	V/mV
		$R_L = 2k\Omega$	250	400	—	125	200	—	125	200	—	
Input Voltage Range	IVR	(Note 1)	± 11	± 12	—	± 11	± 12	—	± 11	± 12	—	V
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	± 13	—	± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	—	3.2	10	—	18	31.6	—	18	31.6	$\mu V/V$
Supply Current (All Amplifiers)	I_{SY}	No Load	—	9.3	11	—	9.3	11	—	9.3	11	mA

NOTE:

1. Guaranteed by CMR test.



DICE CHARACTERISTICS



1. OUT A
2. -IN A
3. +IN A
4. V+
5. +IN B
6. -IN B
7. OUT B
8. OUT C
9. -IN C
10. +IN C
11. V-
12. +IN D
13. -IN D
14. OUT D

DIE SIZE 0.163 × 0.106 inch, 17,278 sq. mils
(4.14 × 2.69 mm, 11.14 sq. mm)

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

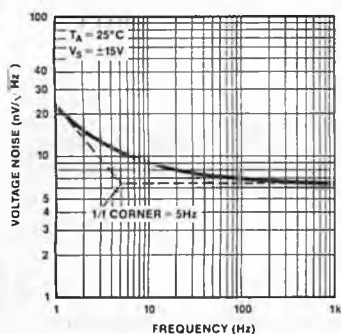
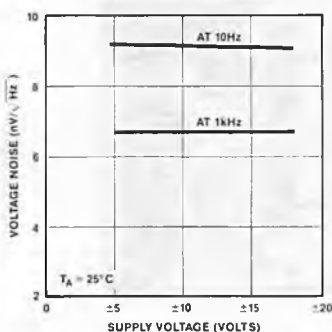
PARAMETER	SYMBOL	CONDITIONS	OP-471GBC LIMIT	UNITS
Input Offset Voltage	V_{OS}		1.5	mV MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	20	nA MAX
Input Bias Current	I_B	$V_{CM} = 0V$	50	nA MAX
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 10V$	300	V/mV MIN
		$R_L = 10k\Omega$	175	
		$R_L = 2k\Omega$		
Input Voltage Range	IVR	Note 1	± 11	V MIN
Output Voltage Swing	V_O	$R_L \geq 2k\Omega$	± 12	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	17.8	$\mu V/V$ MAX
Slew Rate	SR		6.5	V/ μs MIN
Supply Current (All Amplifiers)	I_{SY}	No Load	11	mA MAX

NOTES:

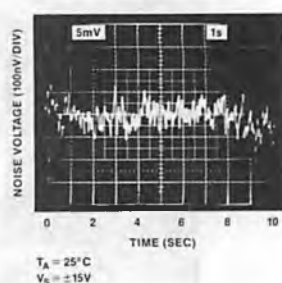
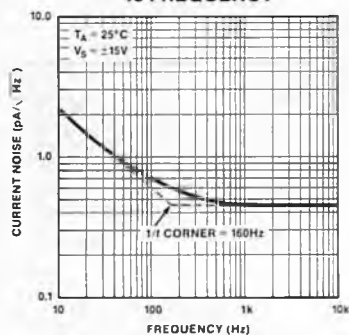
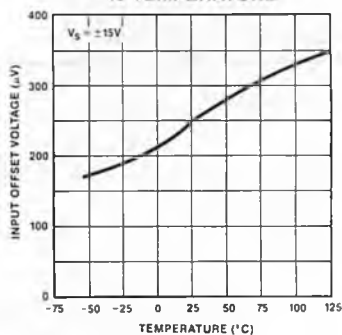
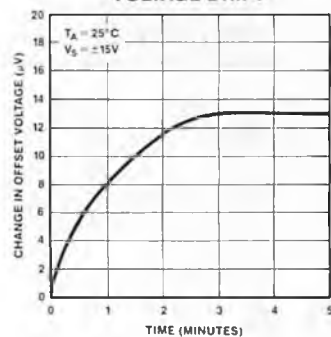
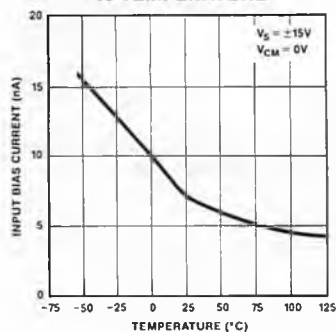
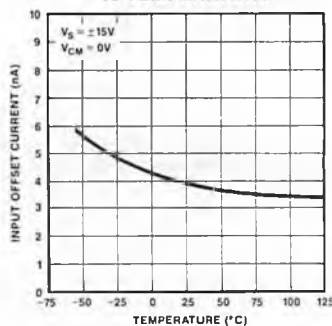
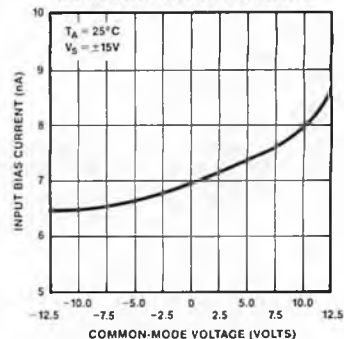
1. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE NOISE DENSITY
vs FREQUENCY

VOLTAGE NOISE DENSITY
vs SUPPLY VOLTAGE


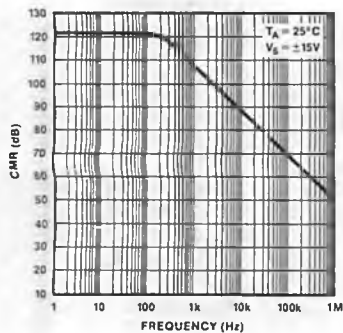
0.1Hz TO 10Hz NOISE


CURRENT NOISE DENSITY
vs FREQUENCY

INPUT OFFSET VOLTAGE
vs TEMPERATURE

WARM-UP OFFSET
VOLTAGE DRIFT

INPUT BIAS CURRENT
vs TEMPERATURE

INPUT OFFSET CURRENT
vs TEMPERATURE

INPUT BIAS CURRENT vs
COMMON-MODE VOLTAGE


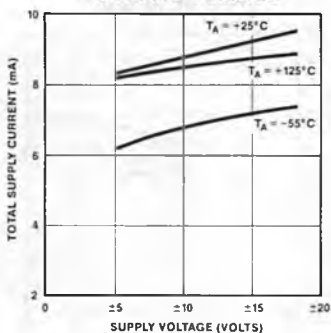


TYPICAL PERFORMANCE CHARACTERISTICS

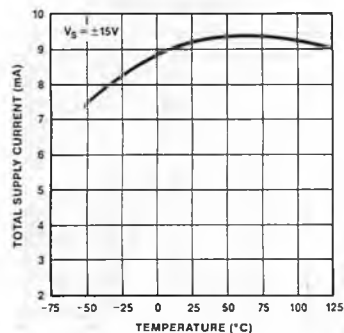
CMR vs FREQUENCY



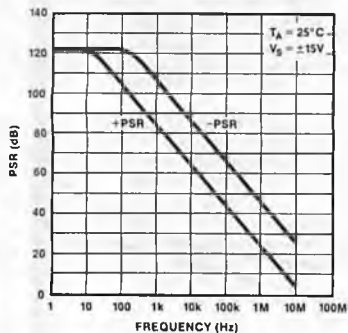
TOTAL SUPPLY CURRENT vs SUPPLY VOLTAGE



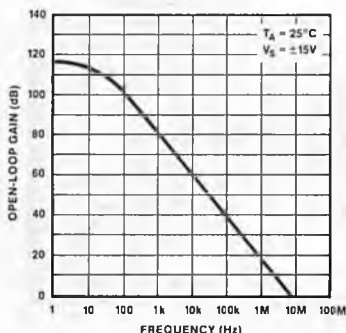
TOTAL SUPPLY CURRENT vs TEMPERATURE



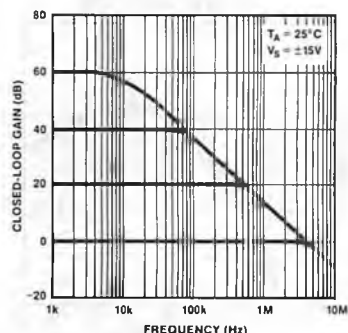
PSR vs FREQUENCY



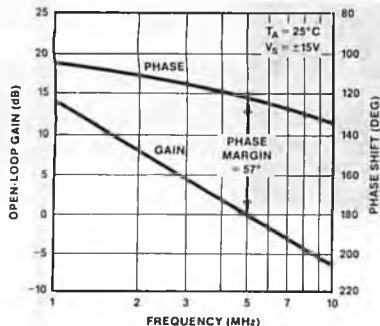
OPEN-LOOP GAIN vs FREQUENCY



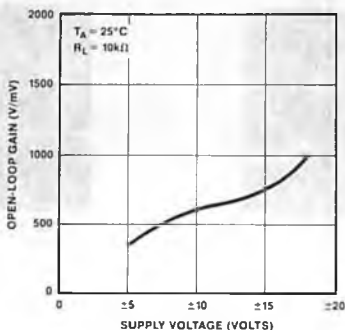
CLOSED-LOOP GAIN vs FREQUENCY



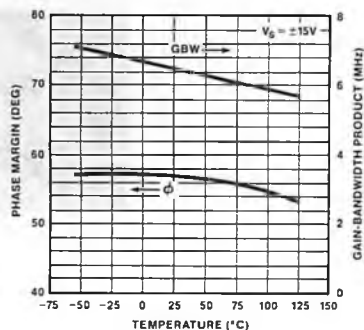
OPEN-LOOP GAIN, PHASE SHIFT vs FREQUENCY



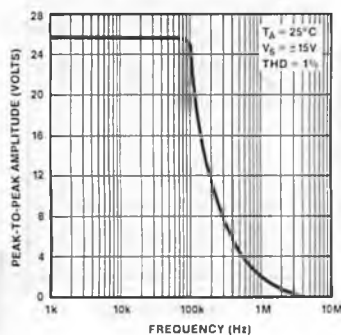
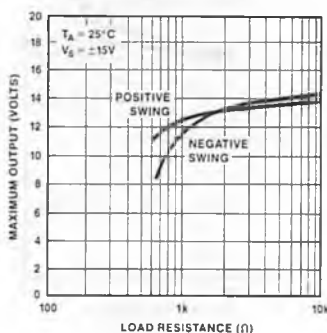
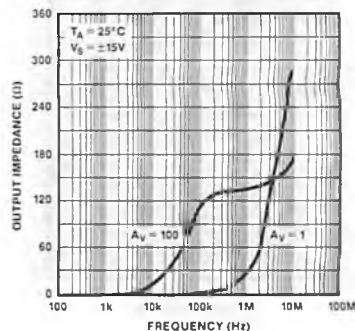
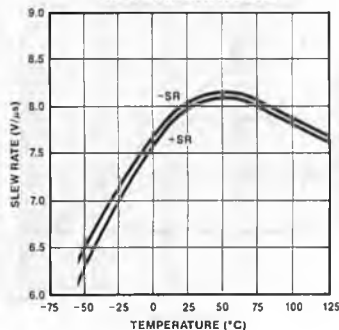
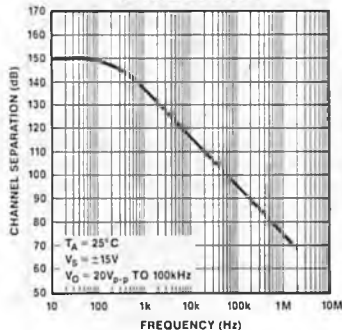
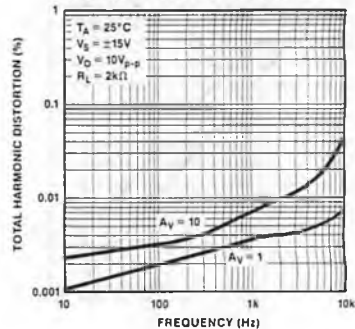
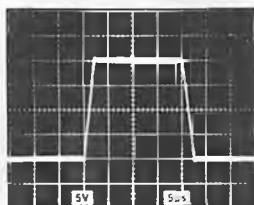
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



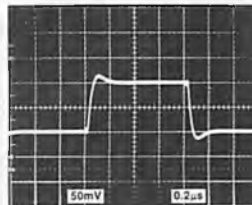
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS

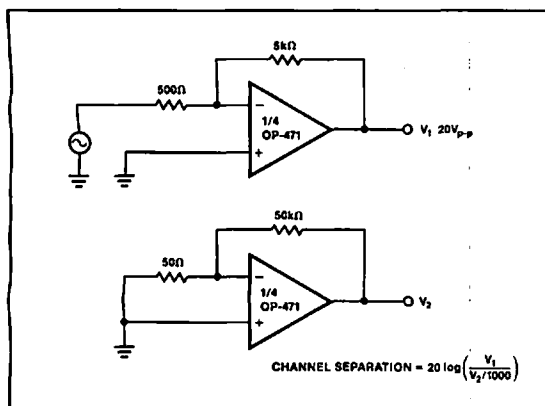
MAXIMUM OUTPUT SWING
vs FREQUENCY

MAXIMUM OUTPUT
VOLTAGE vs
LOAD RESISTANCE

CLOSED-LOOP
OUTPUT IMPEDANCE
vs FREQUENCY

SLEW RATE
vs TEMPERATURE

CHANNEL SEPARATION
vs FREQUENCY

TOTAL HARMONIC
DISTORTION vs FREQUENCY

LARGE-SIGNAL
TRANSIENT RESPONSE


$T_A = 25^\circ\text{C}$
 $V_S = \pm 15\text{V}$
 $A_V = +1$

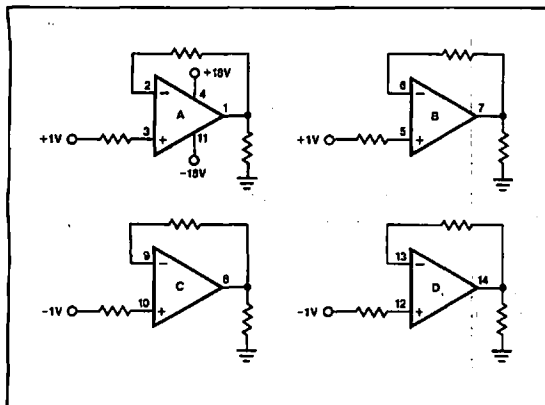
SMALL-SIGNAL
TRANSIENT RESPONSE


$T_A = 25^\circ\text{C}$
 $V_S = \pm 15\text{V}$
 $A_V = +1$

CHANNEL SEPARATION TEST CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

VOLTAGE AND CURRENT NOISE

The OP-471 is a very low-noise quad op amp, exhibiting a typical voltage noise of only $6.5\text{nV}/\sqrt{\text{Hz}}$ @ 1kHz. The low noise characteristic of the OP-471 is in part achieved by operating the input transistors at high collector currents since the voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise performance of the OP-471 is gained at the expense of current noise performance which is typical for low noise amplifiers.

To obtain the best noise performance in a circuit it is vital to understand the relationship between voltage noise (e_n), current noise (i_n), and resistor noise (e_i).

TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calculated by:

$$E_n = \sqrt{(e_n)^2 + (i_n R_S)^2 + (e_i)^2}$$

where:

E_n = total input referred noise

e_n = op amp voltage noise

i_n = op amp current noise

e_i = source resistance thermal noise

R_S = source resistance

The total noise is referred to the input and at the output would be amplified by the circuit gain.

Figure 1 shows the relationship between total noise at 1kHz and source resistance. For $R_S < 1\text{k}\Omega$ the total noise is domi-

FIGURE 1: Total Noise vs Source Resistance (Including Resistor Noise) at 1kHz

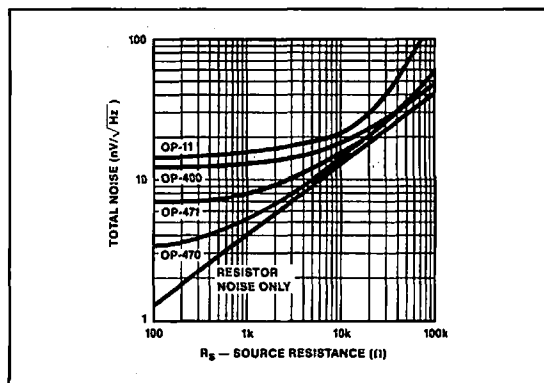
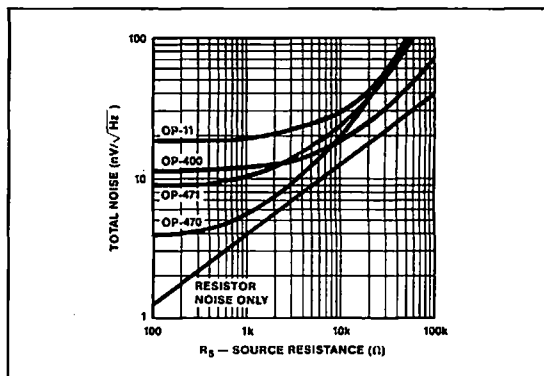


FIGURE 2: Total Noise vs Source Resistance (Including Resistor Noise) at 10Hz



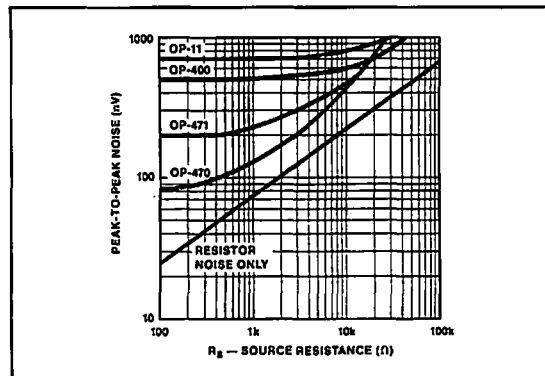
nated by the voltage noise of the OP-471. As R_S rises above $1\text{k}\Omega$, total noise increases and is dominated by resistor noise rather than by voltage or current noise of the OP-471. When R_S exceeds $20\text{k}\Omega$, current noise of the OP-471 becomes the major contributor to total noise.

Figure 2 also shows the relationship between total noise and source resistance, but at 10Hz . Total noise increases more quickly than shown in Figure 1 because current noise is inversely proportional to the square root of frequency. In Figure 2, current noise of the OP-471 dominates the total noise when $R_S > 5\text{k}\Omega$.

From Figures 1 and 2 it can be seen that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP-400, with lower current noise than the OP-471, will provide lower total noise.

Figure 3 shows peak-to-peak noise versus source resistance over the 0.1Hz to 10Hz range. Once again, at low values of R_S ,

FIGURE 3: Peak-To-Peak Noise (0.1Hz To 10Hz) vs Source Resistance (Includes Resistor Noise)



the voltage noise of the OP-471 is the major contributor to peak-to-peak noise. Current noise becomes the major contributor as R_S increases. The crossover point between the OP-471 and the OP-400 for peak-to-peak noise is at $R_S = 17\text{k}\Omega$.

The OP-470 is a lower noise version of the OP-471, with a typical noise voltage density of $3.2\text{nV}/\sqrt{\text{Hz}}$ @ 1kHz . The OP-470 offers lower offset voltage and higher gain than the OP-471, but is a slower speed device, with a slew rate of $2\text{V}/\mu\text{s}$ compared to a slew rate of $8\text{V}/\mu\text{s}$ for the OP-471.

For reference, typical source resistances of some signal sources are listed in Table I.

TABLE I

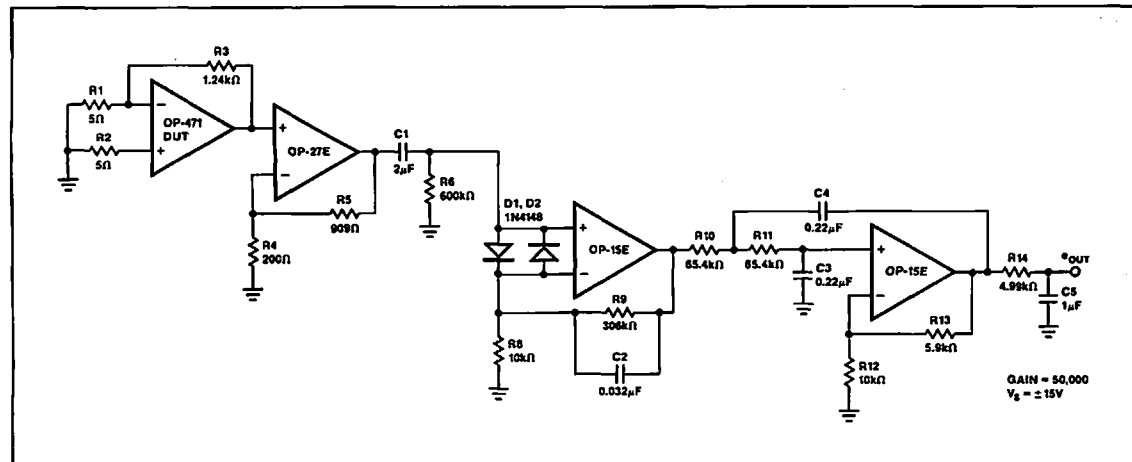
DEVICE	SOURCE IMPEDANCE	COMMENTS
Strain gauge	$<500\Omega$	Typically used in low-frequency applications.
Magnetic tapehead	$<1500\Omega$	Low I_B very important to reduce self-magnetization problems when direct coupling is used. OP-471 I_B can be neglected.
Magnetic phonograph cartridges	$<1500\Omega$	Similar need for low I_B in direct coupled applications. OP-471 will not introduce any self-magnetization problem.
Linear variable differential transformer	$<1500\Omega$	Used in rugged servo-feedback applications. Bandwidth of interest is 400Hz to 5kHz .

For further information regarding noise calculations, see "Minimization of Noise in Op-Amp Applications", Application Note AN-15.

NOISE MEASUREMENTS — PEAK-TO-PEAK VOLTAGE NOISE

The circuit of Figure 4 is a test setup for measuring peak-to-peak voltage noise. To measure the 500nV peak-to-peak

FIGURE 4: Peak-To-Peak Voltage Noise Test Circuit (0.1Hz To 10Hz)



noise specification of the OP-471 in the 0.1Hz to 10Hz range, the following precautions must be observed:

1. The device has to be warmed-up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes $13\mu\text{V}$ due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding also minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feed-through" to increase the observed noise.

FIGURE 5: 0.1Hz To 10Hz Peak-To-Peak Voltage Noise Test Circuit Frequency Response

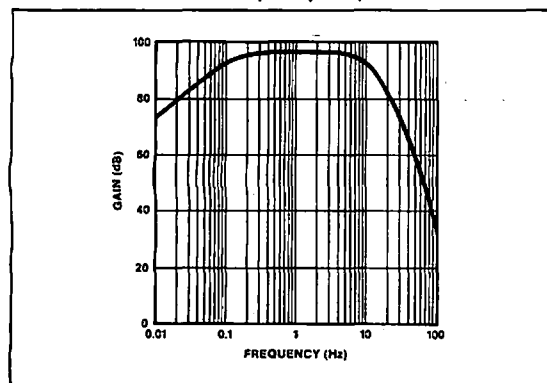
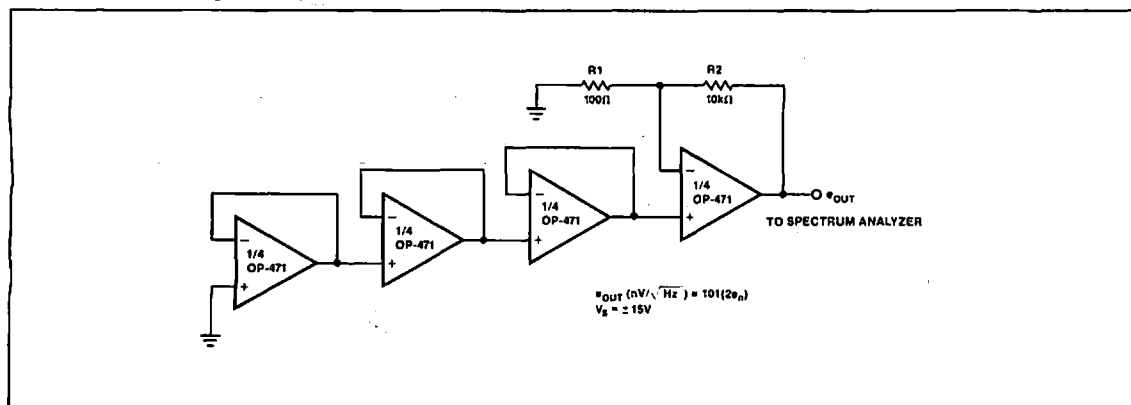


FIGURE 6: Noise Voltage Density Test Circuit



4. The test time to measure 0.1Hz-to-10Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency-response curve of Figure 5, the 0.1Hz corner is defined by only one pole. The test time of 10 seconds acts as an additional pole to eliminate noise contribution from the frequency band below 0.1Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage-density measurement will correlate well with a 0.1Hz-to-10Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the $1/f$ corner frequency.
6. Power should be supplied to the test circuit by well bypassed low-noise supplies, e.g. batteries. These will minimize output noise introduced through the amplifier supply pins.

NOISE MEASUREMENT — NOISE VOLTAGE DENSITY

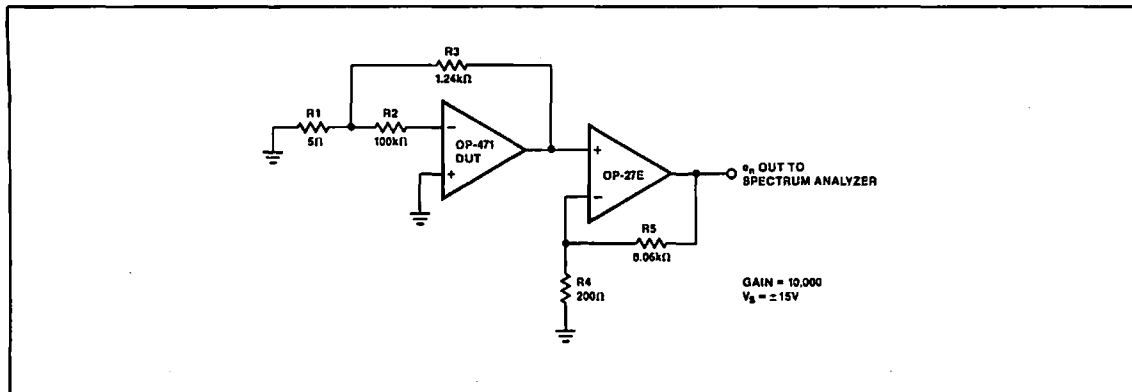
The circuit of Figure 6 shows a quick and reliable method of measuring the noise voltage density of quad op amps. Each individual amplifier is series-connected and is in unity-gain, save the final amplifier which is in a noninverting gain of 101. Since the ac noise voltages of each amplifier are uncorrelated, they add in rms fashion to yield:

$$e_{OUT} = 101 (\sqrt{e_{nA}^2 + e_{nB}^2 + e_{nC}^2 + e_{nD}^2})$$

The OP-471 is a monolithic device with four identical amplifiers. The noise voltage density of each individual amplifier will match, giving:

$$e_{OUT} = 101 (\sqrt{4e_n^2}) = 101 (2e_n)$$

FIGURE 7: Current Noise Density Test Circuit



NOISE MEASUREMENT — CURRENT NOISE DENSITY

The test circuit shown in Figure 7 can be used to measure current noise density. The formula relating the voltage output to current noise density is:

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - \left(40nV/\sqrt{Hz}\right)^2}}{R_S}$$

where:

G = gain of 10000

R_S = 100kΩ source resistance

CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS

The OP-471 is unity-gain stable and is capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP-471.

In the standard feedback amplifier, the op amp's output resistance combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 8. The added components, C1 and R3, decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 8 are for load capacitances of up to 1000pF when used with the OP-471.

In applications where the OP-471's inverting or noninverting inputs are driven by a low source impedance (under 100Ω) or connected to ground, if V+ is applied before V-, or when V- is disconnected, excessive parasitic currents will flow. Most

FIGURE 8: Driving Large Capacitive Loads

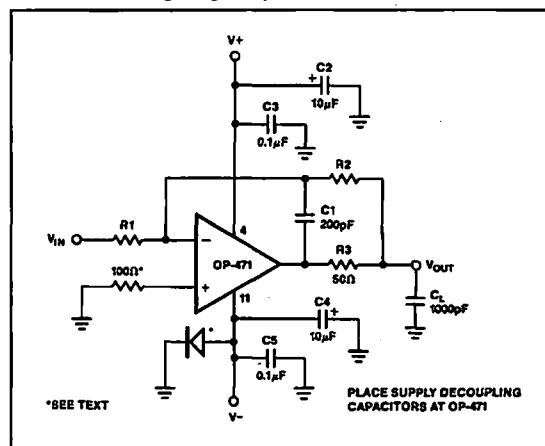
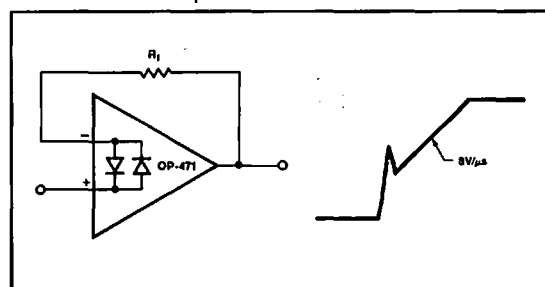


FIGURE 9: Pulsed Operation



applications use dual tracking supplies and with the device supply pins properly bypassed, power-up will not present a problem. A source resistance of at least 100Ω in series with all inputs (Figure 8) will limit the parasitic currents to a safe level if V_- is disconnected. It should be noted that any source resistance, even 100Ω , adds noise to the circuit. Where noise is required to be kept at a minimum, a germanium or Schottky diode can be used to clamp the V_- pin and eliminate the parasitic current flow instead of using series limiting resistors. For most applications, only one diode clamp is required per board or system.

UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\Omega$ and the input is driven with a fast, large-signal pulse ($>1V$), the output waveform will look as shown in Figure 9.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at $10V$); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 3k\Omega$, a pole created by R_f and the amplifier's input capacitance ($2.6pF$) creates additional phase shift and reduces phase margin. A small capacitor (20 to $50pF$) in parallel with R_f helps eliminate this problem.

APPLICATIONS

LOW NOISE AMPLIFIER

A simple method of reducing amplifier noise by paralleling amplifiers is shown in Figure 10. Amplifier noise, depicted in Figure 11, is around $5nV/\sqrt{Hz}$ @ $1kHz$ (R.T.I.). Gain for each paralleled amplifier and the entire circuit is 100. The 200Ω resistors limit circulating currents and provide an effective output resistance of 50Ω . The amplifier is stable with a $10nF$ capacitive load and can supply up to $30mA$ of output drive.

HIGH-SPEED DIFFERENTIAL LINE DRIVER

The circuit of Figure 12 is a unique line driver widely used in professional audio applications. With $\pm 18V$ supplies the line driver can deliver a differential signal of $30V_{p-p}$ into a $1.5k\Omega$ load. The output of the differential line driver looks exactly like a transformer. Either output can be shorted to ground without changing the circuit gain of 5, so the amplifier can easily be set for inverting, noninverting, or differential operation. The line driver can drive unbalanced loads, like a true transformer.

HIGH OUTPUT AMPLIFIER

The amplifier shown in Figure 13 is capable of driving $20V_{p-p}$ into a floating 400Ω load. Design of the amplifier is based on a bridge configuration. A1 amplifies the input signal and drives the load with the help of A2. Amplifier A3 is a unity-gain inverter which drives the load with help from A4. Gain of the high output amplifier with the component values shown is 10, but can easily be changed by varying R_1 or R_2 .

FIGURE 10: Low Noise Amplifier

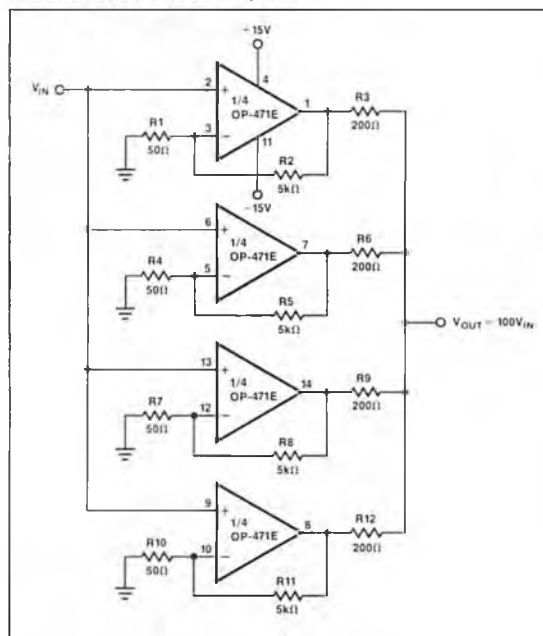
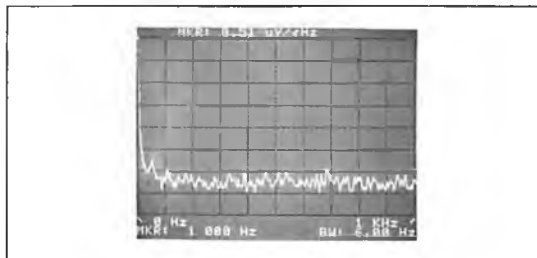


FIGURE 11: Noise Density of Low Noise Amplifier, $G = 100$

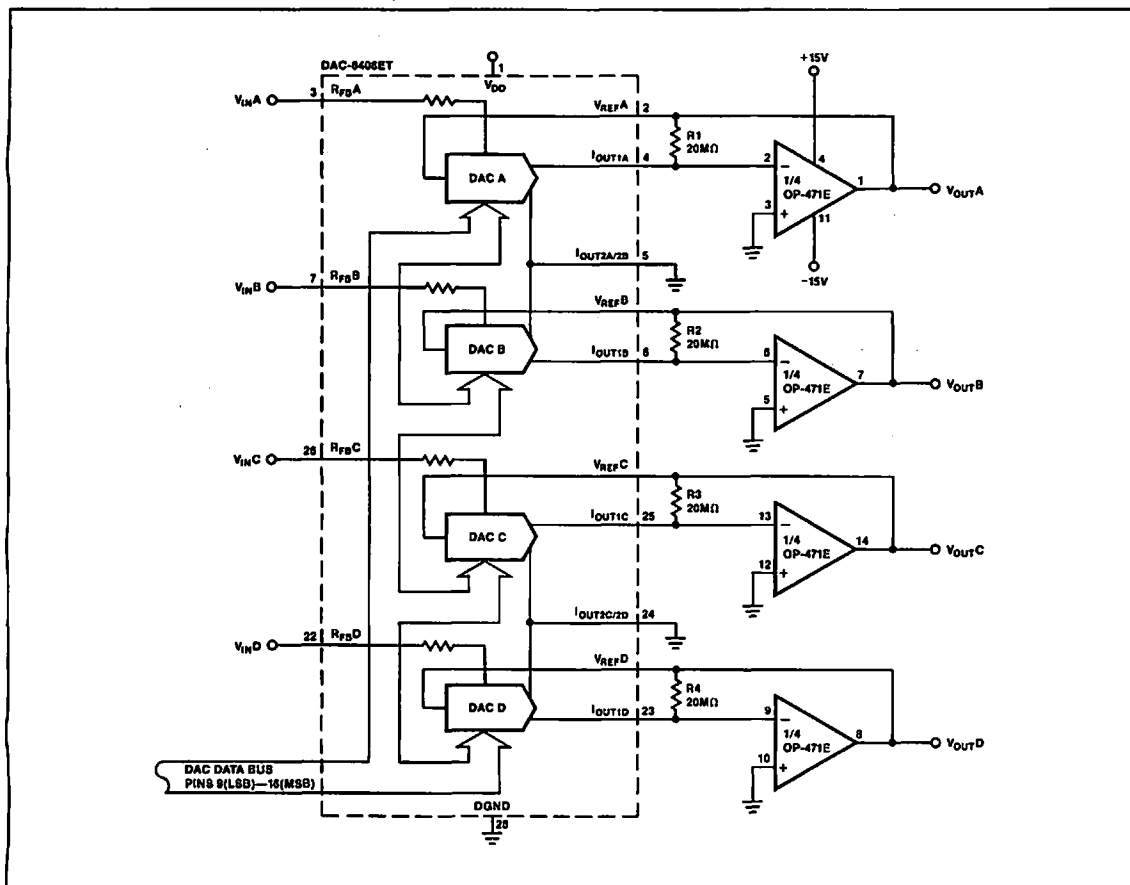


QUAD PROGRAMMABLE GAIN AMPLIFIER

The combination of the quad OP-471 and the DAC-8408, a quad 8-bit CMOS DAC, creates a space-saving quad programmable gain amplifier. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the fixed DAC feedback resistor and the impedance the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = - \frac{256}{n}$$

where n equals the decimal equivalent of the 8-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will be open causing the op amp output to saturate. The 20MΩ resistors placed in parallel with the DAC feedback loop eliminates this problem with a very small reduction in gain accuracy.

FIGURE 14: Quad Programmable Gain Amplifier

LOW PHASE ERROR AMPLIFIER

The simple amplifier depicted in Figure 15 utilizes monolithic matched operational amplifiers and a few resistors to substantially reduce phase error compared to conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is over a decade greater than for a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of op amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces $V_2/(K1 + 1) = V_{IN}$. The A2 feedback loop forces $V_O/(K1 + 1) = V_2/(K1 + 1)$ yielding an overall transfer function of $V_O/V_{IN} = K1 + 1$. The DC gain is deter-

mined by the resistor divider at the output, V_O , and is not directly affected by the resistor divider around A2. Note, that like a conventional single op amp amplifier, the DC gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

Figure 16 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where $\omega/\beta\omega_T < 0.1$. For example, phase error of -0.1° occurs at $0.002 \omega/\beta\omega_T$ for the single op amp amplifier, but at $0.11 \omega/\beta\omega_T$ for the low phase error amplifier.

For more detailed information on the low phase error amplifier, see Application Note AN-107.

FIGURE 15: Low Phase Error Amplifier

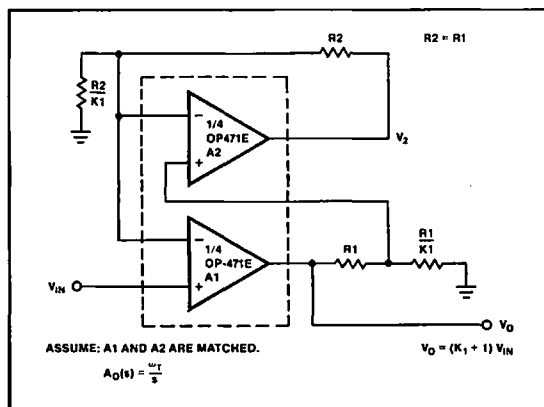
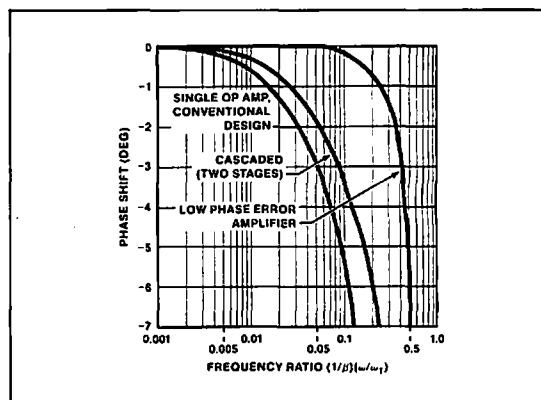


FIGURE 16: Phase Error Comparison





OP-490

LOW-VOLTAGE MICROPOWER
QUAD OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Single/Dual Supply Operation +1.6V to +36V
..... $\pm 0.8V$ to $\pm 18V$
- True Single-Supply Operation; Input and Output Voltage Ranges Include Ground
- Low Supply Current 80 μ A Max
- High Output Drive 5mA Min
- Low Input Offset Voltage 0.5mV Max
- High Open-Loop Gain 700V/mV Min
- Outstanding PSRR 5.6 μ V/V Max
- Industry Standard Quad Pinouts

ORDERING INFORMATION†

$T_A = 25^\circ C$ V_{OS} MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC	
0.5	OP490AY*	—	OP490ATC/883	MIL
0.5	OP490EY	—	—	IND
0.75	OP490FY	—	—	IND
1.0	—	OP490GP	—	COM
1.0	—	OP490GS††	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

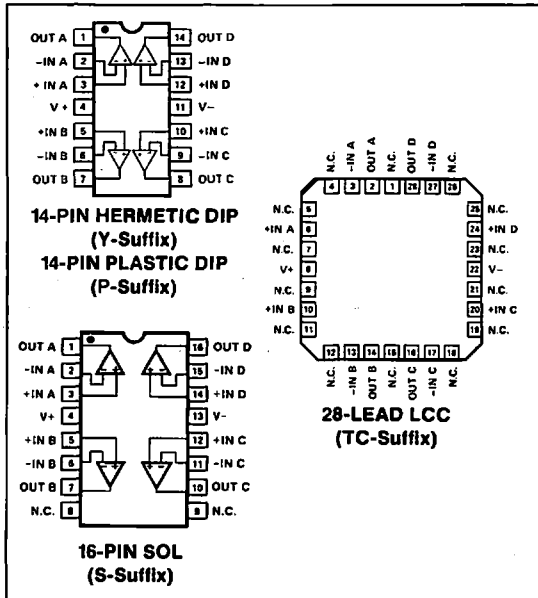
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

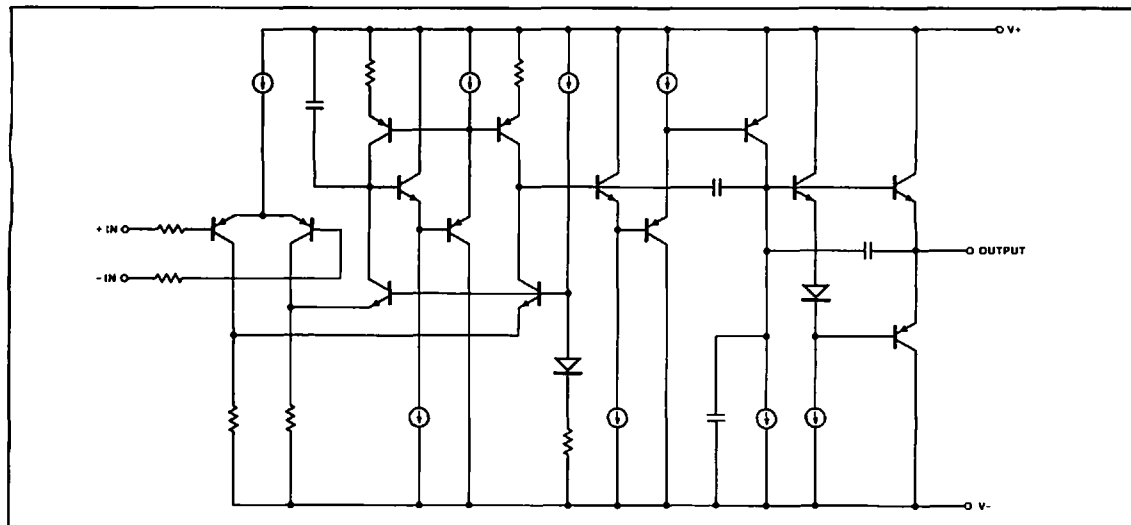
The OP-490 is a high performance micropower quad op amp that operates from a single supply of +1.6V to +36V or from dual supplies of $\pm 0.8V$ to $\pm 18V$. Input voltage range includes

the negative rail allowing the OP-490 to accommodate input signals down to ground in single-supply operation. The OP-490's output swing also includes ground when operating from a single supply, enabling "zero-in, zero-out" operation.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (One of four amplifiers is shown.)





The quad OP-490 draws less than 20 μ A of quiescent supply current per amplifier, but each amplifier is able to deliver over 5mA of output current to a load. Input offset voltage is under 0.5mV with offset drift below 5 μ V/ $^{\circ}$ C over the military temperature range. Gain exceeds 700,000 and CMR is better than 100dB. A PSRR of under 5.6 μ V/V minimizes offset voltage changes experienced in battery powered systems.

The quad OP-490 combines high performance with the space and cost savings of quad amplifiers. The minimal voltage and current requirements of the OP-490 makes it ideal for battery and solar powered applications, such as portable instruments and remote sensors.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	± 18 V
Power Dissipation (Note 1)	
Y Package	800mW
TC, P Package	500mW
Differential Input Voltage	[(V-) - 20V] to [(V+) + 20V]
Common-Mode Input Voltage	[(V-) - 20V] to [(V+) + 20V]

Output Short-Circuit Duration Continuous
Storage Temperature Range

TC, Y, P Package -65 $^{\circ}$ C to +150 $^{\circ}$ C

Operating Temperature Range

OP-490A -55 $^{\circ}$ C to +125 $^{\circ}$ C

OP-490E, OP-490F -25 $^{\circ}$ C to +85 $^{\circ}$ C

OP-490G 0 $^{\circ}$ C to +70 $^{\circ}$ C

DICE Junction Temperature (T_j) -65 $^{\circ}$ C to +150 $^{\circ}$ C

Lead Temperature Range (Soldering, 60 sec) 300 $^{\circ}$ C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	70 $^{\circ}$ C	10mW/ $^{\circ}$ C
28-Pin LCC (TC)	100 $^{\circ}$ C	10mW/ $^{\circ}$ C
14-Pin Plastic DIP (P)	70 $^{\circ}$ C	9.1mW/ $^{\circ}$ C

ELECTRICAL CHARACTERISTICS at V_S = ± 1.5 V to ± 15 V, T_A = +25 $^{\circ}$ C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-490A/E			OP-490F			OP-490G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}		—	0.2	0.5	—	0.4	0.75	—	0.6	1.0	mV
Input Offset Current	I _{OS}	V _{CM} = 0V	—	0.4	3	—	0.4	5	—	0.4	5	nA
Input Bias Current	I _B	V _{CM} = 0V	—	4.2	15	—	4.2	20	—	4.2	25	nA
Large Signal Voltage Gain	A _{VO}	V _S = ± 15 V, V _O = ± 10 V										V/mV
		R _L = 100k Ω	700	1200	—	500	1000	—	400	800	—	
		R _L = 10k Ω	350	600	—	250	500	—	200	400	—	
		R _L = 2k Ω	125	250	—	100	200	—	100	200	—	
		V ₊ = 5V, V ₋ = 0V, 1V < V _O < 4V										
		R _L = 100k Ω	200	400	—	125	300	—	100	250	—	V
		R _L = 10k Ω	100	160	—	75	140	—	70	140	—	
Input Voltage Range	IVR	V ₊ = 5V, V ₋ = 0V	0/4	—	—	0/4	—	—	0/4	—	—	V
		V _S = ± 15 V (Note 1)	-15/13.5	—	—	-15/13.5	—	—	-15/13.5	—	—	
Output Voltage Swing	V _O	V _S = ± 15 V										V
		R _L = 10k Ω	± 13.5	± 14.2	—	± 13.5	± 14.2	—	± 13.5	± 14.2	—	
		R _L = 2k Ω	± 10.5	± 11.5	—	± 10.5	± 11.5	—	± 10.5	± 11.5	—	
	V _{OH}	V ₊ = 5V, V ₋ = 0V										
		R _L = 2k Ω	4.0	4.2	—	4.0	4.2	—	4.0	4.2	—	
	V _{OL}	V ₊ = 5V, V ₋ = 0V										μ V
		R _L = 10k Ω	—	100	500	—	100	500	—	100	500	
Common Mode Rejection	CMR	V ₊ = 5V, V ₋ = 0V, 0V < V _{CM} < 4V	90	110	—	80	100	—	80	100	—	dB
		V _S = ± 15 V, -15V < V _{CM} < 13.5V	100	130	—	90	120	—	90	120	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	3.2	10	—	3.2	10	μ V/V
Slew Rate	SR	V _S = ± 15 V	5	12	—	5	12	—	5	12	—	V/ms
Supply Current (All Amplifiers)	I _{SV}	V _S = ± 1.5 V	—	40	60	—	40	60	—	40	60	μ A
		V _S = ± 15 V No Load	—	60	80	—	60	80	—	60	80	
Capacitive Load Stability	A _V	A _V = +1	—	650	—	—	650	—	—	650	—	pF
Input Noise Voltage	e _{np-p}	f _O = 0.1Hz to 10Hz V _S = ± 15 V	—	3	—	—	3	—	—	3	—	μ V _{p-p}

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 1.5V$ to $\pm 15V$, $T_A = +25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-490A/E			OP-490F			OP-490G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Resistance Differential Mode	R_{IN}	$V_S = \pm 15V$	—	30	—	—	30	—	—	30	—	M Ω
Input Resistance Common Mode	R_{INCM}	$V_S = \pm 15V$	—	20	—	—	20	—	—	20	—	G Ω
Gain Bandwidth Product	GBWP	$A_V = +1$	—	20	—	—	20	—	—	20	—	kHz
Channel Separation	CS	$f_O = 10Hz$ $V_O = 20V_{p-p}$ $V_S = \pm 15V$ (Note 2)	120	150	—	120	150	—	120	150	—	dB

NOTES:

1. Guaranteed by CMR test.
2. Guaranteed but not 100% tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-490A			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.4	1.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	$V_S = \pm 15V$	—	2	5	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	1.5	5	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.4	20	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100k\Omega$	225	400	—	V/mV
		$R_L = 10k\Omega$	125	240	—	
		$R_L = 2k\Omega$	50	110	—	
		$V^+ = 5V$, $V^- = 0V$, $1V < V_O < 4V$ $R_L = 100k\Omega$	100	200	—	
		$R_L = 10k\Omega$	50	110	—	
Input Voltage Range	IVR	$V^+ = 5V$, $V^- = 0V$ $V_S = \pm 15V$ (Note 1)	0/3.5 -15/13.5	— —	— —	V
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 13 ± 10	± 13.7 ± 11	— —	V
	V_{OH}	$V^+ = 5V$, $V^- = 0V$ $R_L = 2k\Omega$	3.9	4.1	—	V
	V_{OL}	$V^+ = 5V$, $V^- = 0V$ $R_L = 10k\Omega$	—	100	500	μV
Common Mode Rejection	CMR	$V^+ = 5V$, $V^- = 0V$, $0V < V_{CM} < 3.5V$ $V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	85 95	105 115	— —	dB
Power Supply Rejection Ratio	PSRR		—	3.2	10	$\mu V/V$
Supply Current (All Amplifiers)	I_{SV}	$V_S = \pm 1.5V$ No Load $V_S = \pm 15V$	— —	70 90	100 120	μA

NOTE:

1. Guaranteed by CMR test.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 1.5V$ to $\pm 15V$, $-25^\circ C \leq T_A \leq 85^\circ C$ for OP-490E/F, $0^\circ C \leq T_A \leq 70^\circ C$ for OP-490G, unless otherwise noted.

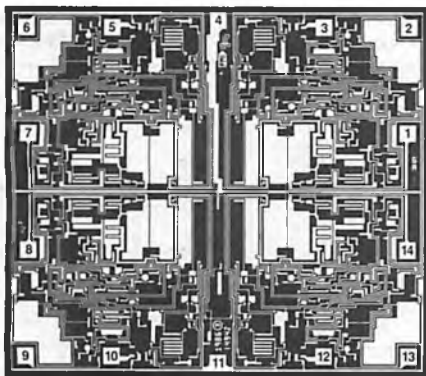
PARAMETER	SYMBOL	CONDITIONS	OP-490E			OP-490F			OP-490G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.32	0.6	—	0.6	1.35	—	0.8	1.5	mV
Average Input Offset Voltage Drift	TCV_{OS}	$V_S = \pm 15V$	—	2	5	—	4	—	—	4	—	$\mu V/^\circ C$
Input Offset Current	I_{OS}	$V_{CM} = 0V$	—	0.8	3	—	1.0	5	—	1.3	7	nA
Input Bias Current	I_B	$V_{CM} = 0V$	—	4.4	15	—	4.4	20	—	4.4	25	nA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_O = \pm 10V$										V/mV
		$R_L = 100k\Omega$	500	600	—	350	700	—	300	600	—	
		$R_L = 10k\Omega$	250	400	—	175	350	—	150	250	—	
		$R_L = 2k\Omega$	100	200	—	75	150	—	75	125	—	
		$V^+ = 5V, V^- = 0V,$ $1V < V_O < 4V$										
Input Voltage Range	IVR	$R_L = 100k\Omega$	150	280	—	100	220	—	80	160	—	V
		$R_L = 10k\Omega$	75	140	—	50	110	—	40	90	—	
Output Voltage Swing	V_O	$V^+ = 5V, V^- = 0V$ $V_S = \pm 15V$ (Note 1)	0/3.5	—	—	0/3.5	—	—	0/3.5	—	—	V
			—15/13.5	—	—	—15/13.5	—	—	—15/13.5	—	—	
		$V_S = \pm 15V$										
		$R_L = 10k\Omega$	± 13	± 14	—	± 13	± 14	—	± 13	± 14	—	
		$R_L = 2k\Omega$	± 10	± 11	—	± 10	± 11	—	± 10	± 11	—	
Output Voltage Swing	V_{OH}	$V^+ = 5V, V^- = 0V$ $R_L = 2k\Omega$	3.9	4.1	—	3.9	4.1	—	3.9	4.1	—	V
Common Mode Rejection	CMR	$V^+ = 5V, V^- = 0V,$ $0V < V_{CM} < 3.5V$	90	110	—	80	100	—	80	100	—	dB
		$V_S = \pm 15V,$ $-15V < V_{CM} < 13.5V$	100	120	—	90	110	—	90	110	—	
Power Supply Rejection Ratio	PSRR		—	1.0	5.6	—	3.2	10	—	5.6	17.8	$\mu V/V$
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 1.5V$	—	65	100	—	65	100	—	60	100	μA
		$V_S = \pm 15V$ No Load	—	80	120	—	80	120	—	75	120	

NOTE:

1. Guaranteed by CMR test.



DICE CHARACTERISTICS



DIE SIZE 0.139×0.121 inch, 16,819 sq. mils
(3.53×3.07 mm, 10.84 sq. mm)

- | | |
|----------|-----------|
| 1. OUT A | 8. OUT C |
| 2. -IN A | 9. -IN C |
| 3. +IN A | 10. +IN C |
| 4. V+ | 11. V- |
| 5. +IN B | 12. +IN D |
| 6. -IN B | 13. -IN D |
| 7. OUT B | 14. OUT D |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 1.5V$ to $\pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

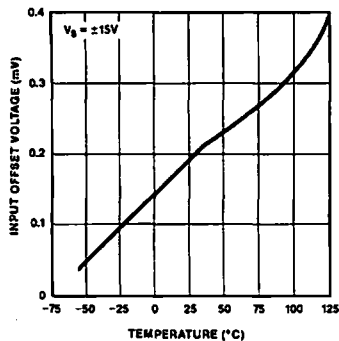
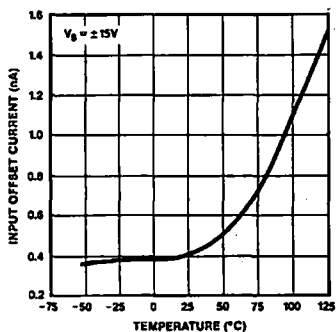
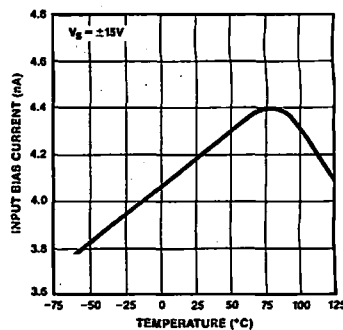
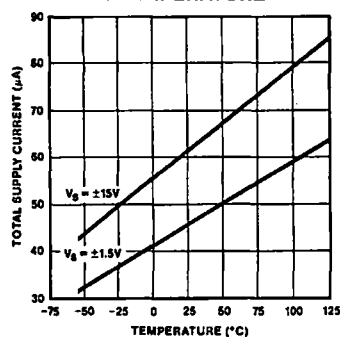
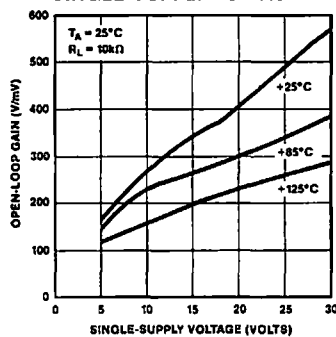
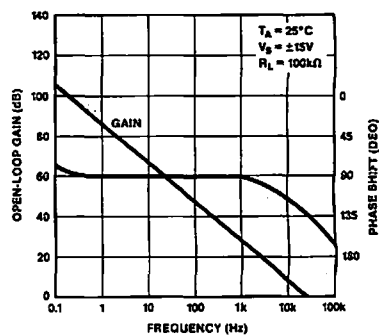
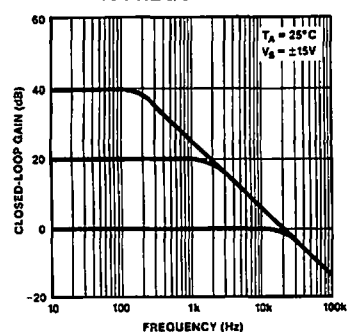
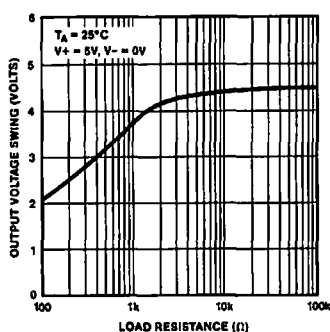
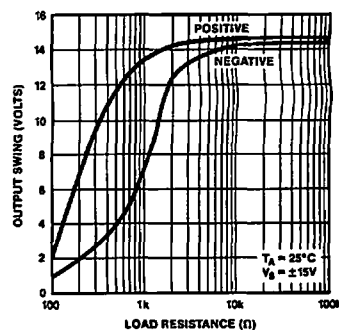
		OP-490GBC	
PARAMETER	SYMBOL	CONDITIONS	LIMIT
Input Offset Voltage	V_{OS}		0.75
Input Offset Current	I_{OS}	$V_{CM} = 0V$	5
Input Bias Current	I_B	$V_{CM} = 0V$	20
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_O = \pm 10V$ $R_L = 100k\Omega$	500
		$R_L = 10k\Omega$	250
		$V^+ = 5V$, $V^- = 0V$, $1V < V_O < 4V$, $R_L = 100k\Omega$	125
Input Voltage Range	IVR	$V^+ = 5V$, $V^- = 0V$ $V_S = \pm 15V$ (Note 1)	0/4 -15/13.5
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 13.5 ± 10.5
	V_{OH}	$V^+ = 5V$, $V^- = 0V$ $R_L = 2k\Omega$	4.0
	V_{OL}	$V^+ = 5V$, $V^- = 0V$ $R_L = 10k\Omega$	500
			μV MAX
Common Mode Rejection	CMR	$V^+ = 5V$, $V^- = 0V$, $0V < V_{CM} < 4V$	80
		$V_S = \pm 15V$, $-15V < V_{CM} < 13.5V$	90
Power Supply Rejection Ratio	PSRR		10
Supply Current (All Amplifiers)	I_{SY}	$V_S = \pm 15V$, No Load	80

NOTES:

1. Guaranteed by CMR test.

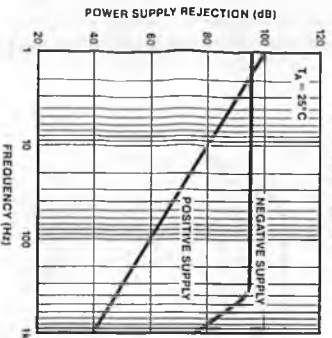
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

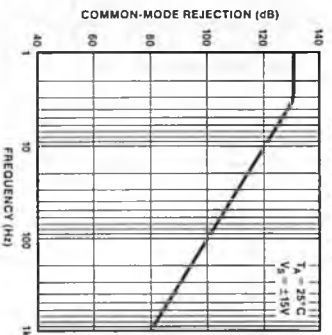
INPUT OFFSET VOLTAGE
vs TEMPERATUREINPUT OFFSET CURRENT
vs TEMPERATUREINPUT BIAS CURRENT
vs TEMPERATURETOTAL SUPPLY CURRENT
vs TEMPERATUREOPEN-LOOP GAIN vs
SINGLE-SUPPLY VOLTAGEOPEN-LOOP GAIN AND
PHASE SHIFT vs FREQUENCYCLOSED-LOOP GAIN
vs FREQUENCYOUTPUT VOLTAGE SWING
vs LOAD RESISTANCEOUTPUT VOLTAGE SWING
vs LOAD RESISTANCE

TYPICAL PERFORMANCE CHARACTERISTICS

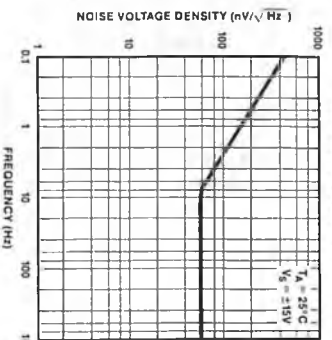
POWER SUPPLY REJECTION
VS FREQUENCY



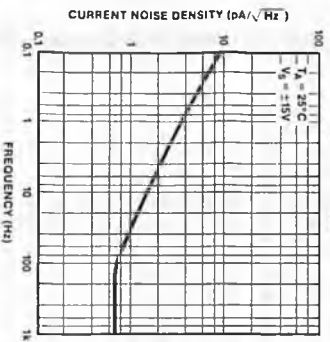
COMMON-MODE REJECTION
VS FREQUENCY



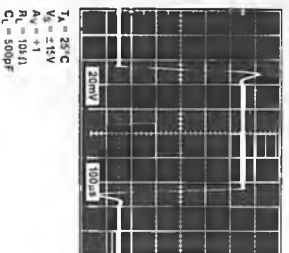
NOISE VOLTAGE DENSITY
VS FREQUENCY



CURRENT NOISE DENSITY
VS FREQUENCY

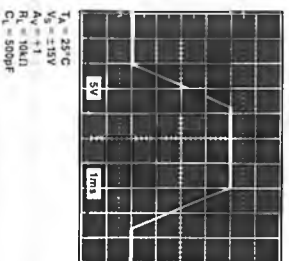


SMALL-SIGNAL
TRANSIENT RESPONSE



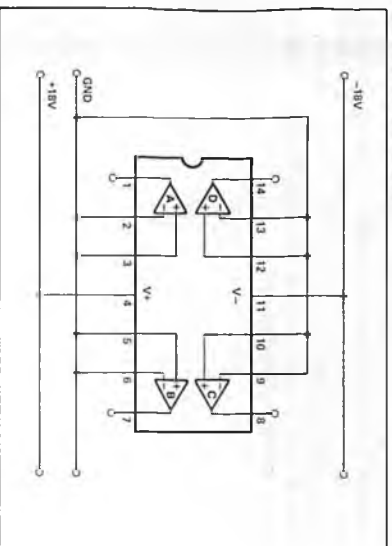
TA = 25°C
VS = ±15V
AV = 1
RL = 10kΩ
CL = 100pF

LARGE-SIGNAL
TRANSIENT RESPONSE

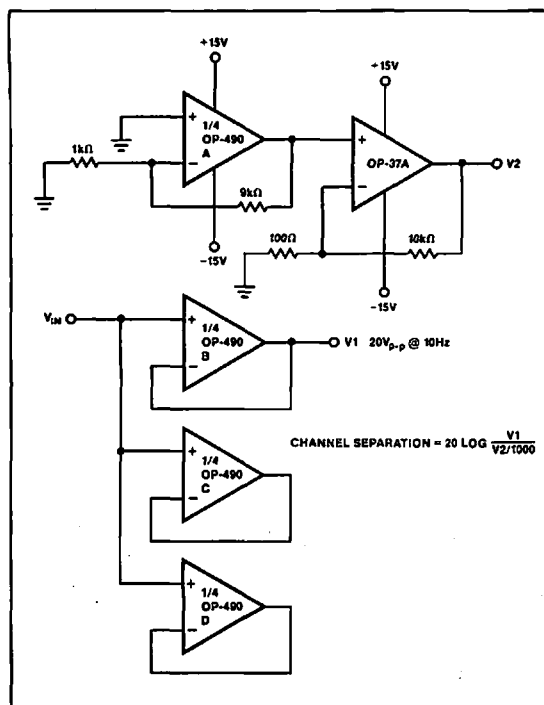


TA = 25°C
VS = ±15V
AV = 1
RL = 10kΩ
CL = 500pF

BURN-IN CIRCUIT



CHANNEL SEPARATION TEST CIRCUIT



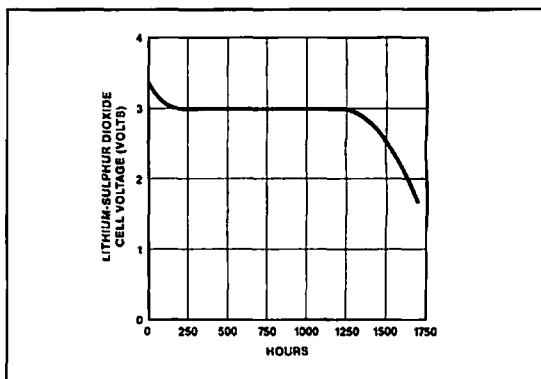
APPLICATIONS INFORMATION

BATTERY-POWERED APPLICATIONS

The OP-490 can be operated on a minimum supply voltage of +1.6V, or with dual supplies $\pm 0.8V$, and draws only $60\mu A$ of supply current. In many battery-powered circuits, the OP-490 can be continuously operated for hundreds of hours before requiring battery replacement, reducing equipment downtime and operating cost.

High-performance portable equipment and instruments frequently use lithium cells because of their long shelf-life, light weight, and high energy density relative to older primary cells. Most lithium cells have a nominal output voltage of 3V and are noted for a flat discharge characteristic. The low

FIGURE 1: Lithium-Sulphur Dioxide Cell Discharge Characteristic With OP-490 and 100k Ω Loads



supply voltage requirement of the OP-490, combined with the flat discharge characteristic of the lithium cell, indicates that the OP-490 can be operated over the entire useful life of the cell. Figure 1 shows the typical discharge characteristic of a 1Ah lithium cell powering an OP-490 with each amplifier, in turn, driving full output swing into a 100k Ω load.

SINGLE-SUPPLY OUTPUT VOLTAGE RANGE

In single-supply operation the OP-490's input and output ranges include ground. This allows true "zero-in, zero-out" operation. The output stage provides an active pull-down to around 0.8V above ground. Below this level, a load resistance of up to 1M Ω to ground is required to pull the output down to zero.

In the region from ground to 0.8V the OP-490 has voltage gain equal to the data sheet specification. Output current source capability is maintained over the entire voltage range including ground.

INPUT VOLTAGE PROTECTION

The OP-490 uses a PNP input stage with protection resistors in series with the inverting and noninverting inputs. The high breakdown of the PNP transistors coupled with the protection resistors provides a large amount of input protection, allowing the inputs to be taken 20V beyond either supply without damaging the amplifier.

MICROPOWER VOLTAGE-CONTROLLED OSCILLATOR

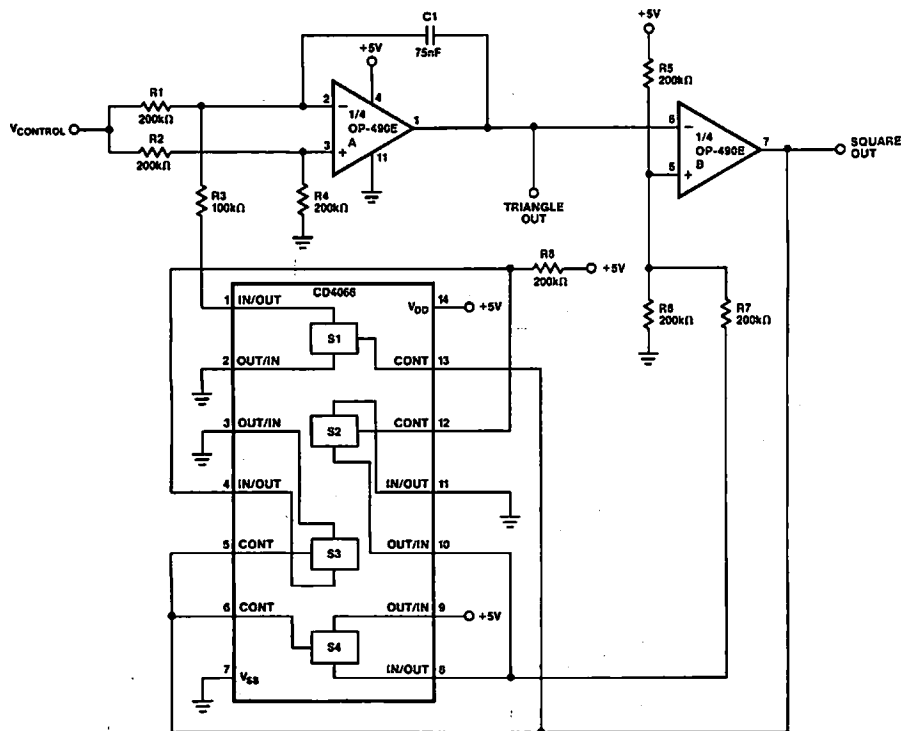
An OP-490 in combination with an inexpensive quad CMOS switch comprise the precision VCO of Figure 2. This circuit provides triangle and square wave outputs and draws only 75 μ A from a single 5V supply. A acts as an integrator; S1 switches the charging current symmetrically to yield positive and negative ramps. The integrator is bounded by B which acts as a Schmitt trigger with a precise hysteresis of 1.67 volts, set by resistors R5, R6, and R7, and associated CMOS

switches. The resulting output of A is a triangle wave with upper and lower levels of 3.33 and 1.67 volts. The output of B is a square wave with almost rail-to-rail swing. With the components shown, frequency of operation is given by the equation:

$$f_{OUT} = V_{CONTROL} \text{ (Volts)} \times 10\text{Hz/V}$$

but this is easily changed by varying C1. The circuit operates well up to a few hundred hertz.

FIGURE 2: Micropower Voltage Controlled Oscillator



MICROPOWER SINGLE-SUPPLY QUAD VOLTAGE-OUTPUT 8-BIT DAC

The circuit of Figure 3 uses the DAC-8408 CMOS quad 8-bit DAC, and the OP-490 to form a single-supply quad voltage-output DAC with a supply drain of only 140 μ A. The DAC-8408

is used in the voltage switching mode and each DAC has an output resistance ($\approx 10k\Omega$) independent of the digital input code. The output amplifiers act as buffers to avoid loading the DACs. The 100k Ω resistors insure that the OP-490 outputs will swing below 0.8V when required.

FIGURE 3: Micropower Single-Supply Quad Voltage-Output 8-Bit DAC

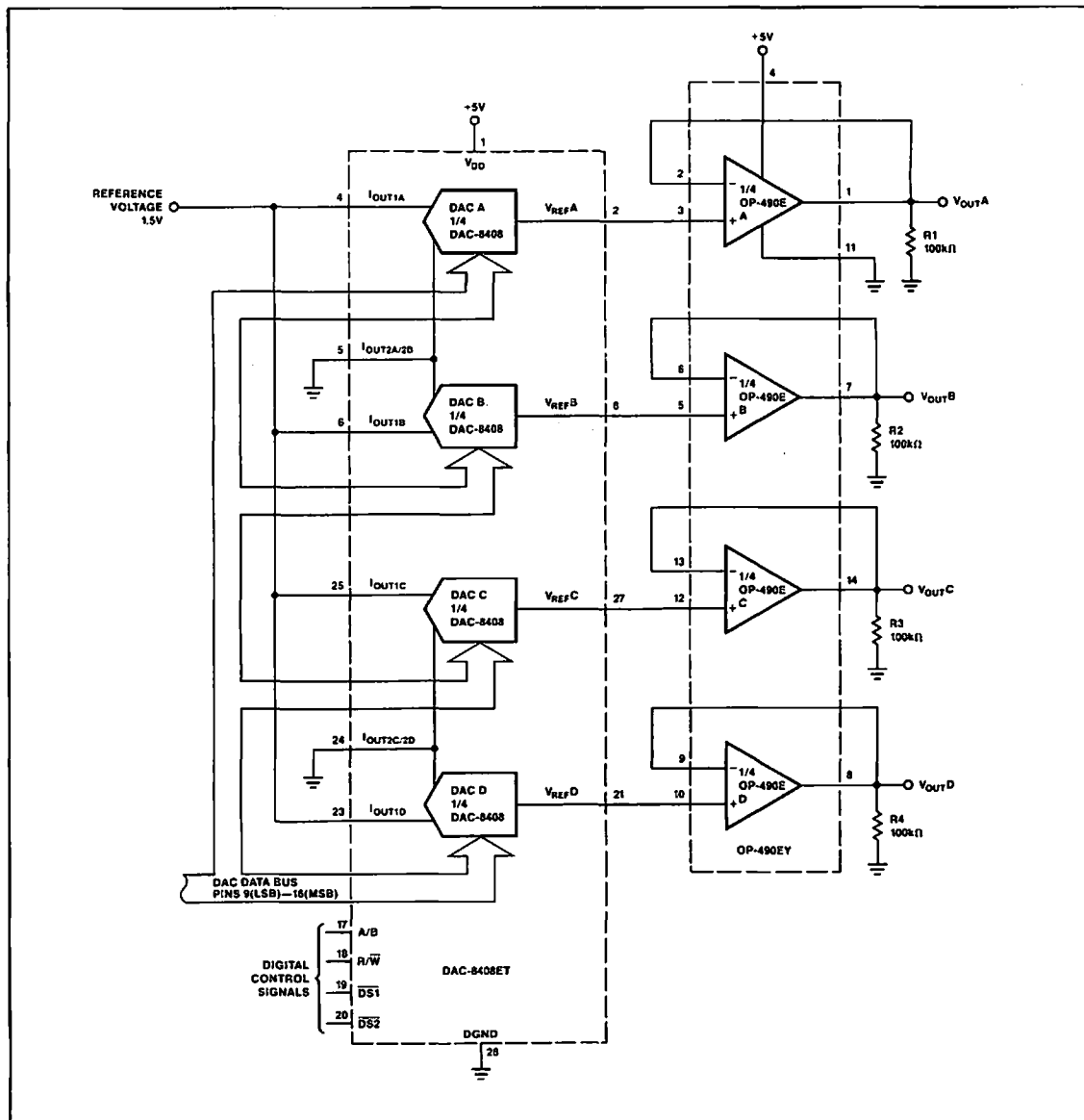
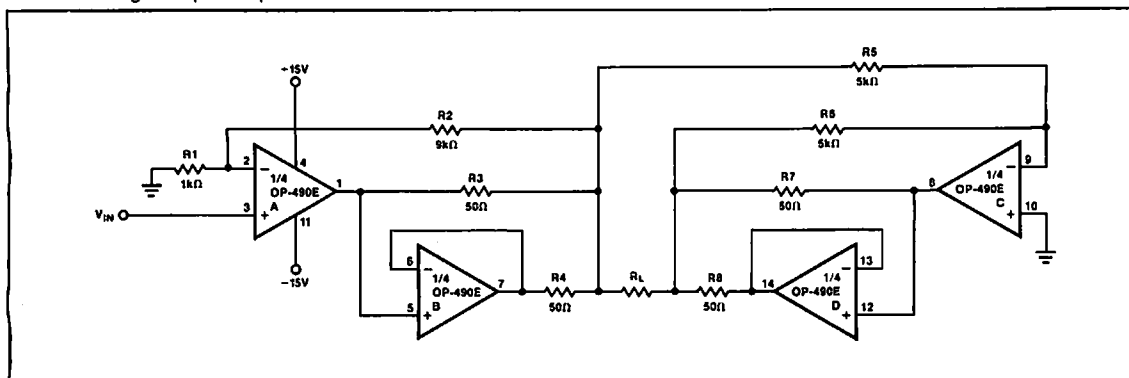


FIGURE 4: High Output Amplifier

**HIGH OUTPUT AMPLIFIER**

The amplifier shown in Figure 4 is capable of driving 25V_{p-p} into a 1kΩ load. Design of the amplifier is based on a bridge configuration. A amplifies the input signal and drives the load with the help of B. Amplifier C is a unity-gain inverter which drives the load with help from D. Gain of the high output amplifier with the component values shown is 10, but can easily be changed by varying R1 or R2.

SINGLE-SUPPLY MICROPOWER QUAD PROGRAMMABLE GAIN AMPLIFIER

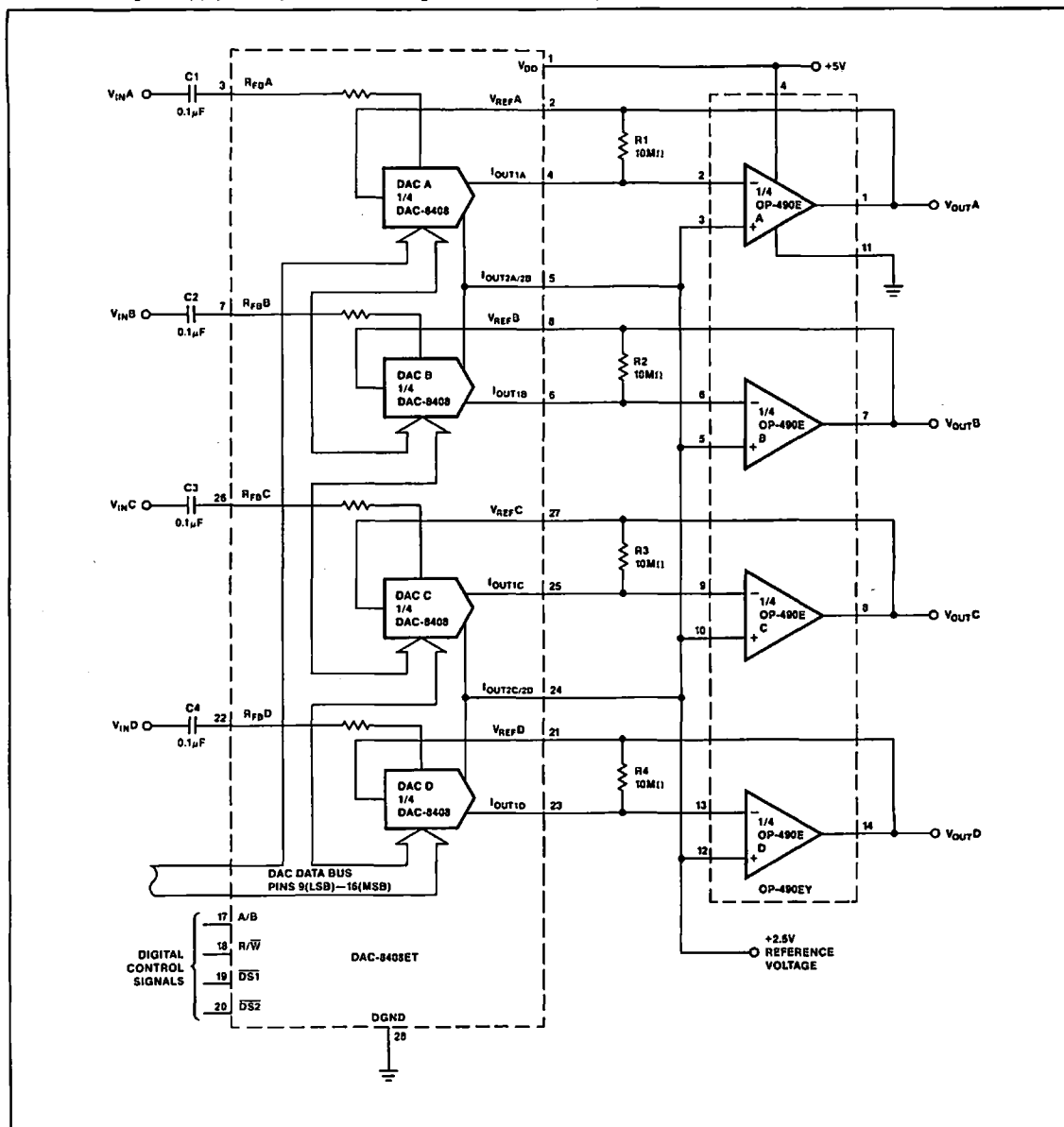
The combination of the quad OP-490 and the DAC-8408 quad 8-bit CMOS DAC, creates a quad programmable gain amplifier with a quiescent supply drain of only 140μA. The digital code present at the DAC, which is easily set by a

microprocessor, determines the ratio between the fixed DAC feedback resistor and the resistance the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{256}{n}$$

where n equals the decimal equivalent of the 8-bit digital code present at the DAC. If the digital code present at the DAC consists of all zeros, the feedback loop will be open causing the op amp output to saturate. The 10MΩ resistors placed in parallel with the DAC feedback loop eliminates this problem with a very small reduction in gain accuracy. The 2.5V reference biases the amplifiers to the center of the linear region providing maximum output swing.

FIGURE 5: Single-Supply Micropower Quad Programmable-Gain Amplifier





PM-108A/PM-2108A

LOW-INPUT-CURRENT OPERATIONAL AMPLIFIERS

PM-108A/PM-208A/PM-308A/PM-108/PM-208/PM-308/PM-2108A/PM-2108

Precision Monolithics Inc.

FEATURES

- Low Offset Current 200pA Max
- Low Bias Current 2nA Max
- Low Power Consumption 18mW Max @ $\pm 15V$
- Wide Supply Range $\pm 3V$ to $\pm 20V$
- High Power-Supply Rejection Ratio 96dB Min
- Low Offset Voltage Drift $5\mu V/^{\circ}C$ Max
- High Common-Mode Input Range $\pm 13.5V$ Min
- High Common-Mode Rejection Ratio 96dB Min
- MIL-STD-883 Processing Models Available
- Silicon-Nitride Passivation

GENERAL DESCRIPTION

The PM-108A series of precision operational amplifiers feature very low input offset and bias currents. Although

directly interchangeable with industry-standard types, Precision Monolithics' advanced processing provides the PM-108A series with a significant improvement in input noise voltage. Low supply current drain over a wide power-supply range makes the PM-108A attractive in battery operated and other low-power applications. The low bias current provides excellent performance with piezoelectric and capacitive transducers and in such high-impedance circuits as long-period integrators and sample-and-holds. For improved performance see OP-08, OP-12, OP-20, OP-21, and OP-22.

The PM-2108A contains two superbeta, PM-108A op amps in a single 16-pin DIP. Compared to the single PM-108A types, this model offers higher packaging density, closer thermal tracking between the two amplifiers, and reduced insertion cost.

5

ORDERING INFORMATION†

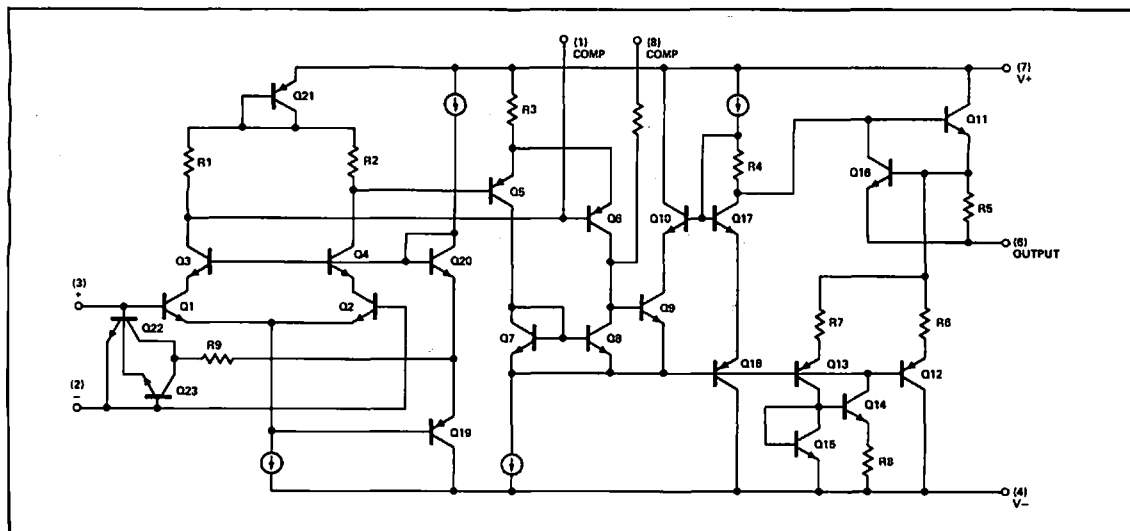
T _A = 25°C V _{OS} MAX (mV)	PACKAGE					OPERATING TEMPERATURE RANGE
	HERMETIC				PLASTIC DIP 8-PIN	
	TD-99 8-PIN	DIP		LCC		
		8-PIN	16-PIN			
0.5	PM108AJ/883	PM108AZ*	PM2108AQ	PM108ARC/883	—	MIL
0.5	PM208AJ	PM208AZ	—	—	—	IND
0.5	PM308AJ	PM308AZ	—	—	PM308AP	COM
2.0	PM108J/883	PM108Z*	PM2108Q	—	—	MIL
2.0	PM208J	PM208Z	—	—	—	IND
7.5	PM308J	PM308Z	—	—	—	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in

cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

SIMPLIFIED SCHEMATIC (Pin numbers for PM-108 only. Circuit is 1/2 2108)



**ABSOLUTE MAXIMUM RATINGS****Supply Voltage**

PM-108A, PM-108, PM-208A, PM-208,

PM-2108A, PM-2108, PM-108ARC $\pm 20V$ PM-308A, PM-308 $\pm 18V$

Internal Power Dissipation (Note 1) 500mW

Differential Input Current (Note 2) $\pm 10mA$ Input Voltage (Note 3) $\pm 15V$

Output Short-Circuit Duration Indefinite

Operating Temperature Range

PM-108A, PM-108, PM-2108A,

PM-2108, PM-108ARC $-55^{\circ}C$ to $+125^{\circ}C$ PM-208A, PM-208 $-25^{\circ}C$ to $+85^{\circ}C$ PM-308A, PM-308 $0^{\circ}C$ to $+70^{\circ}C$ **Storage Temperature Range**(Q-, J-, Z- or ARC-Package) $-65^{\circ}C$ to $+150^{\circ}C$ (P-Package) $-65^{\circ}C$ to $+125^{\circ}C$ Lead Temperature Range (Soldering, 60 sec) $300^{\circ}C$ **NOTES:**

1. Maximum package power dissipation vs. ambient temperature.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	$80^{\circ}C$	$7.1mW/^{\circ}C$
Plastic 8-Pin DIP (P)	$36^{\circ}C$	$5.6mW/^{\circ}C$
Hermetic 8-Pin DIP (Z)	$75^{\circ}C$	$6.7mW/^{\circ}C$
Hermetic 16-Pin DIP (Q)	$100^{\circ}C$	$10.0mW/^{\circ}C$
LCC (RC)	$80^{\circ}C$	$7.8mW/^{\circ}C$

2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, if a differential input voltage in excess of 1V is applied between the inputs, excessive current will flow, unless some limiting resistance is provided.

3. For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS at $\pm 5V \leq V_S \leq \pm 20V$ and $T_A = 25^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-108A/PM-2108A PM-208A			PM-108/PM-2108 PM-208			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.3	0.5	—	0.7	2.0	mV
Input Offset Current	I_{OS}		—	0.05	0.2	—	0.05	0.2	nA
Input Bias Current	I_B		—	0.8	2.0	—	0.8	2.0	nA
Input Resistance	R_{IN}	(Note 1)	30	70	—	30	70	—	M Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10k\Omega$	80	300	—	50	300	—	V/mV
Supply Current	I_{SV}	$I_{OUT} = 0$, $V_{OUT} = 0$, Each Amplifier	—	0.3	0.6	—	0.3	0.6	mA

ELECTRICAL CHARACTERISTICS at $\pm 5V \leq V_S \leq \pm 20V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ for PM-108A, PM-108, PM-2108A and PM-2108, $-25^{\circ}C \leq T_A \leq +85^{\circ}C$ for PM-208A, PM-208, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-108A/PM-2108A PM-208A			PM-108/PM-2108 PM-208			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.4	1.0	—	1.0	3.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 2)	—	1	5	—	3	15	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}		—	0.1	0.4	—	0.1	0.4	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	—	0.5	2.5	—	0.5	2.5	$pA/^{\circ}C$
Input Bias Current	I_B		—	1	3	—	1	3	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10k\Omega$	40	200	—	25	200	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$	± 13	± 14	—	± 13	± 14	—	V
Input Voltage Range	IVR	$V_S = \pm 15V$	± 13.5	—	—	± 13.5	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 15V$, $V_{CM} = \pm 13.5V$	96	110	—	85	100	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 20V$	—	3	15	—	15	100	$\mu V/V$
Supply Current	I_{SV}	$V_{OUT} = 0$, $T_A = MAX$, Each Amplifier	—	0.15	0.4	—	0.15	0.4	mA

NOTES:

1. Guaranteed by input bias current.

2. Sample tested.

**ELECTRICAL CHARACTERISTICS** at $\pm 5V \leq V_S \leq \pm 15V$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

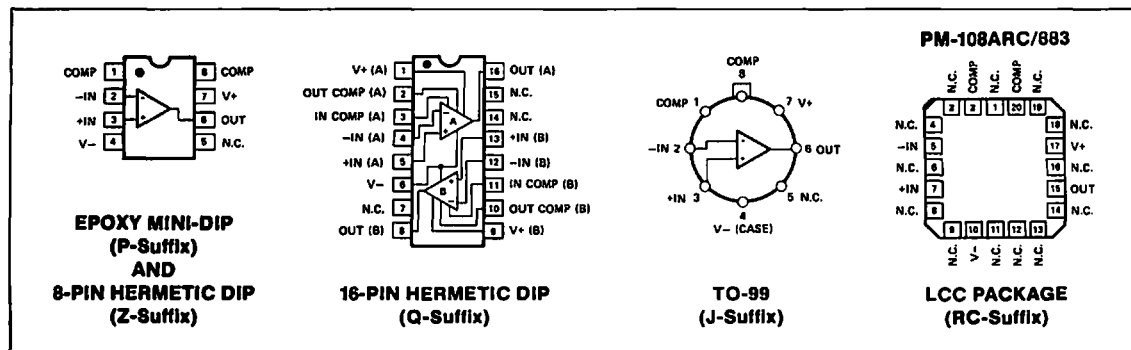
PARAMETER	SYMBOL	CONDITIONS	PM-308A			PM-308			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.3	0.5	—	2.0	7.5	mV
Input Offset Current	I_{OS}		—	0.2	1.0	—	0.2	1.0	nA
Input Bias Current	I_B		—	1.5	7.0	—	1.5	7.0	nA
Input Resistance	R_{IN}	(Note 1)	10	40	—	10	40	—	M Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10k\Omega$	80	300	—	25	300	—	V/mV
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_{OUT} = 0$, Each Amplifier	—	0.3	0.8	—	0.3	0.8	mA

ELECTRICAL CHARACTERISTICS at $\pm 5V \leq V_S \leq \pm 15V$ and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$, unless otherwise noted.

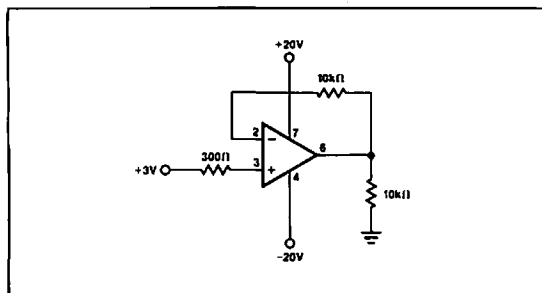
PARAMETER	SYMBOL	CONDITIONS	PM-308A			PM-308			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}		—	0.4	0.73	—	3.0	10.0	mV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	1	5	—	6	30	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{OS}		—	0.3	1.5	—	0.3	1.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	2	10	—	2	10	$\text{pA}/^\circ\text{C}$
Input Bias Current	I_B		—	2	10	—	2	10	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 10k\Omega$	60	200	—	15	100	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$	± 13	± 14	—	± 13	± 14	—	V
Input Voltage Range	IVR	$V_S = \pm 15V$	± 14	—	—	± 13	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	96	110	—	80	100	—	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	3	15	—	15	100	$\mu\text{V}/V$
Supply Current	I_{SY}	$V_{OUT} = 0$, $T_A = \text{MAX}$, Each Amplifier	—	0.23	—	—	0.23	—	mA

NOTE:

1. Guaranteed by Input bias current.

PIN CONNECTIONS

BURN-IN CIRCUIT

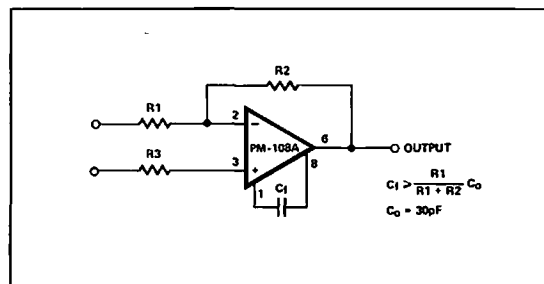


APPLICATIONS INFORMATION

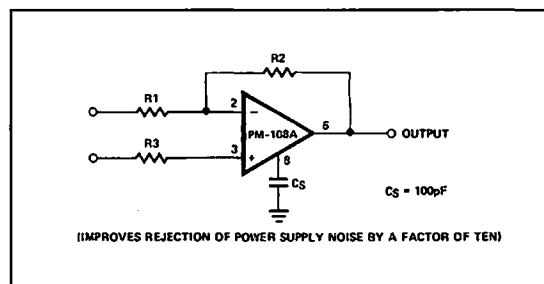
The PM-108A series has very low input offset and bias currents; the user is cautioned that printed circuit board leakages can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is required to achieve the PM-108A's rated performance. It is suggested that board leakage be minimized by encircling the input pins with a guard ring maintained at a potential close to that of the inputs. The guard ring should be driven by a low impedance source such as an amplifier's output or ground.

COMPENSATION CIRCUITS

STANDARD



ALTERNATE





PM-148/PM-248

QUAD 741
OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

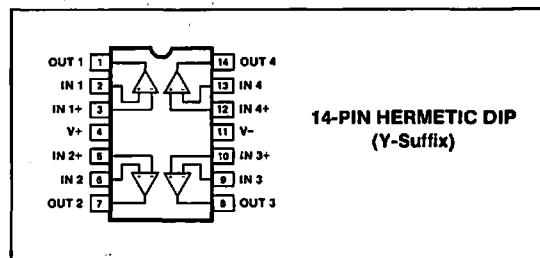
FEATURES

Improved Specifications Over Industry Standard LM148

- Input Offset Voltage 2.5mV Max
- Input Offset Current 10nA Max
- Input Bias Current 75nA Max
- Small Signal Bandwidth 0.8MHz Typ
- Common-Mode Rejection Ratio 105dB Typ
- Power Supply Rejection Ratio 115dB Typ
- Phase Margin 80° Typ

Fully Specified Over Military and Industrial Temperature Range

PIN CONNECTIONS



ORDERING INFORMATION†

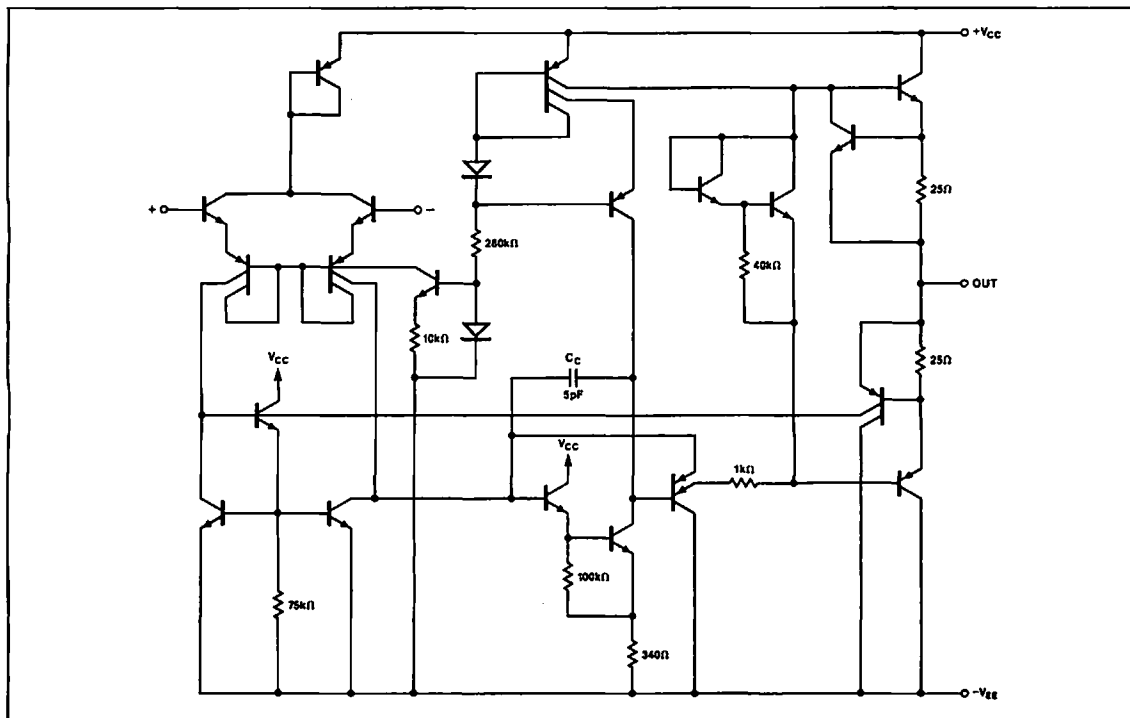
V _{OS} MAX (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
2.5	PM-148Y	MIL
2.5	PM-248Y	IND

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The PM-148 is Precision Monolithics' improved version of the industry-standard LM148 quad 741, high gain, internally compensated, low-power operational amplifier, offered over the full military and industrial temperature ranges. The PM-148 provides functional characteristics identical to the LM148 and is a pin-for-pin replacement with significant improvements on the key parameters of input offset voltage, input bias current, and input offset current.

SIMPLIFIED SCHEMATIC (One of Four Amplifiers)





Excellent isolation between amplifiers is achieved by independently biasing each amplifier and using layout techniques that minimize thermal coupling.

The PM-148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required. The improved performance of the PM-148 allows immediate upgrading of LM148 applications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage $\pm 22V$
Differential Input Voltage $\pm 44V$

Input Voltage $\pm 22V$
Output Short Circuit Duration (Note 1) Continuous
Power Dissipation (P_d at $25^\circ C$) 900mW
Thermal Resistance (θ_{JA}) $100^\circ C/W$
Maximum Junction Temperature $150^\circ C$
Operating Temperature Range

PM-148 $-55^\circ C \leq T_A \leq +125^\circ C$

PM-248 $-25^\circ C \leq T_A \leq +85^\circ C$

Storage Temperature Range $-65^\circ C$ to $150^\circ C$

Lead Temperature Range $300^\circ C$

NOTE:

- Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-148/PM-248			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.1	2.5	mV
Input Offset Current	I_{OS}		—	0.1	10	nA
Input Bias Current	I_B		—	20	75	nA
Input Resistance	R_{IN}	(Note 1)	0.8	2.5	—	M Ω
Supply Current	I_{SY}	$V_S = \pm 15V$	—	2.4	3.6	mA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	50	150	—	V/mV
Positive Short Circuit Current	I_{SC+}		—	18	—	mA
Negative Short Circuit Current	I_{SC-}		—	36	—	mA
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$	80	105	—	dB
Input Voltage Range	IVR	$V_S = \pm 15V$	± 12	—	—	V
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	85	115	—	dB
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 12 ± 11	± 13 ± 12.5	—	V
Slew Rate	SR	$A_V = 1$	—	0.4	—	V/ μs
Small Signal Bandwidth	BW		—	0.8	—	MHz
Phase Margin	0°	$A_V = 1$	—	80	—	degrees

NOTE:

- Guaranteed by formula $R_{IN} = \frac{4KT}{qI_B}$.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

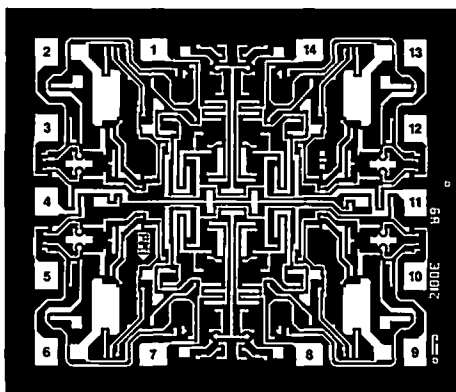
PARAMETER	SYMBOL	CONDITIONS	PM-148			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	0.6	6	mV
Input Offset Current	I_{OS}		—	0.5	25	nA
Input Bias Current	I_B		—	30	100	nA
Supply Current	I_{SV}	$V_S = \pm 15V$ $T_A \leq +125^\circ C$ $T_A \geq -55^\circ C$	—	2.4	3.6	mA
			—	3.5	4.5	
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	25	75	—	V/mV
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$	80	100	—	dB
Power Supply Rejection Ratio	PSRR		80	95	—	dB
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 12	± 13	—	V
			± 10	± 12	—	
Input Voltage Range	IVR	$V_S = \pm 15V$	± 12	—	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-248			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	—	—	7.5	mV
Input Offset Current	I_{OS}		—	—	125	nA
Input Bias Current	I_B		—	—	500	nA
Supply Current	I_{SV}	$V_S = \pm 15V$	—	2.4	4.5	mA
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	15	—	—	V/mV
			—	—	—	
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$	70	90	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	77	96	—	dB
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 12	± 13	—	V
			± 10	± 12	—	
Input Voltage Range	IVR	$V_S = \pm 15V$	± 12	—	—	V



DICE CHARACTERISTICS



DIE SIZE 0.064×0.075 inch, 4800 sq. mils
 $(1.62 \times 1.90$ mm, 3.08 sq. mm)

1. OUT 1
2. IN 1
3. IN 1+
4. V+
5. IN 2+
6. IN 2
7. OUT 2
8. OUT 3
9. IN 3
10. IN 3+
11. V-
12. IN 4+
13. IN 4
14. OUT 4

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

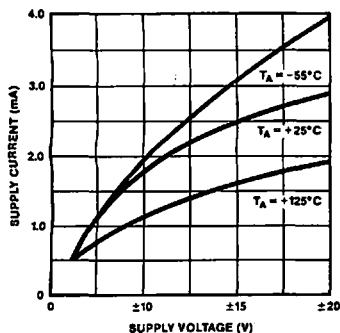
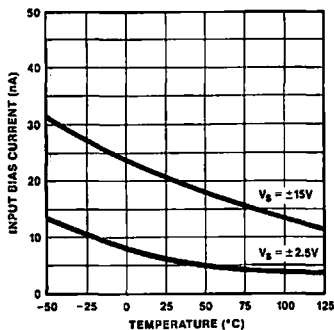
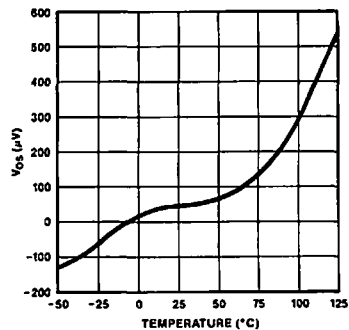
WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ for PM-148GBC, $T_A = 125^\circ C$ for PM-148GTBC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-148GBC LIMIT	PM-148GTBC LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 10k\Omega$	2.5	6.0	mV MAX
Input Offset Current	I_{OS}		10	25	nA MAX
Input Bias Current	I_B		75	100	nA MAX
Supply Current	I_{SY}	$V_S = \pm 15V$	3.6	3.6	mA MAX
Large Signal Voltage Gain	A_{VO}	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	50	25	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	$R_S \leq 10k\Omega$	85	80	dB MIN
Output Voltage Swing	V_O	$V_S = \pm 15V$, $R_L = 10k\Omega$ $R_L = 2k\Omega$	± 12 ± 11	± 12 ± 10	V MIN
Input Voltage Range	IVR	$V_S = \pm 15V$	± 12	± 12	V MIN

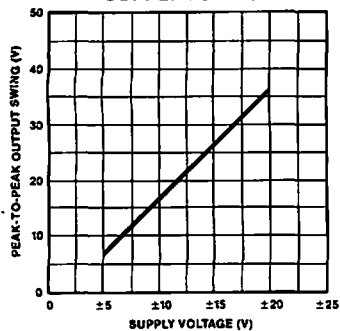
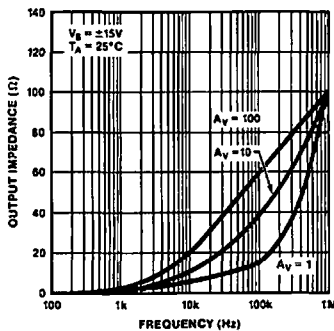
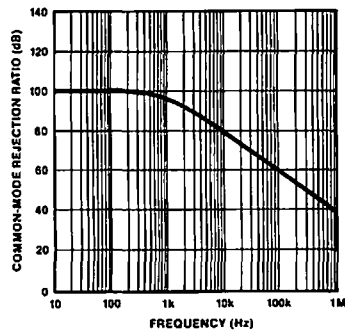
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

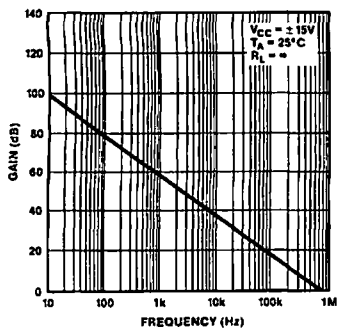
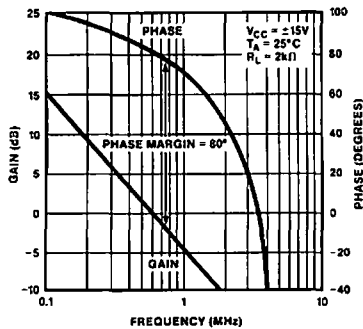
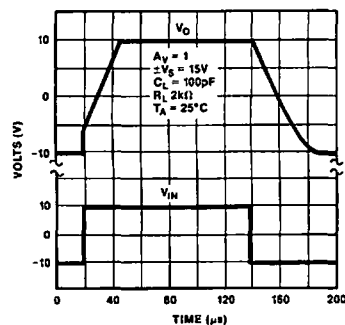
TYPICAL PERFORMANCE CHARACTERISTICS

 SUPPLY CURRENT vs
SUPPLY VOLTAGE

 INPUT BIAS CURRENT
vs TEMPERATURE

 INPUT OFFSET VOLTAGE
vs TEMPERATURE


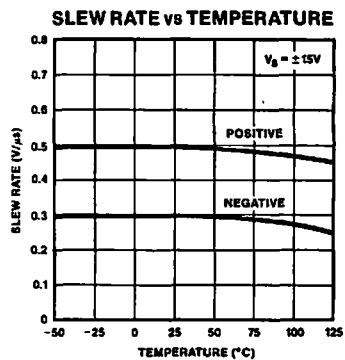
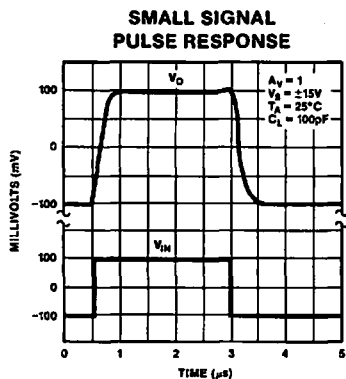
5

 VOLTAGE SWING vs
SUPPLY VOLTAGE

 OUTPUT IMPEDANCE
vs FREQUENCY

 COMMON-MODE
REJECTION RATIO
vs FREQUENCY


OPERATIONAL AMPLIFIERS

 OPEN-LOOP
FREQUENCY RESPONSE
vs GAIN

 GAIN AND PHASE
vs FREQUENCY

 LARGE SIGNAL
PULSE RESPONSE


TYPICAL PERFORMANCE CHARACTERISTICS





PM-155A/PM-156A/PM-157A

MONOLITHIC JFET-INPUT
OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

LOW SUPPLY CURRENT — PM-155A/PM-355A/PM-155
GENERAL PURPOSE — PM-156A/PM-356A/PM-156
WIDE-BANDWIDTH — PM-157A/PM-357A/PM-157

FEATURES

All Devices

- Low Input Bias and Offset Currents
- Low Input Offset Voltage 1.0mV
- Low Input Offset Voltage Drift $3.0\mu\text{V}/^\circ\text{C}$
- Low Input Noise Current $0.01\text{pA}/\sqrt{\text{Hz}}$
- High Common-Mode Rejection Ratio 100dB

- PM-155 (Only) LF155 Replacement
- Low Supply Current 2mA

- PM-156 (Only) LF156 Replacement
- High Slew Rate $12\text{V}/\mu\text{sec}$
- Fast Settling to $\pm 0.01\%$ $4.0\mu\text{sec}$

- PM-157 (Only) LF157 Replacement
- Wide-Bandwidth Decompensated ($A_{VCL}=5$ Min) ... 20MHz
- High Slew Rate $45\text{V}/\mu\text{sec}$
- Fast Settling to $\pm 0.01\%$ $4.0\mu\text{sec}$

GENERAL DESCRIPTION

The PM JFET-input series provides low input current, high slew rate, and direct interchangeability with LF155, 156, and 157 types. These operational amplifiers use a new process which allows fabrication of matched JFET transistors and standard bipolar transistors on the same chip. High accuracy and low cost make the PM JFET-input series useful in new designs and as replacements for modular and hybrid types. Unlike many designs, nulling the input offset voltage does not degrade common-mode rejection ratio or input offset voltage drift. Low input voltage noise and current noise plus a low 1/f noise corner frequency allow these amplifiers to be used in a variety of low noise, wide-bandwidth applications.

Dynamic specifications for the PM-155 include a slew rate of $5\text{V}/\mu\text{s}$, a 2.5MHz gain bandwidth product, and settling time to within $\pm 0.01\%$ of final value in $5.0\mu\text{s}$. The PM-156 has a slew rate of $12\text{V}/\mu\text{s}$ and a settling time of $4.0\mu\text{s}$ to $\pm 0.01\%$ of final value.

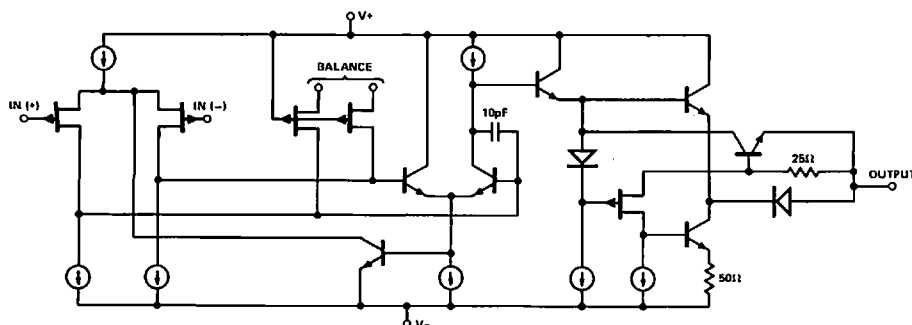
The PM-157 is a very fast decompensated device. This results in a $45\text{V}/\mu\text{s}$ slew rate, a 20MHz gain bandwidth product, and a settling time of $4.0\mu\text{s}$. Decompensation requires a minimum closed-loop gain of five because of stability considerations.

For improved performance, see the OP-15/OP-16/OP-17 data sheet. For duals, see the OP-215 data sheet.

5

OPERATIONAL AMPLIFIERS

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS****Supply Voltage**

PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157,
PM-355A, PM-356A, PM-357A $\pm 22\text{V}$

Internal Power Dissipation

PM-155A, PM-156A, PM-157, PM-155, PM-156,
PM-157 670mW
PM-355A, PM-356A, PM-357A 500mW
(Derate based on a thermal resistance of 150°C/W
junction to ambient or 45°C/W junction to case.)

Operating Temperature Range

PM-155A, PM-156A, PM-157A, PM-155, PM-156,
PM-157 -55°C to $+125^\circ\text{C}$
PM-355A, PM-356A, PM-357A 0°C to $+70^\circ\text{C}$

Maximum Junction Temperature (T_J)

PM-155A, PM-156A, PM-157A, PM-155, PM-156,
PM-157 $+150^\circ\text{C}$
PM-355A, PM-356A, PM-357A $+100^\circ\text{C}$

Differential Input Voltage

PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157,
PM-355A, PM-356A, PM-357A $\pm 40\text{V}$

Input Voltage

PM-155A, PM-156A, PM-157A, PM-155, PM-156, PM-157,
PM-355A, PM-356A, PM-357A $\pm 20\text{V}$

NOTE:

The absolute maximum negative input voltage is equal to the negative power supply voltage.

Output Short-Circuit Duration Indefinite

Storage Temperature Range -65°C to $+150^\circ\text{C}$

Lead Temperature Range (Soldering, 60 sec) $+300^\circ\text{C}$

ELECTRICAL CHARACTERISTICS at $\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ and $T_{\text{HIGH}} = +125^\circ\text{C}$ for PM-155A, PM-156A and PM-157A, $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ and $T_{\text{HIGH}} = +70^\circ\text{C}$ for PM-355A, PM-356A and PM-357A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-155A/ PM-156A/ PM-157A			PM-355A/ PM-356A/ PM-357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	1.4	2.5	—	1.2	2.3	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	3	5	—	3	5	$\mu\text{V}/^\circ\text{C}$
Change in Input Offset Drift with V_{OS} Adjust	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}}\right)$	$R_S = 50\Omega$	—	0.5	—	—	0.5	—	$\mu\text{V}/^\circ\text{C}$ per mV
Input Offset Current	I_{OS}	$T_J \leq T_{\text{HIGH}}$ (Note 1)	—	4.0	10	—	0.4	1.0	nA
Input Bias Current	I_B	$T_J \leq T_{\text{HIGH}}$ (Note 1)	—	± 10	± 25	—	± 2	± 5	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	25	75	—	25	75	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$ $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$	± 12	± 13	—	± 12	± 13	—	V
			± 10	± 12	—	± 10	± 12	—	
Input Voltage Range	IVR	$V_S = \pm 15\text{V}$	± 10.4	$+15.1$ -12.0	—	± 10.4	$+15.1$ -12.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm \text{IVR}$	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	—	10	57	$\mu\text{V/V}$

NOTES:

- PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

**ELECTRICAL CHARACTERISTICS** at $\pm 15V \leq V_S \leq \pm 20V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-155A/ PM-156A/ PM-157A			PM-355A/ PM-356A/ PM-357A			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage	V_{OS}	$R_B = 50\Omega$	—	1	2	—	1	2	mV	
Input Offset Current	I_{OS}	$T_J = 25^\circ\text{C}$ (Note 1)	—	3	10	—	3	10	pA	
Input Bias Current	I_B	$T_J = 25^\circ\text{C}$ (Note 1)	—	± 30	± 50	—	± 30	± 50	pA	
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	Ω	
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	50	200	—	50	200	—	V/mV	
Supply Current	I_{SY}	$V_S = \pm 15\text{V}$	PM-155	—	2	4	—	2	4	mA
			PM-156/PM-157	—	5	7	—	5	7	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15\text{V}$	PM-155	3	5	—	3	5	—	V/ μs
			PM-156	10	12	—	10	12	—	
		$A_{VCL} = +5$, $V_S = \pm 15\text{V}$	PM-157	40	45	—	40	45	—	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15\text{V}$	PM-155	—	2.5	—	—	2.5	—	MHz
			PM-156	4.0	4.5	—	4.0	4.5	—	
		$A_{VCL} = +5$, $V_S = \pm 15\text{V}$	PM-157	15	20	—	15	20	—	
Settling Time (to $\pm 0.01\%$)	t_S	$V_S = \pm 15\text{V}$ (Note 2)	PM-155	—	5.0	—	—	4.0	—	μs
			PM-156	—	4.0	—	—	1.5	—	
		$V_S = \pm 15\text{V}$ (Note 3)	PM-157	—	4.0	—	—	1.5	—	
Input Noise Voltage	e_n	$R_S = 100\Omega$, $f = 100\text{Hz}$	PM-155	—	25	—	—	25	—	$\text{nV}/\sqrt{\text{Hz}}$
		$R_S = 100\Omega$, $f = 1000\text{Hz}$		—	20	—	—	20	—	
		$R_S = 100\Omega$, $f = 100\text{Hz}$	PM-156/PM-157	—	15	—	—	15	—	
		$R_S = 100\Omega$, $f = 1000\text{Hz}$		—	12	—	—	12	—	
Input Noise Current	i_n	$f = 100\text{Hz}$, $V_S = \pm 15\text{V}$		—	0.01	—	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
		$f = 1000\text{Hz}$, $V_S = \pm 15\text{V}$		—	0.01	—	—	0.01	—	
Input Capacitance	C_{IN}		—	3	—	—	3	—	pF	

NOTES:

- PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Settling time is defined here for a unity gain inverter connection using $2k\Omega$ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
- Settling time is defined here for a $A_V = -5$ connection with $R_F = 2k\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.

**ELECTRICAL CHARACTERISTICS** at $T_A = +25^\circ\text{C}$, $\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$ for PM-155, PM-156 and PM-157, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-155 PM-156 PM-157			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_g = 50\Omega$	—	3	5	mV
Input Offset Current	I_{OS}	$T_j = 25^\circ\text{C}$ (Note 1)	—	3	20	pA
Input Bias Current	I_B	$T_j = 25^\circ\text{C}$ (Note 1)	—	± 30	± 100	pA
Input Resistance	R_{IN}		—	10^{12}	—	Ω
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$	50	200	—	V/mV
Supply Current	I_{SY}	$V_S = \pm 15\text{V}$	PM-155	—	2	mA
			PM-156/PM-157	—	5	
Slew Rate	SR	$A_{VCL} = +1$, $V_S = \pm 15\text{V}$	PM-155	—	5	V/ μs
		$A_{VCL} = +5$, $V_S = \pm 15\text{V}$	PM-156	7.5	12	
Gain Bandwidth Product	GBW	$A_{VCL} = +1$, $V_S = \pm 15\text{V}$	PM-155	—	2.5	MHz
		$A_{VCL} = +5$, $V_S = \pm 15\text{V}$	PM-156	—	5	
		$A_{VCL} = +5$, $V_S = \pm 15\text{V}$	PM-157	—	20	
Settling Time (to $\pm 0.01\%$)	t_S	$V_S = \pm 15\text{V}$ (Note 2)	PM-155	—	5	μs
		$V_S = \pm 15\text{V}$ (Note 3)	PM-156	—	4	
		$V_S = \pm 15\text{V}$ (Note 3)	PM-157	—	4	
Input Noise Voltage	e_n	$R_S = 100\Omega$, $f = 100\text{Hz}$	PM-155	—	25	$\text{nV}/\sqrt{\text{Hz}}$
		$R_S = 100\Omega$, $f = 1000\text{Hz}$	PM-155	—	20	
		$R_S = 100\Omega$, $f = 100\text{Hz}$	PM-156/PM-157	—	15	
		$R_S = 100\Omega$, $f = 1000\text{Hz}$	PM-156/PM-157	—	12	
Input Noise Current	i_n	$f = 100\text{Hz}$, $V_S = \pm 15\text{V}$ $f = 1000\text{Hz}$, $V_S = \pm 15\text{V}$	—	0.01	—	$\text{pA}/\sqrt{\text{Hz}}$
Input Capacitance	C_{IN}		—	3	—	pF

NOTES:

- PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0$.
- Settling time is defined here for a unity gain inverter connection using $2\text{k}\Omega$ resistors. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. See settling time test circuit.
- Settling time is defined here for a $A_V = -5$ connection with $R_F = 2\text{k}\Omega$. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 2V step input is applied to the inverter. See settling time test circuit.



ELECTRICAL CHARACTERISTICS at $\pm 15V \leq V_S \leq \pm 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$ and $T_{HIGH} = +125^\circ C$ for PM-155, PM-156 and PM-157, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-155 PM-156 PM-157			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	4	7	mV
Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	5	—	$\mu V/^\circ C$
Change In Input Offset Drift With V_{OS} Adjust.	$\left(\frac{\Delta TCV_{OS}}{\Delta V_{OS}} \right)$	$R_S = 50\Omega$	—	0.5	—	$\mu V/^\circ C$ per mV
Input Offset Current	I_{OS}	$T_J \leq T_{HIGH}$ (Note 1)	—	8	20	nA
Input Bias Current	I_B	$T_J \leq T_{HIGH}$ (Note 1)	—	± 2	± 50	nA
Large-Signal Voltage Gain	A_{VO}	$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 2k\Omega$	25	75	—	V/mV
Output Voltage Swing	V_O	$V_S = \pm 15V, R_L = 10k\Omega$	± 12	± 13	—	V
		$V_S = \pm 15V, R_L = 2k\Omega$	± 10	± 12	—	
Input Voltage Range	IVR	$V_S = \pm 15V$	± 10.4	$+15.1$ -12.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm IVR$	85	100	—	dB
Power Supply Rejection Ratio	PSRR	(Note 2)	—	10	57	$\mu V/V$

NOTES:

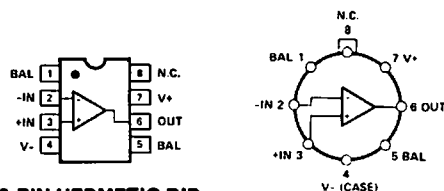
- PMI has a bias current compensation circuit which gives improved bias current over the standard JFET input op amps. I_B and I_{OS} are measured at $V_{CM} = 0, T_J = +125^\circ C$.
- Power supply rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ORDERING INFORMATION†

$T_A = 25^\circ C$ $V_{OS} \text{ MAX}$ (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	8-PIN HERMETIC DIP	LCC	
2.0	PM155AJ*	PM155AZ/883	PM155ARC/883	MIL
	PM156AJ*	PM156AZ*	PM156ARC/883	
	PM157AJ/883	PM157AZ*	—	
2.0	PM355AJ	PM355AZ	—	COM
	PM356AJ	PM356AZ	—	
	PM357AJ	PM357AZ	—	
5.0	PM155J*	PM155Z*	—	MIL
	PM156J*	PM156Z*	—	
	PM157J*	PM157Z*	—	

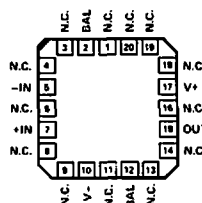
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

PIN CONNECTIONS

**8-PIN HERMETIC DIP
(Z-Suffix)**

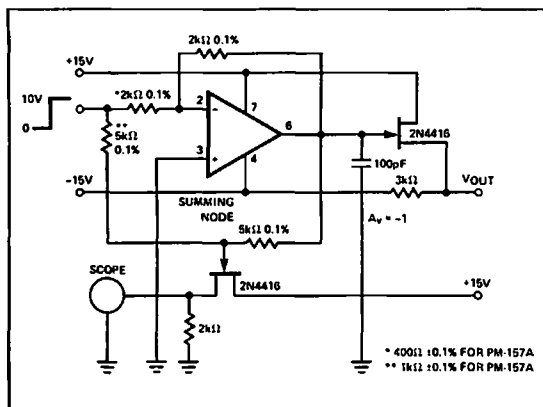
TO-99 (J-Suffix)



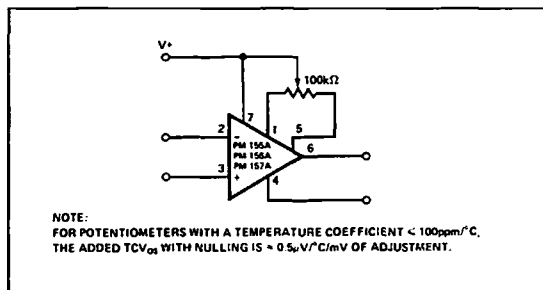
**PM-155ARC/883,
PM-156ARC/883
20-LEAD LCC
(RC-Suffix)**

BASIC CONNECTIONS

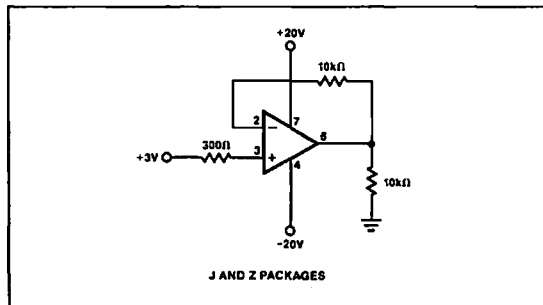
SETTLING-TIME TEST CIRCUIT



INPUT OFFSET VOLTAGE NULLING



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

INPUT VOLTAGE CONSIDERATIONS

The PM series JFET input stages can accommodate large input differential voltages without external clamping as long as neither input exceeds the negative power supply. An input voltage which is more negative than V_- can result in a destroyed unit.

If both inputs exceed the negative common-mode voltage limit, the amplifier will be forced to a high positive output. If only one input exceeds the negative common-mode voltage limit, a phase reversal takes place forcing the output to the corresponding high or low state. In either of the above conditions, normal operation will return when both inputs are returned to within the specified common-mode voltage range.

Exceeding the positive common-mode limit on a single input will not change the phase of the output. However, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

POWER SUPPLY CONSIDERATIONS

Power supply polarity reversal can result in a destroyed unit.

DYNAMIC OPERATING CONSIDERATIONS

As with most amplifiers, care should be taken with lead dress, component placement, and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input. This minimizes "pick-up" and increases the frequency of the feedback pole by minimizing the capacitance from input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device to AC ground sets the frequency of the pole. In many instances, the frequency of this pole is much greater than the expected 3dB frequency of the closed-loop gain. Consequently, the pole has negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency, a lead capacitor should be placed from the output to the inverting input of the op amp. The capacitor value should be such that the RC time constant of the capacitor and feedback resistor is greater than, or equal to, the original feedback-pole time constant.



Precision Monolithics Inc.

PM-741

COMPENSATED OPERATIONAL AMPLIFIER

FEATURES

- Industry Standard 741 Specifications
- Internal Frequency Compensation
- Continuous Short-Circuit Protection
- Silicon-Nitride Passivation
- Low Noise

ORDERING INFORMATION†

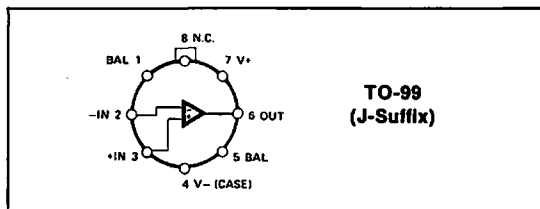
$T_A = 25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	OPERATING TEMPERATURE RANGE
5.0	PM741J	MIL
6.0	PM741CJ	COM

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

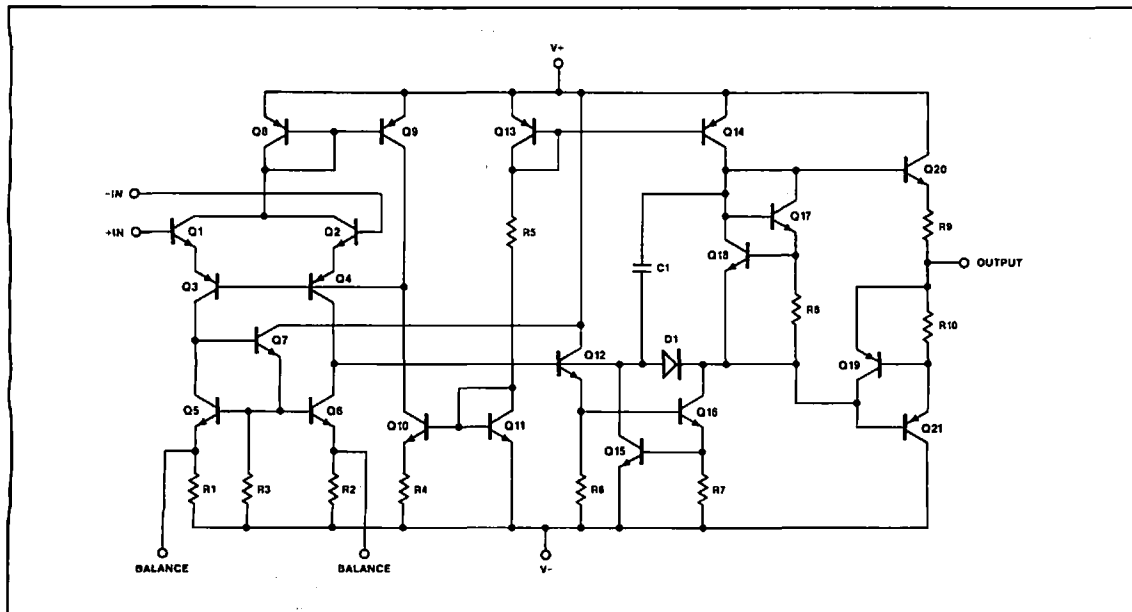
The PM-741 series of internally-compensated operational amplifiers provide industry-standard 741 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process provides high reliability and long-term stability of parameters. For higher performance general purpose op amps, refer to the OP-02 data sheet. See the OP-04/OP-14 data sheet for duals.

PIN CONNECTIONS



TO-99
(J-Suffix)

SIMPLIFIED SCHEMATIC



5
OPERATIONAL AMPLIFIERS

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	
PM-741	$\pm 22\text{V}$
PM-741C	$\pm 18\text{V}$
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	$\pm 30\text{V}$
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

PM-741	-55°C to $+125^{\circ}\text{C}$
PM-741C	0°C to $+70^{\circ}\text{C}$

NOTE:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	$7.1\text{mW}/^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS at $T_A = 25^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

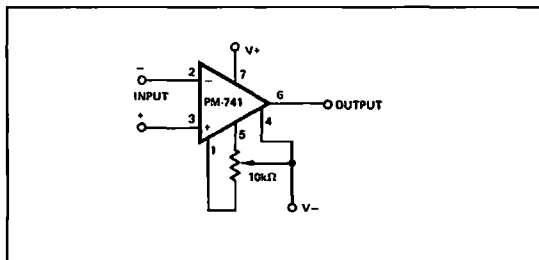
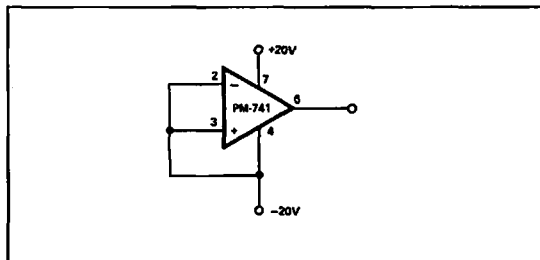
PARAMETER	SYMBOL	CONDITIONS	PM-741			PM-741C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10\text{k}\Omega$	—	—	5.0	—	—	6.0	mV
Input Offset Current	I_{OS}		—	—	200	—	—	200	nA
Input Bias Current	I_B		—	—	500	—	—	500	nA
Input Resistance	R_{IN}	(Note 1)	0.3	—	—	0.3	—	—	M Ω
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	50,000	—	—	25,000	—	—	V/V
Supply Current	I_{SY}	$V_{OUT} = 0$	—	—	2.8	—	—	2.8	mA

ELECTRICAL CHARACTERISTICS at $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for PM741, $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for PM741C, $V_S = \pm 15\text{V}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-741			PM-741C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 10\text{k}\Omega$	—	—	6.0	—	—	7.5	mV
Input Offset Current	I_{OS}		—	—	500	—	—	300	nA
Input Bias Current	I_B		—	—	1.5	—	—	0.8	μA
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	25,000	—	—	15,000	—	—	V/V
Output Voltage Swing	V_O	$R_L \geq 10\text{k}\Omega$	± 12	—	—	± 12	—	—	V
		$R_L \geq 1\text{k}\Omega$	± 10	—	—	± 10	—	—	
Input Voltage Range	IVR		± 12	—	—	± 12	—	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 10\text{V}$	70	—	—	70	—	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 10\text{k}\Omega$	—	—	142	—	—	142	$\mu\text{V/V}$

NOTE:

1. Guaranteed by design.

TYPICAL OFFSET NULLING CIRCUIT**TYPICAL BURN-IN CIRCUIT**



PM-747

DUAL COMPENSATED OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Dual PM-741 Internally-Compensated Operational Amplifier
- Internal Frequency Compensation
- Low Power Consumption
- Continuous Short-Circuit Protection
- Silicon-Nitride Passivation

ORDERING INFORMATION†

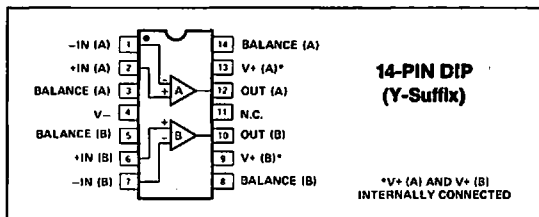
$T_A = 25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
	HERMETIC DIP 14-PIN	
5.0	PM747Y	MIL
6.0	PM747CY	COM

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

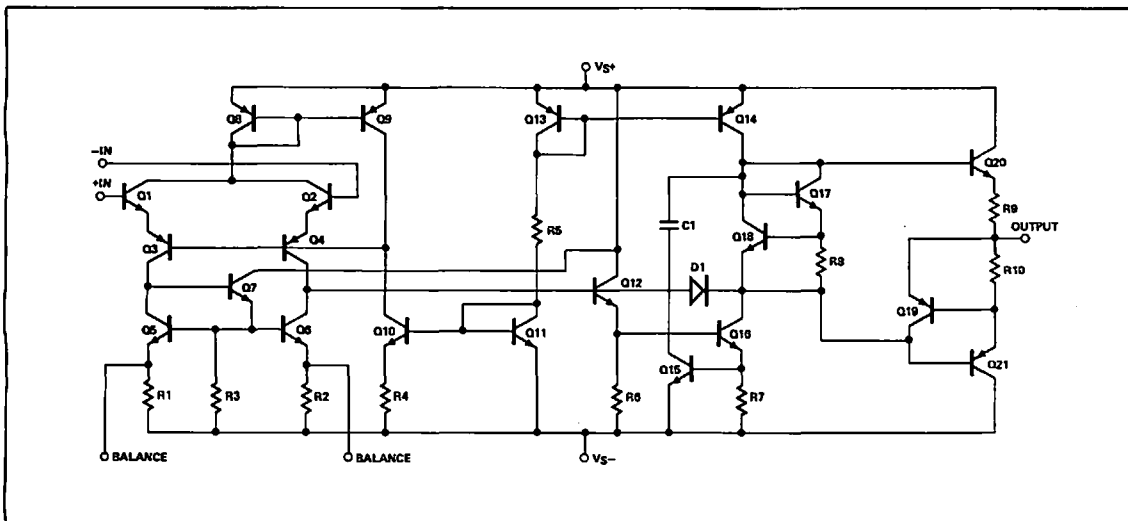
GENERAL DESCRIPTION

The PMI series of internally-compensated operational amplifiers provides industry-standard 747 specifications. In addition, Precision Monolithics' exclusive Silicon-Nitride "Triple Passivation" process provides maximum reliability and long-term stability of parameters for lowest overall system operating cost.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/2 of Circuit Shown)



OPERATIONAL AMPLIFIERS

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage	
PM-747	$\pm 22\text{V}$
PM-747C	$\pm 18\text{V}$
Internal Power Dissipation (Note 1)	
Y Package	670mW
Differential Input Voltage	$\pm 30\text{V}$
Input Voltage	Supply Voltage
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-85°C to $+150^{\circ}\text{C}$
Lead Temperature Range (Soldering, 60 sec)	300°C

Operating Temperature Range

PM-747	-55°C to $+125^{\circ}\text{C}$
PM-747C	0°C to $+70^{\circ}\text{C}$

NOTE:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	83°C	$10.0\text{mW}/^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS at $T_A = 25^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-747			PM-747C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20\text{k}\Omega$	—	1.0	5.0	—	1.0	6.0	mV
Input Offset Current	I_{OS}		—	20	200	—	20	200	nA
Input Bias Current	I_B		—	80	500	—	80	500	nA
Input Resistance	R_{IN}	(Note 1)	0.22	2.0	—	0.3	2.0	—	M Ω
Input Capacitance	C_{IN}		—	1.4	—	—	1.4	—	pF
Offset Voltage Adjustment Range			—	± 15	—	—	± 15	—	mV
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 10\text{V}$	50	200	—	25	200	—	V/mV
Output Voltage Swing	V_O	$R_L \geq 10\text{k}\Omega$ $R_L \geq 2\text{k}\Omega$	± 12 ± 10	± 14 ± 13	—	± 12 ± 10	± 14 ± 13	—	V
Output Resistance	R_O		—	75	—	—	75	—	Ω
Output Short-Circuit Current	I_{SC}		—	25	—	—	25	—	mA
Supply Current	I_{SV}	Per Amplifier, No Load	—	1.7	2.8	—	1.7	2.8	mA
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 20\text{k}\Omega$, $V_{CM} = \pm 10\text{V}$	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5\text{V}$ to $\pm 20\text{V}$ $V_S = \pm 5\text{V}$ to $\pm 18\text{V}$	—	30	150	—	—	—	$\mu\text{V/V}$
Power Consumption	P_d	Per Amplifier, No Load	—	50	85	—	50	85	mW
Transient Response, Unity Gain	Risetime Overshoot	$V_{IN} = 20\text{mV}$, $R_L = 2\text{k}\Omega$ $C_L \leq 100\text{pF}$	—	0.3	—	—	0.3	—	μs %
Slew Rate	SR	$R_L \geq 2\text{k}\Omega$	—	0.7	—	—	0.7	—	V/ μs
Channel Separation	CS		—	120	—	—	120	—	dB

NOTE:

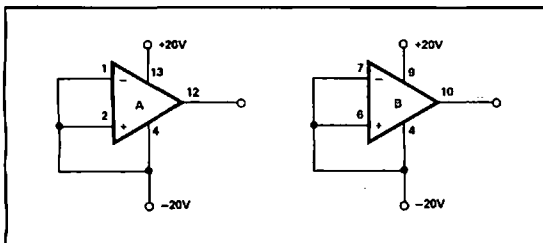
1. Guaranteed by input bias current.



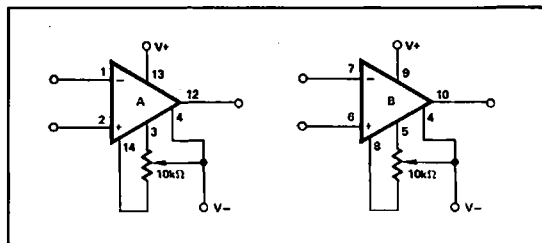
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for PM-747, $0^\circ C \leq T_A \leq +70^\circ C$ for PM-747C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-747			PM-747C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	—	1.0	6.0	—	1.0	7.5	mV
Input Offset Current	I_{OS}	$T_A = \text{MAX}$	—	7	200	—	7	200	nA
		$T_A = \text{MIN}$	—	85	500	—	30	300	
Input Bias Current	I_B	$T_A = \text{MAX}$	—	0.03	0.5	—	0.03	0.5	μA
		$T_A = \text{MIN}$	—	0.3	1.5	—	0.10	0.8	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	± 12	± 14	—	± 12	± 14	—	V
		$R_L \geq 2k\Omega$	± 10	± 13	—	± 10	± 13	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	50	—	15	25	—	V/mV
Input Voltage Range	IVR		± 12	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 20k\Omega$, $V_{CM} = \pm 10V$	70	90	—	70	90	—	dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 20k\Omega$, $V_S = \pm 5V$ to $\pm 20V$	—	30	150	—	—	—	$\mu V/V$
		$V_S = \pm 5V$ to $\pm 18V$	—	—	—	—	30	150	
Supply Current	I_{SY}	$T_A = \text{MAX}$ Per Amplifier,	—	1.5	2.5	—	1.5	2.5	mA
		$T_A = \text{MIN}$ No Load	—	2.0	3.3	—	2.0	3.3	
Power Consumption	P_d	$T_A = \text{MAX}$ Per Amplifier,	—	45	75	—	45	75	mW
		$T_A = \text{MIN}$ No Load	—	60	100	—	60	100	
Channel Separation	CS		—	120	—	—	120	—	dB

BURN-IN CIRCUIT

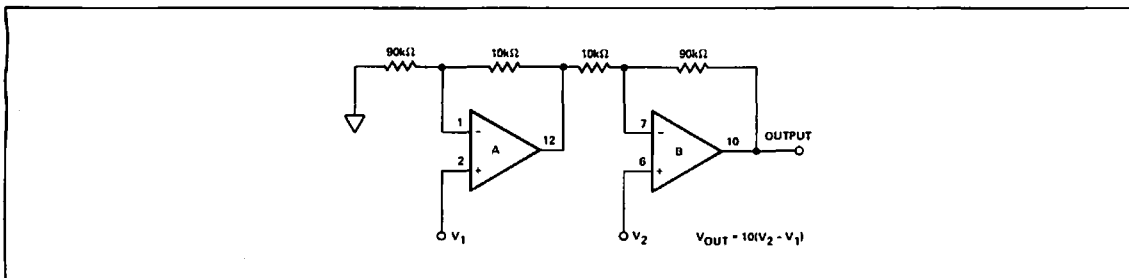


TYPICAL OFFSET NULLING CIRCUIT



TYPICAL APPLICATION

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER





PM-1008

LOW-POWER, PRECISION EXTERNALLY-COMPENSATED OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Supply Current 600 μ A Max
- Low Offset Voltage 120 μ V Max
- Low Drift 1.5 μ V/ $^{\circ}$ C Max
- Very Low Bias Current
25 $^{\circ}$ C 100pA Max
-55 $^{\circ}$ C to +125 $^{\circ}$ C 600pA Max
- Low Noise 0.5 μ V_{p-p} Typ
- High Common-Mode Rejection 114dB Min

ORDERING INFORMATION†

V _{OS} (μ V)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	
120	PM1008AJ*	PM1008AZ*	—	MIL
120	PM1008GJ	PM1008GZ	PM1008GP	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

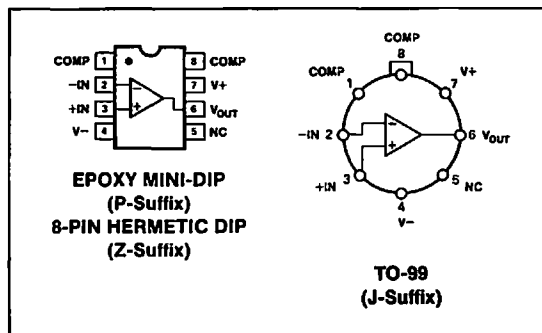
The PM-1008 is a general-purpose, externally-compensated precision operational amplifier. AC performance of the PM-1008 matches that of 108A/308A type amplifiers, while DC precision is greatly improved. Exceptionally low bias currents of only

± 80 pA, typical, over the full military temperature range combine with low noise of only 17nV/ $\sqrt{\text{Hz}}$ at 10Hz. The PM-1008's low offset voltage of 120 μ V maximum frees the user from external nulling in most circuits.

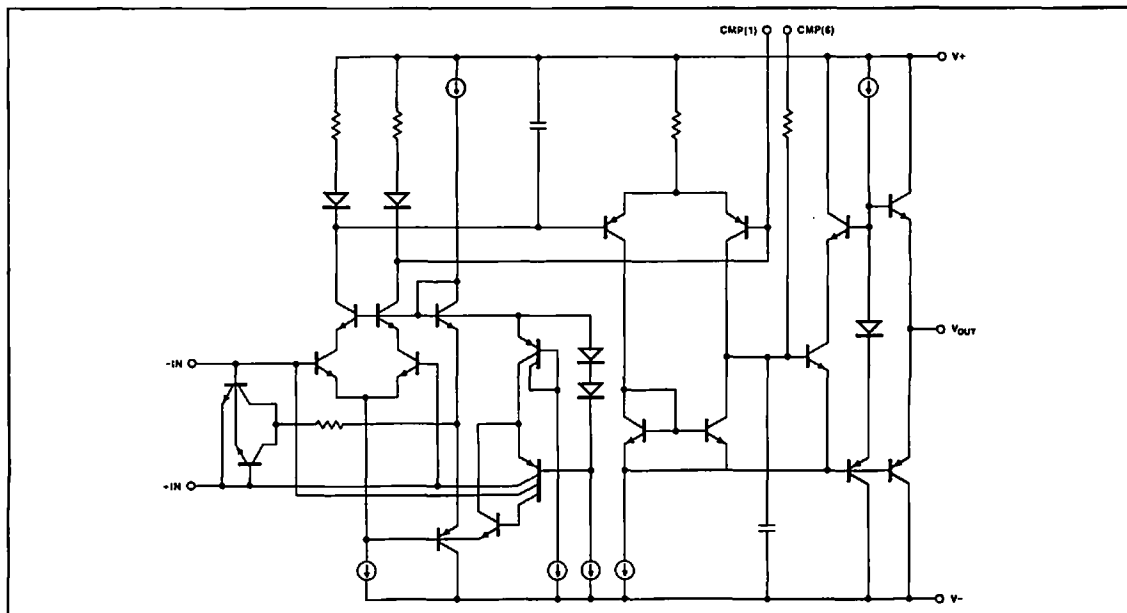
An open-loop gain of two million into a 10k Ω load ensures that excellent linearity is maintained even in high-gain configurations, and 5mA of output current allows 2k Ω loads to be driven with an open-loop gain of 600V/mV. High gain and 132dB of common-mode rejection and power-supply rejection eliminates the need for many tedious error calculations.

External frequency compensation allows the PM-1008's AC response to be optimized for each application. The PM-1008 will

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





directly upgrade 108A/308A and OP-08 sockets without modifying compensation. Compensation is usually achieved with a single capacitor, although more complex schemes may be used to further tailor the amplifier's response for a particular circuit.

For an internally compensated unity-gain stable amplifier with improved DC precision, see the OP-97 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	$\pm 20\text{V}$
Internal Power Dissipation (Note 2)	500mW
Input Voltage (Note 3)	$\pm 20\text{V}$
Differential Input Voltage (Note 4)	$\pm 1\text{V}$
Differential Input Current (Note 4)	$\pm 10\text{mA}$
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
PM1008A (J, Z)	-55°C to $+125^{\circ}\text{C}$
PM1008G (J, Z, P)	0°C to 70°C

Storage Temperature Range	-65°C to 150°C
Junction Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. See table for maximum ambient temperature and rating.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	$7.1\text{mW}/^{\circ}\text{C}$
8-Pin Hermetic DIP (Z)	75°C	$6.7\text{mW}/^{\circ}\text{C}$
8-Pin Plastic DIP (P)	62°C	$5.6\text{mW}/^{\circ}\text{C}$

3. For supply voltages less than $\pm 20\text{V}$, the absolute maximum input voltage is equal to the supply voltage.
4. The PM-1008's inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $C_F = 30\text{pF}$, $T_A = 25^{\circ}\text{C}$ unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-1008A			PM-1008G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	30	120	—	30	120	μV
			—	40	180	—	40	180	
Long-Term V_{OS} Stability	$\Delta V_{OS}/\text{Time}$		—	0.3	—	—	0.3	—	$\mu\text{V}/\text{month}$
Input Offset Current	I_{OS}	(Note 1)	—	30	100	—	30	100	pA
			—	40	150	—	40	150	
Input Bias Current	I_B	(Note 1)	—	± 30	± 100	—	± 30	± 100	pA
			—	± 40	± 150	—	± 40	± 150	
Input Noise Voltage	$e_{n_{p-p}}$	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 3)	—	17	30	—	17	30	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 1000\text{Hz}$ (Note 4)	—	14	22	—	14	22	
Input Noise Current Density	I_N	$f_O = 10\text{Hz}$	—	20	—	—	20	—	$\text{fA}/\sqrt{\text{Hz}}$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 12\text{V}$; $R_L = 10\text{k}\Omega$	200	2000	—	200	2000	—	V/mV
		$V_O = \pm 10\text{V}$; $R_L = 2\text{k}\Omega$	120	600	—	120	600	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5\text{V}$	114	132	—	114	132	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2\text{V}$ to $\pm 20\text{V}$	114	132	—	114	132	—	dB
Input Voltage Range	IVR	(Note 2)	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Output Voltage Swing	V_O	$R_L = 10\text{k}\Omega$	± 13	± 14	—	± 13	± 14	—	V
Slow Rate	SR		0.1	0.2	—	0.1	0.2	—	$\text{V}/\mu\text{s}$
Full-Power Bandwidth	BW_P		—	3	—	—	3	—	kHz
Gain-Bandwidth Product	GBW	$A_V = 100$	—	0.5	—	—	0.5	—	MHz
Supply Current	I_{SY}	(Note 1)	—	380	600	—	380	600	μA
Supply Voltage	V_S	Operating Range	± 2	± 15	± 20	± 2	± 15	± 20	V

NOTES:

1. These specifications apply for $\pm 2\text{V} \leq V_S \leq \pm 20\text{V}$ and $-13.5\text{V} \leq V_{CM} \leq +13.5\text{V}$ (for $V_S = \pm 15\text{V}$).
2. Guaranteed by CMR test.
3. 10Hz noise voltage density is sample tested. Devices 100% tested for noise are available on request.
4. Sample tested.

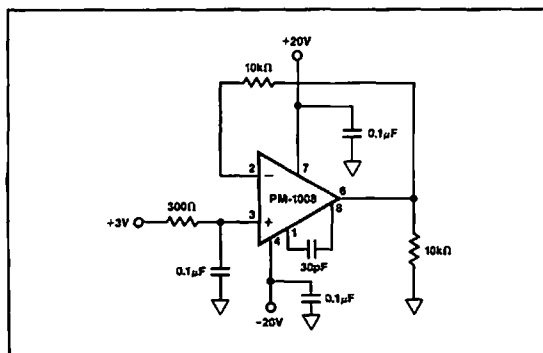


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $C_F = 30pF$, $0^\circ C \leq T_A \leq 70^\circ C$ for the PM1008G and $-55^\circ C \leq T_A \leq 125^\circ C$ for the PM-1008A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-1008A			PM-1008G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	50	250	—	40	180	μV
Average Temperature Coefficient of V_{OS}	TCV_{OS}		—	0.2	1.5	—	0.2	1.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}	(Note 1)	—	60	250	—	40	180	pA
Average Temperature Coefficient of I_{OS}	TCI_{OS}		—	0.4	2.5	—	0.4	2.5	$pA/^\circ C$
Input Bias Current	I_B	(Note 1)	—	± 80	± 600	—	± 40	± 180	pA
Average Temperature Coefficient of I_B	TCI_B		—	0.6	6.0	—	0.4	2.5	$pA/^\circ C$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 12V$; $R_L = 10k\Omega$	100	1000	—	150	1500	—	V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	108	128	—	110	130	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2.5V$ to $\pm 20V$	108	126	—	110	128	—	dB
Input Voltage Range	IVR	(Note 2)	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 13	± 14	—	± 13	± 14	—	V
Slew Rate	SR		0.05	0.15	—	0.05	0.15	—	$V/\mu s$
Supply Current	I_{SY}	(Note 1)	—	400	800	—	400	800	μA
Supply Voltage	V_S	Operating Range	± 2.5	± 15	± 20	± 2.5	± 15	± 20	V

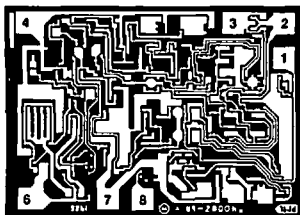
NOTES:

- These specifications apply for $\pm 2.5V \leq V_S \leq \pm 20V$ and $-13.5V \leq V_{CM} \leq +13.5V$ (for $V_S = \pm 15V$).
- Guaranteed by CMR test.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.054 X 0.074 inch, 3996 sq. mils
(1.37 X 1.88 mm, 2.58 sq. mm)

1. COMPENSATION
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V₋
6. OUTPUT
7. V₊
8. COMPENSATION

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $V_{CM} = 0V$, $C_F = 30pF$, $T_A = 25^\circ C$ unless otherwise noted.

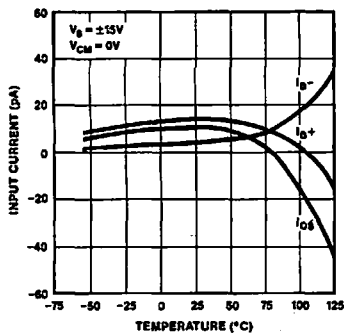
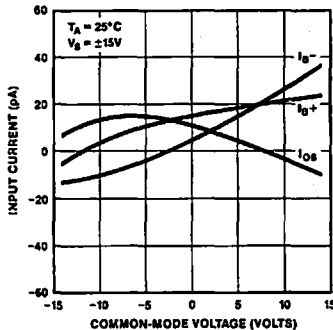
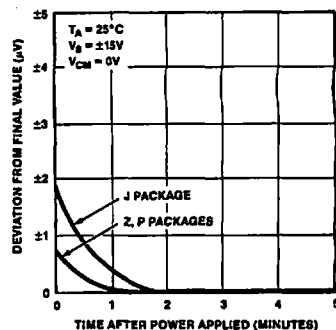
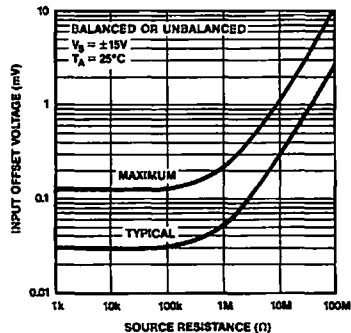
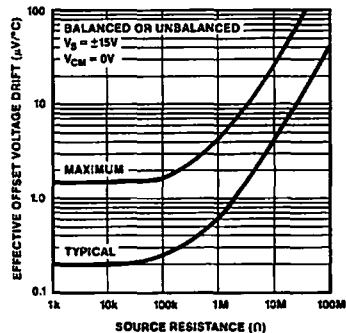
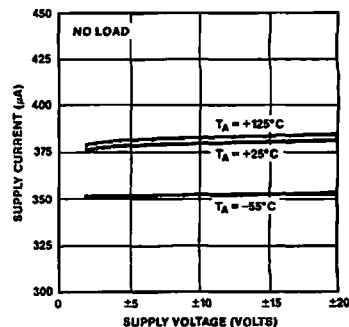
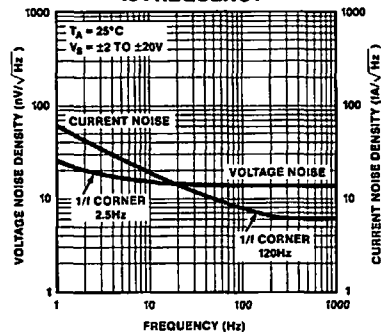
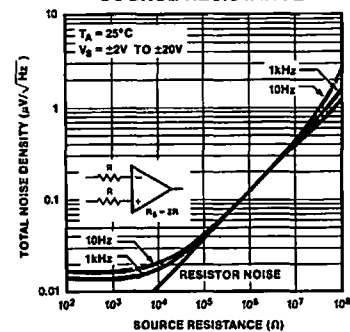
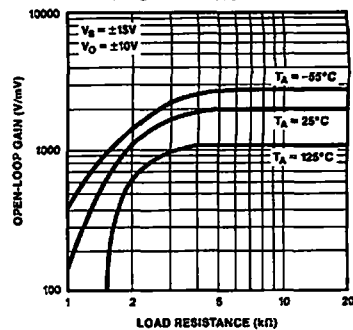
PARAMETER	SYMBOL	CONDITIONS	PM-1008N	UNITS
			LIMIT	
Input Offset Voltage	V_{OS}	(Note 1)	120	μV MAX
			180	
Input Offset Current	I_{OS}	(Note 1)	100	pA MAX
			150	
Input Bias Current	I_b	(Note 1)	± 100	pA MAX
			± 150	
Large-Signal Voltage Gain	A_{VO}	$V_{OUT} = \pm 12V$, $R_L = 10k\Omega$ $V_{OUT} = \pm 10V$, $R_L = 2k\Omega$	200	V/mV MIN
			120	
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	114	dB MIN
Power-Supply Rejection	PSR	$V_S = \pm 2V$ to $\pm 20V$	114	dB MIN
Input-Voltage Range	IVR	(Note 2)	± 13.5	V MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 13	V MIN
Slew Rate	SR		0.1	$V/\mu s$ MIN
Supply Current	I_{SV}	No Load	600	μA MAX

NOTES:

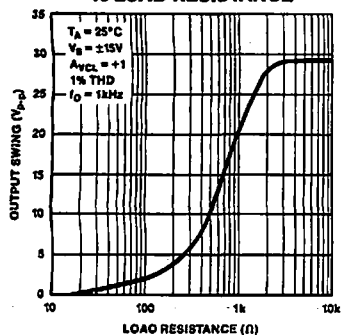
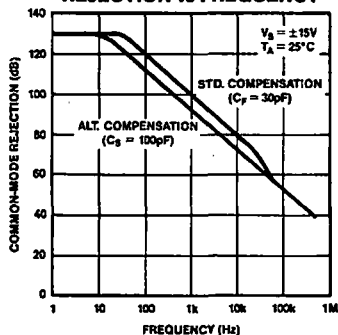
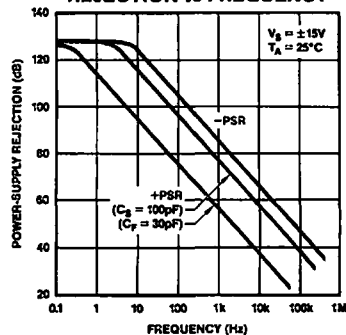
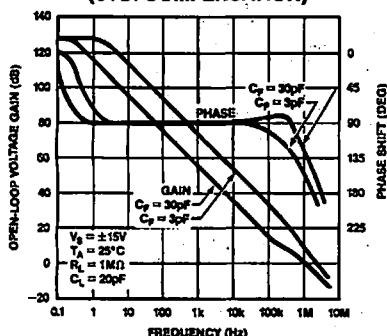
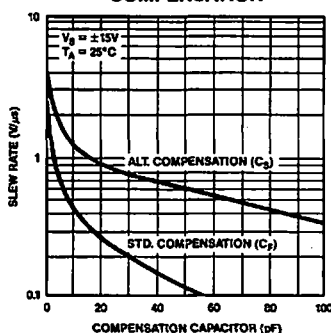
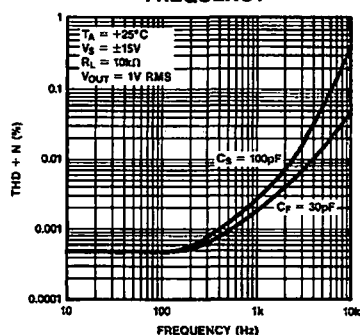
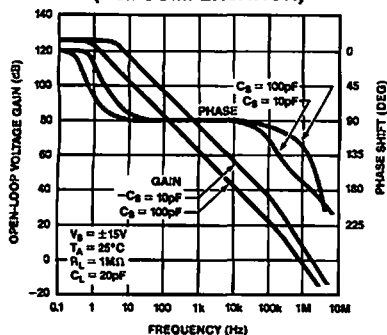
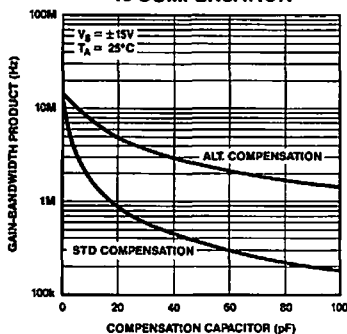
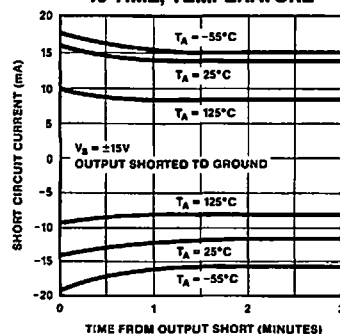
1. These specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ and $-13.5V \leq V_{CM} \leq +13.5V$ (for $V_S = \pm 15V$).
2. Guaranteed by CMR test.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

 INPUT BIAS, OFFSET
CURRENT vs TEMPERATURE

 INPUT BIAS, OFFSET
CURRENT vs
COMMON-MODE VOLTAGE

 INPUT OFFSET VOLTAGE
WARM-UP DRIFT

 EFFECTIVE OFFSET VOLTAGE
vs SOURCE RESISTANCE

 EFFECTIVE TCV_{OS} vs
SOURCE RESISTANCE

 SUPPLY CURRENT vs
SUPPLY VOLTAGE

 NOISE DENSITY
vs FREQUENCY

 TOTAL NOISE DENSITY vs
SOURCE RESISTANCE

 OPEN-LOOP GAIN
vs LOAD RESISTANCE


TYPICAL PERFORMANCE CHARACTERISTICS

 MAXIMUM OUTPUT SWING
vs LOAD RESISTANCE

 COMMON-MODE
REJECTION vs FREQUENCY

 POWER-SUPPLY
REJECTION vs FREQUENCY

 OPEN-LOOP GAIN, PHASE
vs FREQUENCY
(STD. COMPENSATION)

 SLEW RATE vs
COMPENSATION

 TOTAL HARMONIC
DISTORTION PLUS NOISE vs
FREQUENCY

 OPEN-LOOP GAIN, PHASE
vs FREQUENCY
(ALT. COMPENSATION)

 GAIN-BANDWIDTH PRODUCT
vs COMPENSATION

 SHORT-CIRCUIT CURRENT
vs TIME, TEMPERATURE




APPLICATIONS INFORMATION

The PM-1008 is an externally compensated amplifier for use in circuits where precision is critical, yet power dissipation must be minimized. An upgrade to the OP-08 and 108A type amplifiers, the PM-1008 offers exceptional performance for a low-power amplifier. Its wide supply range coupled with minimal current drain makes it an excellent choice for battery-powered and portable instruments. External compensation allows the maximum bandwidth to be achieved with any given gain.

Input bias and offset currents remain extremely low over the full military temperature range, and make the PM-1008 attractive in a variety of logging circuits and peak detectors. Balancing of input resistances is not necessary with the PM-1008. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the PM-1008 are protected against large differential voltages by back-to-back diodes. To preserve low-noise performance, current limiting resistors are not used in the inputs. If differential voltages above $\pm 1V$ are expected at the inputs, series resistors must be used to limit the current flow to a maximum of 10mA. Common-mode voltages at the inputs are not restricted and may vary over the full range of the supply voltages used.

The PM-1008 requires very little operating headroom about the supply rails and is specified for operation with supplies as low as $\pm 2V$. Typically, the common-mode range extends to within one volt of either rail. The output typically swings to within one volt of the rails when driving a 10k Ω load.

FREQUENCY COMPENSATION

A high degree of flexibility in shaping the AC response of the amplifier to specific applications is achieved with two compensation pins. Compensation usually consists of a single capacitor and is achieved using the same circuits as the OP-08 or 108A type amplifiers. The PM-1008 will directly upgrade these sockets to obtain increased DC precision with similar AC performance.

Standard compensation using the circuit of Figure 1 introduces feedback in the second stage. The feedback capacitor must be greater than $(R1 \times 30pF)/(R1 + R2)$ to ensure stability. Figure 2 shows the large-signal and small-signal response of the PM-1008 using standard compensation.

FIGURE 1: Standard Frequency Compensation

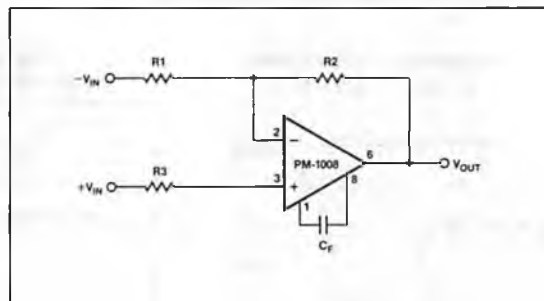
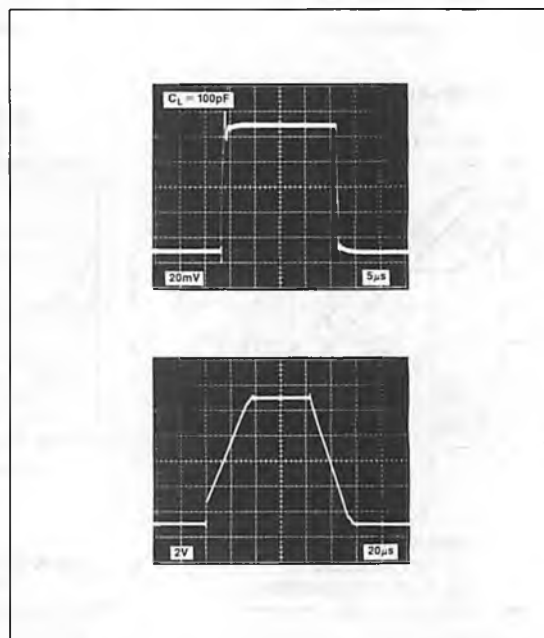


FIGURE 2: Standard Compensation Transient Response ($C_F = 30pF$, $A_{VCL} = +1$)



The alternate compensation method of Figure 3 improves AC power-supply rejection by a factor of five. This is an advantage in circuits where digital noise is injected onto supply lines, or noisy switching power-supplies are used. Figure 4 depicts transient response with alternate compensation.

Bandwidth and slew rate are inversely proportional to the compensation capacitor, regardless of which method used. Compensation with $C_F = 30\text{pF}$ results in AC performance similar to the internally compensated OP-97. Phase margin is approximately 60 degrees. Additional compensation will result in increased stability useful for circuits with capacitive loads, or with gain in the feedback loop. Overcompensation reduces overall noise by limiting bandwidth. Less compensation is useful to obtain higher bandwidth and slew rate with higher closed-loop gains greater than 200.

In unity-gain large-signal applications, the input protection diodes effectively short the output to the input during transients

in the usual unity-gain configuration. The output enters short-circuit current limit, with the flow going through the protection diodes. Improved transient response is obtained by using a feedback resistor (R_2) between the output and the inverting input to limit this current. The preceding large-signal photos used a $10\text{k}\Omega$ feedback resistor, R_2 , with $R_1 = R_3 = 0$.

Feedforward compensation may be used in low-gain applications to enhance slew rate. The inverting circuit of Figure 5 has a slew rate of $1.4\text{V}/\mu\text{s}$, while the follower circuit of Figure 7 approaches $10\text{V}/\mu\text{s}$. Inverting feedforward compensation does not degrade the accuracy of the PM-1008, and can be valuable in many applications. Follower feedforward compensation may introduce errors if the output is loaded, even with $10\text{k}\Omega$. It should be used with care to ensure that performance is not compromised.

FIGURE 3: Alternate Frequency Compensation

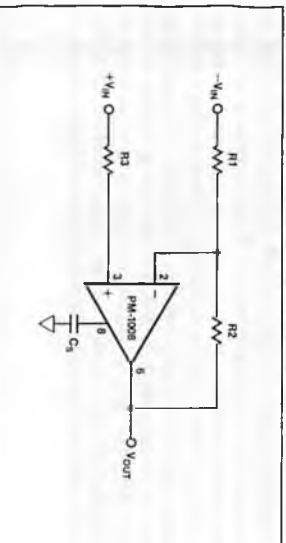


FIGURE 5: Inverter Feedforward Compensation

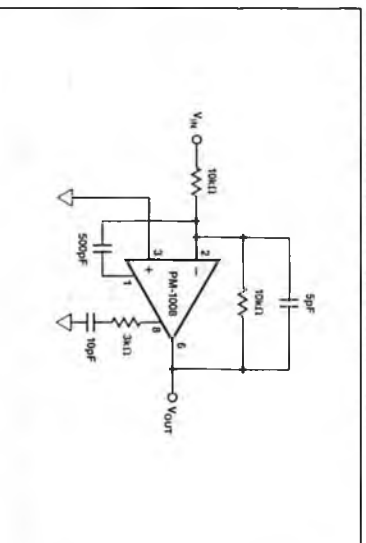
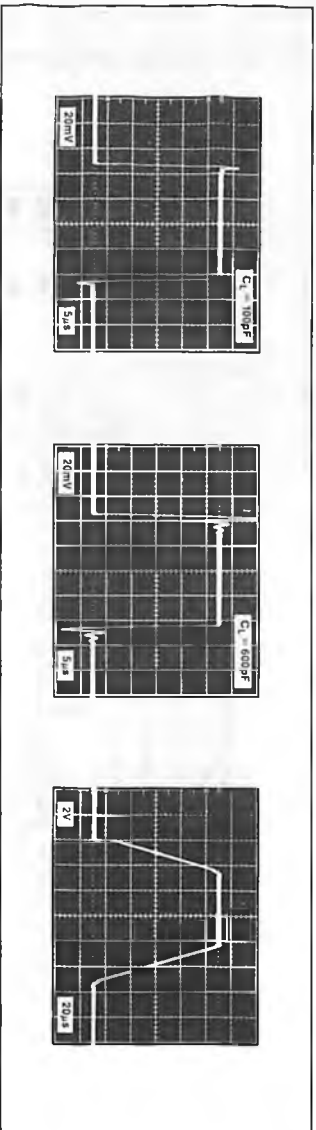
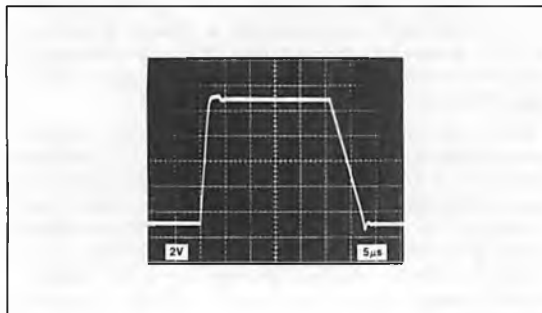
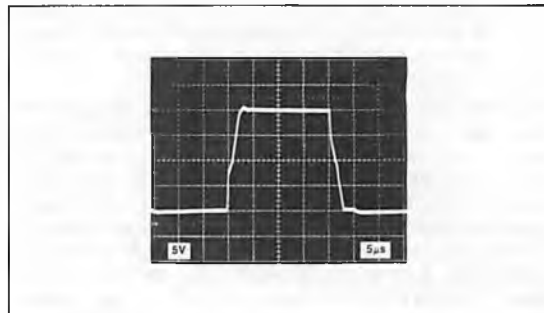
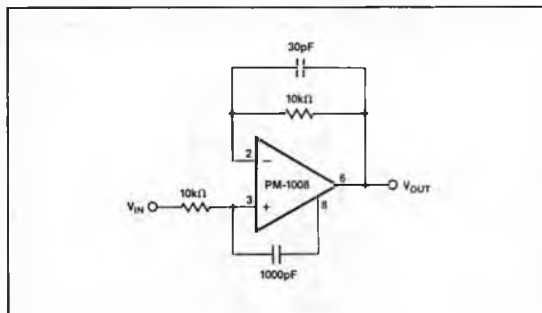


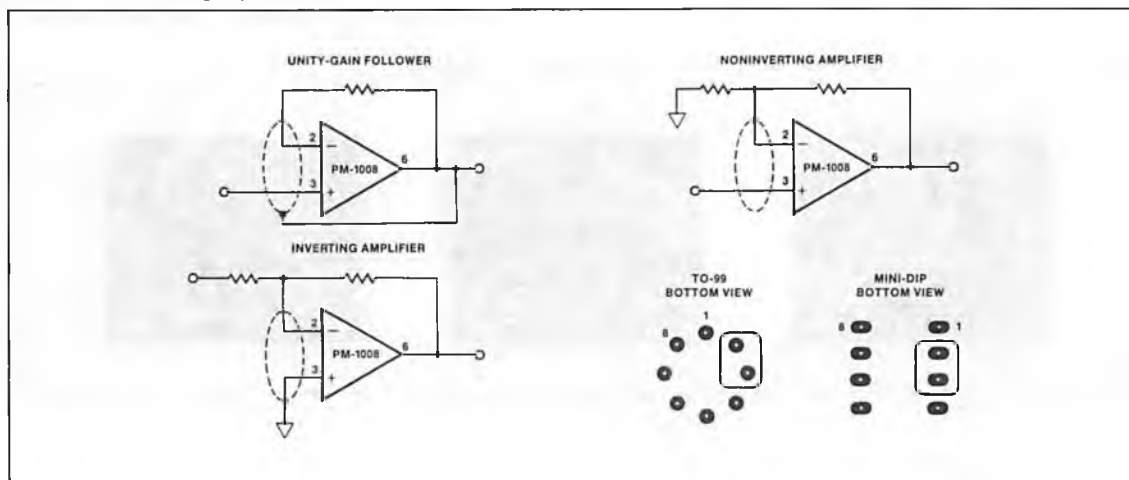
FIGURE 4: Alternate Frequency Compensation Transient Response ($C_F = 100\text{pF}$, $A_{VCL} = +1$)



**FIGURE 6:** Inverter Feedforward Transient Response**FIGURE 8:** Follower Feedforward Transient Response**FIGURE 7:** Follower Feedforward Compensation

GUARDING AND SHIELDING

To maintain the extremely high input impedances of the PM-1008, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100pA of leakage currents between adjacent traces, so that guard rings should be used around the inputs. Guard traces are operated at a voltage close to that on the inputs, so that leakage currents become minimal. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input (pin 2). In inverting applications, both inputs remain at ground, so that the guard trace should be grounded. Guard traces should be made on both sides of the circuit board.

FIGURE 9: Guard Ring Layout and Connections

High impedance circuitry is extremely susceptible to RF pickup, line-frequency hum and radiated noise from switching power-supplies. Enclosing sensitive analog sections within grounded shields is generally necessary to prevent excessive noise pickup. Twisted-pair cable will aid in rejection of line-frequency hum.

The circuit of Figure 10 multiplies capacitor values by a factor of ($R1/R3$). Equivalent leakage of the capacitance multiplier is much smaller than that available with extremely large capacitors. The equivalent leakage current is determined by the offset voltage and offset currents of the amplifier used, both of which are quite low with the PM-1008, even over temperature. The equivalent series resistance of the multiplied capacitor is $R3$, which prevents the circuit from generated high-Q capacitances. In timing circuits where a series resistance is connected with the capacitor, $R3$ should be considered a part of that resistance.

FIGURE 10: Capacitance Multiplier

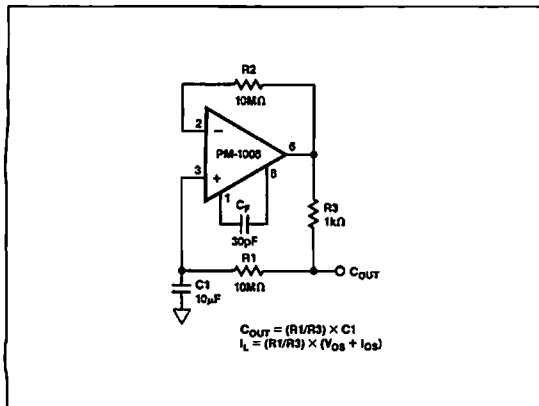


FIGURE 11: Photodiode Amplifier

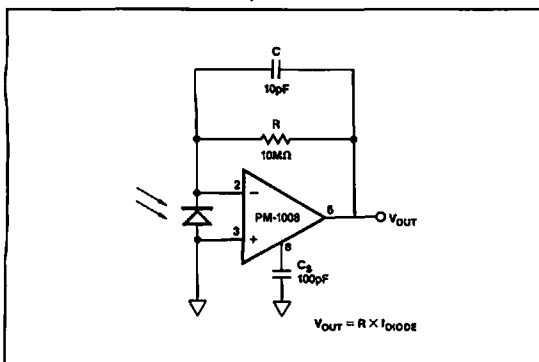


FIGURE 12: Zero-Crossing Detector

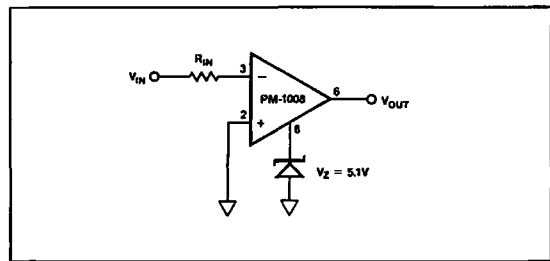


Figure 11 shows an amplifier for photodiodes. The diode is operated with only the V_{OS} of the amplifier as bias. Thus, the diode's leakage currents remain minimal even at high temperatures. The capacitor in the feedback loop acts to prevent gain peaking at high frequencies due to the diode capacitance.

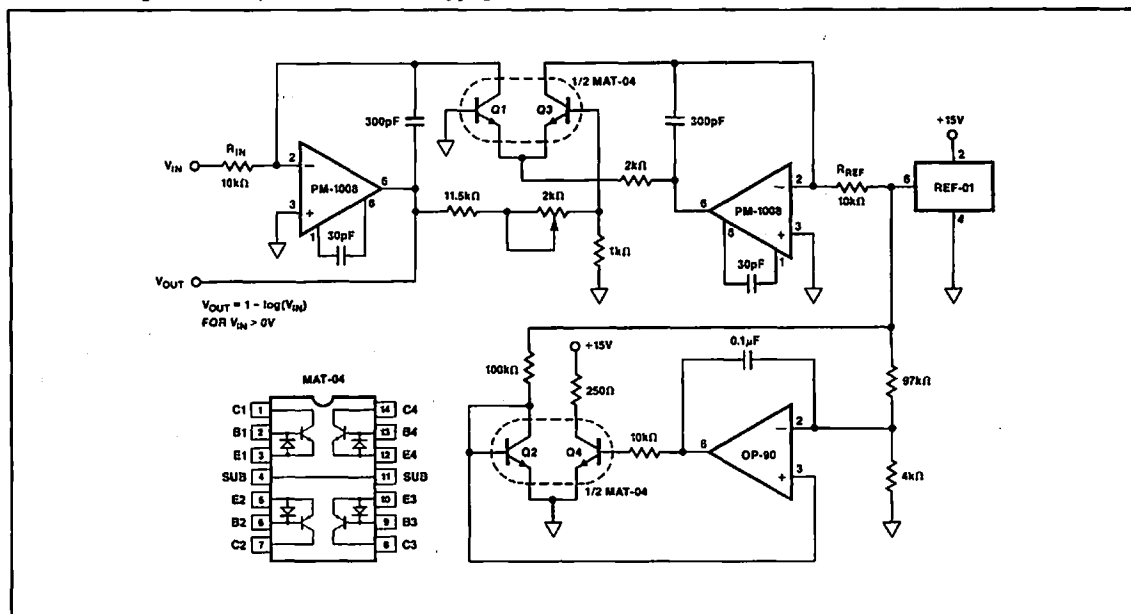
The output swing of the PM-1008 may be clamped to specific levels using pin 8. The zero-crossing detector of Figure 12 uses a zener diode to clamp the maximum positive swing to approximately 5V, and the maximum negative swing to the forward-biased voltage drop across the diode. R_{IN} limits the current-flow through the protection diodes for voltage excursions beyond $\pm 1V$. With $R_{IN} = 1M\Omega$, the circuit will tolerate as much as 1kV at the input.

The logarithmic amplifier in Figure 13 eliminates thermal drift caused by temperature dependencies of the logging transistors by maintaining a monolithic quad matched transistor at a predetermined temperature. The MAT-04 has four transistors laid-out at the corners of a square die. Two transistors across a diagonal are used for logging elements. One of the remaining transistors is used as a heater to maintain a constant chip temperature, and the remaining transistor, diagonally opposite to the heater, is used as a temperature sensor.

The OP-90 servo amplifier uses thermal feedback to set the temperature of the MAT-04 die. The base-to-emitter voltage of Q2 is maintained at the level set by the resistive divider from the REF-01, by controlling the current flowing through Q4. Although Q4 may operate beyond the MAT-04's rated levels, this does not degrade operation since the characteristics of the heater transistor are non-critical. For best thermal regulation, the MAT-04 package should be encased in insulation. Urethane foam used for housing insulation is excellent for this purpose.

Gain is trimmed using the 2kΩ potentiometer. The zero-crossing point is adjusted by changing the value of R_{REF} . Input scaling may be changed by varying resistor R_{IN} .

FIGURE 13: Logarithmic Amplifier with Heated Logging Transistors





PM-1012

LOW-POWER, PRECISION OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Supply Current 600 μ A Max
- Very Low Offset 35 μ V Max
- Low Drift 1.5 μ V/ $^{\circ}$ C Max
- Very Low Bias Current
25 $^{\circ}$ C 100pA Max
-55 $^{\circ}$ C to +125 $^{\circ}$ C 250pA Max
- Low Noise 0.5 μ V_{p-p} Typ
- High Common-Mode Rejection 114dB Min

ORDERING INFORMATION †

V _{OS} (μ V)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 8-PIN	PLASTIC DIP 8-PIN	
35	PM1012AJ*	PM1012AZ*	—	MIL
50	PM1012GJ	PM1012GZ	PM1012GP	COM

Contact factory for SOIC (PM1012S) specifications and availability.

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

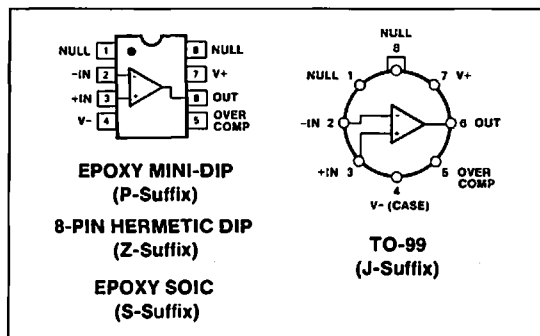
GENERAL DESCRIPTION

The PM-1012 is a general-purpose, precision operational amplifier. Offering several performance enhancements over

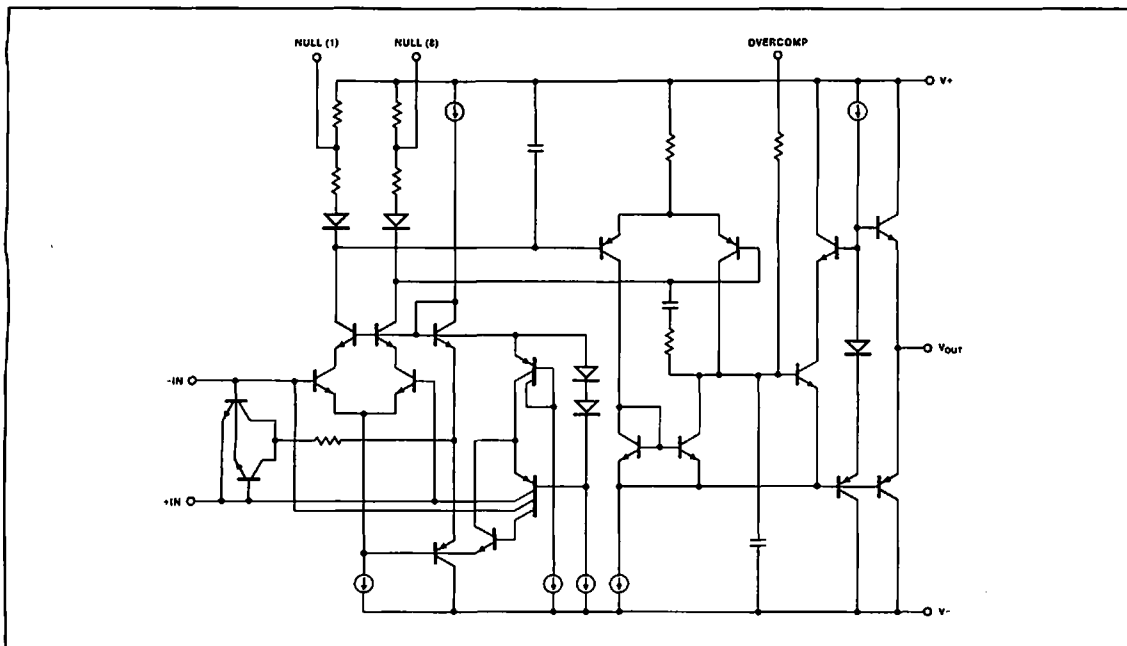
industry-standard precision op amps such as the OP-07, the PM-1012 requires less than 1/6 the supply current. These enhancements include exceptionally low bias currents of only ± 80 pA, typical, over the full military temperature range and 132dB of common-mode rejection and power-supply rejection. The PM-1012's low offset voltage of 35 μ V maximum frees the user from external nulling in most circuits.

An open-loop gain of two million into a 10k Ω load ensures that excellent linearity is maintained even in high-gain configurations, and 5mA of output current allows 2k Ω loads to be driven

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





with an open-loop gain of one million. The PM-1012 offers low noise, especially for a low-power amplifier — only $17\text{ nV}/\sqrt{\text{Hz}}$ at 10Hz. Exceptionally low current-noise minimizes noise contributions when high source impedances are used. The PM-1012 may be overcompensated using pin 5 to limit the amplifier's bandwidth, further reducing system noise and increasing stability with large capacitive loads.

The PM-1012 conforms to the OP-07 pinout with nulling through pins 1 and 8 to the positive supply. It offers an upgrade to the OP-07 in sockets where reduced power dissipation or low bias currents are attractive. It may also be used as an upgrade from the OP-12, OP-05 and 725 type op amps. The PM-1012 may replace 741 type op amps by removing the nulling potentiometer, if used. For an externally compensated amplifier sharing many of the PM-1012's precision specifications, see the PM-1008 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	$\pm 20\text{V}$
Internal Power Dissipation (Note 2)	500mW
Input Voltage (Note 3)	$\pm 20\text{V}$
Differential Input Voltage (Note 4)	$\pm 1\text{V}$
Differential Input Current (Note 4)	$\pm 10\text{mA}$

Output Short-Circuit Duration Indefinite
Operating Temperature Range:

PM-1012A (J, Z)	-55°C to $+125^{\circ}\text{C}$
PM-1012G (J, Z, P)	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Junction Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. See table for maximum ambient temperature and rating.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	$7.1\text{mW}/^{\circ}\text{C}$
8-Pin Hermetic DIP (Z)	75°C	$6.7\text{mW}/^{\circ}\text{C}$
8-Pin Plastic DIP (P)	62°C	$5.6\text{mW}/^{\circ}\text{C}$

3. For supply voltages less than $\pm 20\text{V}$, the absolute maximum input voltage is equal to the supply voltage.
4. The PM-1012's inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $V_{CM} = 0\text{V}$, $T_A = 25^{\circ}\text{C}$ unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-1012A			PM-1012G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	8 20	35 90	—	10 25	50 120	μV
Long-Term V_{OS} Stability	$\Delta V_{OS}/\text{Time}$		—	0.3	—	—	0.3	—	$\mu\text{V}/\text{month}$
Input Offset Current	I_{OS}	(Note 1)	—	15 25	100 150	—	20 30	150 200	pA
Input Bias Current	I_B	(Note 1)	—	± 25 ± 35	± 100 ± 150	—	± 30 ± 40	± 150 ± 200	pA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.5	—	—	0.5	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10\text{Hz}$ (Note 3) $f_O = 1000\text{Hz}$ (Note 4)	—	17 14	30 22	—	17 14	30 22	$\text{nV}/\sqrt{\text{Hz}}$
Input Noise Current Density	i_n	$f_O = 10\text{Hz}$	—	20	—	—	20	—	$1\text{A}/\sqrt{\text{Hz}}$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 12\text{V}$; $R_L = 10\text{k}\Omega$ $V_O = \pm 10\text{V}$; $R_L = 2\text{k}\Omega$	300 200	2000 1000	—	200 120	2000 1000	—	V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5\text{V}$	114	132	—	110	132	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2\text{V}$ to $\pm 20\text{V}$	114	132	—	110	132	—	dB
Input Voltage Range	IVR	(Note 2)	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Output Voltage Swing	V_O	$R_L = 10\text{k}\Omega$	± 13	± 14	—	± 13	± 14	—	V
Slew Rate	SR		0.1	0.2	—	0.1	0.2	—	V/ μs
Full-Power Bandwidth	BW_P		—	3	—	—	3	—	kHz
Gain-Bandwidth Product	GBW	$A_V = 100$	—	0.5	—	—	0.5	—	MHz
Supply Current	I_{SY}	(Note 1)	—	380	600	—	380	600	μA
Supply Voltage	V_S	Operating Range	± 2	± 15	± 20	± 2	± 15	± 20	V

NOTES:

1. These specifications apply for $\pm 2\text{V} \leq V_S \leq \pm 20\text{V}$ and $-13.5\text{V} \leq V_{CM} \leq +13.5\text{V}$ (for $V_S = \pm 15\text{V}$).
2. Guaranteed by CMR test.
3. 10Hz noise voltage density is sample tested. Devices 100% tested for noise are available on request.
4. Sample Tested.

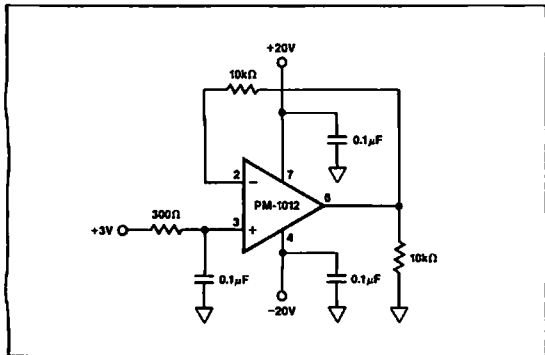


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$ for the PM-1012G and $-55^\circ C \leq T_A \leq 125^\circ C$ for the PM-1012A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-1012A			PM-1012G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	30	180	—	20	120	μV
Average Temperature Coefficient of V_{OS}	TCV_{OS}		—	0.2	1.5	—	0.2	1.5	$\mu V/^\circ C$
Input Offset Current	I_{OS}	(Note 1)	—	30	250	—	20	230	pA
Average Temperature Coefficient of I_{OS}	TCI_{OS}		—	0.3	2.5	—	0.3	2.5	$pA/^\circ C$
Input Bias Current	I_B	(Note 1)	—	± 50	± 250	—	± 35	± 230	pA
Average Temperature Coefficient of I_B	TCI_B		—	0.3	2.5	—	0.3	2.5	$pA/^\circ C$
Large-Signal Voltage Gain	A_{VO}	$V_O = \pm 12V$; $R_L = 10k\Omega$ $V_O = \pm 10V$; $R_L = 2k\Omega$	150 100	1000 600	—	150 100	1500 800	—	V/mV
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	108	128	—	108	130	—	dB
Power-Supply Rejection	PSR	$V_S = \pm 2.5V$ to $\pm 20V$	108	126	—	108	128	—	dB
Input Voltage Range	IVR	(Note 2)	± 13.5	± 14.0	—	± 13.5	± 14.0	—	V
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 13	± 14	—	± 13	± 14	—	V
Slew Rate	SR		0.05	0.15	—	0.05	0.15	—	$V/\mu s$
Supply Current	I_{SY}	(Note 1)	—	400	800	—	400	800	μA
Supply Voltage	V_S	Operating Range	± 2.5	± 15	± 20	± 2.5	± 15	± 20	V

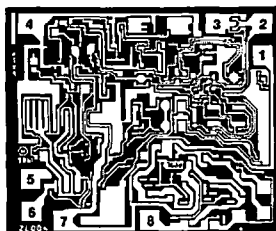
NOTES:

- These specifications apply for $\pm 2.5V \leq V_S \leq \pm 20V$ and $-13.5V \leq V_{CM} \leq +13.5V$ (for $V_S = \pm 15V$).
- Guaranteed by CMR test.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.063×0.074 inch, 4662 sq. mils
(1.60×1.88 mm, 3.01 sq. mm)

1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V_-
5. OVERCOMPENSATION
6. OUTPUT
7. V_+
8. NULL

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-1012N LIMIT	UNITS
Input Offset Voltage	V_{OS}	(Note 1)	250	μV MAX
		(Note 2)	300	
Input Offset Current	I_{OS}	(Note 2)	150	pA MAX
			200	
Input Bias Current	I_B	(Note 2)	± 150	pA MAX
			± 200	
Large-Signal Voltage Gain	A_{VO}	$V_{OUT} = \pm 12V$, $R_L = 10k\Omega$	200	V/mV MIN
		$V_{OUT} = \pm 10V$, $R_L = 2k\Omega$	120	
Common-Mode Rejection	CMR	$V_{CM} = \pm 13.5V$	110	dB MIN
Power-Supply Rejection	PSR	$V_S = \pm 2V$ to $\pm 20V$	110	dB MIN
Input Voltage Range	IVR	(Note 3)	± 13.5	V MIN
Output Voltage Swing	V_O	$R_L = 10k\Omega$	± 13	V MIN
Slew Rate	SR		0.1	$V/\mu s$ MIN
Supply Current	I_{SY}	No Load	600	μA MAX

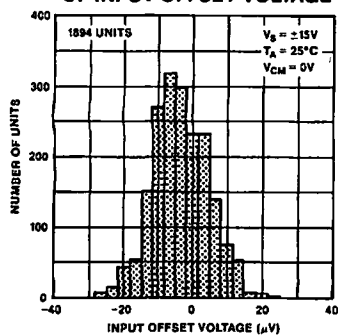
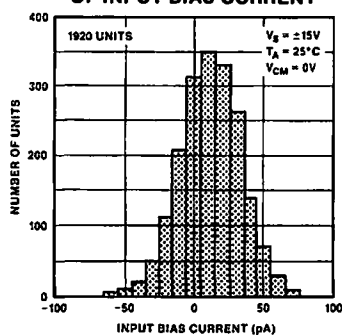
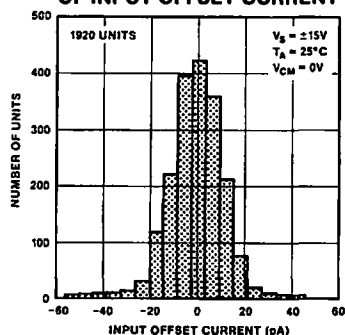
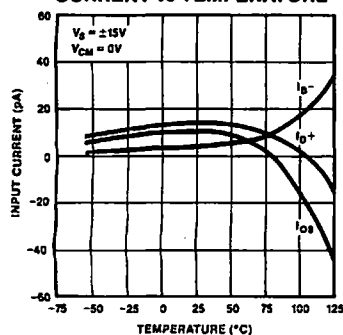
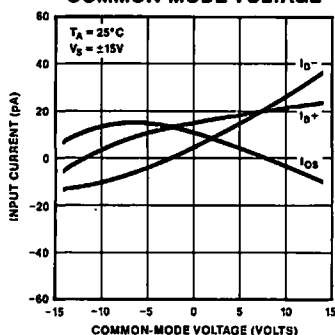
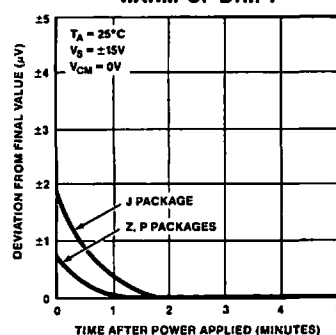
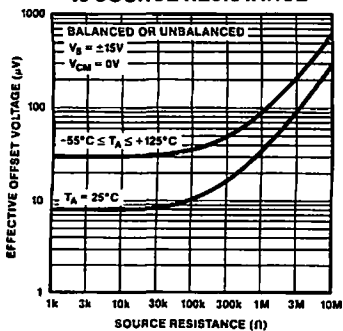
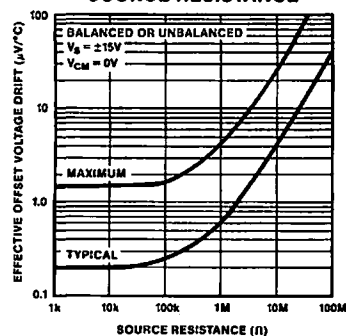
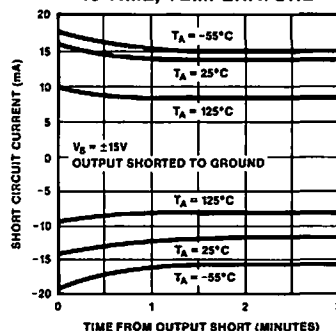
NOTES:

1. Final offset trims are not performed on dice. These trims are typically performed after packaging. Precision Monolithics Inc. assumes no responsibility for improper trimming by the customer. Contact factory for trim methods.
2. These specifications apply for $\pm 2V \leq V_S \leq \pm 20V$ and $-13.5V \leq V_{CM} \leq +13.5V$ (for $V_S = \pm 15V$).
3. Guaranteed by CMR test.

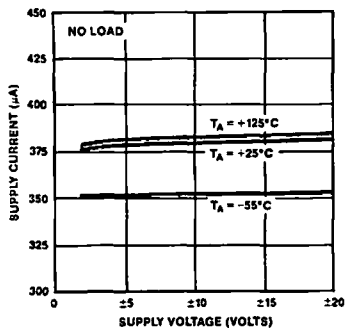
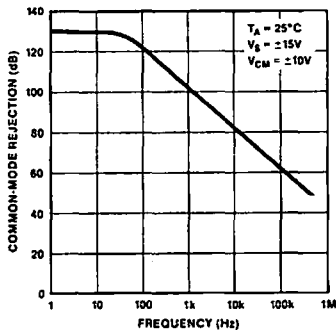
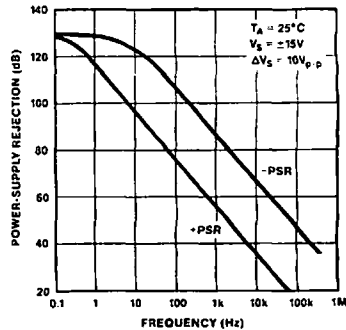
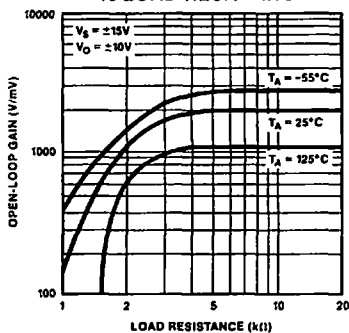
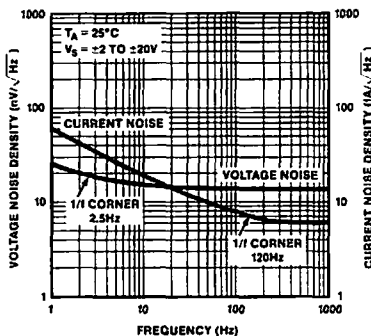
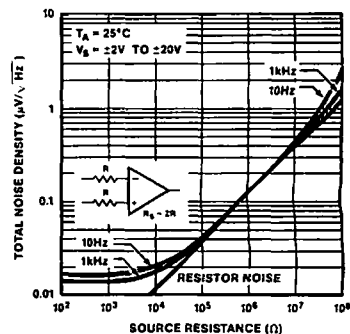
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



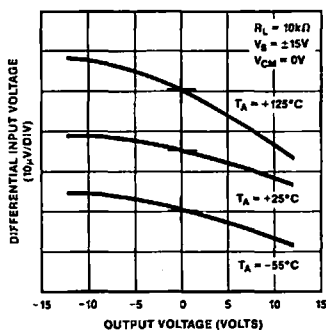
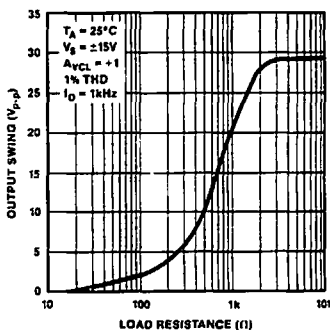
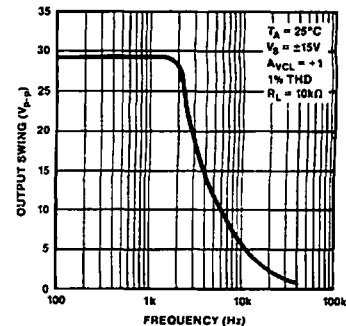
TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL DISTRIBUTION
OF INPUT OFFSET VOLTAGETYPICAL DISTRIBUTION
OF INPUT BIAS CURRENTTYPICAL DISTRIBUTION
OF INPUT OFFSET CURRENTINPUT BIAS, OFFSET
CURRENT vs TEMPERATUREINPUT BIAS, OFFSET
CURRENT vs
COMMON-MODE VOLTAGEINPUT OFFSET VOLTAGE
WARM-UP DRIFTEFFECTIVE OFFSET VOLTAGE
vs SOURCE RESISTANCEEFFECTIVE TCV_{OS} vs
SOURCE RESISTANCESHORT CIRCUIT CURRENT
vs TIME, TEMPERATURE

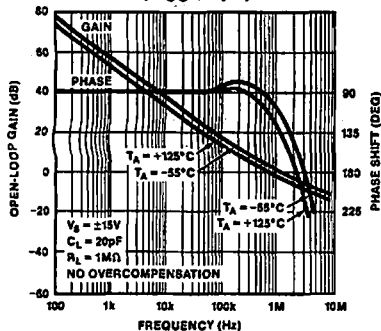
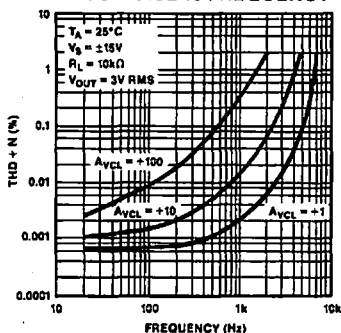
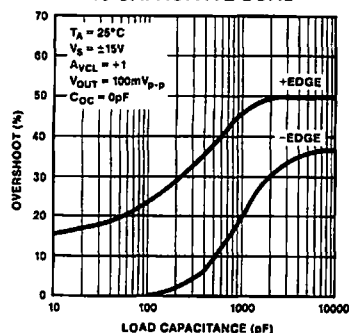
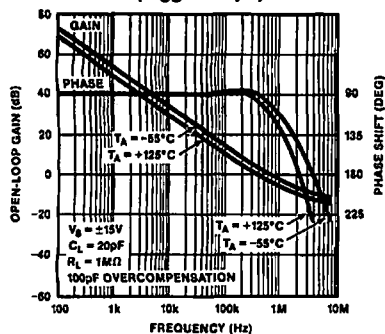
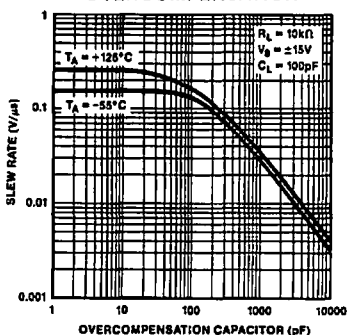
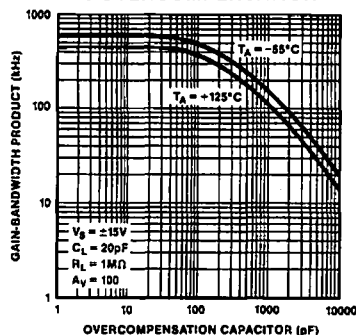
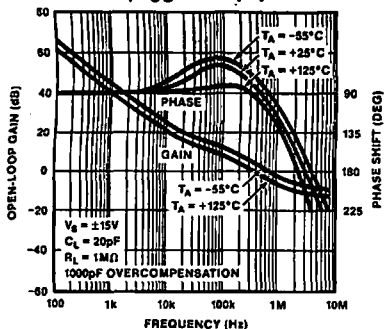
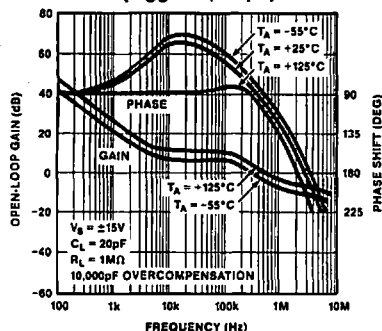
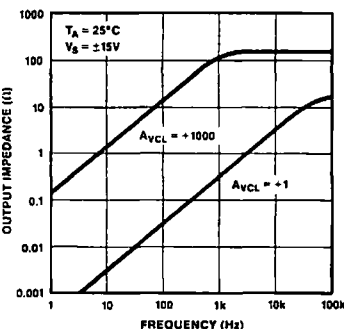
TYPICAL PERFORMANCE CHARACTERISTICS

 SUPPLY CURRENT vs
SUPPLY VOLTAGE

 COMMON-MODE REJECTION
vs FREQUENCY

 POWER-SUPPLY REJECTION
vs FREQUENCY

 OPEN-LOOP GAIN
vs LOAD RESISTANCE

 NOISE DENSITY
vs FREQUENCY

 TOTAL NOISE DENSITY
vs SOURCE RESISTANCE


OPEN-LOOP GAIN LINEARITY


 MAXIMUM OUTPUT SWING
vs LOAD RESISTANCE

 MAXIMUM OUTPUT SWING
vs FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS

**OPEN-LOOP GAIN,
PHASE vs FREQUENCY
($C_{OC} = 0\text{pF}$)**

**TOTAL HARMONIC
DISTORTION
PLUS NOISE vs FREQUENCY**

**SMALL-SIGNAL OVERSHOOT
vs CAPACITIVE LOAD**

**OPEN-LOOP GAIN,
PHASE vs FREQUENCY
($C_{OC} = 100\text{pF}$)**

**SLEW RATE vs
OVERCOMPENSATION**

**GAIN-BANDWIDTH PRODUCT
vs OVERCOMPENSATION**

**OPEN-LOOP GAIN,
PHASE vs FREQUENCY
($C_{OC} = 1000\text{pF}$)**

**OPEN-LOOP GAIN,
PHASE vs FREQUENCY
($C_{OC} = 10,000\text{pF}$)**

**CLOSED-LOOP OUTPUT
RESISTANCE vs FREQUENCY**




APPLICATIONS INFORMATION

The PM-1012 is an ideal amplifier for general-purpose applications where precision is critical and power dissipation must be minimized. Excellent input specifications and a wide supply-voltage range allows the PM-1012 to be stocked as a standard amplifier for a wide variety of circuits. Overall performance of the PM-1012 is similar to, and in many respects better than traditional amplifiers such as the OP-07, and the PM-1012 will directly upgrade these sockets.

Extremely low bias current over the full military temperature range makes the PM-1012 attractive for use in sample-and-hold amplifiers, peak detectors, and log amplifiers that must operate over a wide temperature range. Balancing input resistances is not necessary with the PM-1012. Offset voltage and TCV_{OS} are degraded only minimally by high source resistance, even when unbalanced.

The input pins of the PM-1012 are protected against large differential voltages by back-to-back diodes. Current-limiting resistors are not used so that low-noise performance is maintained. If differential voltages above $\pm 1V$ are expected at the inputs, series resistors must be used to limit the current flow to a maximum of 10mA. Common-mode voltages at the inputs are not restricted, and may vary over the full range of the supply voltages used.

The PM-1012 requires very little operating headroom about the supply rails, and is specified for operation with supplies as low as $\pm 2V$. Typically, the common-mode range extends to within one volt of either rail. The output typically swings to within one volt of the rails when using a 10k Ω load.

Offset nulling is achieved utilizing the same circuitry as an OP-07. A potentiometer between 5k Ω and 100k Ω is connected between pins 1 and 8 with the wiper connected to the positive supply. The trim range is between 300 μV and 850 μV , depending upon the internal trimming of the device.

FIGURE 1: Optional Input Offset Voltage Nulling and Over-compensation Circuits

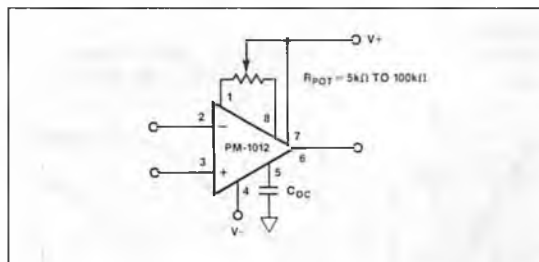
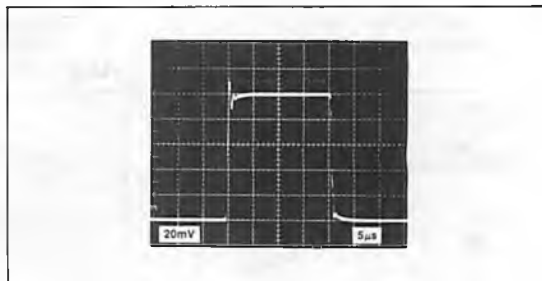


FIGURE 2: Small Signal Transient Response
($C_{LOAD} = 100pF$, $A_{VCL} = +1$)



AC PERFORMANCE

The PM-1012's AC characteristics are highly stable over its full operating temperature range. Unity-gain small signal response is shown in Figure 2. Extremely tolerant of capacitive loading on the output, the PM-1012 displays excellent response even with 1000pF loads (Figure 3). In large-signal applications, the input protection diodes effectively short the input to the output during the transients if the amplifier is connected in the usual unity-gain configuration. The output enters short-circuit current limit, with the flow going through the protection diodes. Improved large-signal transient response is obtained by using a feedback resistor between the output and the inverting input. Figure 4 shows the large-signal response of the PM-1012 in unity-gain with a 10k Ω feedback resistor. The unity-gain follower circuit is shown in Figure 5.

FIGURE 3: Small-Signal Transient Response
($C_{LOAD} = 1000pF$, $A_{VCL} = +1$)

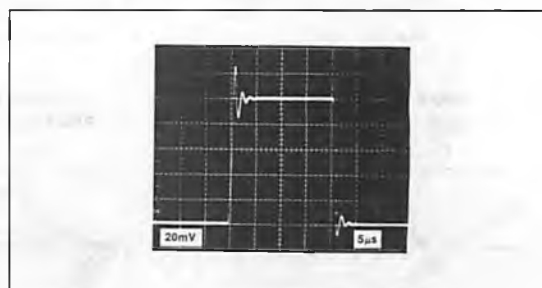


FIGURE 4: Large Signal Transient Response ($A_{VCL} = +1$)

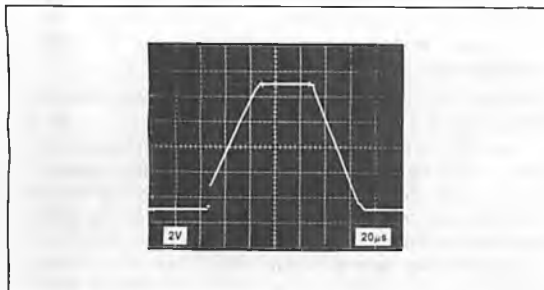
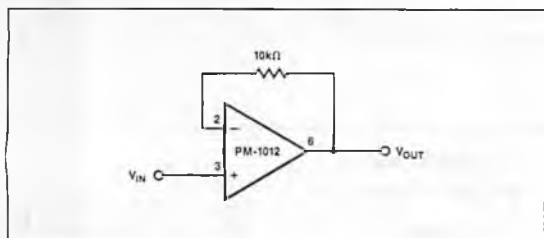


FIGURE 5: Unity-Gain Follower



USING OVERCOMPENSATION

The overcompensation pin provides flexibility for shaping AC response to an application's requirements. This pin may be used to increase the stability of circuits with large capacitive loads or gain in the feedback loop, or for feedforward compensation to improve slew rate.

Figure 6 shows feedforward compensation for a unity-gain follower. Slew rate is increased to close to $10V/\mu s$ in this circuit. Load driving ability is adversely affected by this compensation, and gain errors are incurred even with $10k\Omega$ loads. Feedforward compensation should be used with care to ensure that significant errors are not introduced.

Capacitive load driving ability is improved by using overcompensation in the circuit of Figure 1. The signal response in Figure 8 was made under the same conditions as Figure 3, except for the addition of a $220pF$ capacitor placed between pin 5 and ground. Overcompensation in this manner increases phase margin and decreases the gain-bandwidth product of the amplifier.

FIGURE 6: Follower Feedforward Compensation

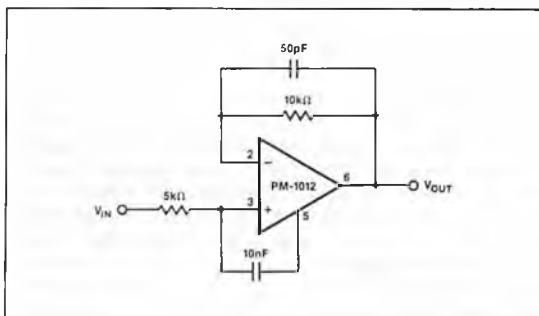


FIGURE 7: Feedforward Compensation Transient Response

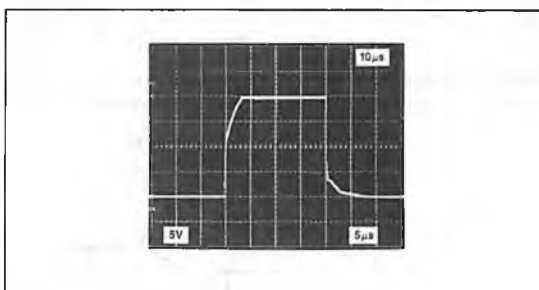
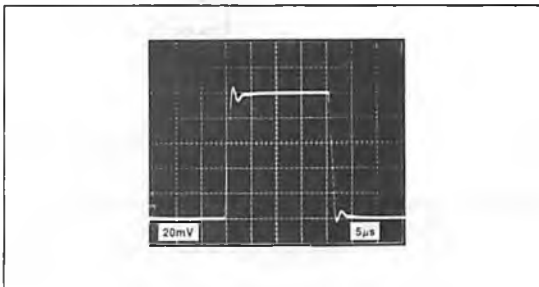


FIGURE 8: Small Signal Transient Response with Overcompensation ($C_{LOAD} = 1000pF$, $A_{VCL} = +1$, $C_{OC} = 220pF$)



GUARDING AND SHIELDING

To maintain the extremely high input impedances of the PM-1012, care must be taken in circuit board layout and manufacturing. Board surfaces must be kept scrupulously clean and free of moisture. Conformal coating is recommended to provide a humidity barrier. Even a clean PC board can have 100pA of leakage currents between adjacent traces, so that guard rings should be used around the inputs. Guard traces are operated at a voltage close to that on the inputs, so that leakage currents become minimal. In noninverting applications, the guard ring should be connected to the common-mode voltage at the inverting input (pin 2). In inverting applications, both inputs remain at ground, so that the guard trace should be grounded. Guard traces should be made on both sides of the circuit board.

High impedance circuitry is extremely susceptible to RF pickup, line-frequency hum, and radiated noise from switching

power-supplies. Enclosing sensitive analog sections within grounded shields is generally necessary to prevent excessive noise pickup. Twisted-pair cable will aid in rejection of line-frequency hum.

A precision absolute-value current-to-voltage converter that operates over a wide temperature range is shown in Figure 10. The PM-1012's low bias current over its full common-mode and temperature ranges ensures a high degree of linearity in this circuit. The PM-1012 acts as an inverting or noninverting current-to-voltage converter, depending upon the polarity of the input. While the input is sinking current, the voltage is developed across the resistor at the noninverting input, hence sources must have reasonable compliance. While the input is sourcing current, it remains at one diode drop below ground; compliance of a current sink at the input is less critical. If 1M Ω resistors are used, the circuit will output 1V/ μ A of input current.

FIGURE 9: Guard Ring Layout and Connections

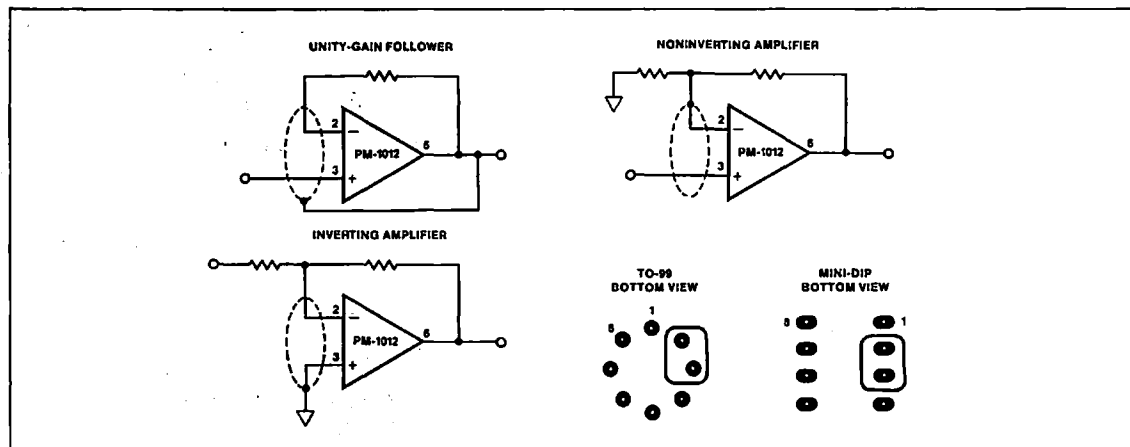


FIGURE 10: Precision Absolute-Value Current-to-Voltage Converter

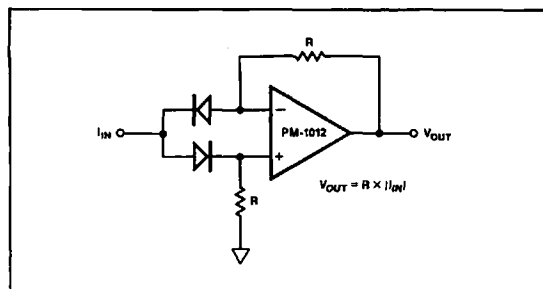
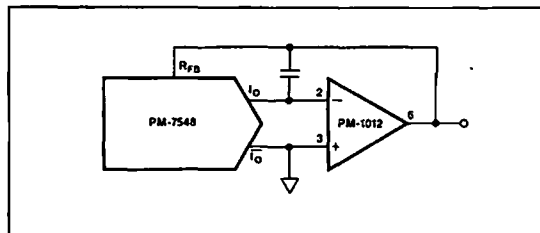


FIGURE 11: DAC Output Amplifier



The PM-1012 is an excellent amplifier for CMOS and bipolar DACs where high linearity is critical. Its low bias current and offset voltage ensures that linearity errors are negligible, even when operating with high resolution DACs and low reference voltages. A capacitor should be placed in the feedback loop of the amplifier to cancel the pole formed by the additional input capacitance from the DAC. Twenty to forty picofarads is usually adequate for compensation with CMOS or bipolar DACs.

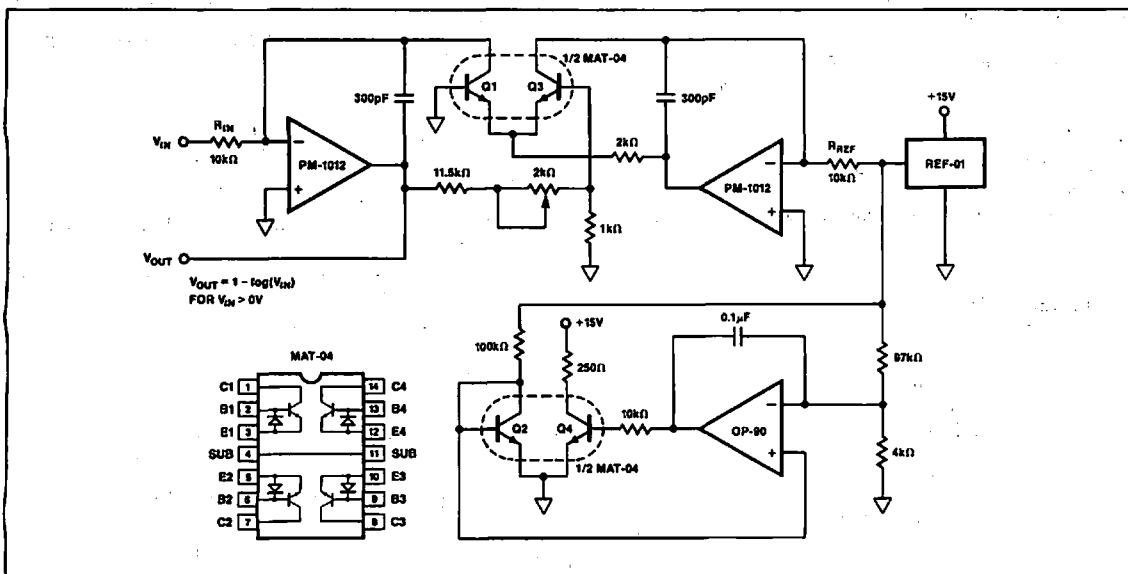
The logarithmic amplifier in Figure 12 eliminates thermal drift caused by temperature dependencies of the logging transistors by maintaining a monolithic quad matched transistor at a predetermined temperature. The MAT-04 has four transistors laid-out at the corners of a square die. Two transistors across a diagonal are used for logging elements. One of the remaining transistors is used as a heater to maintain a constant chip

temperature, and the remaining transistor, diagonally opposite to the heater, is used as a temperature sensor.

The OP-90 servo amplifier uses thermal feedback to set the temperature of the die. The base-to-emitter voltage of Q2 is maintained at the level set by the resistive divider from the REF-01, by controlling the current flowing through Q4. Although Q4 may operate at higher than the MAT-04's rated levels, this does not degrade operation since the characteristics of the heater transistor are non-critical. For best thermal regulation, the MAT-04 package should be encased in insulation. Urethane foam used for housing insulation is excellent for this purpose.

Gain is trimmed using the 2k Ω potentiometer. The zero-crossing point is adjusted by changing the value of R_{REF}. Input scaling may be changed by varying resistor R_{IN}.

FIGURE 12: Logarithmic Amplifier with Heated Logging Transistors





JM38510/10104

JAN SINGLE LOW-INPUT-CURRENT
OPERATIONAL AMPLIFIER [EXTERNALLY COMPENSATED]

Precision Monolithics Inc.

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low input-current, externally-compensated operational amplifier as specified in MIL-M-38510/101 for device type 04. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/101 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type
04

Generic-industry Type
LM108A

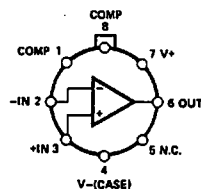
CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline A-1 (8 Lead Can), Package Type Designator "G"; and Appendix C, Case Outline D-4 (8 Lead Dual-in-Line), Package Type Designator "P".

ORDERING INFORMATION

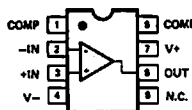
JAN SLASH SHEET	PMI DEVICE
JM38510/10104BGC	PM108AJ1/38510
JM38510/10104BGA	PM108AJ5/38510
JM38510/10104BPB	PM108AZ2/38510
JM38510/10104BPA	PM108AZ5/38510

PIN CONNECTIONS



TO-99
GOLD PLATE LEAD TYPE
(J1-Suffix)

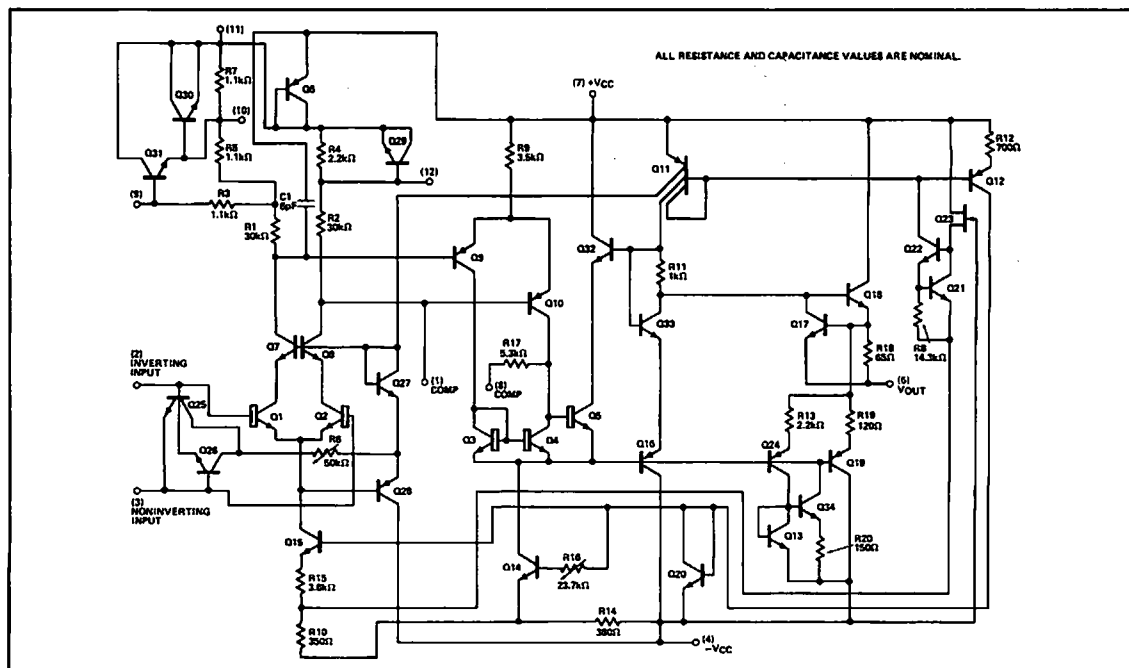
SOLDER DIPPED LEAD TYPE
(J5-Suffix)



8-PIN HERMETIC DIP
TIN REFLOW LEAD TYPE
(Z2-Suffix)

SOLDER DIPPED LEAD TYPE
(Z5-Suffix)

SIMPLIFIED SCHEMATIC



**ELECTRICAL CHARACTERISTICS** at $5V \leq V_{CC} \leq 20V$ and $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	(Note 2) $T_A = 25^{\circ}C$ $R_S = 50\Omega$ $-55^{\circ}C \leq T_A \leq 125^{\circ}C$	-0.5 -1.0	+0.5 +1.0	mV
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from $-55^{\circ}C$ to $+25^{\circ}C$ ΔT_A from $+25^{\circ}C$ to $+125^{\circ}C$	-5.0 -5.0	+5.0 +5.0	$\mu V/^{\circ}C$
Input Offset Current	I_{IO}	(Note 2) $T_A = 25^{\circ}C$ $-55^{\circ}C \leq T_A \leq 125^{\circ}C$	-0.2 -0.4	+0.2 +0.4	nA
Input Offset Current Temperature Sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from $-55^{\circ}C$ to $+25^{\circ}C$ ΔT_A from $+25^{\circ}C$ to $+125^{\circ}C$	-2.5 -2.5	+2.5 +2.5	$pA/^{\circ}C$
Input Bias Current	$+I_{IB}$	(Note 2) $25^{\circ}C \leq T_A \leq 125^{\circ}C$ $-55^{\circ}C \leq T_A \leq +25^{\circ}C$	-1.0 -0.1	+2.0 +3.0	nA
	$-I_{IB}$	(Note 2) $25^{\circ}C \leq T_A \leq 125^{\circ}C$ $-55^{\circ}C \leq T_A \leq +25^{\circ}C$	-1.0 -0.1	+2.0 +3.0	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 10V$ $T_A = 25^{\circ}C$ $-V_{CC} = 20V$ $R_S = 50\Omega$ $-55^{\circ}C \leq T_A \leq 125^{\circ}C$	-16 -16	+16 +16	$\mu V/V$
Power Supply Rejection Ratio	-PSRR	$+V_{CC} = 20V$ $T_A = 25^{\circ}C$ $-V_{CC} = -10V$ $R_S = 50\Omega$ $-55^{\circ}C \leq T_A \leq 125^{\circ}C$	-16 -16	+16 +16	$\mu V/V$
Input Voltage Common-Mode Rejection	CMR	$\pm V_{CC} = 20V$ $V_{IN} = \pm 15V$ $R_S = 50\Omega$	96	—	dB
Adjustment For Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Adjustment For Input Offset Voltage	V_{IO} ADJ (-)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Output Short-Circuit Current (For Positive Output)	$I_{OS(+)}$	$\pm V_{CC} = 15V$ $t \leq 25ms$ (Note 3)	15	—	mA
Output Short-Circuit Current (For Negative Output)	$I_{OS(-)}$	$\pm V_{CC} = 15V$ $t \leq 25ms$ (Note 3)	—	15	mA
Supply Current	I_{CC}	$T_A = -55^{\circ}C$	—	0.8	mA
		$T_A = +25^{\circ}C$	—	0.6	
		$T_A = +125^{\circ}C$	—	0.6	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = 20V$, $R_L = 10k\Omega$	± 16	—	V
		$\pm V_{CC} = 20V$, $R_L = 2k\Omega$	—	—	
Open-Loop Voltage Gain (Single Ended) (Note 1)	$A_{VS(1)}$	$\pm V_{CC} = 20V$ $T_A = 25^{\circ}C$ $R_L = 10k\Omega$ $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ $V_{OUT} = \pm 15V$	80 40	— —	V/mV
Open-Loop Voltage Gain (Single Ended) (Note 1)	A_{VS}	$\pm V_{CC} = 5V$ $R_L = 10k\Omega$ $V_{OUT} = \pm 2V$	20	—	V/mV
Transient Response Rise Time	$TR_{(tr)}$	$C_F = 10pF$	—	1000	nsec
Transient Response Overshoot	$TR_{(OS)}$	$C_F = 10pF$	—	50	%
Noise (Referred to Input) Broadband	$N_1(BB)$	$V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25^{\circ}C$	—	15	μV rms
Noise (Referred to Input) Popcorn	$N_1(PC)$	$\pm V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25^{\circ}C$	—	40	μV peak

NOTES:

- Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed-loop applications (closed-loop gain less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements

exist (positive open-loop gain or open-loop gain linearity), they should be specified in the individual procurement document as additional requirements.

- Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
- Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75^{\circ}C$ will cause T_J to exceed the maximum of $175^{\circ}C$.

ELECTRICAL CHARACTERISTICS at $5V \leq V_{CC} \leq 20V$ and $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Slew Rate	SR (+)	$A_V = 1$	0.05	—	$V/\mu\text{sec}$
		$V_{IN} = +5V$ $-55^{\circ}C \leq T_A \leq 25^{\circ}C$ $T_A = 125^{\circ}C$	0.05	—	
Slew Rate	SR (-)	$A_V = 1$	0.05	—	$V/\mu\text{sec}$
		$V_{IN} = \pm 5V$ $-55^{\circ}C \leq T_A \leq 25^{\circ}C$ $T_A = 125^{\circ}C$	0.05	—	

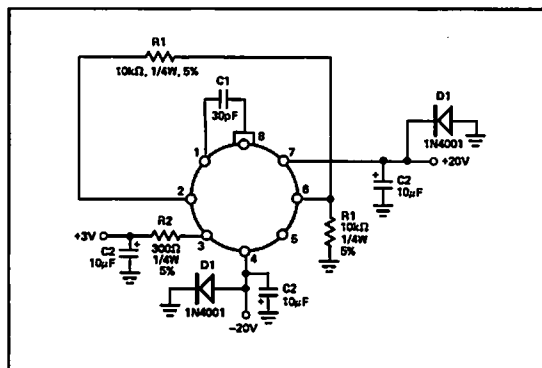
NOTES:

- Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed-loop applications (closed-loop gain less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open-loop gain or open-loop gain linearity), they should be

specified in the individual procurement document as additional requirements.

- Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
- Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75^{\circ}C$ will cause T_I to exceed the maximum of $175^{\circ}C$.

For Other Test Circuit Diagrams, See MIL-M-38510/101

BURN-IN CIRCUIT**POWER AND THERMAL CHARACTERISTICS**

Package	Case outline	Maximum allowable power dissipation	Maximum $\theta_{JA}-C$	Maximum $\theta_{JA}-A$
8 Lead Can (TO-99)	G	330mW at $T_A = 125^{\circ}C$	40^{\circ}C/W	150^{\circ}C/W
8 Lead Hermetic (Dual-in-Line)	P	417mW at $T_A = 125^{\circ}C$	50^{\circ}C/W	120^{\circ}C/W



JM38510/10106

JAN DUAL LOW-INPUT-CURRENT OPERATIONAL AMPLIFIER (EXTERNALLY COMPENSATED)

Precision Monolithics Inc.

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a dual low input-current, externally-compensated operational amplifier as specified in MIL-M-38510/101 for device type 06.

Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/101 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

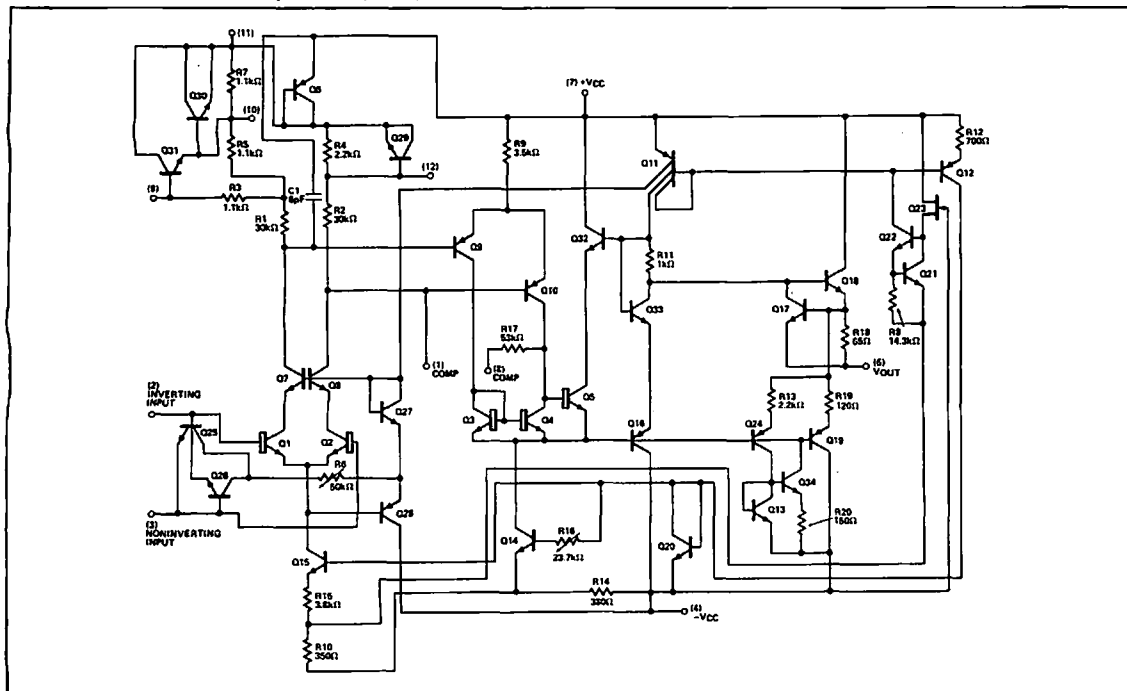
This cross-reference information is presented for the convenience of the user. The generic industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type	Generic Industry Type
06	LM2108A

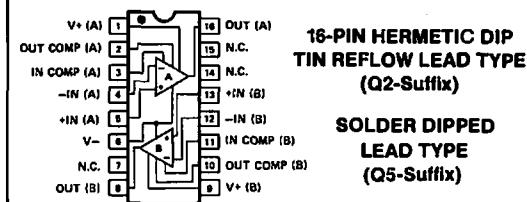
CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline D-2 (16-pin DIP). Package Type Designator "E".

SIMPLIFIED SCHEMATIC (Each Amplifier)



PIN CONNECTIONS



ORDERING INFORMATION

Jan Device Type	PMI Device Type
JM38510/10106BEB	PM2108AQ2/38510
JM38510/10106BEA	PM2108AQ5/38510

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{JA}	Maximum θ_{JC}
Dual-in-line	E	400mW at $T_A = 125^\circ\text{C}$	35°C/W	120°C/W

OPERATIONAL AMPLIFIERS

**ELECTRICAL CHARACTERISTICS** at $5V \leq V_{CC} \leq 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Offset Voltage	V_{IO}	(Note 2) $T_A = 25^\circ C$ $R_S = 50\Omega$ $-55^\circ C \leq T_A \leq 125^\circ C$	-0.5 -1.0	+0.5 +1.0	mV
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	ΔT_A from $-55^\circ C$ to $+25^\circ C$ ΔT_A from $+25^\circ C$ to $+125^\circ C$	-5.0 -5.0	+5.0 +5.0	$\mu V/^\circ C$
Input Offset Current	I_{IO}	(Note 2) $T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq 125^\circ C$	-0.2 -0.4	+0.2 +0.4	nA
Input Offset Current Temperature Sensitivity	$\frac{\Delta I_{IO}}{\Delta T}$	ΔT_A from $-55^\circ C$ to $+25^\circ C$ ΔT_A from $+25^\circ C$ to $+125^\circ C$	-2.5 -2.5	+2.5 +2.5	$pA/^\circ C$
Input Bias Current	$+I_{IB}$	(Note 2) $25^\circ C \leq T_A \leq 125^\circ C$ $-55^\circ C \leq T_A \leq +25^\circ C$	-1.0 -0.1	+2.0 +3.0	nA
	$-I_{IB}$	(Note 2) $25^\circ C \leq T_A \leq 125^\circ C$ $-55^\circ C \leq T_A \leq +25^\circ C$	-1.0 -0.1	+2.0 +3.0	nA
Power Supply Rejection Ratio	$+PSRR$	$+V_{CC} = 10V$ $R_S = 50\Omega$ $T_A = 25^\circ C$ $-V_{CC} = -20V$ $-55^\circ C \leq T_A \leq 125^\circ C$	-16 -16	+16 +16	$\mu V/V$
	$-PSRR$	$+V_{CC} = 20V$ $R_S = 50\Omega$ $T_A = 25^\circ C$ $-V_{CC} = -10V$ $-55^\circ C \leq T_A \leq 125^\circ C$	-16 -16	+16 +16	$\mu V/V$
Input Voltage Common-Mode Rejection	CMR	$\pm V_{CC} = 20V$ $V_{IN} = \pm 15V$ $R_S = 50\Omega$	96	—	dB
Adjustment For Input Offset Voltage	V_{IO} ADJ (+)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Adjustment For Input Offset Voltage	V_{IO} ADJ (-)	$\pm V_{CC} = 20V$	No External Adjustment		mV
Output Short-Circuit Current (For Positive Output)	$I_{OS (+)}$	$\pm V_{CC} = 15V$ $t \leq 25ms$ (Note 3)	15	—	mA
Output Short-Circuit Current (For Negative Output)	$I_{OS (-)}$	$\pm V_{CC} = 15V$ $t \leq 25ms$ (Note 3)	—	15	mA
Supply Current	I_{CC}	$T_A = -55^\circ C$	—	0.8	mA
		$T_A = +25^\circ C$	—	0.6	
		$T_A = +125^\circ C$	—	0.6	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = 20V$, $R_L = 10k\Omega$	± 16	—	V
		$\pm V_{CC} = 20V$, $R_L = 2k\Omega$	—	—	
Open-Loop Voltage Gain (Single Ended) (Note 1)	$A_{VS} (\pm)$	$\pm V_{CC} = 20V$ $T_A = 25^\circ C$ $R_L = 10k\Omega$ $-55^\circ C \leq T_A \leq 125^\circ C$ $V_{OUT} = \pm 15V$	80 40	— —	V/mV
Open-Loop Voltage Gain (Single Ended) (Note 1)	A_{VS}	$\pm V_{CC} = 5V$ $R_L = 10k\Omega$ $V_{OUT} = \pm 2V$	20	—	V/mV
Transient Response Rise Time	$TR_{(tr)}$	$C_F = 10pF$	—	1000	nsec
Transient Response Overshoot	$TR_{(OS)}$	$C_F = 10pF$	—	50	%
Noise (Referred to Input) Broadband	$N_I (BB)$	$V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25^\circ C$	—	15	μV rms
Noise (Referred to Input) Popcorn	$N_I (PC)$	$\pm V_{CC} = 20V$ Bandwidth = 5kHz $T_A = 25^\circ C$	—	40	μV peak

NOTES:

1. Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed-loop applications (closed-loop gain less than 1,000), the open-loop tests (A_{VS}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open-loop gain or open-loop gain linearity), they should be specified in the individual procurement document as additional requirements.

2. Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.

3. Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75^\circ C$ will cause T_J to exceed the maximum of $175^\circ C$. For dual devices, I_{OS} is measured one channel at a time.

**ELECTRICAL CHARACTERISTICS** at $5V \leq \pm V_{CC} \leq 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Slew Rate	SR (+)	$A_V = 1$ $V_{IN} = +5V$ $-55^\circ C \leq T_A \leq 25^\circ C$ $T_A = 125^\circ C$	0.05 0.05	—	V/ μ sec
Slew Rate	SR (-)	$A_V = 1$ $V_{IN} = \pm 5V$ $-55^\circ C \leq T_A \leq 25^\circ C$ $T_A = 125^\circ C$	0.05 0.05	—	V/ μ sec
Settling Time	$t_s (+)$	$T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq 125^\circ C$	—	—	ns
	$t_s (-)$	$T_A = 25^\circ C$ $-55^\circ C \leq T_A \leq 125^\circ C$	—	—	ns
Channel Separation	CS	$\pm V_{CC} = 20V$ $T_A = 25^\circ C$	80	—	dB

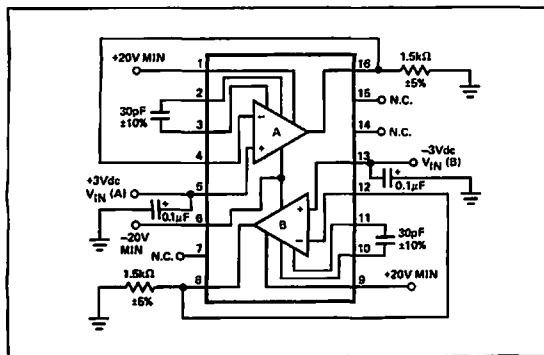
NOTES:

- Note that gain is not specified at $V_{IO(ADJ)}$ extremes. Some gain reduction is usually seen at $V_{IO(ADJ)}$ extremes. For closed-loop applications (closed-loop gain is less than 1,000), the open-loop tests (A_{VSL}) prescribed herein should guarantee a positive, reasonably linear, transfer characteristic. They do not, however, guarantee that the open-loop gain is linear, or even positive, over the operating range. If either of these requirements exist (positive open-loop gain or open-loop gain linearity), they should be

specified in the individual procurement document as additional requirements.

- Tests at common-mode $V_{CM} = 0$, $V_{CM} = -15V$, and $V_{CM} = +15V$.
- Continuous short-circuit limits will be considerably less than the indicated test limits. Continuous I_{OS} at $T_A \leq 75^\circ C$ will cause T_J to exceed the maximum of $175^\circ C$. For dual devices, I_{OS} is measured one channel at a time.

For other Test Circuit Diagrams, See MIL-M-38510/101

BURN-IN CIRCUIT



JM38510/11004

JAN QUAD 741-TYPE
OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low Broadband Noise $5\mu V_{rms}$ Max
- RM-4136 Direct Replacement
- Silicon-Nitride Passivation
- Low Crossover Distortion
- Continuous Short-Circuit Protection
- MIL-M-38510 Processed

ORDERING INFORMATION

JAN SLASH SHEET	PMI DEVICE
JM38510/11004BCB	PM-4136Y2/38510
JM38510/11004BCA	PM-4136Y5/38510

GENERAL DESCRIPTION

The PM-4136Y2/38510 provides four matched 741-type operational amplifiers in a 14-pin hermetic dual-in-line package. The device is manufactured to meet or exceed all terms and conditions of the MIL-M-38510/110A slash sheet, under the requirements of the MIL-M-38510 general microcircuit specifications. Complete device specifications, test configurations, and manufacturing requirements are found in the slash sheet and general specifications.

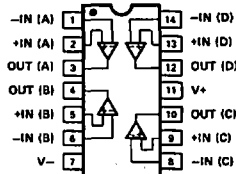
GENERIC CROSS-REFERENCE INFORMATION

The PM-4136Y2/38510 is PMI's product name for the JM38510/11004BCB. The PM-4136Y2/38510 is a 38510-processed version of the industry-standard RM4136.

The generic industry device may not have identical operational performance characteristics across the Military temperature range, or reliability factors equivalent to the 38510 device.

For an 883-processed device with improved electrical specifications, review the OP-09 data sheet.

PIN CONNECTIONS



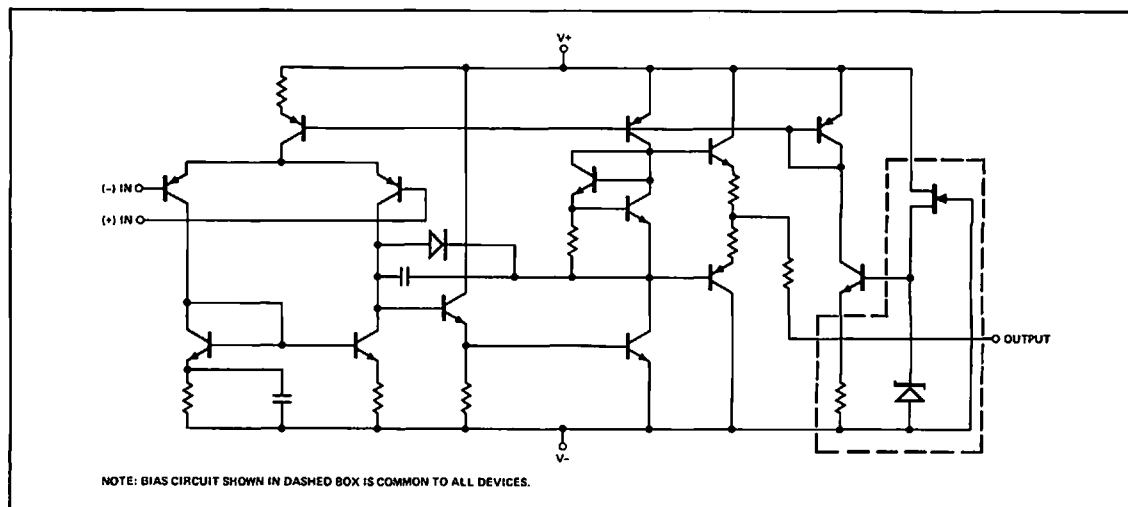
14-PIN HERMETIC DIP
TIN REFLOW LEAD TYPE
(Y2-Suffix)

SOLDER DIPPED LEAD TYPE
(Y5-Suffix)

POWER AND THERMAL CHARACTERISTICS

Case Outline	Package	Maximum Allowable Power Dissipation	Maximum θ_{JC}	Maximum θ_{JA}
Y	Dual-In-Line	400mW @ $T_A = 125^\circ C$	$35^\circ C/W$	$120^\circ C/W$

SIMPLIFIED SCHEMATIC (One of Four Amplifiers is Shown)



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage Range (Note 1) $\pm 22\text{V}$
 Input Voltage Range (Note 2) $\pm 22\text{V}$
 Differential Input Voltage Range (Note 3) $\pm 30\text{V}$
 Input Current Range 10 to 0.1mA
 Storage Temperature Range -65°C to $+150^{\circ}\text{C}$
 Output Short-Circuit Duration (Note 4) Unlimited
 Lead Temperature (Soldering, 60 sec) 300°C
 Junction Temperature (T_J) (Note 5) 175°C

NOTES:

1. Voltages in excess of these may be applied for short-term tests if voltage difference does not exceed 44 volts.
2. For supply voltages less than $\pm 20\text{V}$, the absolute maximum input voltage is equal to the supply voltage.

3. The differential input voltage range shall not exceed the supply voltage range.
4. Short circuit may be to ground or either supply. Rating applies to $+125^{\circ}\text{C}$ case temperature or $+75^{\circ}\text{C}$ ambient temperature.
5. For short-term test (in the specific burn-in and life-test configuration where required and up to 168 hours maximum) $T_J = 275^{\circ}\text{C}$.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range $\pm 5\text{V}$ to $\pm 20\text{V}$
 Ambient Temperature Range -55° to $+125^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS at $\pm 5\text{V} \leq V_{CC} \leq \pm 20\text{V}$ and $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $R_S = 50\Omega$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	04 LIMITS		UNITS
			MIN	MAX	
Input Offset Voltage	V_{IO}	$T_A = 25^{\circ}\text{C}$ $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ (Note 1)	-5 -6	5 6	mV
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}/\Delta T$	$-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$	-25	25	$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current	I_{IO}	$25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$, $R_S = 20\text{k}\Omega$ (Note 1)	-75	75	nA
		$T_A = -55^{\circ}\text{C}$, $R_S = 20\text{k}\Omega$ (Note 1)	-150	150	
Input Offset Current Temperature Sensitivity	$\Delta I_{IO}/\Delta T$	$-55^{\circ}\text{C} \leq T_A \leq 25^{\circ}\text{C}$	-1000	1000	$\text{pA}/^{\circ}\text{C}$
		$25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$	-500	500	
Input Bias Current	$+I_{IB}$	$R_S = 20\text{k}\Omega$, $25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ $T_A = -55^{\circ}\text{C}$ (Note 1)	-250 -400	-1 -1	nA
	$-I_{IB}$	$R_S = 20\text{k}\Omega$, $25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ $T_A = -55^{\circ}\text{C}$ (Note 1)	-250 -400	-1 -1	
Power Supply Rejection Ratio	$+PSRR$	$+V_{CC} = 10\text{V}$, $-V_{CC} = -20\text{V}$	-100	100	$\mu\text{V/V}$
	$-PSRR$	$+V_{CC} = 20\text{V}$, $-V_{CC} = -10\text{V}$	-100	100	
Input Voltage Common-Mode Rejection	CMR	Common-Mode Range = 30V (Note 2)	76	—	dB
Output Short Circuit Current	$I_{OS(+)}$	$\pm V_{CC} = \pm 15\text{V}$, $25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ (Note 3)	-80	—	mA
Output Short Circuit Current	$I_{OS(-)}$	$\pm V_{CC} = \pm 15\text{V}$, $T_A = -55^{\circ}\text{C}$ (Note 3)	—	80	
Supply Current	I_{CC}	$V_{CC} = \pm 15\text{V}$, $T_A = -55^{\circ}\text{C}$	—	13	mA
		(Note 4), $T_A = 25^{\circ}\text{C}$	—	11	
		$T_A = 125^{\circ}\text{C}$	—	11	
Output Voltage Swing (Maximum)	$+V_{OP}$	$V_{CC} = \pm 20\text{V}$, $R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$	+16 +15	—	V
	$-V_{OP}$	$V_{CC} = \pm 20\text{V}$, $R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$	—	-16 -15	

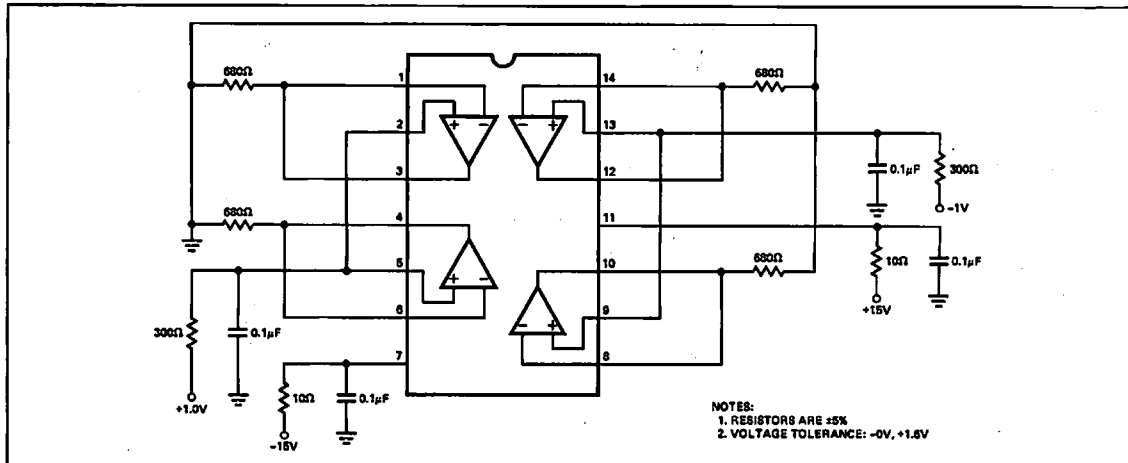
ELECTRICAL CHARACTERISTICS at $\pm 5V \leq V_{CC} \leq \pm 20V$ and $-55^\circ C \leq T_A \leq 125^\circ C$, $R_S = 50\Omega$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	04 LIMITS		UNITS
			MIN	MAX	
Open-Loop Voltage Gain (Single Ended)	$A_{VS(+)}$	$R_L = 10k\Omega$, $\pm V_O = \pm 15V$, $T_A = 25^\circ C$	50	—	V/mV
		$-55^\circ C \leq T_A \leq 125^\circ C$	25	—	
	$A_{VS(-)}$	$R_L = 2k\Omega$, $\pm V_O = \pm 15V$, $T_A = 25^\circ C$	50	—	
		$-55^\circ C \leq T_A \leq 125^\circ C$	25	—	
	A_{VS}	$R_L = 10k\Omega$, $T_A = 25^\circ C$	10	—	
		$R_L = 2k\Omega$, $\pm V_{CC} = \pm 5V$, $-55^\circ C \leq T_A \leq 125^\circ C$	10	—	
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 20V$, $A_V = 1$	—	0.3	μs
Transient Response Overshoot	$TR_{(OS)}$	$\pm V_{CC} = \pm 20V$	—	50	μs
Slew Rate	$SR(+)$	$\pm V_{CC} = \pm 20V$, $A_V = 1$	0.6	—	V/ μs
Noise (Broadband)	$N_1(BB)$	$T_A = 25^\circ C$, $\pm V_{CC} = \pm 20V$, $R_S = 50\Omega$	—	5	μV_{rms}
Noise (Popcorn)	$N_1(PC)$	$T_A = 25^\circ C$, $\pm V_{CC} = \pm 20V$, $R_S = 20k\Omega$	—	50	μV_{pk}
Channel Separation	CS	$T_A = 25^\circ C$	80	—	dB

NOTES:

- Tested at $V_{CM} = 0$, $+15V$ and $-15V$ with $\pm V_{CC} = \pm 20V$; and at $V_{CM} = 0V$ and $-2.5V$ with $\pm V_{CC} = \pm 5V$.
- CMR is determined by measuring input offset voltage as follows:
- Only one amplifier shorted to ground at one time, $0 \leq t \leq 25ms$. Continuous limits will be considerably lower and apply for $-55^\circ C \leq T_A \leq 25^\circ C$.
- I_{CC} limits are the total for all four amplifiers at no load, connected as followers with the noninverting inputs grounded.

OFFSET VOLTAGE CONDITION	$+V_{CC}$	$-V_{CC}$	V_O
1	35V	-5V	15V
2	5V	-35V	-15V

BURN-IN CIRCUIT




JM38510/11401/11402/11403/ 11404/11405/11406

JAN JFET-INPUT
OPERATIONAL AMPLIFIERS

Precision Monolithics Inc.

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low-power, internally-compensated JFET-input operational amplifier as specified in MIL-M-38510/114 for device types 01 to 06. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/114 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

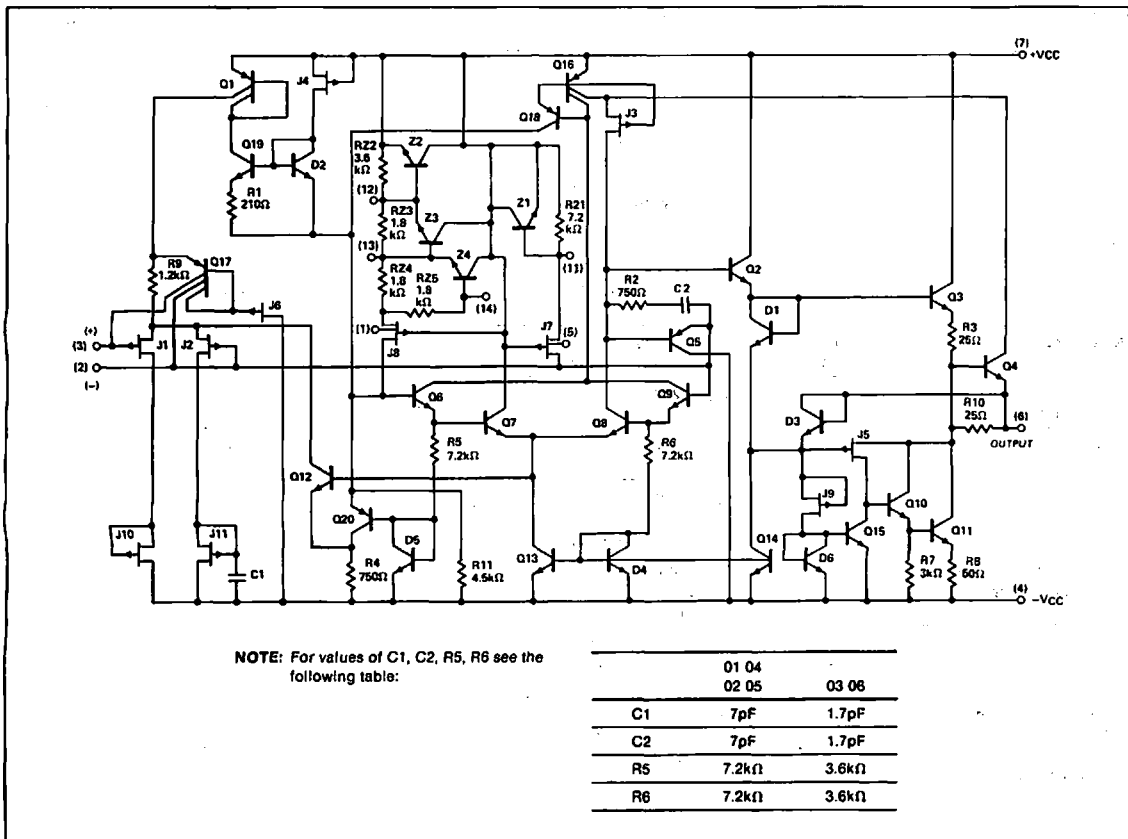
This cross-reference information is presented for the convenience of the user. The generic-industry types listed may

not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

Military Device Type	Generic-Industry Type
01	LF-155
04	LF-155A
02	LF-156
05	LF-156A
03	LF-157
06	LF-157A

5

SIMPLIFIED SCHEMATIC



OPERATIONAL AMPLIFIERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	$\pm 22\text{V}$
Input Voltage Range (Note 1)	$\pm 20\text{V}$
Differential Input Voltage Range	$\pm 40\text{V}$
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature	$T_J = 175^\circ\text{C}$ (Note 3)
Storage Temperature Range	-85°C to $+150^\circ\text{C}$
Output Short-Circuit Duration	Unlimited (Note 2)

NOTES:

1. The absolute maximum negative input voltage is equal to the negative power supply voltage.

2. Short circuit may be to ground to either supply. Rating applies to $+125^\circ\text{C}$ case temperature or $+75^\circ\text{C}$ ambient temperature.
3. For short-term test (in the specific burn-in and life test configuration when required and up to 168 hours maximum), $T_J = 275^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	± 5 to $\pm 20\text{VDC}$
Ambient Temperature Range	-55°C to $+125^\circ\text{C}$

ELECTRICAL CHARACTERISTICS at V_{CC} from $\pm 5\text{V}$ to $\pm 20\text{V}$; source resistance = 50 ohm ; ambient temperature range = -55°C to $+125^\circ\text{C}$ and figure 1, unless otherwise noted.

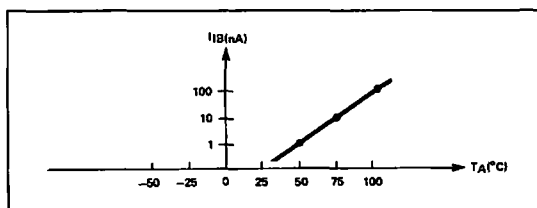
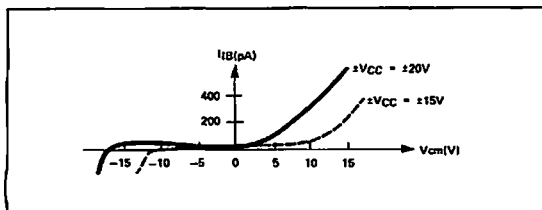
PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		04 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5\text{V}$, $V_{CM} = 0\text{V}$ $T_A = 25^\circ\text{C}$	-5	5	-2	2	mV
		$\pm V_{CC} = \pm 20\text{V}$ $V_{CM} = \pm 15\text{V}$, 0V $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	-7	7	-2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20\text{V}$ $V_{CM} = 0\text{V}$	-30	30	-10	10	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20\text{V}$, $V_{CM} = 0\text{V}$, $T_J = 25^\circ\text{C}$	-20	20	-20	20	pA
		$T_J = 125^\circ\text{C}$	-20	20	-20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$	$\pm V_{CC} = \pm 20\text{V}$, $V_{CM} = +15\text{V}$ $T_J = 25^\circ\text{C}$	-100	3500	-100	3500	pA
		$t \leq 25\text{ms}$, $T_J = 125^\circ\text{C}$	-10	60	-10	60	nA
	$-I_{IB}$	$\pm V_{CC} = \pm 15\text{V}$, $V_{CM} = +10\text{V}$ $T_J = 25^\circ\text{C}$	-100	300	-100	300	pA
		$t \leq 25\text{ms}$, $T_J = 125^\circ\text{C}$	-10	50	-10	50	nA
		$\pm V_{CC} = \pm 20\text{V}$, $-15\text{V} \leq V_{CM} \leq 0\text{V}$ $T_J = 25^\circ\text{C}$	-100	100	-100	100	pA
		$t \leq 25\text{ms}$, $T_J = 125^\circ\text{C}$	-10	50	-10	50	nA
Power Supply Rejection Ratio	$+PSRR$ $-PSRR$	$+V_{CC} = 10\text{V}$, $-V_{CC} = -20\text{V}$	85	—	85	—	dB
		$+V_{CC} = 20\text{V}$, $-V_{CC} = -10\text{V}$	—	—	—	—	—
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20\text{V}$ $V_{IN} = \pm 15\text{V}$	85	—	85	—	dB
Adjustment for Input Offset Voltage	$V_{IO\text{ ADJ}(+)}$	$\pm V_{CC} = \pm 20\text{V}$	+8	—	+8	—	mV
	$V_{IO\text{ ADJ}(-)}$	$\pm V_{CC} = \pm 20\text{V}$	—	-8	—	-8	
Output Short-Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15\text{V}$ $t \leq 25\text{ms}$ (Short Circuit to Ground)	-50	—	-50	—	mA
Output Short-Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15\text{V}$ $t \leq 25\text{ms}$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$T_A = -55^\circ\text{C}$	—	6	—	6	mA
		$\pm V_{CC} = \pm 15\text{V}$, $T_A = +25^\circ\text{C}$	—	4	—	4	
		$T_A = +125^\circ\text{C}$	—	4	—	4	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20\text{V}$, $R_L = 10\text{k}\Omega$	± 16	—	± 16	—	V
		$\pm V_{CC} = \pm 20\text{V}$, $R_L = 2\text{k}\Omega$	± 15	—	± 15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$ $A_{VS(-)}$	$\pm V_{CC} = \pm 20\text{V}$, $V_{OUT} = \pm 15\text{V}$ $R_L = 2\text{k}\Omega$, $T_A = 25^\circ\text{C}$	50	—	50	—	V/mV
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5\text{V}$ $R_L = 2\text{k}\Omega$ $V_{OUT} = \pm 2\text{V}$	10	—	10	—	V/mV

ELECTRICAL CHARACTERISTICS at V_{CC} from $\pm 5V$ to $\pm 20V$; source resistance = 50 ohm; ambient temperature range = $-55^{\circ}C$ to $+125^{\circ}C$ and figure 1, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		04 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Transient Response Rise Time	$T_{R(Tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	150	—	150	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	40	—	40	%
Slew Rate	$SR(+)$ and $SR(-)$	$V_{IN} = \pm 5V$, $\pm V_{CC} = \pm 15V$ $A_V = 1$, See Figure 2 $T_A = 25^{\circ}C$ $T_A = -55^{\circ}C$, $+125^{\circ}C$	2 1	—	3 1.5	—	$V/\mu s$
Settling Time	$t_s(+)$ and $t_s(-)$	$\pm V_{CC} = \pm 15V$ (0.1% error) $T_A = 25^{\circ}C$, $A_V = -1$ See Figure 3	—	4000	—	4000	ns
Noise (Referred to Input) Broadband	$N_I(BB)$	$\pm V_{CC} = \pm 20V$, $T_A = 25^{\circ}C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_I(PC)$	$\pm V_{CC} = \pm 20V$, $T_A = 25^{\circ}C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

- Bias currents are actually junction leakage currents which double (approximately) for each $10^{\circ}C$ increase in junction temperature T_J . Measurement of bias current is specified at T_J rather than T_A , since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms or 5 loop time constants after power is first applied to the device for test. Measurement at $T_A = -55^{\circ}C$ is not necessary since expected values are too small for typical test systems.
- Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:



- Negative I_B minimum limits reflect the characteristics of device with bias current compensation.
- CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and $-15V$.
- Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_J(max) \leq 175^{\circ}C$.
- Because of thermal feedback effects from output to input, open-loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

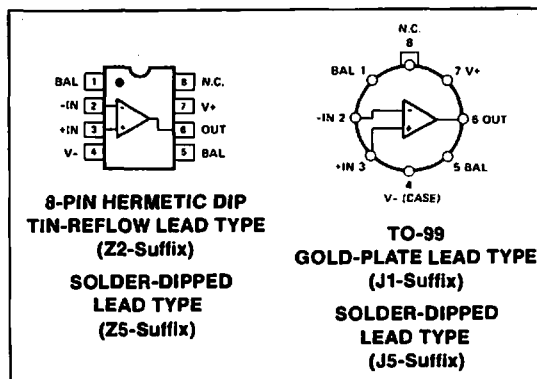
CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline A-1 (8 Lead Can), Package Type Designator "G"; and Appendix C, Case Outline D-4 (8 Lead Dual-in-Line) Package Type Designator "P".

POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{JA}	Maximum θ_{JC}	Maximum θ_{JA}
8 Lead Can (TO-99)	G	330mW at $T_A = 125^{\circ}C$	40^{\circ}C/W	150^{\circ}C/W	
8 Lead Hermetic DIP (Dual-in-Line)	P	417mW at $T_A = 125^{\circ}C$	50^{\circ}C/W	120^{\circ}C/W	

PIN CONNECTIONS





ELECTRICAL CHARACTERISTICS at V_{CC} from $\pm 5V$ to $\pm 20V$; source resistance = 50 ohm; ambient temperature range = $-55^{\circ}C$ to $+125^{\circ}C$ and figure 1, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	02 LIMITS		05 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5V, V_{CM} = 0V$ $T_A = 25^{\circ}C$	-5	5	-2	2	mV
		$\pm V_{CC} = \pm 20V$ $V_{CM} = \pm 15V, 0V$ $-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-7	7	-2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20V$ $V_{CM} = 0V$	-30	30	-10	10	$\mu V/^{\circ}C$
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20V, V_{CM} = 0V,$ $T_I = 25^{\circ}C$	-20	20	-20	20	pA
		$T_I = 125^{\circ}C$	-20	20	-20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$	$\pm V_{CC} = \pm 20V, V_{CM} = +15V$ $T_I = 25^{\circ}C$	-100	3500	-100	3500	pA
		$t \leq 25ms, T_I = 125^{\circ}C$	-10	60	-10	60	nA
	$-I_{IB}$	$\pm V_{CC} = \pm 15V, V_{CM} = +10V$ $T_I = 25^{\circ}C$	-100	300	-100	300	pA
		$t \leq 25ms, T_I = 125^{\circ}C$	-10	50	-10	50	nA
		$\pm V_{CC} = \pm 20V, -15V \leq V_{CM} \leq 0V$ $T_I = 25^{\circ}C$	-100	100	-100	100	pA
		$t \leq 25ms, T_I = 125^{\circ}C$	-10	50	-10	50	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 10V, -V_{CC} = -20V$	85	—	85	—	dB
	-PSRR	$+V_{CC} = 20V, -V_{CC} = -10V$	—	—	—	—	
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20V$ $V_{IN} = \pm 15V$	85	—	85	—	dB
Adjustment for Input Offset Voltage	$V_{IO} \text{ ADJ}(+)$	$\pm V_{CC} = \pm 20V$	+8	—	+8	—	mV
	$V_{IO} \text{ ADJ}(-)$	$\pm V_{CC} = \pm 20V$	—	-8	—	-8	
Output Short-Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15V$ $t \leq 25ms$ (Short Circuit to Ground)	-50	—	-50	—	mA
Output Short-Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15V$ $t \leq 25ms$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$T_A = -55^{\circ}C$	—	11	—	11	mA
		$\pm V_{CC} = \pm 15V, T_A = +25^{\circ}C$	—	7	—	7	
		$T_A = +125^{\circ}C$	—	7	—	7	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20V, R_L = 10k\Omega$	± 16	—	± 16	—	V
		$\pm V_{CC} = \pm 20V, R_L = 2k\Omega$	± 15	—	± 15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$ $A_{VS(-)}$	$\pm V_{CC} = \pm 20V, V_{OUT} = \pm 15V$ $R_L = 2k\Omega, T_A = 25^{\circ}C$	50	—	50	—	V/mV
		$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5V$ $R_L = 2k\Omega$ $V_{OUT} = \pm 2V$	10	—	10	—	V/mV
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V, R_L = 2k\Omega, A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	100	—	100	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V, R_L = 2k\Omega, A_V = 1$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	40	—	40	%
Slew Rate	$SR(+)$ and $SR(-)$	$V_{IN} = \pm 5V, \pm V_{CC} = \pm 15V$ $A_V = 1$, See Figure 2 $T_A = 25^{\circ}C$	7.5	—	10	—	V/ μs
		$T_A = -55^{\circ}C, +125^{\circ}C$	5	—	7	—	
Settling Time	$t_s(+)$ and $t_s(-)$	$\pm V_{CC} = \pm 15V$ (0.1% error) $T_A = 25^{\circ}C, A_V = -1$ See Figure 3	—	1500	—	1500	ns

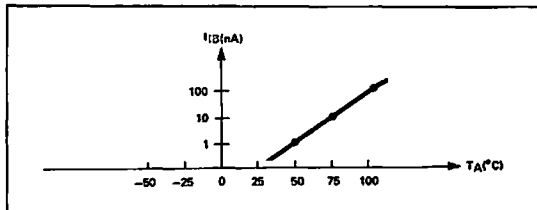
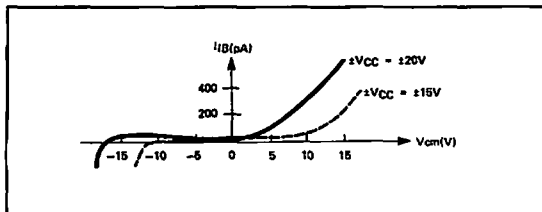


ELECTRICAL CHARACTERISTICS at V_{CC} from $\pm 5V$ to $\pm 20V$; source resistance = 50 ohm; ambient temperature range = $-55^{\circ}C$ to $+125^{\circ}C$ and figure 1, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	02 LIMITS		05 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Noise (Referred to Input) Broadband	$N_I(BB)$	$\pm V_{CC} = \pm 20V$, $T_A = 25^{\circ}C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_I(PC)$	$\pm V_{CC} = \pm 20V$, $T_A = 25^{\circ}C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

1. Bias currents are actually junction leakage currents which double (approximately) for each $10^{\circ}C$ increase in junction temperature T_J . Measurement of bias current is specified at T_J rather than T_A , since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms or 5 loop time constants after power is first applied to the device for test. Measurement at $T_A = -55^{\circ}C$ is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:



3. Negative I_{IB} minimum limits reflect the characteristics of device with bias current compensation.
4. CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and $-15V$.
5. Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_J(max) \leq 175^{\circ}C$.
6. Because of thermal feedback effects from output to input, open-loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

ORDERING INFORMATION

JAN SLASH SHEET	PMI DEVICE
JM38510/11401BGC	PM155J1/38510
JM38510/11401BGA	PM155J5/38510
JM38510/11401BPB	PM155Z2/38510
JM38510/11401BPA	PM155Z5/38510
JM38510/11404BGC	PM155AJ1/38510
JM38510/11404BGA	PM155AJ5/38510
JM38510/11404BPB	PM155AZ2/38510
JM38510/11404BPA	PM155AZ5/38510
JM38510/11402BGC	PM156J1/38510
JM38510/11402BGA	PM156J5/38510
JM38510/11402BPB	PM156Z2/38510
JM38510/11402BPA	PM156Z5/38510

JAN SLASH SHEET	PMI DEVICE
JM38510/11405BGC	PM156AJ1/38510
JM38510/11405BGA	PM156AJ5/38510
JM38510/11405BPB	PM156AZ2/38510
JM38510/11405BPA	PM156AZ5/38510
JM38510/11403BGC	PM157J1/38510
JM38510/11403BGA	PM157J5/38510
JM38510/11403BPB	PM157Z2/38510
JM38510/11403BPA	PM157Z5/38510
JM38510/11406BGC	PM157AJ1/38510
JM38510/11406BGA	PM157AJ5/38510
JM38510/11406BPB	PM157AZ2/38510
JM38510/11406BPA	PM157AZ5/38510

ELECTRICAL CHARACTERISTICS at V_{CC} from $\pm 5V$ to $\pm 20V$; source resistance = 50 ohm; ambient temperature range = $-55^{\circ}C$ to $+125^{\circ}C$ and figure 1, unless otherwise noted.

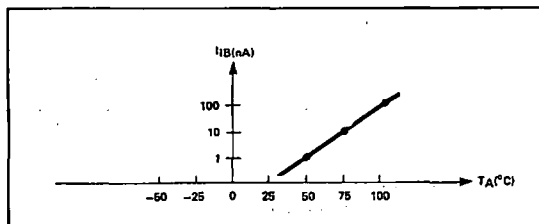
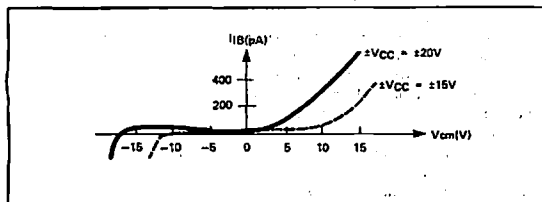
PARAMETER	SYMBOL	CONDITIONS	03 LIMITS		06 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	$\pm V_{CC} = \pm 5V, V_{CM} = 0V$ $T_A = 25^{\circ}C$	-5	5	-2	2	mV
		$\pm V_{CC} = \pm 20V$ $V_{CM} = \pm 15V, 0V$ $-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-7	7	-2.5	2.5	
Input Offset Voltage Temperature Sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$\pm V_{CC} = \pm 20V$ $V_{CM} = 0V$	-30	30	-10	10	$\mu V/^{\circ}C$
Input Offset Current	I_{IO}	$\pm V_{CC} = \pm 20V, V_{CM} = 0V$ $T_J = 25^{\circ}C$	-20	20	-20	20	pA
		$T_J = 125^{\circ}C$	-20	20	-20	20	nA
Input Bias Current (Note 1) (Note 2) (Note 3)	$+I_{IB}$	$\pm V_{CC} = \pm 20V, V_{CM} = +15V$ $T_J = 25^{\circ}C$	-100	3500	-100	3500	pA
		$t \leq 25ms$ $T_J = 125^{\circ}C$	-10	60	-10	60	nA
		$\pm V_{CC} = \pm 15V, V_{CM} = +10V$ $T_J = 25^{\circ}C$	-100	300	-100	300	pA
		$t \leq 25ms$ $T_J = 125^{\circ}C$	-10	50	-10	50	nA
	$-I_{IB}$	$\pm V_{CC} = \pm 20V, -15V \leq V_{CM} \leq 0V$ $T_J = 25^{\circ}C$	-100	100	-100	100	pA
		$t \leq 25ms$ $T_J = 125^{\circ}C$	-10	50	-10	50	nA
		$\pm V_{CC} = \pm 10V, -V_{CC} = -20V$ $+V_{CC} = 20V, -V_{CC} = -10V$	85	—	85	—	dB
Power Supply Rejection Ratio	+PSRR -PSRR						
Input Voltage Common-Mode Rejection (Note 4)	CMR	$\pm V_{CC} = \pm 20V$ $V_{IN} = \pm 15V$	85	—	85	—	dB
Adjustment for Input Offset Voltage	$V_{IO} ADJ (+)$	$\pm V_{CC} = \pm 20V$	+8	—	+8	—	mV
	$V_{IO} ADJ (-)$	$\pm V_{CC} = \pm 20V$	—	-8	—	-8	
Output Short-Circuit Current (for Positive Output) (Note 5)	$I_{OS(+)}$	$\pm V_{CC} = \pm 15V$ $t \leq 25ms$ (Short Circuit to Ground)	-50	—	-50	—	mA
Output Short-Circuit Current (for Negative Output) (Note 5)	$I_{OS(-)}$	$\pm V_{CC} = \pm 15V$ $t \leq 25ms$ (Short Circuit to Ground)	—	50	—	50	mA
Supply Current	I_{CC}	$T_A = -55^{\circ}C$	—	11	—	11	mA
		$\pm V_{CC} = \pm 15V, T_A = +25^{\circ}C$	—	7	—	7	
		$T_A = +125^{\circ}C$	—	7	—	7	
Output Voltage Swing (Maximum)	V_{OP}	$\pm V_{CC} = \pm 20V, R_L = 10k\Omega$	± 16	—	± 16	—	V
		$\pm V_{CC} = \pm 20V, R_L = 2k\Omega$	± 15	—	± 15	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	$A_{VS(+)}$	$\pm V_{CC} = \pm 20V, V_{OUT} = \pm 15V$ $R_L = 2k\Omega, T_A = 25^{\circ}C$	50	—	50	—	V/mV
	$A_{VS(-)}$	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	25	—	25	—	
Open-Loop Voltage Gain (Single Ended) (Note 6)	A_{VS}	$\pm V_{CC} = \pm 5V$ $R_L = 2k\Omega$ $V_{OUT} = \pm 2V$	10	—	10	—	V/mV

ELECTRICAL CHARACTERISTICS at V_{CC} from $\pm 5V$ to $\pm 20V$; source resistance = 50 ohm; ambient temperature range = $-55^\circ C$ to $+125^\circ C$ and figure 1, unless otherwise noted. (Continued)

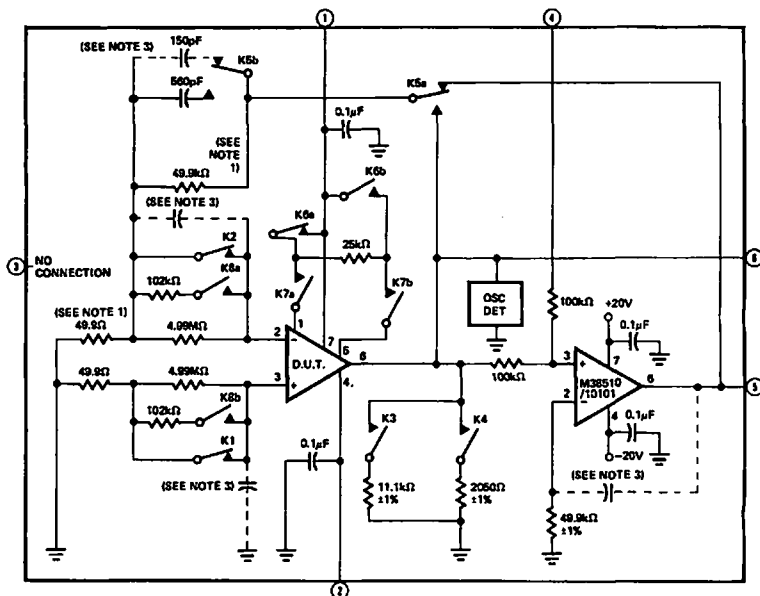
PARAMETER	SYMBOL	CONDITIONS	03 LIMITS		06 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Transient Response Rise Time	$TR_{(tr)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 5$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	450	—	450	ns
Transient Response Overshoot	$TR_{(os)}$	$\pm V_{CC} = \pm 15V$, $R_L = 2k\Omega$, $A_V = 5$ $C_L = 100pF$, See Figure 2 $V_{IN} = 50mV$	—	25	—	25	%
Slew Rate	$SR(+)$ and $SR(-)$	$V_{IN} = \pm 1V$, $\pm V_{CC} = \pm 15V$ $A_V = 5$, See Figure 2 $T_A = 25^\circ C$ $T_A = -55^\circ C$, $+125^\circ C$	30	—	40	—	$V/\mu s$
			20	—	25	—	
Settling Time	$ts(+)$ and $ts(-)$	$\pm V_{CC} = \pm 15V$ (0.1% error) $T_A = 25^\circ C$, $A_V = -5$ See Figure 3	—	800	—	800	ns
			—	800	—	800	
Noise (Referred to Input) Broadband	$N_i(BB)$	$\pm V_{CC} = \pm 20V$, $T_A = 25^\circ C$ Bandwidth = 5kHz	—	10	—	10	μV_{rms}
Noise (Referred to Input) Popcorn	$N_i(PC)$	$\pm V_{CC} = \pm 20V$, $T_A = 25^\circ C$ Bandwidth = 5kHz	—	80	—	80	μV_{pk}

NOTES:

1. Bias currents are actually junction leakage currents which double (approximately) for each $10^\circ C$ increase in junction temperature T_J . Measurement of bias current is specified at T_J rather than T_A , since normal warm-up thermal transients will affect the bias currents. The measurements for bias currents must be made within 25ms or 5 loop time constants after power is first applied to the device for test. Measurement at $T_A = -55^\circ C$ is not necessary since expected values are too small for typical test systems.
2. Bias current is sensitive to power supply voltage, common-mode voltage and temperature as shown by the following typical curves:

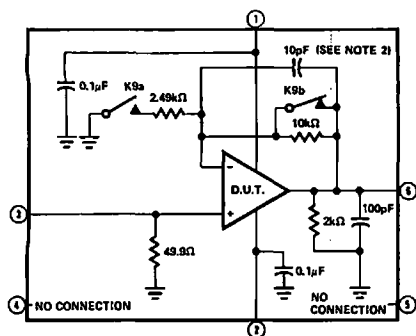


3. Negative I_B minimum limits reflect the characteristics of device with bias current compensation.
4. CMR is calculated from V_{IO} measurements at $V_{CM} = +15V$ and $-15V$.
5. Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that $T_J(max) \leq 175^\circ C$.
6. Because of thermal feedback effects from output to input, open-loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

**NOTES:**

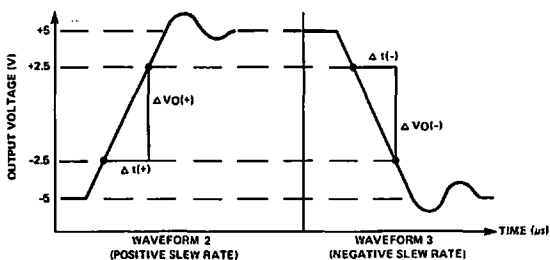
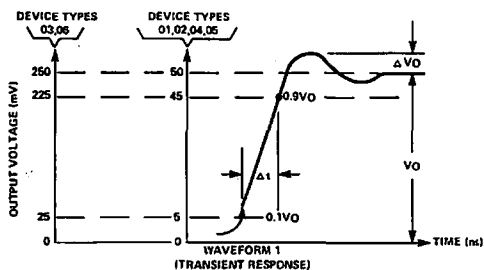
1. All resistors are $\pm 0.1\%$ tolerance and all capacitors are $\pm 10\%$ tolerance, unless otherwise specified.
2. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and change of state of relays (i.e. disable voltage supplies, current limit $\pm V_{CC}$, etc.).
3. Compensation capacitors should be added as required for test circuit stability. Two general methods for stability compensation exist. One method is with a capacitor for nulling amp feedback. The other method is with a capacitor in parallel with the 49.9kΩ closed-loop feedback resistor. Both methods should not be used simultaneously. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations, etc. Loop response and settling time shall be consistent with the test rate such that any value has settled for at least five loop time constants before the value is measured.
4. Adequate settling time should be allowed such that each parameter has settled to within 5% of its final value.
5. All relays are shown in the normal de-energized state.
6. The nulling amplifier shall be a M38510/10101XXX. Saturation of the nulling amplifier is not allowed on tests where the E (Pin 5) value is measured.
7. The load resistors 2050Ω and 11.1kΩ yield effective load resistances of 2kΩ and 10kΩ respectively.
8. Any oscillation greater than 300mV in amplitude (peak-to-peak) shall be cause for device failure.

Figure 1. Test Circuit for Static Tests



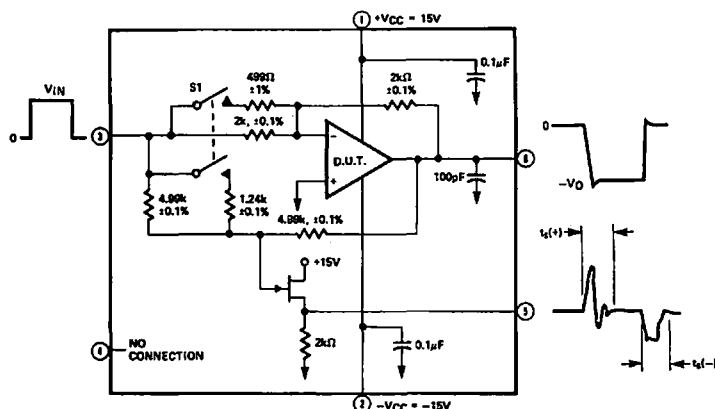
NOTES:

1. Resistors are $\pm 1.0\%$ tolerance and capacitors are $\pm 10\%$ tolerance.
2. This capacitance includes the actual measured value with stray and wire capacitance.
3. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.



PARAMETER SYMBOL	DEVICE TYPE	INPUT PULSE SIGNAL AT $t_r \leq 50\text{ns}$	OUTPUT PULSE SIGNAL	EQUATION
TR (t_r)	ALL	+50mV	WAVEFORM 1	TR (t_r) = Δt
TR (O_S)	ALL	+50mV	WAVEFORM 1	TR (O_S) = $100 (\Delta V_O / V_O) \%$
SR (+)	01, 02, 04, 05 03, 06	-5V to +5V STEP -1V to +1V STEP	WAVEFORM 2 WAVEFORM 2	SR (+) = $\Delta V_O(+)/\Delta t(+)$
SR (-)	01, 02, 04, 05 03, 06	+5V to -5V STEP +1V to -1V STEP	WAVEFORM 3 WAVEFORM 3	SR (-) = $\Delta V_O(-)/\Delta t(-)$

Figure 2. Test Circuit for Transient Response and Slew Rate.


NOTES:

1. Resistors are $\pm 1.0\%$ and capacitors are $\pm 10\%$, unless otherwise specified.
2. Precaution shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.
3. For device types 01, 02, 04 and 05, S1 is open, $A_V = -1$ and $V_{IN} = 10V$.
4. For device types 03 and 06, S1 is closed, $A_V = -5$ and $V_{IN} = 2V$.
5. Settling time, t_s measured on Pin 5, is the interval during which the summing node is not null within the specified accuracy referred to the output.

Figure 3. Test Circuit for Settling Time

BURN-IN

Devices supplied by PMI have been subjected to burn-in per Method 1015 of MIL-STD-883 using test condition C with circuit shown on Figure 4 or test condition F using circuit shown on Figure 5.

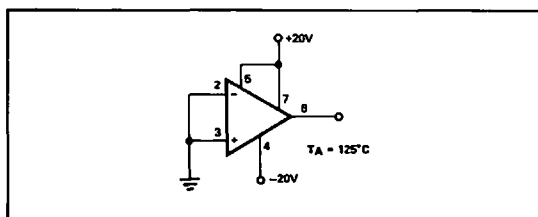


Figure 4. Test Circuit, Burn-In (Steady-State Power and Reverse Bias) and Operating Life Test

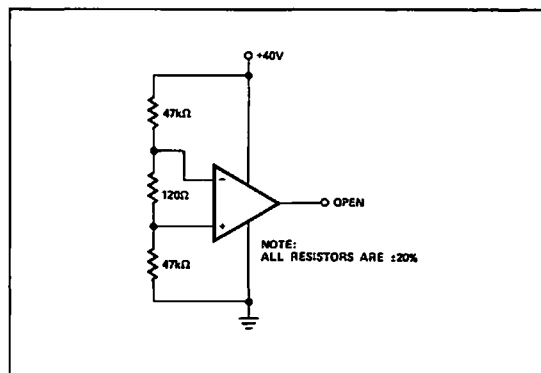


Figure 5. Accelerated Burn-In and Life Test Circuit

Precision Monolithics Inc.

FEATURES

- Low V_{OS} $25\mu V$
- Low V_{OS} Drift $0.6\mu V/^{\circ}C$
- Low Noise $0.6\mu V_{p-p}$
- Wide Supply Voltage Range $\pm 4.5V$ to $\pm 20V$

ORDERING INFORMATION

JAN SLASH SHEET	PMI DEVICE
JM38510/13501BGC	OP07AJ1/38510
JM38510/13501BGA	OP07AJ5/38510
JM38510/13501BPB	OP07AZ2/38510
JM38510/13501BPA	OP07AZ5/38510
JM38510/13502BGC	OP07J1/38510
JM38510/13502BGA	OP07J5/38510
JM38510/13502BPB	OP07Z2/38510
JM38510/13502BPA	OP07Z5/38510

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low offset voltage, internally-compensated operational amplifier as specified in MIL-M-38510/135 for device type 01 and 02. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/135 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

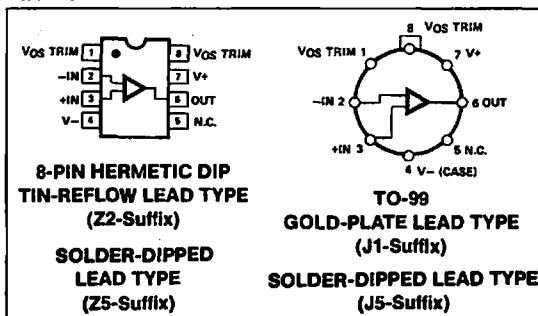
This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not

have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

MILITARY DEVICE TYPE	GENERIC-INDUSTRY TYPE
01	OP07A
02	OP07

For an 833-processed device with improved electrical specifications, review the OP-07 data sheet.

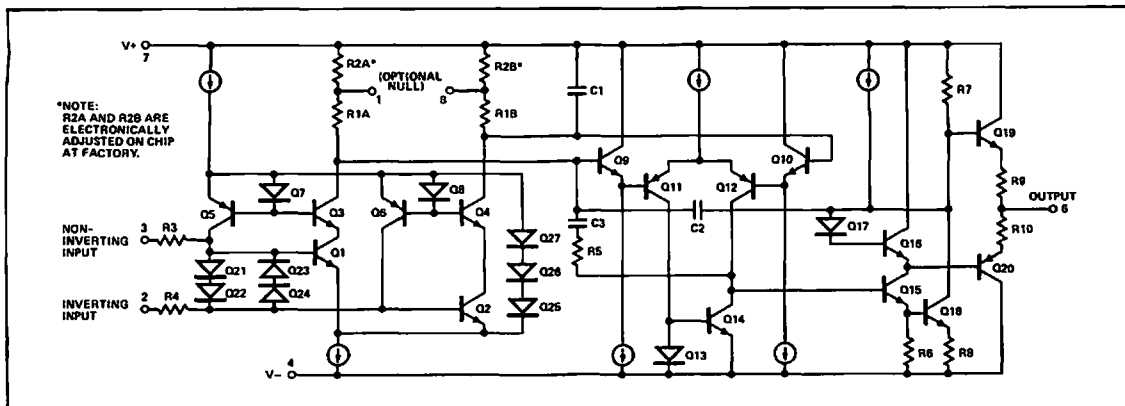
PIN CONNECTIONS



POWER AND THERMAL CHARACTERISTICS

Case Outline	Package	Maximum Allowable Power Dissipation	Maximum θ_{JC}	Maximum θ_{JA}
P	Dual-In-Line	208mW @ $T_A = 125^{\circ}C$	50^{\circ}C/W	120^{\circ}C/W
G	8-Lead CAN	167mW @ $T_A = 125^{\circ}C$	40^{\circ}C/W	150^{\circ}C/W

SIMPLIFIED SCHEMATIC





ELECTRICAL CHARACTERISTICS at $\pm 4.5V \leq V_{CC} \leq \pm 20V$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, $R_S = 50\Omega$ unnullled, unless otherwise noted.
(Continued)

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$, $T_A = 25^{\circ}C$, $V_{CC} = \pm 15V$	110	—	110	—	dB
		$V_{CM} = \pm 13V$, $V_{CC} = \pm 15V$	106	—	106	—	
Adjustment for Input Offset	$V_{IO} \text{ Adj (+)}$	$T_A = 25^{\circ}C$ (Note 1)	0.5	—	0.5	—	mV
	$V_{IO} \text{ Adj (-)}$	$T_A = 25^{\circ}C$ (Note 1)	—	-0.5	—	-0.5	
Output Short-Circuit Current	$I_{OS(+)}$	$t \leq 25ms$ (Notes 1, 3)	-65	—	-65	—	mA
	$I_{OS(-)}$	$t \leq 25ms$ (Notes 1, 3)	—	65	—	65	
Supply Current	I_{CC}	$T_A = 25^{\circ}C$ (Note 1)	—	4	—	4	mA
			—	5	—	5	
Output Voltage Swing (Minimum)	V_{OP}	$R_L = 1k\Omega$, (Note 1)	-10	10	-10	10	V
		$R_L = 2k\Omega$, (Note 1)	-12	12	-12	12	
Open Loop Voltage Gain (Single-Ended)	A_{VS}	$T_A = 25^{\circ}C$ (Notes 1, 2)	300	—	200	—	V/mV
			200	—	150	—	
Slew Rate	$SR(+)$, $SR(-)$	$V_{IN} = 10V$, $T_A = 25^{\circ}C$, (Note 1)	.08	—	.08	—	V/ μs
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	18	—	18	nV/ $\sqrt{Hz}$
		$f_O = 100Hz$, $T_A = 25^{\circ}C$ (Note 1)	—	14	—	14	
		$f_O = 1kHz$	—	12	—	12	
Low Frequency Input Noise Voltage	e_{np-p}	$f = 0.1Hz$ to $10Hz$, $T_A = 25^{\circ}C$, (Note 1)	—	0.6	—	0.6	μV_{p-p}

NOTES:

1. Tested at $V_{CM} = 0$, $V_{CC} = \pm 15V$.
2. $V_{OUT} = 0$ to $+10V$ for $A_{VS}(+)$ and $V_{OUT} = 0$ to $-10V$ for $A_{VS}(-)$. $R_L = 2.000\Omega$.
3. Continuous short-circuit limits are considerably less than the indicated test limits, since maximum power dissipation cannot be exceeded.

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (V_{CC})	$\pm 22V$
Input Voltage Range (V_{IN})	$\pm V_{CC}$
Differential Input Voltage Range	$\pm 30V$
Output Short-Circuit Duration (Note 1)	
Lead Temperature (Soldering, 60 sec)	$+300^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Junction Temperature (T_J)	$+150^{\circ}C$
Maximum Power Dissipation (P_D) (Note 2)	500mW

NOTES:

- Output may be shorted to ground indefinitely at $V_S = \pm 15V$, $T_A = 25^{\circ}C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.
- Maximum power dissipation versus ambient temperature.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	$\pm 4.5V$ to $\pm 20V$
Ambient Temperature Range	$-55^{\circ}C$ to $+125^{\circ}C$

ELECTRICAL CHARACTERISTICS at $\pm 4.5V \leq V_{CC} \leq \pm 20V$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, $R_S = 50\Omega$ unnull'd, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}	$T_A = 25^{\circ}C$ (Notes 1, 2)	-25 -60	25 60	-75 -200	75 200	μV
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}/\Delta T$	(Note 1)	-0.6	0.6	-1.3	1.3	$\mu V/^{\circ}C$
Input Bias Current	$+I_{IB}$	$T_A = 25^{\circ}C$ (Note 1)	-2 -4	2 4	-3 -6	3 6	nA
	$-I_{IB}$	$T_A = 25^{\circ}C$ (Note 1)	-2 -4	2 4	-3 -6	3 6	
	I_{IO}	$T_A = 25^{\circ}C$ (Note 1)	-2 -4	2 4	-2.8 -5.6	2.8 5.6	
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 20V$ to $5V$, $-V_{CC} = -15V$ $T_A = 25^{\circ}C$	—	10	—	10	$\mu V/V$
	-PSRR	$+V_{CC} = 15V$, $-V_{CC} = -20V$ to $-5V$ $T_A = 25^{\circ}C$	—	10	—	10	
	+PSRR	$+V_{CC} = 20V$ to $5V$, $-V_{CC} = -15V$	—	20	—	20	
	-PSRR	$+V_{CC} = 15V$, $-V_{CC} = -20V$ to $-5V$	—	20	—	20	
	PSRR	$V_{CC} = \pm 4.5V$ to $\pm 20V$ $T_A = 25^{\circ}C$	—	10	—	10	
		$V_{CC} = \pm 4.5V$ to $\pm 20V$	—	20	—	20	

NOTES:

- Tested at $V_{CM} = 0$, $V_{CC} = \pm 15V$.
- Due to the inherent warm-up drift, testing shall occur no sooner than three (3) minutes after application of power.



JM38510/13503

LOW-NOISE PRECISION
OPERATIONAL AMPLIFIER

Precision Monolithics Inc.

FEATURES

- Low V_{OS} $25\mu V$
- Low V_{OS} Drift $0.6\mu V/^{\circ}C$
- High Speed $1.7V/\mu s$
- Low Noise $0.18\mu V_{p-p}$
- High Gain 1.0 Million
- Wide Supply Voltage Range $\pm 4.5V$ to $\pm 18V$

ORDERING INFORMATION

JAN SLASH SHEET	PMI DEVICE
JM38510/13503BGC	OP27AJ1/38510
JM38510/13503BGA	OP27AJ5/38510
JM38510/13503BPB	OP27AZ2/38510
JM38510/13503BPA	OP27AZ5/38510

GENERAL DESCRIPTION

This data sheet covers the electrical requirements for a monolithic, low offset voltage, internally-compensated operational amplifier as specified in MIL-M-38510/135 for device type 03. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in QPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/135 for Class B processed devices.

GENERIC CROSS-REFERENCE INFORMATION

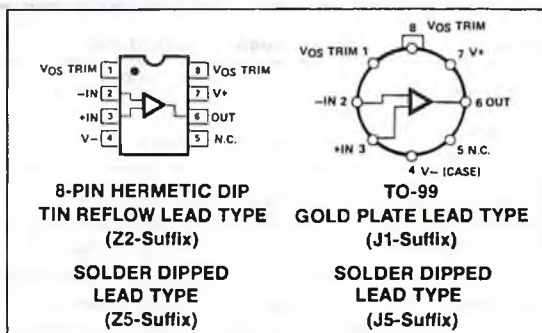
This cross-reference information is presented for the convenience of the user. The generic-industry types listed may not have identical operational performance characteristics across

the military temperature range or reliability factors equivalent to the MIL-M-38510 device.

MILITARY DEVICE TYPE	GENERIC-INDUSTRY TYPE
03	OP27A

For an 833-processed device with improved electrical specifications, review the OP-27 data sheet.

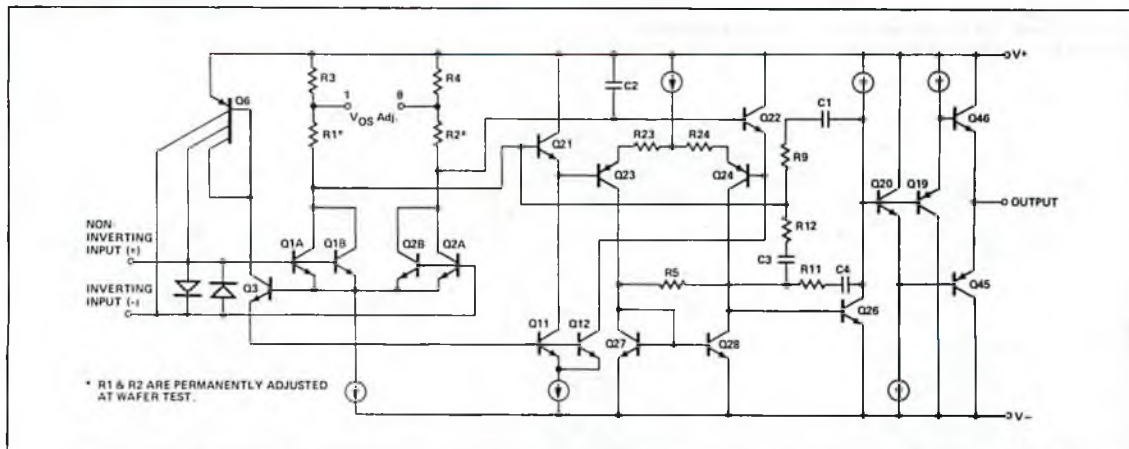
PIN CONNECTIONS



POWER AND THERMAL CHARACTERISTICS

Case Outline	Package	Maximum Allowable Power Dissipation	Maximum θ_{JC}	Maximum θ_{JA}
P	Dual-In-Line	208mW @ $T_A = 125^{\circ}C$	50 $^{\circ}C/W$	120 $^{\circ}C/W$
G	8-Lead CAN	167mW @ $T_A = 125^{\circ}C$	40 $^{\circ}C/W$	150 $^{\circ}C/W$

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (V_{CC})	$\pm 22V$
Input Voltage Range (V_{IN})	$\pm V_{CC}$
Differential Input Voltage Range	$\pm 0.7V$
Output Short-Circuit Duration (Note 1)	
Lead Temperature (Soldering, 60 sec)	$+300^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Junction Temperature (T_J)	$+150^{\circ}C$
Maximum Power Dissipation (P_D) (Note 2)	500mW

NOTES:

- Output may be shorted to ground indefinitely at $V_S = \pm 15V$, $T_A = 25^{\circ}C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.
- Maximum power dissipation versus ambient temperature.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	$\pm 4.5V$ to $\pm 18V$
Ambient Temperature Range	$-55^{\circ}C$ to $+125^{\circ}C$

ELECTRICAL CHARACTERISTICS at $\pm 4.5V \leq V_{CC} \leq \pm 20V$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, $R_S = 50\Omega$ unnullified, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	03 LIMITS		UNITS
			MIN	MAX	
Input Offset Voltage	V_{IO}	$T_A = 25^{\circ}C$ (Notes 1, 2)	-25 -60	25 60	μV
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}/\Delta T$	(Note 1)	-0.6	0.6	$\mu V/^{\circ}C$
Input Bias Current	$+I_{IB}$	$T_A = 25^{\circ}C$ (Note 1)	-40 -60	40 60	nA
	$-I_{IB}$	$T_A = 25^{\circ}C$ (Note 1)	-40 -60	40 60	
Input Offset Current	I_{IO}	$T_A = 25^{\circ}C$ (Note 1)	-35 -50	35 50	nA
Power Supply Rejection Ratio	+PSRR	$+V_{CC} = 18V$ to $5V$, $-V_{CC} = -15V$ $T_A = 25^{\circ}C$	—	10	$\mu V/V$
	-PSRR	$+V_{CC} = 15V$, $-V_{CC} = -18V$ to $-5V$ $T_A = 25^{\circ}C$	—	10	
	+PSRR	$+V_{CC} = 18V$ to $5V$, $-V_{CC} = -15V$	—	16	
	-PSRR	$+V_{CC} = 15V$, $-V_{CC} = -18V$ to $-5V$	—	16	
	PSRR	$V_{CC} = \pm 4.5V$ to $\pm 18V$ $T_A = 25^{\circ}C$	—	10	
		$V_{CC} = \pm 4.5V$ to $\pm 18V$	—	16	

NOTES:

- Tested at $V_{CM} = 0$, $V_{CC} = \pm 15V$.
- Due to the inherent warm-up drift, testing shall occur no sooner than three (3) minutes after application of power.

5

OPERATIONAL AMPLIFIERS



ELECTRICAL CHARACTERISTICS at $\pm 4.5V \leq V_{CC} \leq \pm 20V$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, $R_S = 50\Omega$ unnullled, unless otherwise noted.
(Continued)

PARAMETER	SYMBOL	CONDITIONS	03 LIMITS		UNITS
			MIN	MAX	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 11V$, $T_A = 25^{\circ}C$, $V_{CC} = \pm 15V$	114	—	dB
		$V_{CM} = \pm 11V$, $V_{CC} = \pm 15V$	108	—	
Adjustment for Input Offset	$V_{IO} \text{ Adj (+)}$	$T_A = 25^{\circ}C$, (Note 1)	0.5	—	mV
	$V_{IO} \text{ Adj (-)}$	$T_A = 25^{\circ}C$, (Note 1)	—	-0.5	
Output Short-Circuit Current	$I_{OS(+)}$	$t \leq 25ms$, (Notes 1, 3)	-60	—	mA
	$I_{OS(-)}$	$t \leq 25ms$, (Notes 1, 3)	—	70	
Supply Current	I_{CC}	$T_A = 25^{\circ}C$ (Note 1)	—	4	mA
			—	5	
Output Voltage Swing (Minimum)	V_{OP}	$R_L = 600\Omega$, (Note 1)	-10	10	V
		$R_L = 2k\Omega$, (Note 1)	-11.5	11.5	
Open Loop Voltage Gain (Single-Ended)	A_{VS}	$T_A = 25^{\circ}C$ (Note 2)	1000	—	V/mV
			600	—	
Slew Rate	$SR(+)$, $SR(-)$	$V_{IN} = 10V$, $T_A = 25^{\circ}C$, (Note 1)	1.7	—	V/ μs
Input Noise Voltage Density	e_n	$f_O = 10Hz$	—	5.5	nV/ $\sqrt{Hz}$
		$f_O = 100Hz$	—	4.0	
		$f_O = 1kHz$	—	3.8	
Low Frequency Input Noise Voltage	e_{np-p}	$f = 0.1Hz$ to $10Hz$	—	0.18	μV_{p-p}
		$T_A = 25^{\circ}C$, (Note 1)	—	0.18	
Input Noise Current Density	i_n	$f_O = 10Hz$	—	4.0	pA/ $\sqrt{Hz}$
		$f_O = 100Hz$	—	1.5	
		$f_O = 1kHz$	—	0.8	

NOTES:

1. Tested at $V_{CM} = 0$, $V_{CC} = \pm 15V$.
2. $V_{OUT} = 0$ to $+10V$ for $A_{VS}(+)$ and $V_{OUT} = 0$ to $-10V$ for $A_{VS}(-)$. $R_L = 2,000\Omega$.
3. Continuous short-circuit limits are considerably less than the indicated test limits, since maximum power dissipation cannot be exceeded.

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INSTRUMENTATION AMPLIFIERS

Precision Monolithics Inc.

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AMP-01

Low-Noise Precision
Instrumentation Amplifier6-5

***AMP-02**

High-Accuracy, 8-Pin
Instrumentation Amplifier6-27

***AMP-05**

Fast-Settling JFET
Instrumentation Amplifier6-29

*Indicates new product or product whose data sheet has been finalized since the 1986 data book.



Precision Monolithics Inc.

INSTRUMENTATION AMPLIFIERS

INTRODUCTION

An instrumentation amplifier is a committed gain block that amplifies a differential input voltage by a precisely set gain. Voltages common to both inputs are rejected. Differential gain is set by one or two external resistors, usually over a range of 1 to 1000. Instrumentation amplifiers are designed to have very high input impedance; this assures that the gain will not be affected by signal-source impedances (R_S). Input bias current must be low to minimize input offset voltages due to $I_B \times R_S$. In the output stage, low output impedance keeps the output voltage from being affected by the load impedance. Instrumentation amplifiers employ heavy negative feedback which provides excellent gain linearity even at high gains.

The essential characteristics of instrumentation amplifiers—high input impedance, low output impedance, low offset, high linearity, stable gain, and ability to reject common-mode inputs—make them very useful for amplifying low-level transducer outputs. Transducers such as thermocouples, strain-gage bridges, biological probes, and current shunts produce small differential signals superimposed on common-mode bias voltages. In addition, common-mode ground noise is usually prevalent. Instrumentation amplifiers are gain blocks that have been optimized for preamplifying low-level transducer signals in the presence of common-mode noise.

The PMI AMP-01 instrumentation amplifier has all the features needed for use in high-accuracy data-acquisition systems, and high-performance instruments, including a wide gain range, low noise voltages, and 16-bit linearity.

Unlike conventional instrumentation amplifiers, the AMP-01 has high output drive capability; it can supply $\pm 10V$ at $\pm 50mA$. This enhanced output drive capability enables the AMP-01 to drive unusually large capacitive loads without encountering stability problems.

Output sense and reference points are provided. The AMP-01 is unusually versatile, and can be connected as a precision current source or high-performance op amp as well as a conventional instrumentation amplifier.

The AMP-02 has many similarities to the AMP-01 in terms of precision and accuracy, but is packaged in an 8-pin mini-dip. The small package provides significant saving in board space and complexity. Gain is set with a single external resistor. With its laser-trimmed input offset voltage of less than $50\mu V$, external offset nulling is generally not required, however a reference pin does provide a means of zeroing or offsetting the output as required. The AMP-02 has a laser-trimmed gain equation accuracy of 0.1%, and a gain tempco below $50ppm/^{\circ}C$.

The AMP-05 JFET instrumentation amplifier supports high-speed applications, such as analog-multiplexed data acquisition and fast analog signal processing. The design offers a $15\mu s$ maximum settling-time to 12 bits at gains up to 1000, with 14-bit linearity. The AMP-05 also provides on-board circuits for guard driving, which maximizes input signal speed, and a precision current source for transducer or reference excitation.

DEFINITIONS

Voltage Offsets — Offset at the output of an instrumentation amplifier consists of two terms, a gain-dependent input-offset-voltage and a gain-independent output-offset-voltage. Total offset is the sum of the unity-gain-output-offset (V_{OOS}) plus input-offset (V_{IOS}) multiplied by the gain ($\text{Output Offset} = V_{OOS} + GV_{IOS}$). At high gain, the input offset term dominates. For the AMP-01 and AMP-05, both input and output offsets can be trimmed externally if desired.

Power Supply Rejection — Offset changes with variations in the power supply voltages. The ability of the instrumentation amplifier to reject fluctuation in power supply voltage is referred to as "power supply rejection". It varies with gain and is different for the positive and negative supplies. The offset change referred-to-input (RTI) is usually specified in dB form. For example, a PSR of 100dB at a gain of 1000 would imply an input-offset-voltage change of $10\mu V$ -per-volt of power supply change. The output offset change-per-volt of power-supply change would be 10mV. PSR in the specification tables is measured at DC.

Input Bias Current — The input bias currents are currents flowing into (or out of) the two inputs of the amplifier. The value given in the specification table is the maximum current into either input. Input offset current is the difference between the two input bias currents.

Input Voltage Range — The linear operating range of the amplifier is referred to as the "input voltage range". When operating at high gains with small differential inputs, this input range is the common-mode input voltage range.

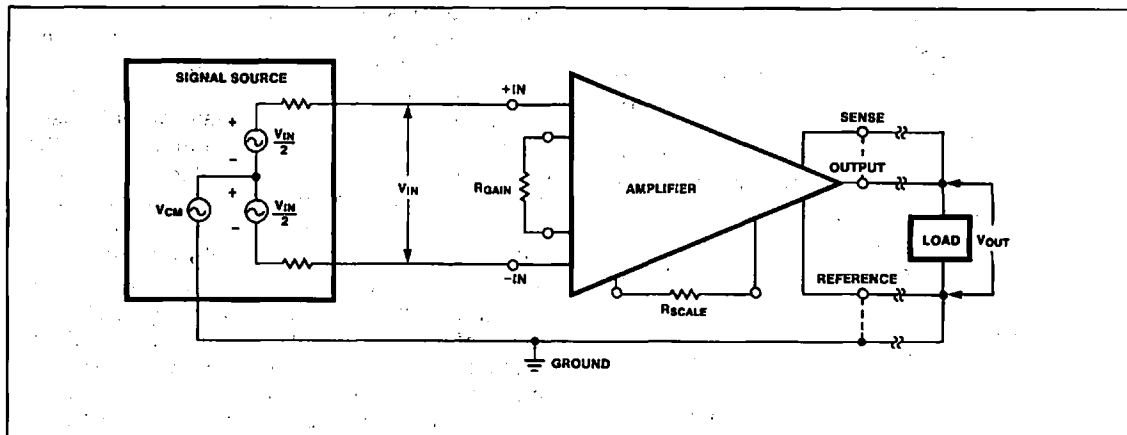
Common-Mode Rejection — Common-mode rejection (CMR) specifies the amplifiers ability to reject common-mode inputs. The ratio of change in output voltage to a change in common-mode input voltage is the common-mode gain ($\Delta V_O / \Delta V_{CM}$). The ratio of differential gain (G) to common-mode gain (A_{CM}) is defined as common-mode rejection ratio (CMRR). The CMR is conventionally specified in log form; $CMR = 20 \log_{10} CMRR$.

Since instrumentation amplifiers are designed to amplify differential signals while rejecting common-mode inputs, common-mode gain stays essentially independent of gain setting. Therefore, CMR increases almost directly with the gain setting.

As an example, consider a CMR of 120dB at a gain of 1000 with a common-mode input range of $\pm 10V$. The 120dB of CMR implies a CMRR of $1000/A_{CM} = 1,000,000$, or a common-mode gain of $1/1000$. A $\pm 10V$ common-mode input will cause an output change of $\pm 10mV$ for this example ($CMR = 120dB$, $G = 1000$).

Gain Equation Accuracy — Differential gain is given as a function of one or two external resistors. The specified accuracy limits indicate the accuracy of the amplifier given an exact ratio of gain setting resistors R_S and R_G , when two resistors are used, or an exact value of R_G when only one resistor is used.

INSTRUMENTATION AMPLIFIER FUNCTIONAL DIAGRAM



Precision Monolithics Inc.

FEATURES

- **Low Offset Voltage** 50 μ V Max
- **Very Low Offset Voltage Drift** 0.3 μ V/ $^{\circ}$ C Max
- **Low Noise** 0.12 μ V_{p-p} (0.1Hz to 10Hz)
- **Excellent Output Drive** $\pm$ 10V at $\pm$ 50mA
- **Capacitive Load Stability** to 1 μ F
- **Gain Range** 0.1 to 10,000
- **Excellent Linearity** 16-Bit at G = 1000
- **High CMR** 125dB Min (G = 1000)
- **Low Bias Current** 4nA Max
- **May be Configured as a Precision Op-Amp**
- **Output-Stage Thermal Shutdown**

ORDERING INFORMATION†

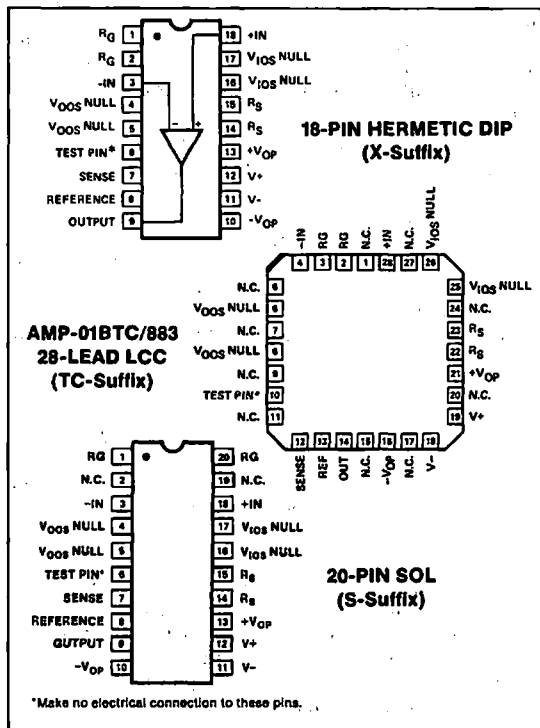
PACKAGE			OPERATING TEMPERATURE RANGE
CERDIP 18-PIN	LCC	PLASTIC 20-PIN	
AMP01AX*	—	—	MIL
AMP01BX*	AMP01BTC/883	—	MIL
AMP01EX	—	—	IND
AMP01FX	—	—	IND
—	—	AMP01GS††	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

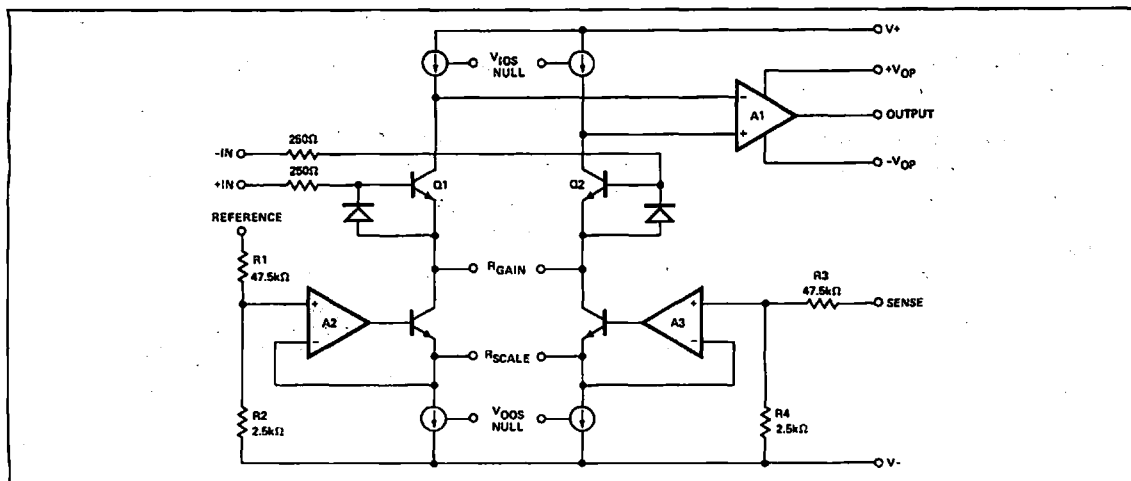
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



Manufactured under the following U.S. patents: 4,471,321 and 4,503,381.



GENERAL DESCRIPTION

The AMP-01 is a monolithic instrumentation amplifier designed for high-precision data acquisition and instrumentation applications. The design combines the conventional features of an instrumentation amplifier with a high-current output stage. The output remains stable with high capacitance loads (1 μ F), a unique ability for an instrumentation amplifier. Consequently, the AMP-01 can amplify low-level signals for transmission through long cables without requiring an output buffer. The output stage may be configured as a voltage or current generator.

Input offset voltage is very low (20 μ V) which generally eliminates the external null potentiometer. Temperature changes have minimal effect on offset; TCV_{IO} is typically 0.15 μ V/ $^{\circ}$ C. Excellent low-frequency noise performance is achieved with a minimal compromise on input protection. Bias current is very low, less than 10 nA over the military temperature range. High common-mode rejection of 130 dB, 16-bit linearity at a gain of 1000, and 50 mA peak output current are achievable simultaneously. This combination takes the instrumentation amplifier one step further towards the ideal amplifier.

AC performance complements the superb DC specifications. The AMP-01 slews at 4.5V/ μ s into capacitive loads of up to 15 nF, settles in 50 μ s to 0.01% at a gain of 1000, and boasts a healthy 26 MHz gain-bandwidth product. These features make the AMP-01 ideal for high-speed data-acquisition systems.

Gain is set by the ratio of two external resistors over a range of 0.1 to 10,000. A very low gain-temperature-coefficient of 10 ppm/ $^{\circ}$ C is achievable over the whole gain range. Output voltage swing is guaranteed with three load resistances; 50 Ω , 500 Ω , and 2 k Ω . Loaded with 500 Ω , the output delivers $\pm$ 13.0V minimum. A thermal shutdown circuit prevents destruction of the output transistors during overload conditions.

The AMP-01 can also be configured as a high-performance operational amplifier. In many applications, the AMP-01 can be used in place of op-amp/power-buffer combinations.

THEORY OF OPERATION

An instrumentation amplifier, unlike an op amp, requires precise internal feedback. The two techniques presently in use are resistive and current feedback.

The AMP-01 employs the current feedback approach which has significant advantages over resistive feedback. Advantages of current-feedback are:

- The technique yields a very high common-mode rejection ratio. The AMP-01 CMR is in excess of 130 dB at a gain of 1000.
- The gain of the current feedback design is set by the ratio of two external resistors. Using external resistors allows any practical gain to be set with high precision and very low gain temperature coefficient.
- The current-feedback design is immune to CMR degradation when series resistance is added to the reference input. A small (trimmable) offset change results from added resistance, e.g. a printed circuit track.

The AMP-01 utilizes low-drift thin-film resistors to minimize output offset temperature drift. A feedback voltage-to-current converter is employed having high linearity and low noise, particularly at low frequencies. Parameter shifts during packaging are eliminated by a post-assembly trimming technique which electronically adjusts the output offset voltage.

The AMP-01 input transistors Q1 and Q2 feed active loads, yielding stage gain in excess of 4000 (see simplified schematic). The output amplifier, A1, is a two-stage design having a gain of about 50,000 driving a 100 Ω load. Overall gain of 2×10^8 yields excellent linearity, even at high closed-loop gains.

Low bias current is achieved by using ion-implanted super-beta transistors combined with a new bias-current cancellation system, patents applied for. Input bias current remains below 10 nA over the military temperature range, -55° C to $+125^{\circ}$ C.

Superbeta transistors use a new transistor geometry resulting in an input noise of only 5 nV/ $\sqrt{\text{Hz}}$ at $G = 1000$. Noise includes contributions from the gain-setting resistor and internal overload-protection resistor. The input stage achieves an offset voltage drift of less than 0.3 μ V/ $^{\circ}$ C (E Grade).

The AMP-01 uses a unique two-pole compensation scheme where the load capacitance is incorporated into the dominate pole. Stable operation results even with high capacitance loads. The high output current capability (90 mA peak) allows the 4.5V/ μ s slew-rate to be maintained with load capacitance as high as 15 nF.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	± 18 V
Internal Power Dissipation (Note 1)	500mW
Common-Mode Input Voltage	Supply Voltage
Differential Input Voltage, $R_G \geq 2k\Omega$	± 20 V
$R_G < 2k\Omega$	± 10 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65° C to $+150^{\circ}$ C
Operating Temperature Range	
AMP-01A, B	-55° C to $+125^{\circ}$ C
AMP-01E, F	-25° C to $+85^{\circ}$ C
AMP-01G	0° C to $+70^{\circ}$ C
Lead Temperature (Soldering, 60 sec)	300° C
DICE Junction Temperature (T_J)	-65° C to $+150^{\circ}$ C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
	100 $^{\circ}$ C	10mW/ $^{\circ}$ C

NOTES:

- See table for maximum ambient temperature rating and derating factor.
- Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A			AMP-01B			UNITS		
			MIN	TYP	MAX	MIN	TYP	MAX			
OFFSET VOLTAGE											
Input Offset Voltage	V_{IOS}	$T_A = 25^{\circ}\text{C}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	20	50	—	40	100	μV		
Input Offset Voltage Drift	TCV_{IOS}	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	0.15	0.3	—	0.3	1.0	$\mu\text{V}/^{\circ}\text{C}$		
Output Offset Voltage	V_{OOS}	$T_A = 25^{\circ}\text{C}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	1	3	—	2	6	mV		
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	20	50	—	50	120	$\mu\text{V}/^{\circ}\text{C}$		
Offset Referred to Input vs. Positive Supply $V+ = +5\text{V}$ to $+15\text{V}$	PSR	$G = 1000$	120	130	—	110	120	—	dB		
		$G = 100$	110	130	—	100	120	—			
		$G = 10$	95	110	—	90	100	—			
		$G = 1$	75	90	—	70	80	—			
		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	$G = 1000$	120	130	—	110	120	—	dB	
		$G = 100$	110	130	—	100	120	—			
		$G = 10$	95	110	—	90	100	—			
		$G = 1$	75	90	—	70	80	—			
		Offset Referred to Input vs. Negative Supply $V- = -5\text{V}$ to -15V	PSR	$G = 1000$	105	125	—	105	115	—	dB
				$G = 100$	90	105	—	90	95	—	
$G = 10$	70			85	—	70	75	—			
$G = 1$	50			65	—	50	60	—			
$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	$G = 1000$			105	125	—	105	115	—	dB	
$G = 100$	90			105	—	90	95	—			
$G = 10$	70			85	—	70	75	—			
$G = 1$	50			65	—	50	60	—			
Input Offset Voltage Trim Range				$V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$ (Note 1)	—	± 6	—	—	± 6	—	mV
Output Offset Voltage Trim Range				$V_S = \pm 4.5\text{V}$ to $\pm 18\text{V}$ (Note 1)	—	± 100	—	—	± 100	—	mV
INPUT CURRENT											
Input Bias Current	I_B	$T_A = 25^{\circ}\text{C}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	1	4	—	2	6	nA		
Input Bias Current Drift	TCI_B	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	40	—	—	50	—	$\text{pA}/^{\circ}\text{C}$		
Input Offset Current	I_{OS}	$T_A = 25^{\circ}\text{C}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	0.2	1.0	—	0.5	2.0	nA		
Input Offset Current Drift	TCI_{OS}	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	3	—	—	5	—	$\text{pA}/^{\circ}\text{C}$		
INPUT											
Input Resistance	R_{IN}	Differential, $G = 1000$	—	1	—	—	1	—	$\text{G}\Omega$		
		Differential, $G \leq 100$	—	10	—	—	10	—			
		Common-Mode, $G = 1000$	—	20	—	—	20	—			
Input Voltage Range	IVR	$T_A = 25^{\circ}\text{C}$ (Note 2) $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	± 10.5 ± 10.0	—	—	± 10.5 ± 10.0	—	—	V		
Common-Mode Rejection	CMR	$V_{CM} = \pm 10\text{V}$, 1k Ω source imbalance	125	130	—	115	125	—	dB		
		$G = 1000$	120	130	—	110	125	—			
		$G = 100$	100	120	—	95	110	—			
		$G = 10$	85	100	—	75	90	—			
		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	$G = 1000$	120	125	—	110	120	—	dB	
		$G = 100$	115	125	—	105	120	—			
		$G = 10$	95	115	—	90	105	—			
		$G = 1$	80	95	—	75	90	—			

- NOTES:**
- V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS} , respectively.
 - Refer to section on common-mode rejection.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01E			AMP-01F/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE									
Input Offset Voltage	V _{IOS}	T _A = 25°C -25°C ≤ T _A ≤ +85°C	—	20 40	50 80	—	40 60	100 150	μV
Input Offset Voltage Drift	TCV _{IOS}	-25°C ≤ T _A ≤ +85°C, (Note 2)	—	0.15	0.3	—	0.3	1.0	μV/°C
Output Offset Voltage	V _{OOS}	T _A = 25°C -25°C ≤ T _A ≤ +85°C	—	1 3	3 6	—	2 6	6 10	mV
Output Offset Voltage Drift	TCV _{OOS}	R _G = ∞, (Note 2) -25°C ≤ T _A ≤ +85°C	—	20	100	—	50	120	μV/°C
Offset Referred to Input vs. Positive Supply V+ = +5V to +15V	PSR	G = 1000	120	130	—	110	120	—	dB
		G = 100	110	130	—	100	120	—	
		G = 10	95	110	—	90	100	—	
		G = 1	75	90	—	70	80	—	
		-25°C ≤ T _A ≤ +85°C							dB
		G = 1000	120	130	—	110	120	—	
		G = 100	110	130	—	100	120	—	
		G = 10	95	110	—	90	100	—	
		G = 1	75	90	—	70	80	—	
Offset Referred to Input vs. Negative Supply V- = -5V to -15V	PSR	G = 1000	110	125	—	105	115	—	dB
		G = 100	95	105	—	90	95	—	
		G = 10	75	85	—	70	75	—	
		G = 1	55	65	—	50	60	—	
		-25°C ≤ T _A ≤ +85°C							dB
		G = 1000	110	125	—	105	115	—	
		G = 100	95	105	—	90	95	—	
		G = 10	75	85	—	70	75	—	
		G = 1	55	65	—	50	60	—	
Input Offset Voltage Trim Range		V _S = ±4.5V to ±18V (Note 1)	—	±6	—	—	±6	—	mV
Output Offset Voltage Trim Range		V _S = ±4.5V to ±18V (Note 1)	—	±100	—	—	±100	—	mV
INPUT CURRENT									
Input Bias Current	I _B	T _A = 25°C -25°C ≤ T _A ≤ +85°C	—	1 4	4 10	—	2 6	6 15	nA
Input Bias Current Drift	TCI _B	-25°C ≤ T _A ≤ +85°C	—	40	—	—	50	—	pA/°C
Input Offset Current	I _{OS}	T _A = 25°C -25°C ≤ T _A ≤ +85°C	—	0.2 0.5	1.0 3.0	—	0.5 1.0	2.0 6.0	nA
Input Offset Current Drift	TCI _{OS}	-25°C ≤ T _A ≤ +85°C	—	3	—	—	5	—	pA/°C
INPUT									
Input Resistance	R _{IN}	Differential, G = 1000	—	1	—	—	1	—	GΩ
		Differential, G ≤ 100	—	10	—	—	10	—	
		Common-Mode, G = 1000	—	20	—	—	20	—	
Input Voltage Range	IVR	T _A = 25°C (Note 3)	±10.5	—	—	±10.5	—	—	V
		-25°C ≤ T _A ≤ +85°C	±10.0	—	—	±10.0	—	—	
Common-Mode Rejection	CMR	V _{CM} = ±10V, 1kΩ source imbalance							dB
		G = 1000	125	130	—	115	125	—	
		G = 100	120	130	—	110	125	—	
		G = 10	100	120	—	95	110	—	
		G = 1	85	100	—	75	90	—	
		-25°C ≤ T _A ≤ +85°C							dB
		G = 1000	120	125	—	110	120	—	
		G = 100	115	125	—	105	120	—	
		G = 10	95	115	—	90	105	—	
		G = 1	80	95	—	75	90	—	

NOTES:

- V_{IOS} and V_{OOS} nulling has minimal affect on TCV_{IOS} and TCV_{OOS} , respectively.
- Sample tested.
- Refer to section on common-mode rejection.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A/E			AMP-01B/F/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
GAIN									
Gain Equation		$G = \frac{20 \times R_S}{R_G}$							
Accuracy		Accuracy Measured from G = 1 to 1000	—	0.3	0.6	—	0.5	0.8	%
Gain Range	G		0.1	—	10k	0.1	—	10k	V/V
Nonlinearity		G = 1000	—	0.0007	0.005	—	0.0007	0.005	%
		G = 100	—	—	0.005	—	—	0.005	
		G = 10 (Note 1)	—	—	0.005	—	—	0.007	
		G = 1	—	—	0.010	—	—	0.015	
Temperature Coefficient	G _{TC}	1 ≤ G ≤ 1000 (Notes 1, 2)	—	5	10	—	5	15	ppm/°C
OUTPUT RATING									
Output Voltage Swing	V _{OUT}	R _L = 2kΩ	±13.0	±13.8	—	±13.0	±13.8	—	V
		R _L = 500Ω	±13.0	±13.5	—	±13.0	±13.5	—	
		R _L = 50Ω	±2.5	±4.0	—	±2.5	±4.0	—	V
		R _L = 2kΩ Over Temp. R _L = 500Ω (Note 3)	±12.0 ±12.0	±13.8 ±13.5	—	±12.0 ±12.0	±13.8 ±13.5	—	
Positive Current Limit		Output-to-Ground Short	60	100	120	60	100	120	mA
Negative Current Limit		Output-to-Ground Short	60	90	120	60	90	120	mA
Capacitive Load Stability		1 ≤ G ≤ 1000 No Oscillations, (Note 1)	0.1	1	—	0.1	1	—	μF
Thermal Shutdown Temperature		Junction Temperature	—	165	—	—	165	—	°C
NOISE									
Voltage Density, RTI	e _n	f _O = 1kHz							nV/√Hz
		G = 1000	—	5	—	—	5	—	
		G = 100	—	10	—	—	10	—	
		G = 10	—	59	—	—	59	—	
		G = 1	—	540	—	—	540	—	
Noise Current Density, RTI	i _n	f _O = 1kHz, G = 1000	—	0.15	—	—	0.15	—	pA/√Hz
Input Noise Voltage	e _{np-p}	0.1Hz to 10Hz							μV _{p-p}
		G = 1000	—	0.12	—	—	0.12	—	
		G = 100	—	0.16	—	—	0.16	—	
		G = 10	—	1.4	—	—	1.4	—	
		G = 1	—	13	—	—	13	—	
Input Noise Current	i _{np-p}	0.1Hz to 10Hz, G = 1000	—	2	—	—	2	—	pA _{p-p}
DYNAMIC RESPONSE									
Small-Signal Bandwidth (~3dB)	BW	G = 1	—	570	—	—	570	—	kHz
		G = 10	—	100	—	—	100	—	
		G = 100	—	82	—	—	82	—	
		G = 1000	—	26	—	—	26	—	
Slew Rate	SR	G = 10	3.5	4.5	—	3.0	4.5	—	V/μs
Settling Time	t _s	To 0.01%, 20V step							μs
		G = 1	—	12	—	—	12	—	
		G = 10	—	13	—	—	13	—	
		G = 100	—	15	—	—	15	—	
		G = 1000	—	50	—	—	50	—	

NOTES:

1. Guaranteed by design.
2. Gain tempco does not include the effects of gain and scale resistor tempco match.
3. $-55^\circ C \leq T_A \leq +125^\circ C$ for A/B grades, $-25^\circ C \leq T_A \leq +85^\circ C$ for E/F grades, $0^\circ C \leq T_A \leq 70^\circ C$ for E grade.

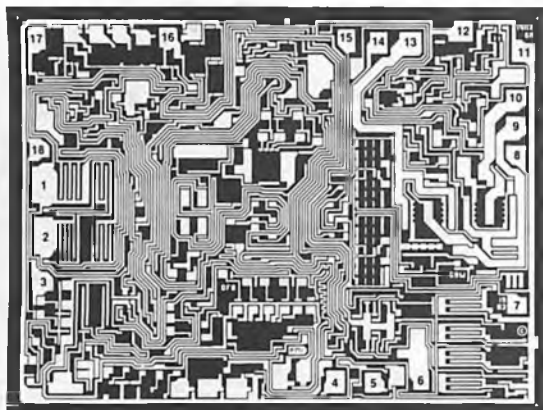
**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01A/E			AMP-01B/F/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SENSE INPUT									
Input Resistance	R _{IN}		35	50	65	35	50	65	kΩ
Input Current	I _{IN}	Referenced to V-	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	-10.5	—	+15	-10.5	—	+15	V
REFERENCE INPUT									
Input Resistance	R _{IN}		35	50	65	35	50	65	kΩ
Input Current	I _{IN}	Referenced to V-	—	280	—	—	280	—	μA
Voltage Range		(Note 1)	-10.5	—	+15	-10.5	—	+15	V
Gain to Output			—	1	—	—	1	—	V/V
POWER SUPPLY -25°C ≤ T _A ≤ +85°C for E/F Grades, -55°C ≤ T _A ≤ +125°C for A/B Grades									
Supply Voltage Range	V _S	+V linked to +V _{OP} -V linked to -V _{OP}	±4.5	—	±18	±4.5	—	±18	V
Quiescent Current	I _O	+V linked to +V _{OP} -V linked to -V _{OP}	—	3.0	4.8	—	3.0	4.8	mA

NOTE:

1. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.111×0.149 inch, 16,539 sq. mils
(2.82×3.78 mm, 10.67 sq. mm)

- | | |
|-------------------|--------------------|
| 1. R_G | 10. V^- (OUTPUT) |
| 2. R_G | 11. V^- |
| 3. $-INPUT$ | 12. V^+ |
| 4. V_{OOS} NULL | 13. V^+ (OUTPUT) |
| 5. V_{OOS} NULL | 14. R_S |
| 6. TEST PIN* | 15. R_S |
| 7. SENSE | 16. V_{IOS} NULL |
| 8. REFERENCE | 17. V_{IOS} NULL |
| 9. OUTPUT | 18. $+INPUT$ |

* Make no electrical connection

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

6

WAFER TEST LIMITS at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-01NBC LIMIT	AMP-01GBC LIMIT	UNITS
Input Offset Voltage	V_{IOS}		60	120	μV MAX
Output Offset Voltage	V_{OOS}		4	8	mV MAX
Offset Referred to Input vs. Positive Supply	PSR	$V^+ = +5V$ to $+15V$			
		$G = 1000$	120	110	dB MIN
		$G = 100$	110	100	
		$G = 10$	95	90	
Offset Referred to Input vs. Negative Supply	PSR	$V^- = -5V$ to $-15V$			
		$G = 1000$	105	105	dB MIN
		$G = 100$	90	90	
		$G = 10$	70	70	
Input Bias Current	I_B	$G = 1$	50	50	nA MAX
			4	8	
			1	3	
Input Offset Current	I_{OS}				nA MAX
Input Voltage Range	IVR	Guaranteed by CMR Tests	± 10	± 10	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 10V$			
		$G = 1000$	125	115	dB MIN
		$G = 100$	120	110	
		$G = 10$	100	95	
		$G = 1$	85	75	
Gain Equation Accuracy		$G = \frac{20 \times R_S}{R_G}$	0.6	0.8	% MAX
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	± 13	± 13	V MIN
		$R_L = 500\Omega$	± 13	± 13	
		$R_L = 50\Omega$	± 2.5	± 2.5	
Output-Current Limit		Output-to-Ground Short	± 60	± 60	mA MIN
Output-Current Limit		Output-to-Ground Short	± 120	± 120	mA MAX
Quiescent Current	I_Q	$-V$ Linked to $+V_{OP}$	4.8	4.8	mA MAX
		$-V$ Linked to $-V_{OP}$			

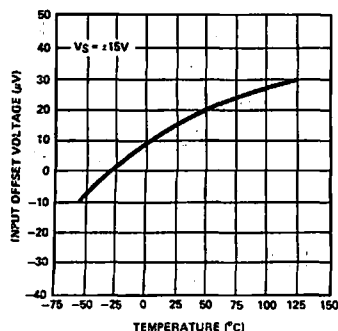
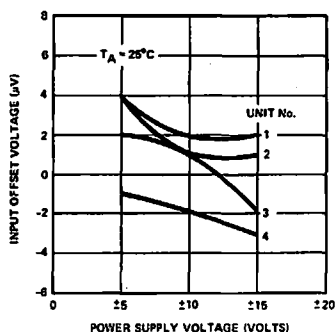
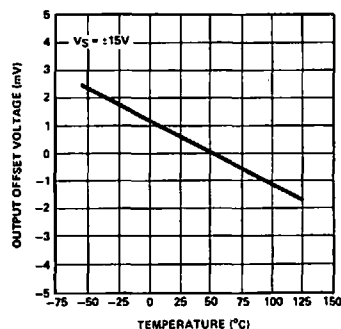
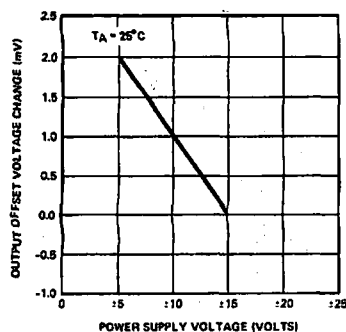
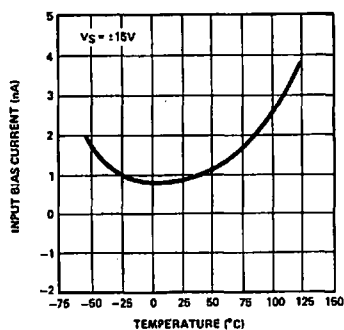
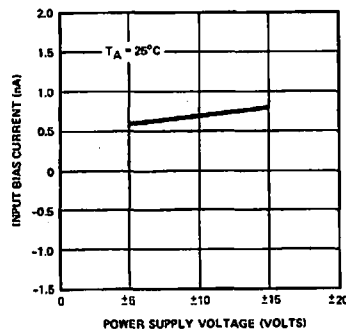
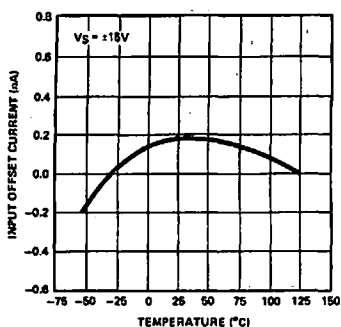
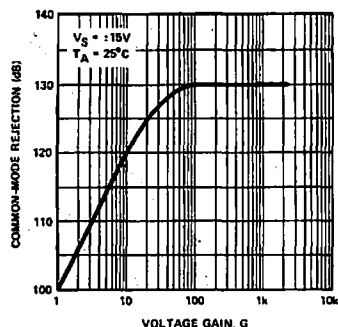
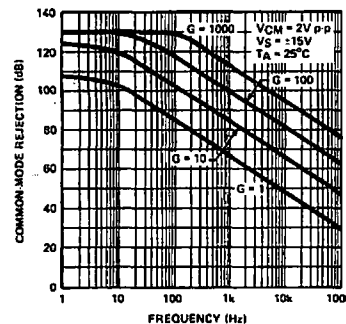
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $R_S = 10k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

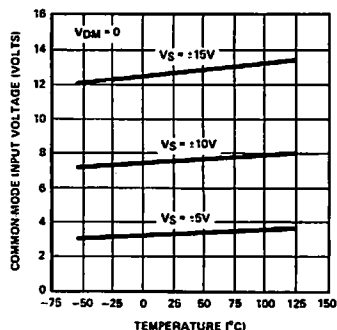
PARAMETER	SYMBOL	CONDITIONS	AMP-01NBC TYPICAL	AMP-01GBC TYPICAL	UNITS
Input Offset Voltage Drift	TCV_{IOS}		0.15	0.30	$\mu V/^\circ C$
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$	20	50	$\mu V/^\circ C$
Input Bias Current Drift	TCI_B		40	50	$pA/^\circ C$
Input Offset Current Drift	TCI_{OS}		3	5	$pA/^\circ C$
Nonlinearity		$G = 1000$	0.0007	0.0007	%
Voltage Noise Density	e_n	$G = 1000$ $f_O = 1kHz$	5	5	$nV/\sqrt{Hz}$
Current Noise Density	i_n	$G = 1000$ $f_O = 1kHz$	0.15	0.15	$pA/\sqrt{Hz}$
Voltage Noise	e_{np-p}	$G = 1000$ 0.1Hz to 10Hz	0.12	0.12	μV_{p-p}
Current Noise	i_{np-p}	$G = 1000$ 0.1Hz to 10Hz	2	2	pA_{p-p}
Small-Signal Bandwidth (-3dB)	BW	$G = 1000$	26	26	kHz
Slew Rate	SR	$G = 10$	4.5	4.5	$V/\mu s$
Settling Time	t_s	To 0.01%, 20V Step $G = 1000$	50	50	μs

TYPICAL PERFORMANCE CHARACTERISTICS

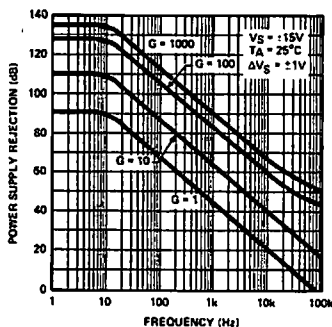
INPUT OFFSET VOLTAGE
vs TEMPERATURE

INPUT OFFSET VOLTAGE
vs SUPPLY VOLTAGE

OUTPUT OFFSET VOLTAGE
vs TEMPERATURE

OUTPUT OFFSET VOLTAGE
CHANGE vs SUPPLY VOLTAGE

INPUT BIAS CURRENT
vs TEMPERATURE

INPUT BIAS CURRENT
vs SUPPLY VOLTAGE

INPUT OFFSET CURRENT
vs TEMPERATURE

COMMON-MODE REJECTION
vs VOLTAGE GAIN

COMMON-MODE REJECTION
vs FREQUENCY


TYPICAL PERFORMANCE CHARACTERISTICS

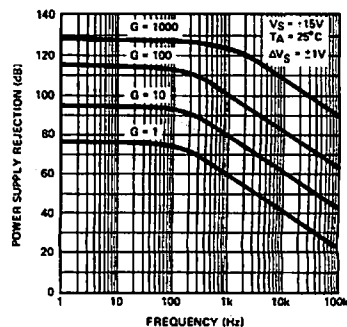
COMMON-MODE VOLTAGE RANGE vs TEMPERATURE



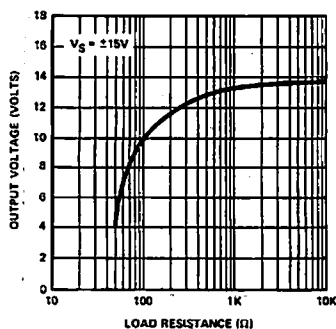
POSITIVE PSR vs FREQUENCY



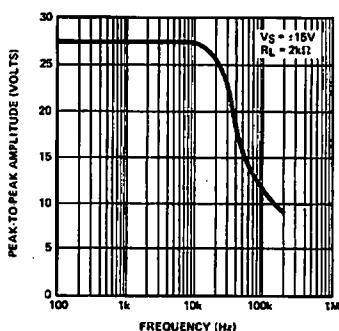
NEGATIVE PSR vs FREQUENCY



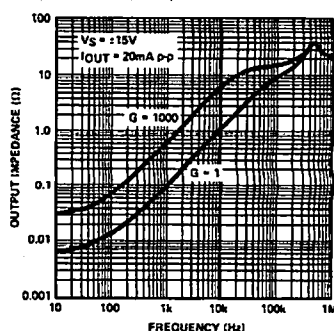
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



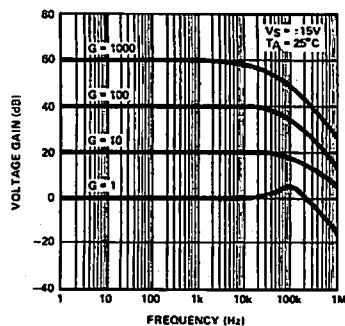
MAXIMUM OUTPUT SWING vs FREQUENCY



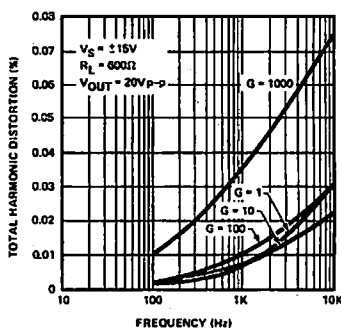
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



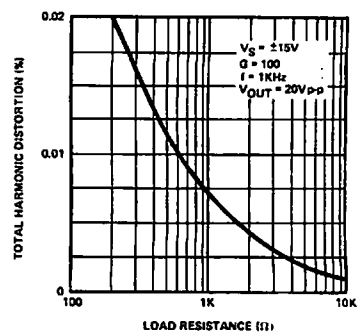
CLOSED-LOOP VOLTAGE GAIN vs FREQUENCY



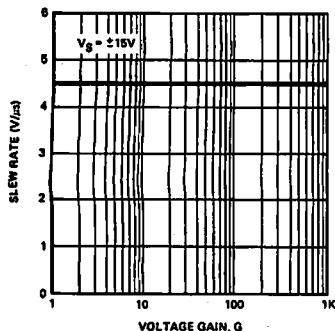
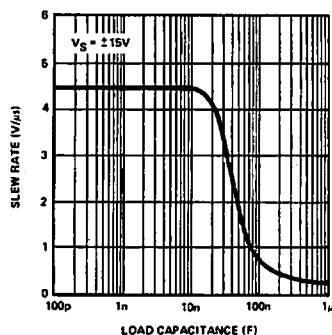
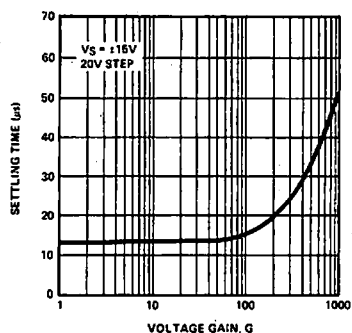
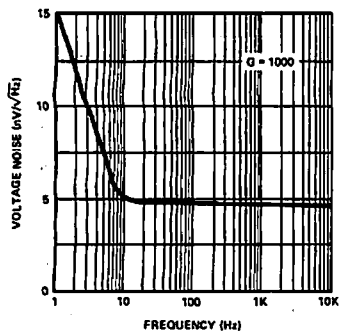
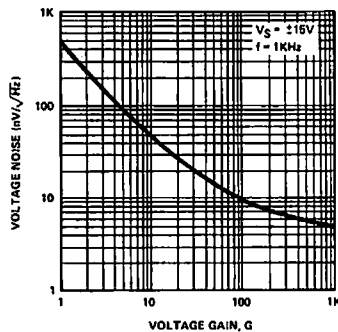
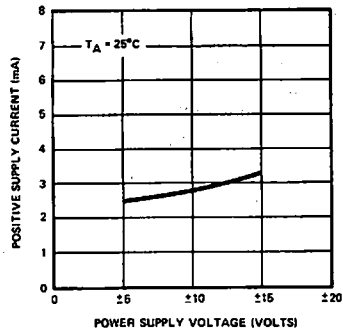
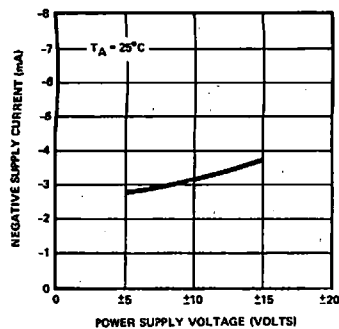
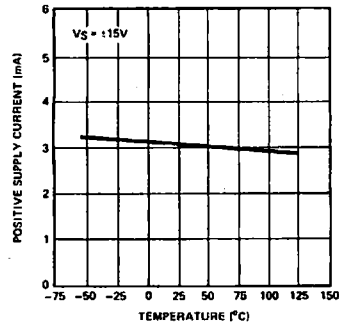
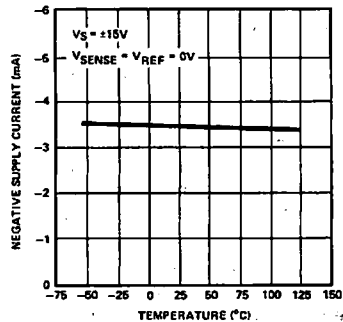
TOTAL HARMONIC DISTORTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs LOAD RESISTANCE



TYPICAL PERFORMANCE CHARACTERISTICS

SLEW RATE vs
VOLTAGE GAIN

SLEW RATE vs
LOAD CAPACITANCE

SETTLING TIME TO 0.01%
vs VOLTAGE GAIN

VOLTAGE NOISE DENSITY
vs FREQUENCY

RTI VOLTAGE NOISE
DENSITY vs GAIN

POSITIVE SUPPLY CURRENT
vs SUPPLY VOLTAGE

NEGATIVE SUPPLY CURRENT
vs SUPPLY VOLTAGE

POSITIVE SUPPLY CURRENT
vs TEMPERATURE

NEGATIVE SUPPLY CURRENT
vs TEMPERATURE


INPUT AND OUTPUT OFFSET VOLTAGES

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. While the initial offsets may be adjusted to zero, temperature variations will cause shifts in offsets. Systems with auto-zero can correct for offset errors, so initial adjustment would be unnecessary. However, many high-gain applications don't have auto zero. For these applications, both offsets can be nulled, which has minimal effect on TCV_{IOS} and TCV_{OOS} .

The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore, at low gain, output-offset-errors dominate, while at high gain, input-offset-errors dominate. Overall offset voltage, V_{OS} , referred to the output (RTO) is calculated as follows:

$$V_{OS}(RTO) = (V_{IOS} \times G) + V_{OOS} \quad (1)$$

where V_{IOS} and V_{OOS} are the input and output offset voltage specifications and G is the amplifier gain. Input offset nulling alone is recommended with amplifiers having fixed gain above 50. Output offset nulling alone is recommended when gain is fixed at 50 or below.

In applications requiring both initial offsets to be nulled, the input offset is nulled first by short-circuiting R_G , then the output offset is nulled with the short removed.

The overall offset voltage drift TCV_{OS} , referred to the output, is a combination of input and output drift specifications. Input offset voltage drift is multiplied by the amplifier gain, G , and summed with the output offset drift:

$$TCV_{OS}(RTO) = (TCV_{IOS} \times G) + TCV_{OOS} \quad (2)$$

where TCV_{IOS} is the input offset voltage drift, and TCV_{OOS} is the output offset voltage specification. Frequently, the amplifier drift is referred back to the input (RTI) which is then equivalent to an input signal change;

$$TCV_{OS}(RTI) = TCV_{IOS} + \frac{TCV_{OOS}}{G} \quad (3)$$

For example, the maximum input-referred drift of an AMP-01EX set to $G = 1000$ becomes:

$$TCV_{OS}(RTI) = 0.3 \mu V/^{\circ}C + \frac{100 \mu V/^{\circ}C}{1000} = 0.4 \mu V/^{\circ}C \text{ max.}$$

INPUT BIAS AND OFFSET CURRENTS

Input transistor bias currents are additional error sources which can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an IA will minimize offset changes due to bias current variations with signal voltage and temperature. However, the difference between the two bias currents, the input offset current, produces a non-trimmable error. The magnitude of the error is the offset current times the source resistance.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs, such as thermocouples, should be grounded close to the signal source for best common-mode rejection.

GAIN

The AMP-01 uses two external resistors for setting voltage gain over the range 0.1 to 10,000. The magnitudes of the scale resistor, R_S , and gain-set resistor, R_G , are related by the formula: $G = 20 \times R_S / R_G$, where G is the selected voltage gain (Refer to Figure 1).

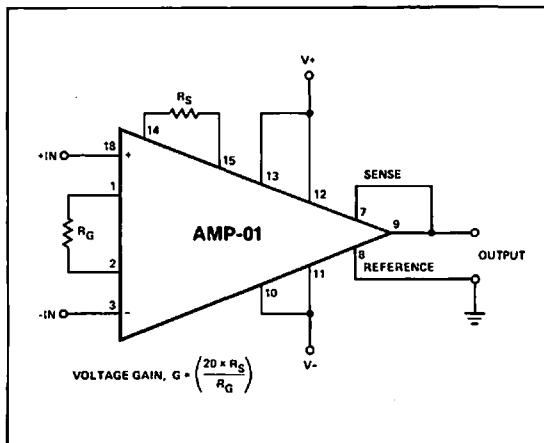
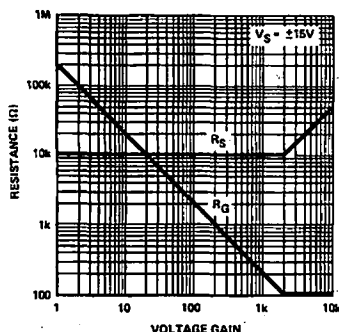


Figure 1. Basic AMP-01 connections for gains 0.1 to 10,000.

The magnitude of R_S affects linearity and output referred errors. Circuit performance is characterized using $R_S = 10k\Omega$ when operating on ± 15 volt supplies and driving a ± 10 volt output. R_S may be reduced to $5k\Omega$ in many applications particularly when operating on ± 5 volt supplies or if the output voltage swing is limited to ± 5 volts. Bandwidth is improved with $R_S = 5k\Omega$ and this also increases common-mode rejection by approximately 6dB at low gain. Lowering the value below $5k\Omega$ can cause instability in some circuit configurations and usually has no advantage. High voltage gains between two and ten thousand would require very low values of R_G . For $R_S = 10k\Omega$ and $A_V = 2000$ we get $R_G = 100\Omega$; this value is the practical lower limit for R_G . Below 100Ω , mismatch of wirebond and resistor temperature coefficients will introduce significant gain tempco errors. Therefore, for gains above 2,000, R_G should be kept constant at 100Ω and R_S increased. The maximum gain of 10,000 is obtained with R_S set to $50k\Omega$.

Metal-film or wirewound resistors are recommended for best results. The absolute values and TC's are not too important, only the ratio-metric parameters.

AC amplifiers require good gain stability with temperature and time, but DC performance is unimportant. Therefore, low cost metal-film types with TC's of $50ppm/^{\circ}C$ are usually adequate for R_S and R_G . Realizing the full potential of the AMP-01's offset voltage and gain stability requires precision metal-film or wirewound resistors. Achieving a $15ppm/^{\circ}C$ gain tempco at all gains requires R_S and R_G temperature coefficient matching to $5ppm/^{\circ}C$ or better.



R_G AND R_S SELECTION

Gain accuracy is determined by the ratio accuracy of R_S and R_G combined with the gain equation error of the AMP-01 (0.6% max for A/E grades).

All instrumentation amplifiers require attention to layout so thermocouple effects are minimized. Thermocouples formed between copper and dissimilar metals can easily destroy the TCV_{OS} performance of the AMP-01 which is typically $0.15\mu V/^\circ C$. Resistors themselves can generate thermoelectric EMFs when mounted parallel to a thermal gradient. "Vishay" resistors are recommended because a maximum value for thermoelectric generation is specified. However, where thermal gradients are low and gain TC's of 20-50ppm are sufficient, general-purpose metal-film resistors can be used for R_G and R_S .

COMMON-MODE REJECTION

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. CMR specifications are normally measured with a full-range input voltage change and a specified source resistance unbalance.

The current-feedback design used in the AMP-01 inherently yields high common-mode rejection. Unlike resistive feedback designs, typified by the three-op-amp IA, the CMR is not degraded by small resistances in series with the reference input. A slight, but trimmable, output offset voltage change results from resistance in series with the reference input.

The common-mode input voltage range, CMVR, for linear operation may be calculated from the formula:

$$CMVR = \pm \left(IVR - \frac{|V_{OUT}|}{2G} \right) \dots (4)$$

IVR is the data sheet specification for input voltage range; V_{OUT} is the maximum output signal; and G is the chosen

voltage gain. For example, at $25^\circ C$, IVR is specified as ± 10.5 volt minimum with ± 15 volt supplies. Using a ± 10 volt maximum swing output and substituting the figures in (4) simplifies the formula to:

$$CMVR = \pm \left(10.5 - \frac{5}{G} \right) \dots (5)$$

For all gains greater than or equal to 10, CMVR is ± 10 volt minimum; at gains below 10, CMVR is reduced.

ACTIVE GUARD DRIVE

Rejection of common-mode noise and line pick-up can be improved by using shielded cable between the signal source and the IA. Shielding reduces pick-up, but increases input capacitance, which in turn degrades the settling-time for signal changes. Further, any imbalance in the source resistance between the inverting and noninverting inputs, when capacitively loaded, converts the common-mode voltage into a differential voltage. This effect reduces the benefits of shielding. AC common-mode rejection is improved by "bootstrapping" the input cable capacitance to the input signal, a technique called "guard driving". This technique effectively reduces the input capacitance. A single guard-driving signal is adequate at gains above 100 and should be the average value of the two inputs. The value of external gain resistor R_G is split between two resistors R_{G1} and R_{G2} ; the center tap provides the required signal to drive the buffer amplifier (Figure 2).

GROUNDING

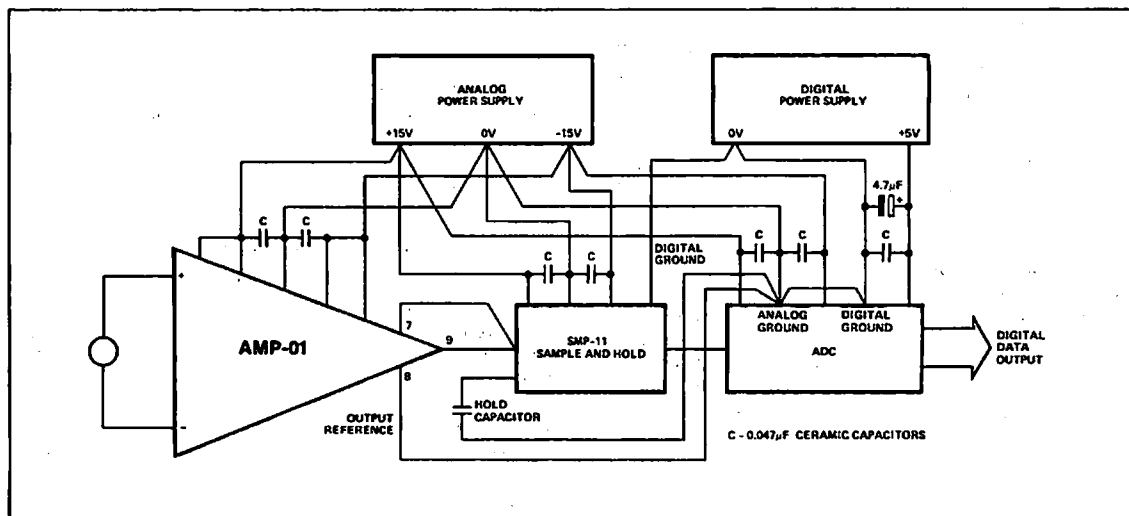
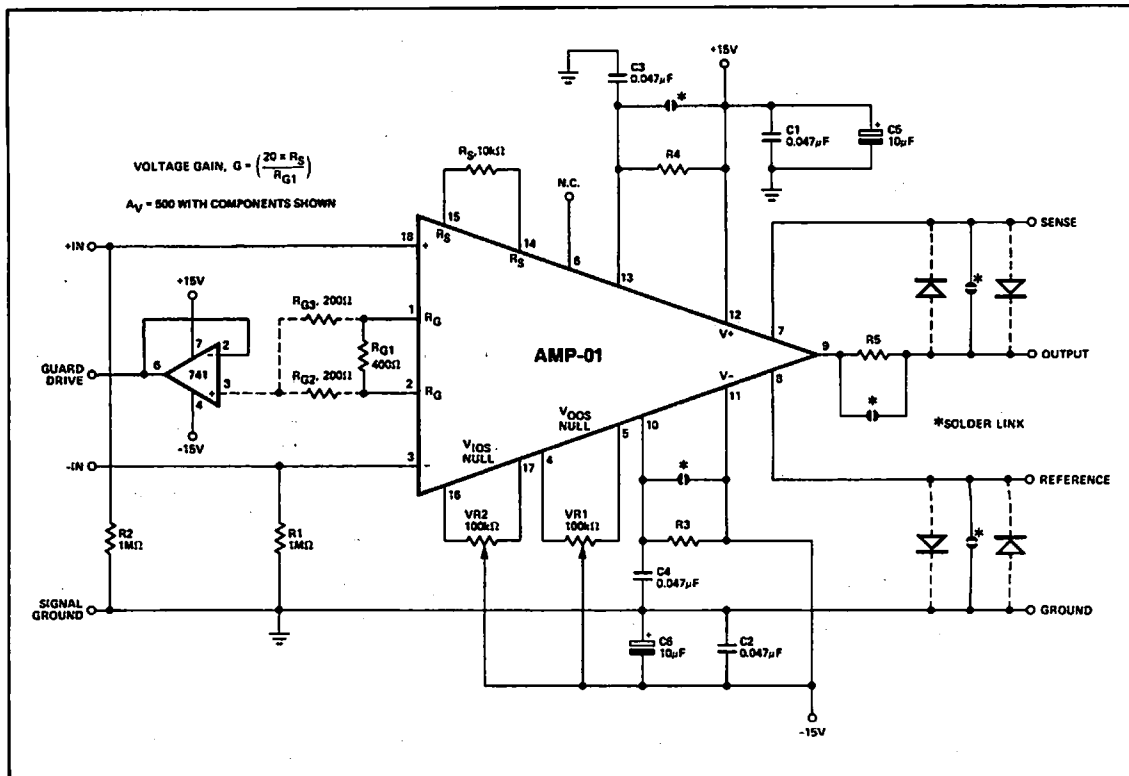
The majority of instruments and data acquisition systems have separate grounds for analog and digital signals. Analog ground may also be divided into two or more grounds which will be tied together at one point, usually the analog power-supply ground. In addition, the digital and analog grounds may be joined, normally at the analog ground pin on the A-to-D converter. Following this basic grounding practice is essential for good circuit performance (Figure 3).

Mixing grounds causes interactions between digital circuits and the analog signals. Since the ground returns have finite resistance and inductance, hundreds of millivolts can be developed between the system ground and the data acquisition components. Using separate ground returns minimizes the current flow in the sensitive analog return path to the system ground point. Consequently, noisy ground currents from logic gates do not interact with the analog signals.

Inevitably, two or more circuits will be joined together with their grounds at differential potentials. In these situations, the differential input of an instrumentation amplifier, with its high CMR, can accurately transfer analog information from one circuit to another.

SENSE AND REFERENCE TERMINALS

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the output. The output signal is specified with respect to the reference terminal, which is normally connected to analog ground.



If heavy output currents are expected and the load is situated some distance from the amplifier, voltage drops due to track or wire resistance will cause errors. Voltage drops are particularly troublesome when driving 50Ω loads. Under these conditions, the sense and reference terminals can be used to "remote sense" the load as shown in Figure 4. This method of connection puts the I×R drops inside the feedback loop and virtually eliminates the error. An unbalance in the load resistances from the sense and reference pins does not degrade CMR, but will change the output offset voltage. For example, a large unbalance of 3Ω will change the output offset by only 1mV.

DRIVING 50Ω LOADS

Output currents of 50mA are guaranteed into loads of up to 50Ω and 28mA into 500Ω. In addition, the output is stable and free from oscillation even with a high load capacitance. The combination of these unique features in an instrumentation amplifier allows low-level transducer signals to be condi-

tioned and directly transmitted through long cables in voltage or current form. Increased output current brings increased internal dissipation, especially with 50Ω loads. For this reason, the power-supply connections are split into two pairs; pins 10 and 13 connect to the output stage only and pins 11 and 12 provide power to the input and following stages. Dual supply pins allow dropper resistors to be connected in series with the output stage so excess power is dissipated outside the package. Additional decoupling is necessary between pins 10 and 13 to ground to maintain stability when dropper resistors are used. Figure 5 shows a complete circuit for driving 50Ω loads.

HEATSINKING

To maintain high reliability, the die temperature of any IC should be kept as low as practicable, preferably below 100°C. Although most AMP-01 application circuits will produce very little internal heat — little more than the quiescent dissipation of 90mW — some circuits will raise that

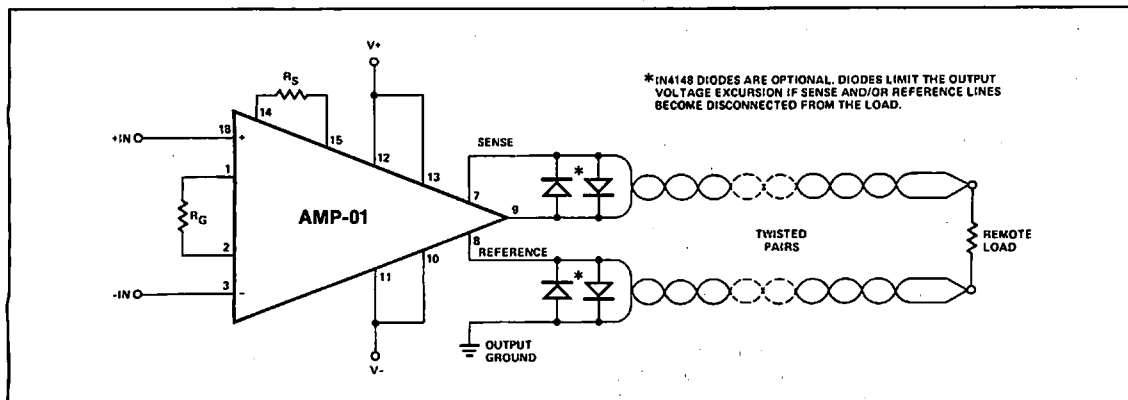


Figure 4. Remote load sensing.

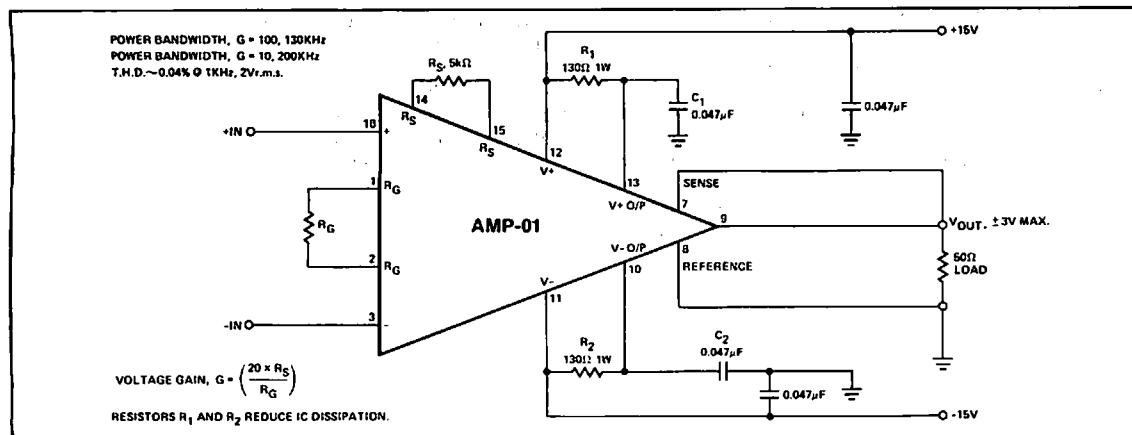


Figure 5. Driving 50Ω loads.

to several hundred milliwatts (for example, the 4-20mA current transmitter application, Figure 8). Excessive dissipation will cause thermal shutdown of the output stage thus protecting the device from damage. A heatsink is recommended in power applications to reduce the die temperature.

Several appropriate heatsinks are available; the Thermalloy 6010B is especially easy to use and is inexpensive. Intended for dual-in-line packages, the heatsink may be attached with a cyanoacrylate adhesive. This heatsink reduces the thermal resistance between the junction and ambient environment to approximately 80° C/W. Junction (die) temperature can then be calculated by using the relationship:

$$P_d = \frac{T_j - T_a}{\theta_{ja}}$$

where T_j and T_a are the junction and ambient temperatures respectively, θ_{ja} is the thermal resistance from junction to ambient, and P_d is the device's internal dissipation.

OVERVOLTAGE PROTECTION

Instrumentation amplifiers invariably sit at the front end of instrumentation systems where there is a high probability of exposure to overloads. Voltage transients, failure of a transducer, or removal of the amplifier power supply while the signal source is connected may destroy or degrade the performance of an unprotected amplifier. Although it is impractical to protect an IC internally against connection to power lines, it is relatively easy to provide protection against typical system overloads.

The AMP-01 is internally protected against overloads for gains of up to 100. At higher gains, the protection is reduced and some external measures may be required. Limited internal overload protection is used so that noise performance would not be significantly degraded.

AMP-01 noise level approaches the theoretical noise floor of the input stage which would be $4nV/\sqrt{Hz}$ at 1kHz when the gain is set at 1000. Noise is the result of shot noise in the input devices and Johnson noise in the resistors. Resistor noise is calculated from the values of R_G (200Ω at a gain of 1000) and the input protection resistors (250Ω). Active loads for the input transistors contribute less than $1nV/\sqrt{Hz}$ of noise. The measured noise level is typically $5nV/\sqrt{Hz}$.

Diodes across the input transistor's base-emitter junctions, combined with 250Ω input resistors and R_G , protect against differential inputs of up to $\pm 20V$ for gains of up to 100. The diodes also prevent avalanche breakdown that would degrade the I_B and I_{OS} specifications. Decreasing the value of R_G for gains above 100 limits the maximum input overload protection to $\pm 10V$. External series resistors could be added to guard against higher voltage levels at the input, but resistors alone increase the input noise and degrade the signal-to-noise ratio, especially at high gains.

Protection can also be achieved by connecting back-to-back 9.1V zener diodes across the differential inputs. This technique does not affect the input noise level and can be used down to a gain of 2 with minimal increase in input current. Although voltage-clamping elements look like short circuits at the limiting voltage, the majority of signal sources provide less than 50mA, producing power levels that are easily handled by low-power zeners.

Simultaneous connection of the differential inputs to a low-impedance signal above 10V during normal circuit operation is unlikely. However, additional protection involves adding 100Ω current-limiting resistors in each signal path prior to the voltage clamp; the resistors increase the input noise level to just $5.4nV/\sqrt{Hz}$ (refer to Figure 6).

Input components, be they multiplexers or resistors, should be carefully selected to prevent the formation of thermocouple junctions which would degrade the input signal.

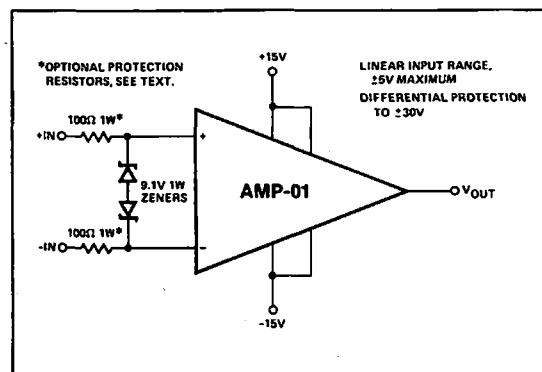
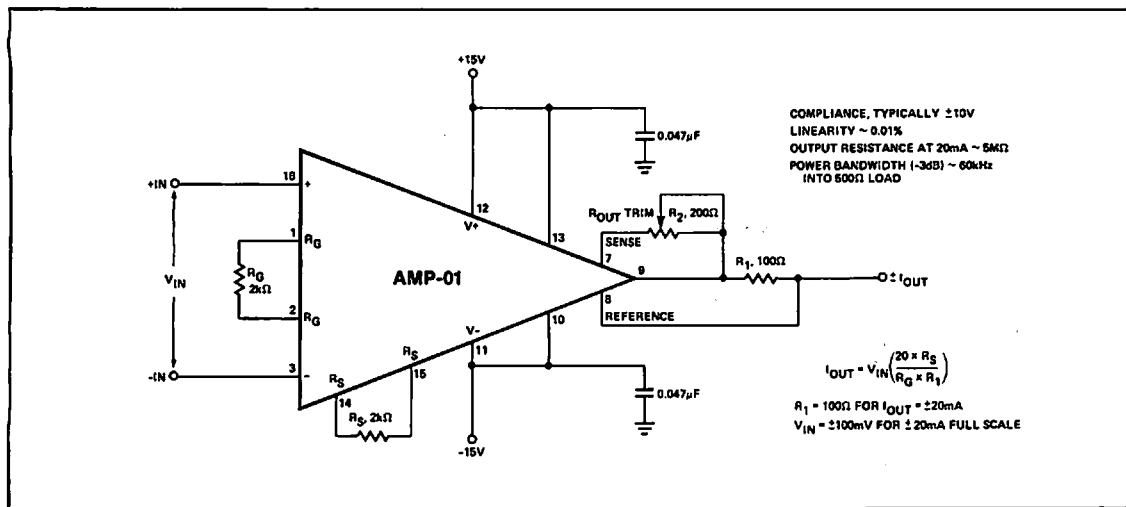
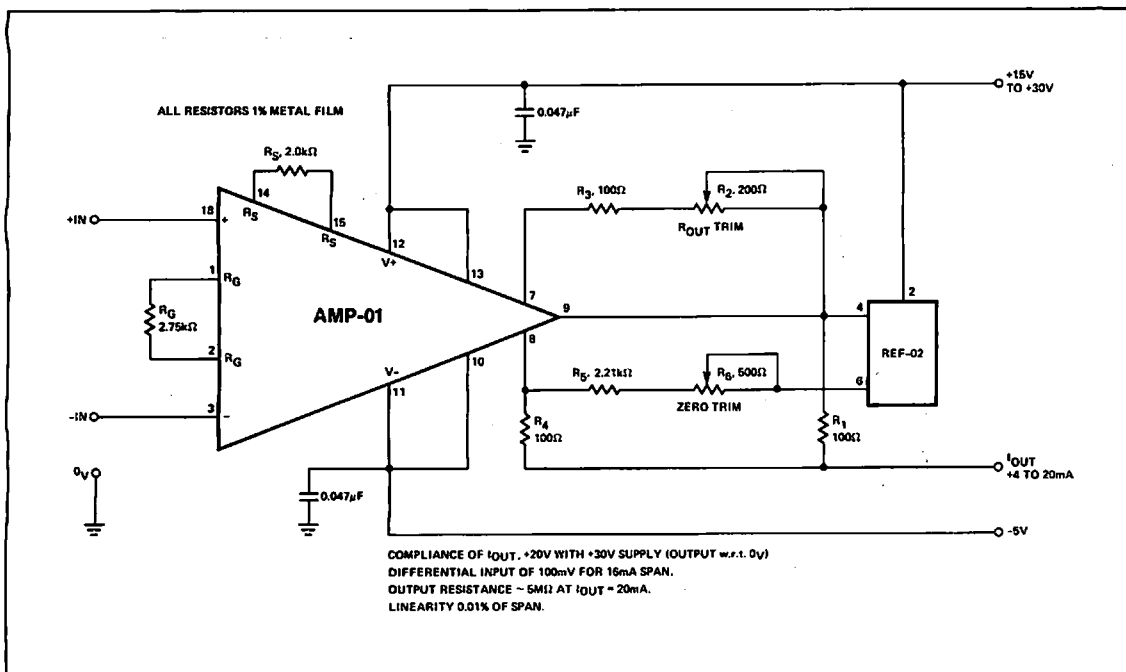


Figure 6. Input overvoltage protection for gains 2 to 10,000.

POWER SUPPLY CONSIDERATIONS

Achieving the rated performance of precision amplifiers in a practical circuit requires careful attention to external influences. For example, supply noise and changes in the nominal voltage directly affect the input offset voltage. A PSR of 80dB means that a change of 100mV on the supply, not an uncommon value, will produce a $10\mu V$ input offset change. Consequently, care should be taken in choosing a power unit that has a low output noise level, good line and load regulation, and good temperature stability.

APPLICATIONS INFORMATION

Figure 7. High-compliance bipolar current source with 13-bit linearity.

Figure 8. 13-bit linear 4-20mA transmitter constructed by adding a voltage reference. Thermocouple signals can be accepted without preamplification.

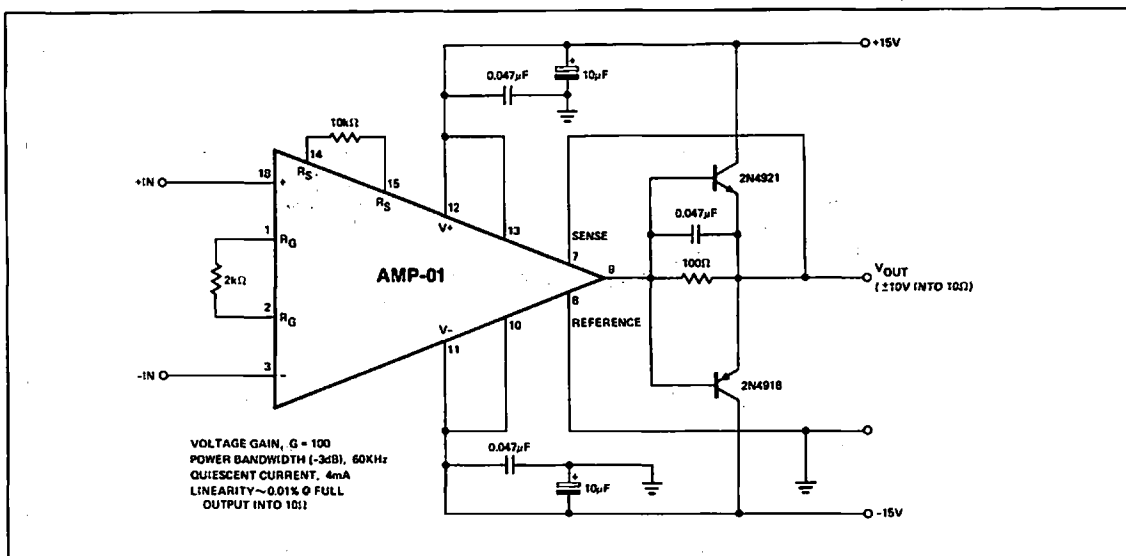


Figure 9. Adding two transistors increases output current to $\pm 1A$ without affecting the quiescent current of 4mA. Power bandwidth is 60kHz.

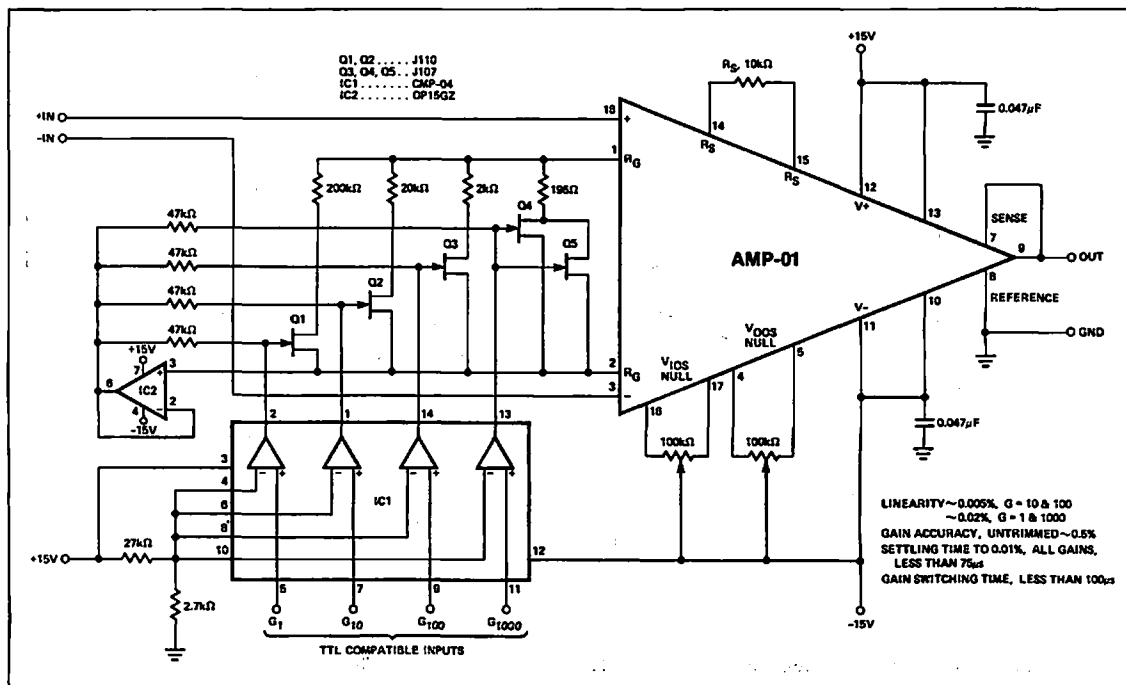


Figure 10. The AMP-01 makes an excellent programmable-gain instrumentation amplifier. Combined gain-switching and settling time to 13-bits falls below 100 μs . Linearity is better than 12-bits over a gain range 1 to 1000.

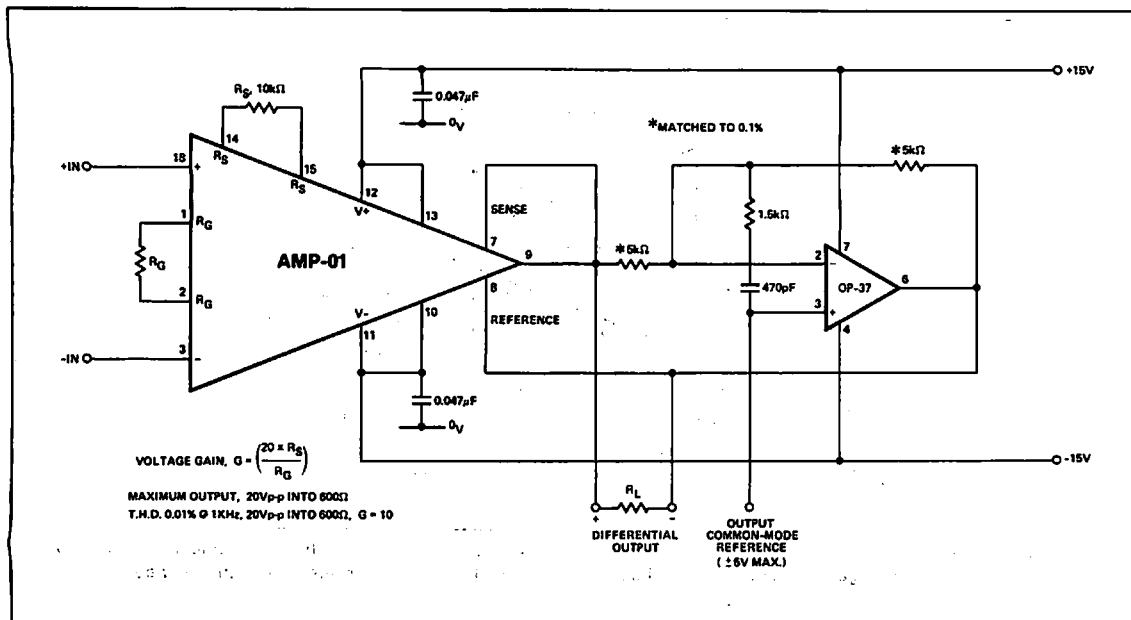


Figure 11. A differential input instrumentation amplifier with differential output replaces a transformer in many applications. The output will drive a 600Ω load at low distortion, (0.01%).

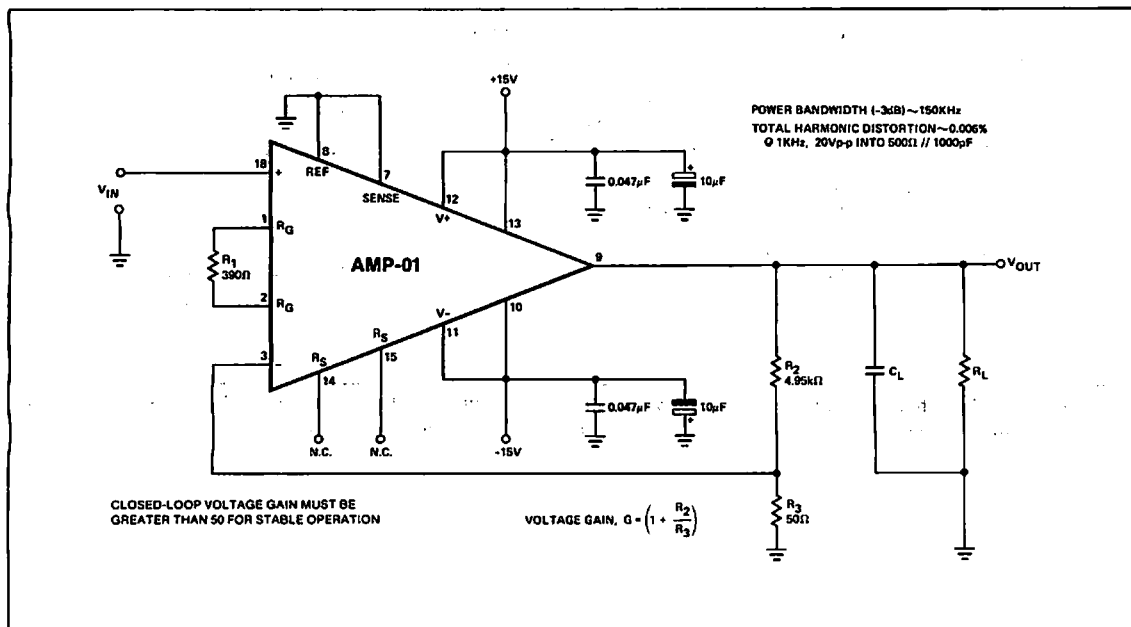


Figure 12. Configuring the AMP-01 as a noninverting operational amplifier provides exceptional performance. The output handles low load impedances at very low distortion, 0.006%.

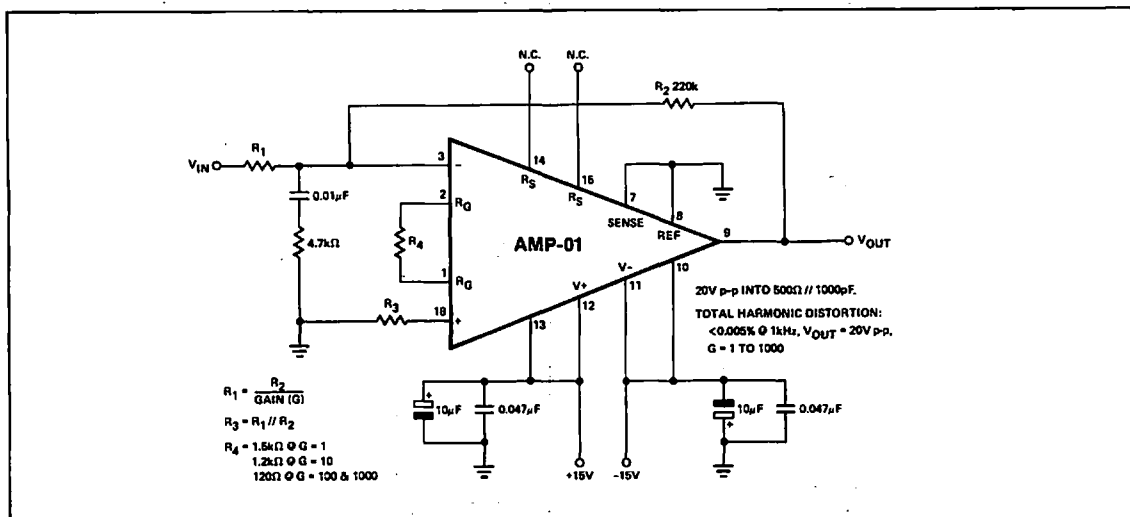


Figure 13. The inverting operational amplifier configuration has excellent linearity over the gain range 1 to 1000, typically 0.005%. Offset voltage drift at unity gain is improved over the drift in the instrumentation amplifier configuration.

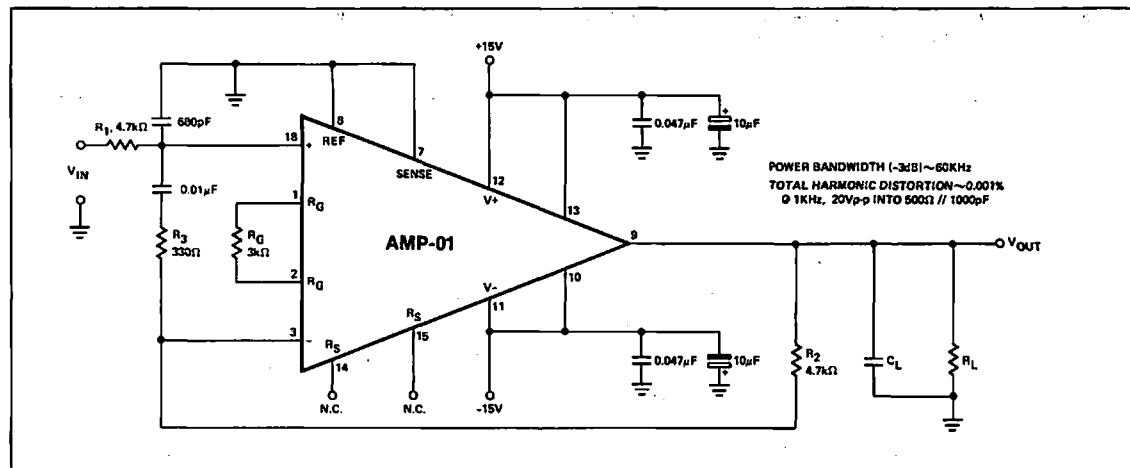
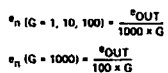


Figure 14. Stability with large capacitive loads combined with high output current capability make the AMP-01 ideal for line driving applications. Offset voltage drift approaches the TCV_{IO5} limit, ($0.3\mu V/^{\circ}C$).

NOISE TEST CIRCUIT (0.1Hz to 10Hz)

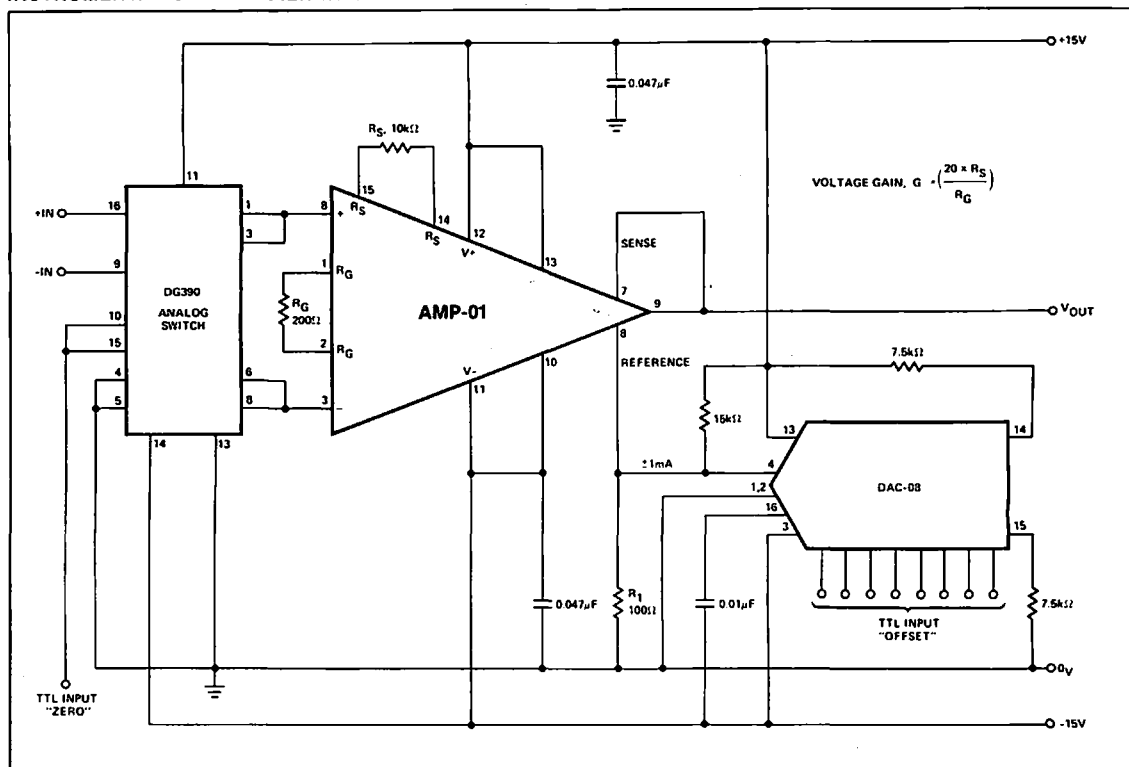


SETTLING-TIME TEST CIRCUIT

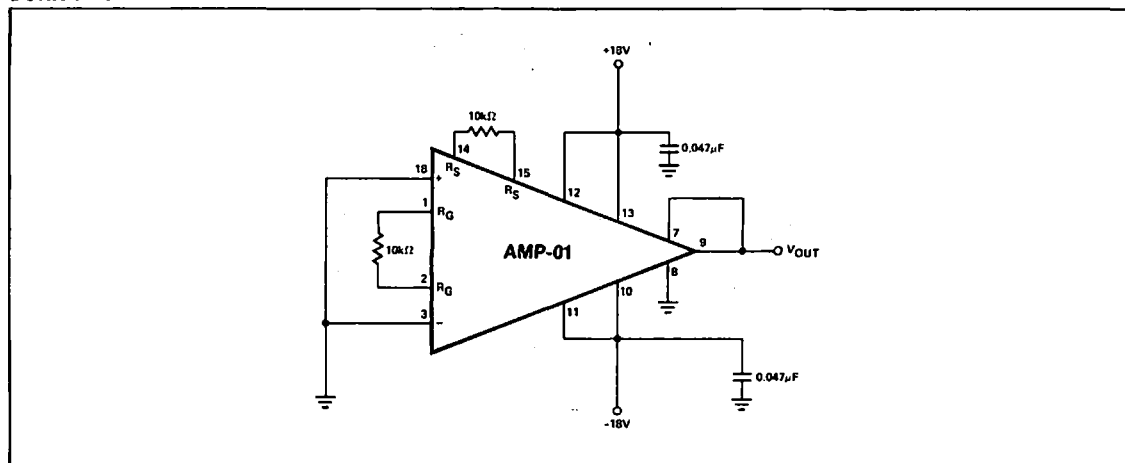




INSTRUMENTATION AMPLIFIER WITH AUTO-ZERO



BURN-IN CIRCUIT





AMP-02

HIGH-ACCURACY, 8-PIN
INSTRUMENTATION AMPLIFIER

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Offset Voltage $50\mu\text{V}$ Max
- Low Drift $0.3\mu\text{V}/^\circ\text{C}$ Max
- Wide Gain Range $G = 1$ to $10,000$
- High Common-Mode Rejection 125dB Min
- Bandwidth Independent of Gain 300kHz Typ
- Low Gain Tempco $50\text{ppm}/^\circ\text{C}$ Max
- Gain Equation Accuracy 0.1% Max
- Extended Industrial Temp Range -40°C to $+85^\circ\text{C}$
- Single Resistor Gain Programmability

GENERAL DESCRIPTION

The AMP-02 is a precision monolithic instrumentation amplifier encased in space-saving 8-pin mini-dips. An instrumentation amp accepts differential input signals into a high-impedance front-end and delivers an amplified single-ended output. High common-mode rejection is achieved without resistor matching. Gain is set by a single external resistor, and is variable over a range of 1 to 10,000. Linearity of the AMP-02 is extremely high in all gain configurations. Input protection networks allow the inputs to be taken 36V beyond either supply rail without damaging the device.

Laser-trimming at wafer-sort reduces input offset voltage to below $50\mu\text{V}$, and maintains gain equation accuracy to a tight 0.1% . Input offset voltage drift less than $0.3\mu\text{V}/^\circ\text{C}$ eliminates the need for nulling circuitry in most applications. PMI's proprietary state-of-the-art thin-film resistor process keeps gain temperature coefficient under $50\text{ppm}/^\circ\text{C}$.

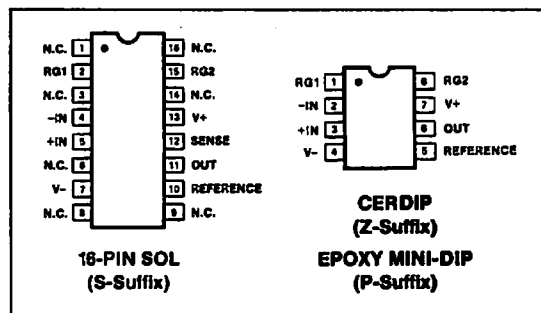
The AMP-02's bandwidth remains constant at 300kHz , regardless of gain-setting. Slew rate is above $2\text{V}/\mu\text{s}$, providing a full-power bandwidth of at least 30kHz for a $20\text{V}_{\text{p-p}}$ sine-wave output. Since full-power bandwidth is directly proportional to signal size, at $2\text{V}_{\text{p-p}}$ the full 300kHz bandwidth of the amplifier may be utilized.

A reference pin is provided to allow the output to be referenced to an arbitrary DC level. This pin may be used for offset correction or level shifting as required. In most applications it will be

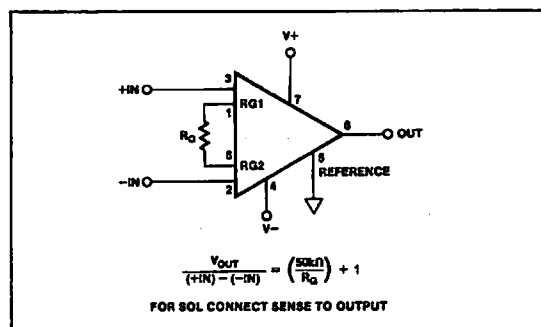
connected to ground to provide a ground-referenced output. In DIP devices, sense is internally connected to the output.

For an instrumentation amplifier having similar precision to the AMP-02, but capable of driving 50mA output current steady-state with 90mA peaks and excellent capacitive load stability, consult the AMP-01 data sheet.

PIN CONNECTIONS



BASIC CIRCUIT CONNECTIONS



INSTRUMENTATION AMPLIFIERS

6

This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage	±18V
Internal Power Dissipation (Note 2)	500mW
Common-Mode Input Voltage	[(V-) - 36V] to [(V+) + 36V]
Differential Input Voltage	[(V-) - 36V] to [(V+) + 36V]
Output Short-Circuit Duration	10 seconds
Operating Temperature Range	
AMP-02A (Z)	-55°C to +125°C
AMP-02E (Z, P)	-40°C to +85°C
Storage Temperature Range	-65°C to +175°C

Junction Temperature Range	-65°C to +175°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. See table for maximum ambient temperature and rating.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
8-Pin Cerdip (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-02A/E			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{IOS}		—	—	50	μV
Output Offset Voltage	V_{OOS}		—	—	2.5	mV
Offset Voltage Temperature Coefficient	TCV_{IOS}	Input Offset	—	—	0.3	$\mu V/^\circ C$
	TCV_{OOS}	Output Offset	—	—	15	
Input Bias Current	I_B		—	—	25	nA
Input Offset Current	I_{OS}		—	—	5	nA
Common-Mode Rejection	CMR		G = 1	—	—	dB
			G = 1000	—	—	
Power-Supply Rejection	PSR	$V_S = \pm 4.5V$ to $\pm 18V$	G = 1	—	—	dB
			G = 1000	—	—	
Gain Equation				$(50k\Omega/R_G) + 1$		
Gain Equation Error			—	—	0.1	%
Temperature Coefficient of Gain	TC_{GAIN}		—	—	50	ppm/°C
Output Voltage Swing	V_O	$R_L = 1k\Omega$	±12	—	—	V
Slew Rate	SR		2	—	—	V/ μs
Closed-Loop Bandwidth	BW	All Gains	—	300	—	kHz
Settling Time	t_S	10V Step, to 0.01%	—	—	20	μs
Noise Voltage Density	e_n	1kHz, Input Referred	—	8	—	nV/ $\sqrt{Hz}$
Supply Current	I_{SY}		—	—	4.5	mA

Precision Monolithics Inc.

FEATURES

- Settling-Time to 12-Bit Accuracy, $G \leq 2000$ $15\mu s$ Max
- Overload Recovery Time, $G = 1000$ $15\mu s$
- 14-Bit Gain Linearity at $G \leq 1000$
- On-Board Dual Guard Drivers
- On-Board $100\mu A$ Precision Current Source
- Low Bias Current $50pA$ Max @ $25^\circ C$
..... $20nA$ Max @ $125^\circ C$
- Temperature Stable CMR
..... $105dB$ Min Over $-55^\circ C$ to $+125^\circ C$
- High Slew-Rate with $500pF$ Load $.5V/\mu s$ Min
- Input Overload Protected to $\pm 30V$ Differential

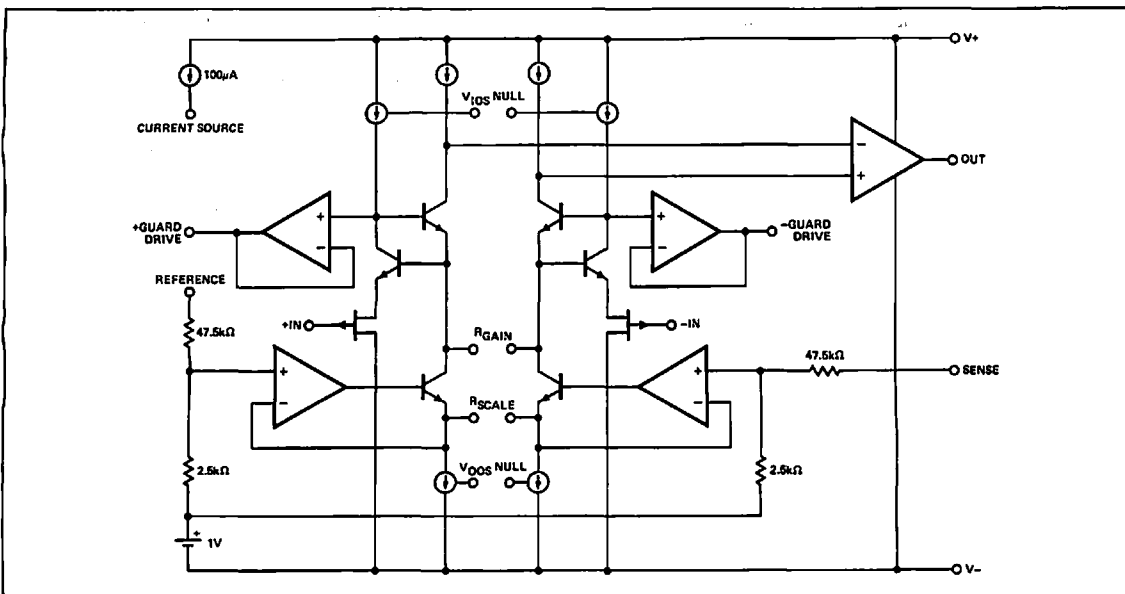
ORDERING INFORMATION†

CERDIP 18-PIN PACKAGE	OPERATING TEMPERATURE RANGE
AMP05AX*	MIL
AMP05BX*	MIL
AMP05EX	IND
AMP05FX	IND

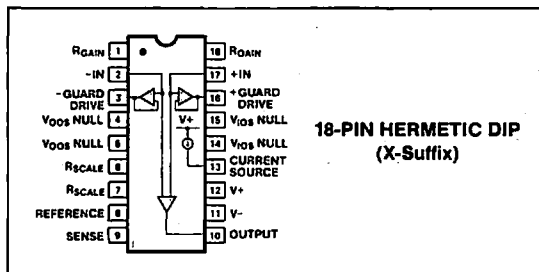
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS



GENERAL DESCRIPTION

The AMP-05 is a fast JFET instrumentation amplifier designed for high-speed analog signal-processing and analog-multiplexed data acquisition systems. Settling-time to 12-bits is $15\mu s$ maximum, with better than 14-bit linearity at all gains up to 1000. Two functions are added to the instrumentation amplifier that reduce external component count in many applications. On-board dual guard drivers maintain good settling-time and common-mode rejection performance when shielded cable connects the input signal to the AMP-05. A precision $100\mu A$ current source is also provided for transducer excitation, powering a low-current voltage reference, and other functions.



The AMP-05 employs a current-feedback technique which provides a high and stable common-mode rejection, 105dB minimum over the military temperature range. JFET inputs reduce bias current to 50pA maximum at 25°C and only 20nA maximum at 125°C; low bias current reduces errors due to signal-source resistance. Internal input protection allows a 30V differential overload at all gain settings. The AMP-05 recovers rapidly when an input overload is removed. Recovery time is typically 15μs following a 1000:1 overload, voltage gain set to 1000. AMP-05 voltage gain is set by the ratio of two external resistors over the range 0.1 to 2000 and a low gain temperature-coefficient of 20ppm/°C maximum is achievable in the range 1 to 1000.

The AMP-05's outputs can all drive large capacitive loads without oscillation. The amplifier output is guaranteed stable with loads up to 2,000pF and the guard drivers can tolerate up to 10,000pF without oscillation.

Sense and reference pins complete the output feedback-loop and provide an output ground reference, respectively. The reference pin may be used for zeroing system offsets, where auto-zero hardware is employed. Resistance in series with the reference terminal does not degrade common-mode rejection on PMI's AMP-05, which is a significant problem with instrumentation amplifiers employing the three op-amp configuration.

For applications requiring very low input offset voltage and low offset drift, or higher output drive capability, refer to the AMP-01 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Common-Mode Input Voltage	Supply Voltage
Differential Input Voltage	±30V
(Inputs must not exceed supply voltages.)	
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
AMP-05A, B	-55°C to +125°C
AMP-05E, F	-25°C to +85°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T _J)	-65°C to +150°C

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
18-Pin Hermetic DIP (X)	100°C	10mW/°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.
- Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-05A/E			AMP-05B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
GAIN									
Gain Range	G _R		0.1	—	2000	0.1	—	2000	
Gain Equation Accuracy		G = 20 × R _S /R _G G = 1 to 1000	—	0.25	0.5	—	0.4	1.0	%
Gain Nonlinearity	G _{NL}	G = 1	—	0.001	—	—	0.001	—	%
		G = 10	—	0.002	—	—	0.002	—	
		G = 100	—	0.007	—	—	0.007	—	
		G = 1000	—	0.020	—	—	0.020	—	
		R _L = 10kΩ	—	0.004	—	—	0.004	—	%
		G = 100 G = 1000	—	0.004	—	—	0.004	—	
Gain Temperature Coefficient	G _{TC}	G = 1 to 100	—	1.7	10	—	1.7	10	ppm/°C
		G = 1000 (Notes 1, 2)	—	8	20	—	8	20	
OUTPUT RATING									
Output Voltage Swing	V _{OUT}	R _L = 1kΩ Over Temperature	±11 ±10.5	±12 ±12	— —	±11 ±10.5	±12 ±12	— —	V
Short Circuit Current	I _{SC}	Output Shorted to Ground	±20	±35	—	±20	±35	—	mA
Capacitive Load Stability		Full Gain Range No Oscillations	2	10	—	2	10	—	nF

NOTES:

- Gain tempco does not include the effects of gain and scale resistor tempco match.
- Guaranteed but not 100% production tested.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	AMP-05A/E			AMP-05B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT									
Input Bias Current	I_B	$T_A \leq 25^{\circ}\text{C}$	—	20	50	—	30	100	pA
		$T_A = 85^{\circ}\text{C}$ (E/F Grades)	—	0.5	4	—	1	8	nA
		$T_A = 125^{\circ}\text{C}$ (A/B Grades)	—	7	20	—	12	30	nA
Input Offset Current	I_{OS}	$T_A \leq 25^{\circ}\text{C}$	—	5	25	—	10	50	pA
		$T_A = 85^{\circ}\text{C}$ (E/F Grades)	—	0.05	0.5	—	0.1	1	nA
		$T_A = 125^{\circ}\text{C}$ (A/B Grades)	—	1	5	—	2	10	nA
Input Resistance	R_{IN}		—	10^{12}	—	—	10^{12}	—	Ω
Input Capacitance	C_{IN}		—	8	—	—	8	—	pF
Input Voltage Range	IVR	$T_A = 25^{\circ}\text{C}$	± 11	± 11.5	—	± 11	± 11.5	—	V
		Over Temperature	± 10	± 11	—	± 10	± 11	—	
Common-Mode Rejection	CMR	$V_{CM} = \pm 11\text{V}$							
		$G = 1000$	110	115	—	100	110	—	dB
		$G = 100$	105	115	—	95	110	—	
		$G = 10$	100	110	—	90	100	—	
		$G = 1$	90	98	—	80	90	—	
		$V_{CM} = \pm 10\text{V}$, Over Temperature							
		$G = 1000$	105	110	—	95	105	—	dB
		$G = 100$	100	110	—	90	105	—	
		$G = 10$	95	105	—	85	95	—	
		$G = 1$	85	95	—	75	85	—	
OFFSET VOLTAGE									
Input Offset Voltage	V_{IOS}	$V_{CM} = 0\text{V}$	—	0.3	1.0	—	0.5	2.0	mV
		$T_A = 25^{\circ}\text{C}$ Over Temperature	—	0.8	2.0	—	1.0	4.0	
Input Offset Voltage Drift	TCV_{IOS}		—	5	10	—	7	20	$\mu\text{V}/^{\circ}\text{C}$
Output Offset Voltage	V_{OOS}	$T_A = 25^{\circ}\text{C}$	—	3	15	—	5	25	mV
		Over Temperature	—	9	25	—	11	40	
Output Offset Voltage Drift	TCV_{OOS}		—	50	100	—	70	150	$\mu\text{V}/^{\circ}\text{C}$
Offset Referred to Input vs. Positive Supply $V_+ = +5\text{V}$ to $+15\text{V}$	+PSR	$G = 1000$	115	120	—	110	115	—	dB
		$G = 100$	110	118	—	105	110	—	
		$G = 10$	95	105	—	90	100	—	
		$G = 1$	75	85	—	70	80	—	
		Over Temperature							
		$G = 1000$	110	116	—	105	110	—	dB
		$G = 100$	105	114	—	100	105	—	
		$G = 10$	90	102	—	85	98	—	
		$G = 1$	75	84	—	70	80	—	
		Over Temperature							
Offset Referred to Input vs. Negative Supply $V_- = -5\text{V}$ to -15V	-PSR	$G = 1000$	110	118	—	105	110	—	dB
		$G = 100$	95	104	—	90	98	—	
		$G = 10$	75	84	—	70	80	—	
		$G = 1$	55	64	—	50	60	—	
		Over Temperature							
		$G = 1000$	105	113	—	100	105	—	dB
		$G = 100$	95	104	—	90	95	—	
		$G = 10$	75	84	—	70	80	—	
		$G = 1$	55	64	—	50	60	—	

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	AMP-05A/E			AMP-05B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$	± 2.5	± 5	—	± 2.5	± 5	—	mV
Output Offset Voltage Trim Range		$V_S = \pm 4.5V$ to $\pm 18V$	± 25	± 40	—	± 25	± 40	—	mV
SENSE INPUT									
Input Resistance	R_{IN}		40	50	60	40	50	60	k Ω
Input Current	I_{IN}	Referenced to V-	—	280	—	—	280	—	μA
REFERENCE INPUT									
Input Resistance	R_{IN}		40	50	60	40	50	60	k Ω
Input Current	I_{IN}	Referenced to V-	—	280	—	—	280	—	μA
Voltage Range			-10.5	—	+20	-10.5	—	+20	V
Gain to Output			—	1	—	—	1	—	V/V
NOISE									
Voltage Density RTI	e_n	$f_0 = 1kHz$	—	16	—	—	16	—	$nV/\sqrt{Hz}$
		$G \geq 100$	—	38	—	—	38	—	
		$G = 10$	—	350	—	—	350	—	
		$G = 1$	—	350	—	—	350	—	
Noise Current Density	i_n	$f_0 = 1kHz$	—	10	—	—	10	—	$fA/\sqrt{Hz}$
Input Noise Voltage	e_{np-p}	Measured at $G = 1000$, 0.1Hz to 10Hz Bandwidth	—	4	—	—	4	—	μV_{p-p}
Output Noise Voltage	e_{np-p}	Measured at $G = 0$, 0.1Hz to 10Hz Bandwidth	—	7	—	—	7	—	μV_{p-p}
Input Noise Current	i_{np-p}	0.1Hz to 10Hz Bandwidth	—	0.12	—	—	0.12	—	pA_{p-p}
DYNAMIC RESPONSE									
Small Signal Bandwidth (-3dB)	BW	$G = 1$	—	3	—	—	3	—	MHz
		$G \geq 10$	—	120	—	—	120	—	kHz
Slew Rate	SR	$C_L = 500pF$	5	7.5	—	5	7.5	—	$V/\mu s$
		Over Temperature	3.5	5.5	—	3.5	5.5	—	
Settling Time	t_s	$1 \leq G \leq 2000$ -10V to +10V Step Note 1:	—	5	7	—	5	7	μs
		to 0.1%	—	7	10	—	7	10	
		to 0.05%	—	10	15	—	10	15	
		to 0.025%	—	10	15	—	10	15	
Overload Recovery Time	t_{rec}	$G = 1000$ $V_{IN} = 10V$ to $10mV$	—	15	—	—	15	—	μs

NOTE:

1. Guaranteed but not 100% production tested.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted. (Continued)

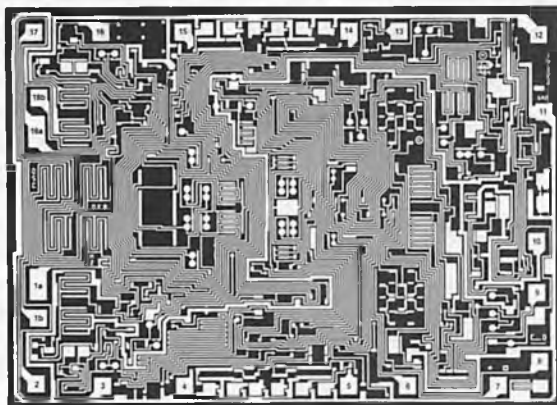
PARAMETER	SYMBOL	CONDITIONS	AMP-05A/E			AMP-05B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
GUARD DRIVERS									
Output Voltage	V _O	Volts above respective input over temperature.	0.5	1.2	2.0	0.5	1.2	2.0	V
Peak Output Current			8	15	—	8	15	—	mA
Slew Rate	SR	C _L = 1000pF	—	16	—	—	16	—	V/μs
Capacitive Load Stability		No Oscillations (Note 1)	10	100	—	10	100	—	nF
CURRENT SOURCE									
Current Output	I _{OUT}	Over Full Compliance Range	90	100	120	90	100	120	μA
Output Compliance Range		V _{OC} Volts Below V+ (Irrespective of V-)	4	—	30	4	—	30	V
Output Impedance	R _{OUT}	Over Full Compliance Range (Note 1)	1	3	—	1	3	—	GΩ
Temperature Coefficient			—	100	—	—	100	—	ppm/°C
Power Supply Rejection			—	150	—	—	150	—	nA/V
POWER SUPPLY -25°C ≤ T _A ≤ +85°C for E/F Grades, -55°C ≤ T _A ≤ +125°C for A/B Grades									
Supply Voltage Range	V _S		±4.5	—	±18	±4.5	—	±18	V
Quiescent Current	I _Q		—	7.0	9.0	—	7.5	10.0	mA

NOTE:

1. Guaranteed but not 100% production tested.



DICE CHARACTERISTICS



DIE SIZE 0.127 × 0.176 inch, 22,352 sq. mils
(3.23 × 4.47mm, 14.42 sq. mm)

- | | |
|----------------------|-----------------------|
| 1a. R_{GAIN} SENSE | 10. OUTPUT |
| 1b. R_{GAIN} FORCE | 11. V_- |
| 2. $-INPUT$ | 12. V_+ |
| 3. $-GUARD$ DRIVE | 13. CURRENT SOURCE |
| 4. V_{OOS} NULL | 14. V_{IOS} NULL |
| 5. V_{OOS} NULL | 15. V_{IOS} NULL |
| 6. R_{SCALE} | 16. $+GUARD$ DRIVE |
| 7. R_{SCALE} | 17. $+INPUT$ |
| 8. REFERENCE | 18a. R_{GAIN} SENSE |
| 9. SENSE | 18b. R_{GAIN} FORCE |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

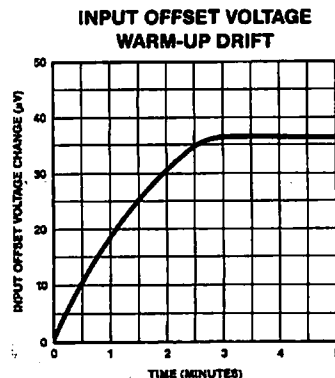
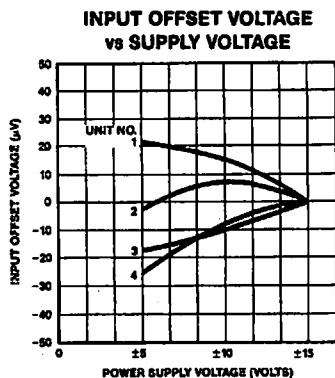
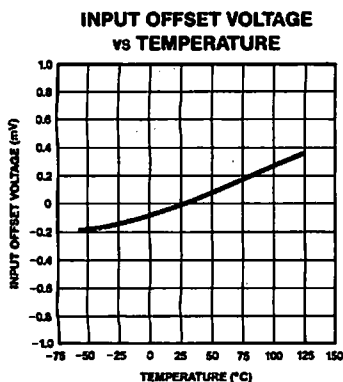
PARAMETER	SYMBOL	CONDITIONS	AMP-05GBC	
			LIMIT	UNITS
Input Offset Voltage	V_{IOS}	$V_{CM} = 0$	2.0	mV MAX
Output Offset Voltage	V_{OOS}		25	mV MAX
Offset Referred to Input vs. Positive Supply	PSR	$V_+ = +5V$ to $-15V$	110	dB MIN
		$G = 1000$	105	
		$G = 100$	90	
		$G = 10$	70	
		$G = 1$	70	
Offset Referred to Input vs. Negative Supply	PSR	$V_- = -5V$ to $-15V$	105	dB MIN
		$G = 1000$	90	
		$G = 100$	70	
		$G = 10$	50	
		$G = 1$	50	
Input Bias Current	I_B		100	pA MAX
Input Offset Current	I_{OS}		50	pA MAX
Input Voltage Range	IVR	Guaranteed by CMR Tests	± 11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$		dB MIN
		$G = 1000$	100	
		$G = 100$	95	
		$G = 10$	90	
		$G = 1$	80	
Gain Equation Accuracy		$G = 20 \times R_S/R_G$ $G = 1$ to 100	1.0	% MAX
Output Voltage Swing	V_{OUT}	$R_L = 1k\Omega$	± 11	V MIN
Output-Current Limit		Output-to-Ground Short	± 20	mA MIN
Current Source	I_{OUT}		90	μA MIN
			120	μA MAX
Quiescent Current	I_Q		± 10.0	mA MAX

NOTE:

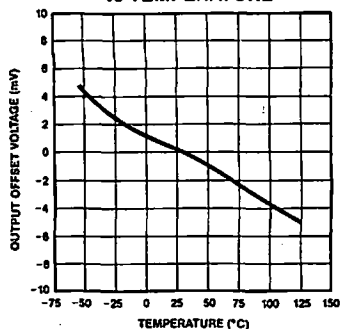
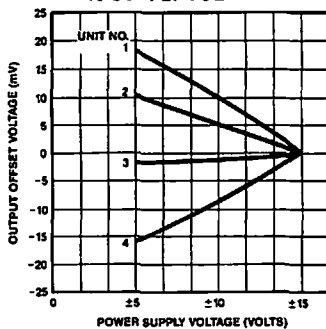
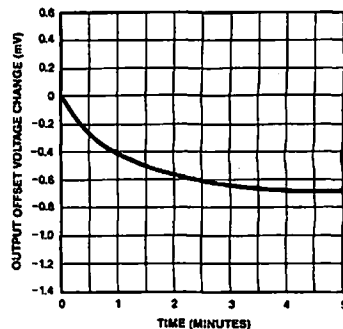
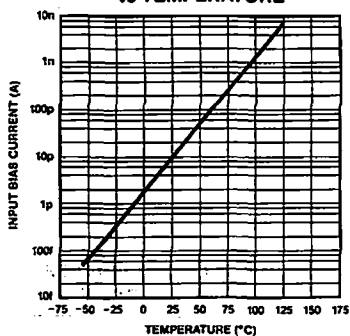
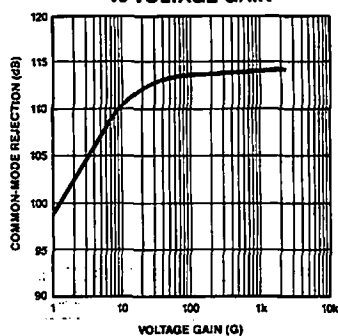
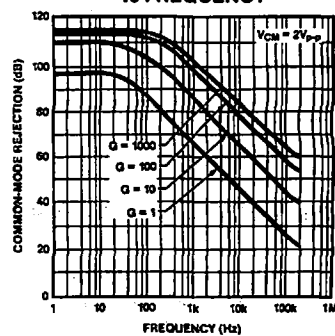
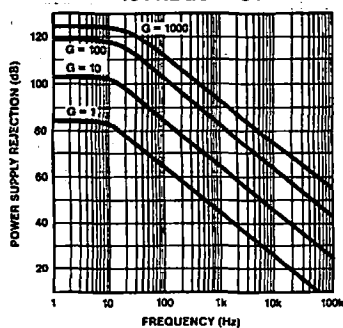
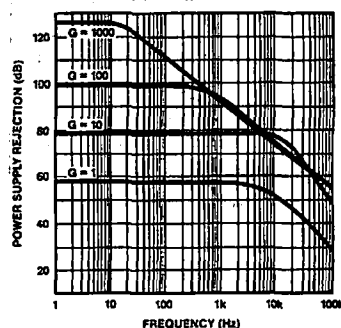
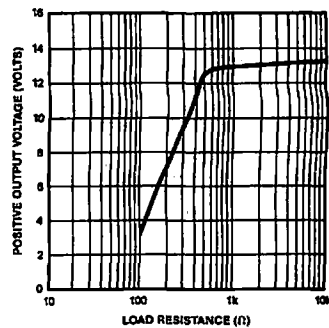
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $R_S = 5k\Omega$, $R_L = 2k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	AMP-05GBC TYPICAL	UNITS
Input Offset Voltage Drift	TCV_{IOS}		7	$\mu V/^\circ C$
Output Offset Voltage Drift	TCV_{OOS}	$R_G = \infty$	70	$\mu V/^\circ C$
Nonlinearity		$G = 1000$ $R_L = 10k\Omega$	0.004	%
Voltage Noise Density	e_n	$G = 1000$ $f_o = 1kHz$	16	$nV/\sqrt{Hz}$
Current Noise Density	i_n	$G = 1000$ $f_o = 1kHz$	10	$IA/\sqrt{Hz}$
Voltage Noise	e_{np-p}	$G = 1000$ 0.1Hz to 10Hz	4	μV_{p-p}
Current Noise	i_{np-p}	$G = 1000$ 0.1Hz to 10Hz	0.12	pA_{p-p}
Small-Signal Bandwidth (-3dB)	BW	$G = 1000$	120	kHz
Slew Rate	SR	$G = 10$	7.5	$V/\mu s$
Settling Time	t_s	To 0.025% -10V to +10V Step $1 \leq G \leq 2000$	10	μs
Overload Recovery Time	t_{rec}	$G = 1000$ $V_{IN} = 10V$ to 10mV	15	μs

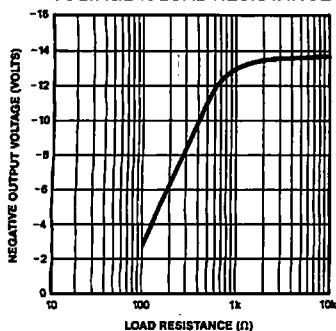
TYPICAL PERFORMANCE CHARACTERISTICS

TYPICAL PERFORMANCE CHARACTERISTICS

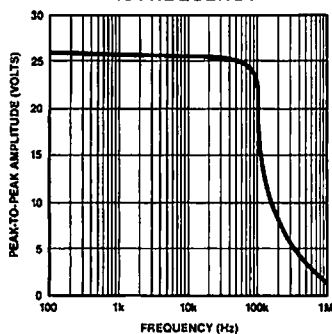
OUTPUT OFFSET VOLTAGE
vs TEMPERATURE

OUTPUT OFFSET VOLTAGE
vs SUPPLY VOLTAGE

OUTPUT OFFSET VOLTAGE
WARM-UP DRIFT

INPUT BIAS CURRENT
vs TEMPERATURE

COMMON-MODE REJECTION
vs VOLTAGE GAIN

COMMON-MODE REJECTION
vs FREQUENCY

POSITIVE PSR
vs FREQUENCY

NEGATIVE PSR
vs FREQUENCY

MAXIMUM POSITIVE OUTPUT
VOLTAGE vs LOAD RESISTANCE


TYPICAL PERFORMANCE CHARACTERISTICS

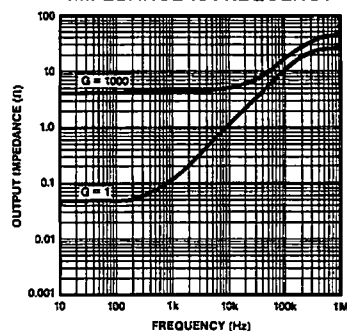
MAXIMUM NEGATIVE OUTPUT VOLTAGE vs LOAD RESISTANCE



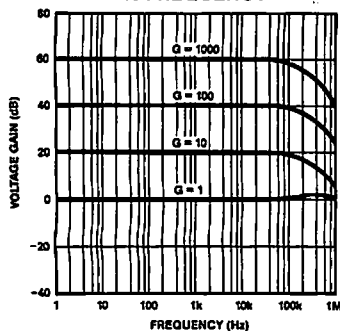
MAXIMUM OUTPUT SWING vs FREQUENCY



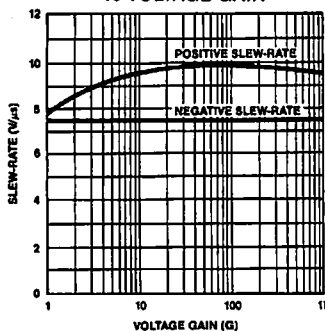
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



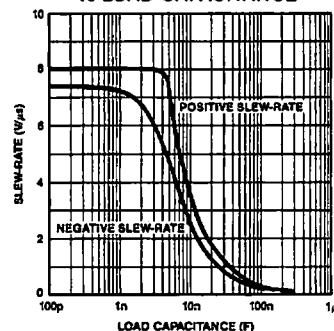
VOLTAGE GAIN vs FREQUENCY



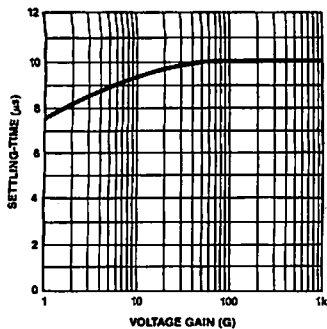
OUTPUT SLEW-RATE vs VOLTAGE GAIN



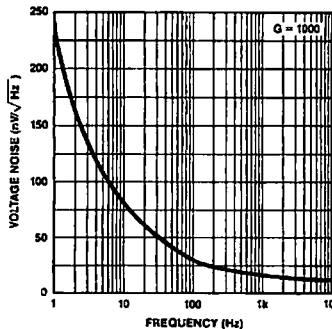
OUTPUT SLEW-RATE vs LOAD CAPACITANCE



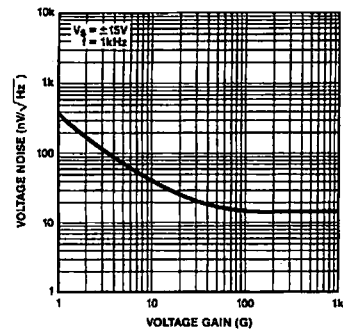
SETTLING-TIME TO 0.025% vs VOLTAGE GAIN



VOLTAGE NOISE DENSITY vs FREQUENCY



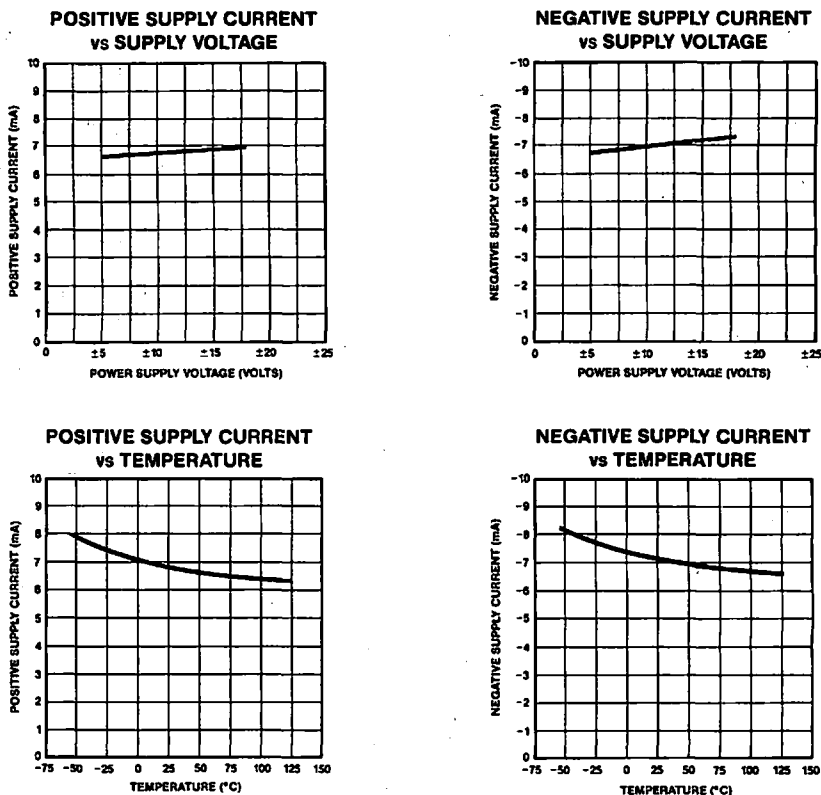
VOLTAGE NOISE DENSITY vs GAIN



6

INSTRUMENTATION AMPLIFIERS

TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

VOLTAGE GAIN

The AMP-05 uses two external resistors for setting voltage gain over the range 0.1 to 2000. The magnitudes of the scale resistor, R_S , and gain-set resistor, R_G , are related by the formula: $G = 20 \times R_S / R_G$, where G is the selected voltage gain. Figure 1 shows the amplifier connections. R_G can be selected using the graph in Figure 2.

Circuit performance is characterized using $R_S = 5k\Omega$ operating on ± 15 volt supplies and driving a ± 10 volt output.

Metal-film or wirewound resistors are recommended for R_S and R_G . The absolute resistance values and temperature coefficients of resistance are not too important; only the ratiometric parameters are important for gain accuracy and stability.

FIGURE 1: Basic AMP-05 Connections For Gains 0.1 to 2000

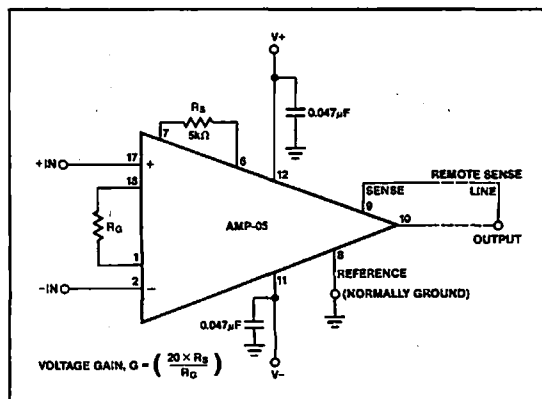
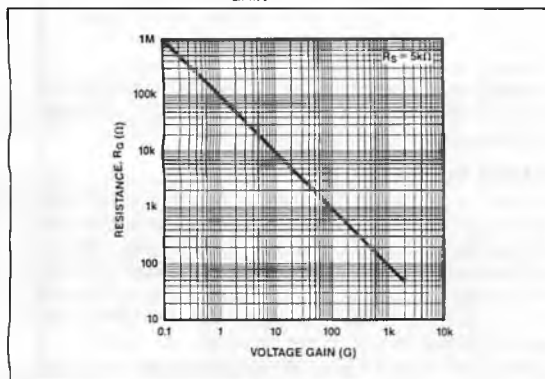


FIGURE 2: Selection of R_{GAIN} 

AC amplifiers require good gain stability with temperature and time, but DC performance is unimportant. Therefore, low cost metal-film types with TCs of 50ppm/°C are usually adequate for R_S and R_G . Realizing the full potential of the AMP-05's gain stability requires precision metal-film or wirewound resistors. Achieving a 25ppm/°C max. gain tempco at all gains will require R_S and R_G temperature coefficient matching to 5ppm/°C max.

Gain accuracy is determined by the ratio accuracy of R_S and R_G combined with the gain equation error of the AMP-05 (0.5% for A/E grades).

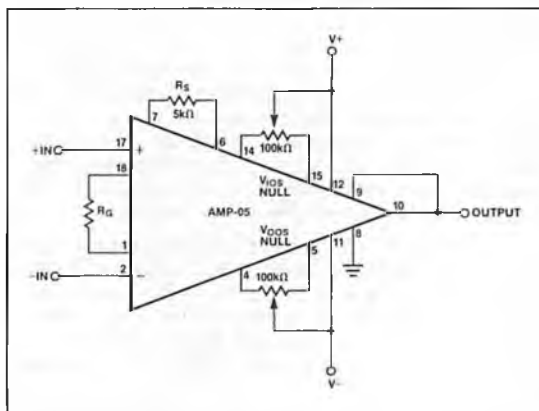
Note: The AMP-05 is inherently stable at all gains. However, like all amplifiers with a high gain-bandwidth product, instability can occur if layout precautions are not observed: (a) the amplifier should be decoupled close to the supply pins, and (b) the output must be kept well away from the inputs, the null pins, and R_{GAIN} .

The AMP-05 is capable of gain-bandwidth products in the hundreds of megahertz when operated at its highest gain settings. Under these conditions, even a few picofarads of stray feedback to the inputs can cause instability, and the situation is exacerbated if the input signal has a high source impedance. If instability does occur, the problem is easily eliminated by placing a small capacitor directly between the AMP-05's input pins, 2 and 17.

INPUT AND OUTPUT OFFSET VOLTAGES

Instrumentation amplifiers have independent offset voltages associated with the input and output stages. While the initial offsets may be adjusted to zero, temperature variations will cause shifts in offsets. Systems with auto-zero can correct for offset errors, so initial adjustment would be unnecessary. However, many high-gain applications do not have auto-zero. For these applications both offsets can be nulled. Nulling has minimal effect on TCV_{IOS} and TCV_{OOS} (refer to Figure 3 for connections).

FIGURE 3: Input and Output Offset Voltage Nulling



The input offset component is directly multiplied by the amplifier gain, whereas output offset is independent of gain. Therefore, at low gain, output offset errors dominate, while at high gain, input offset errors dominate. Overall offset voltage, V_{OS} , referred to the output (RTO) is calculated as follows:

$$V_{OS} (RTO) = (V_{IOS} \times G) + V_{OOS} \quad (1)$$

where V_{IOS} and V_{OOS} are the input and the output offset voltage specifications and G is the amplifier gain. Input offset nulling alone can be used for fixed gains above 50. Otherwise, both nulls are required. When nulling both initial offsets, the input offset is nulled first by short-circuiting R_G , then the output offset is nulled with the short removed.

The overall offset voltage drift, TCV_{OS} , referred to the output, is a combination of input and output drift specifications. Input offset voltage drift is multiplied by the amplifier gain, G , and summed with the output offset drift;

$$TCV_{OS} (RTO) = (TCV_{IOS} \times G) + TCV_{OOS} \quad (2)$$

where TCV_{IOS} is the input offset voltage drift, and TCV_{OOS} is the output offset voltage drift specification. Frequently, the amplifier drift is referred back to the input (RTI) which is then equivalent to an input signal change;

$$TCV_{OS} (RTI) = TCV_{IOS} + \frac{TCV_{OOS}}{G} \quad (3)$$

For example, the maximum input-referred drift of an AMP-05EX set to $G = 100$ becomes:

$$TCV_{OS} (RTI) = 10\mu V/^\circ C + \frac{100\mu V/^\circ C}{100} = 11\mu V/^\circ C \text{ max.}$$

INPUT BIAS AND OFFSET CURRENTS

Input bias currents are additional error sources which can degrade the input signal. Bias currents flowing through the signal source resistance appear as an additional offset voltage. Equal source resistance on both inputs of an instrumentation amplifier will minimize offset changes due to bias current variations with signal voltage and temperature. However, the difference between the two bias currents, the input offset current, produces a nontrimmable error. The magnitude of the error is the offset current times the source resistance.

The AMP-05 has FET inputs which have negligible bias and offset currents at room temperature and consequently can accurately measure signals from high source impedances. However, like all FET devices, the bias current doubles approximately every 10°C increase in junction temperature and therefore bias and offset currents must be carefully considered when operating up to +125°C.

Note: If very high source impedances (~1MΩ) are used and the AMP-05 is used at high gain, then it is recommended that a small capacitor is connected across the inputs to prevent instability.

A current path must always be provided between the differential inputs and analog ground to ensure correct amplifier operation. Floating inputs, such as thermocouples, should be grounded close to the signal source for best common-mode rejection.

OVERVOLTAGE PROTECTION

The AMP-05 features a unique internal protection circuit which permits differential input voltages of up to ±30V even when set for high gain operation. It should be noted however, that the output state during such an overload is not defined. Typically, at gains above 10, severe overloads (=1000% overrange) will cause the output to sit at about +10V with a low-level oscillation apparent.

Additionally, gross overdriving will cause input currents of up to 100μA to flow in the lower of the two inputs. The increased input current should be borne in mind if interfacing to extremely delicate transducers.

OVERLOAD RECOVERY TIME

Following an input overload, an amplifier takes a finite time to recover, i.e. the amplifier's output has to return to the linear operating region after limiting at one or other supply. The AMP-05 is designed to recover rapidly from input overloads; typically recovery time is 15μs following a 1000:1 overload; voltage gain set to 1000.

Rapid overload recovery is particularly important in a multiplexed data acquisition system using programmable gain. In this application, it is possible for the input to be switched to a high-level signal with gain set high, thus overloading the amplifier. To maintain system speed, it is vital for the amplifier to recover quickly once the overload is removed by reprogramming the gain.

COMMON-MODE REJECTION

Ideally, an instrumentation amplifier responds only to the difference between the two input signals and rejects common-mode voltages and noise. In practice, there is a small change in output voltage when both inputs experience the same common-mode voltage change; the ratio of these voltages is called the common-mode gain. Common-mode rejection (CMR) is the logarithm of the ratio of differential-mode gain to common-mode gain, expressed in dB. CMR specifications are normally measured with a full-range input voltage change and a specified source resistance unbalance.

The current-feedback design used in the AMP-05 inherently yields high common-mode rejection. Unlike resistive feedback designs typified by the three-op-amp IA, the CMR is not degraded by small resistances in series with the reference input. A slight, but trimmable, output offset voltage change results from resistance in series with the reference input.

The common-mode input voltage range, CMVR, for linear operation may be calculated from the formula:

$$\text{CMVR} = \pm \left(\text{IVR} - \frac{|V_{\text{OUT}}|}{2G} \right) \dots \dots \dots (4)$$

IVR is the data sheet specification for input voltage range; V_{OUT} is the maximum output signal; and G is the chosen voltage gain. For example, at 25°C, IVR is specified as ±11 volts minimum with ±15 volt supplies. Using a ±10 volt maximum swing output and substituting the figures in (4) simplifies the formula to:

$$\text{CMVR} = \pm \left(11 - \frac{5}{G} \right) \dots \dots \dots (5)$$

For all gains greater than or equal to 5, CMVR is ±10 volt minimum; at gains below 5, CMVR is reduced.

GUARD DRIVERS

Dual guard drivers are included to restore bandwidth, settling-time, and high frequency common-mode rejection (CMR) when shielded cable is used at the input. The guard drivers can handle large capacitive loads and transient currents, but they are not intended for large DC loads. The DC path to ground should be $30\text{k}\Omega$ or greater; lower values can upset the AMP-05's internal biasing circuits.

Shielded cable is often employed to minimize capacitively coupled noise pickup along the signal path from source to amplifier. When coaxial cable connects a transducer to the amplifier's input, the cable's capacitance interacts with the transducer's source impedance to form a low-pass filter. This filter function reduces the amplifier's bandwidth and degrades settling-time and CMR. The AMP-05's differential guard drivers act as an AC "bootstrap" when attached to the coaxial shields. In bootstrapping, each driver follows its corresponding input, and the driver output signals are buffered to handle large capacitive loads. Each driver will typically slew at $16\text{V}/\mu\text{s}$ with a 1000pF load. Bootstrapping reduces the effective input capacitance, since no AC voltage appears between the shield and inner conductor.

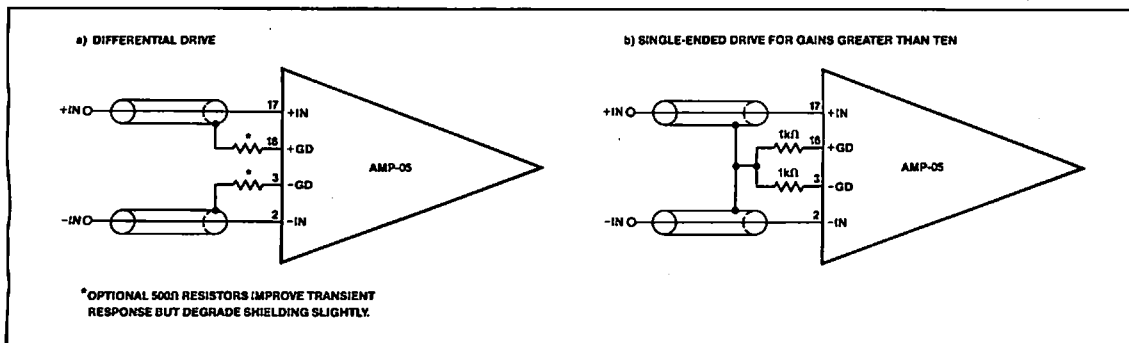
The AMP-05's guard drivers can form either a differential or single-ended drive (refer to Figures 4(a) and (b)). In the single-ended arrangement, the two input cable shields are held at the

same potential, the common-mode voltage (Figure 4(b)). As such, the connection is also appropriate for one shielded twisted-pair cable. The single-ended arrangement maintains a high CMR even at high frequencies, but does not reduce high frequency gain degradation as it does not counteract differential-mode capacitance. Single-ended drive is acceptable for gains greater than ten using the circuit in Figure 4(b). However the differential connection, Figure 4(a), offers better overall performance because it effectively reduces both differential and common-mode capacitance. Reduction in these capacitances improves high-frequency CMR, settling-time, and gain.

It should be noted that all shield drive arrangements are potentially positive feedback configurations and under some conditions high frequency ringing may occur. If this proves troublesome, small resistors (500Ω - $1\text{k}\Omega$) in series with the cable shield outputs will improve transient response and settling-time but reduce the effectiveness of the cable shield, particularly at high frequency.

Short circuits from the cable drives to ground will not damage the AMP-05 but will result in malfunction of the AMP-05 until the short is removed. The package pins adjacent to the two inputs, R_G connections and guard drives, sit within 2 volts of the input signals. This feature reduces leakage currents to the input terminals and eliminates the need for guard-rings which are necessary on many FET input amplifiers.

FIGURE 4: Applying the Guard Drivers to shield the inputs, guard driving reduces the effective input capacitance and improves CMR.



CURRENT SOURCE

The on-board $100\mu\text{A}$ current source is provided for transducer excitation, powering a low-current voltage reference diode, and other functions. The current source is referenced from the positive supply rail (V^+), and provides a high voltage compliance from 4 to $30V$ below V^+ . The output should not be pulled below V^- . Output resistance is typically $3G\Omega$. Simple positive and negative voltage references can be generated by adding two resistors and an inexpensive op amp (Figures 7(a) and (b)). Temperature stability can be improved by replacing $R1$ with a low-current zener or voltage reference diode such as the LM185. The output reference voltage can be increased beyond the zener voltage by adding resistor $R3$ to add gain around the OP-77.

If the current source is not used it may be left floating or connected to V^- .

FIGURE 7: Generating a Reference Voltage Using the On-Board Current-Source

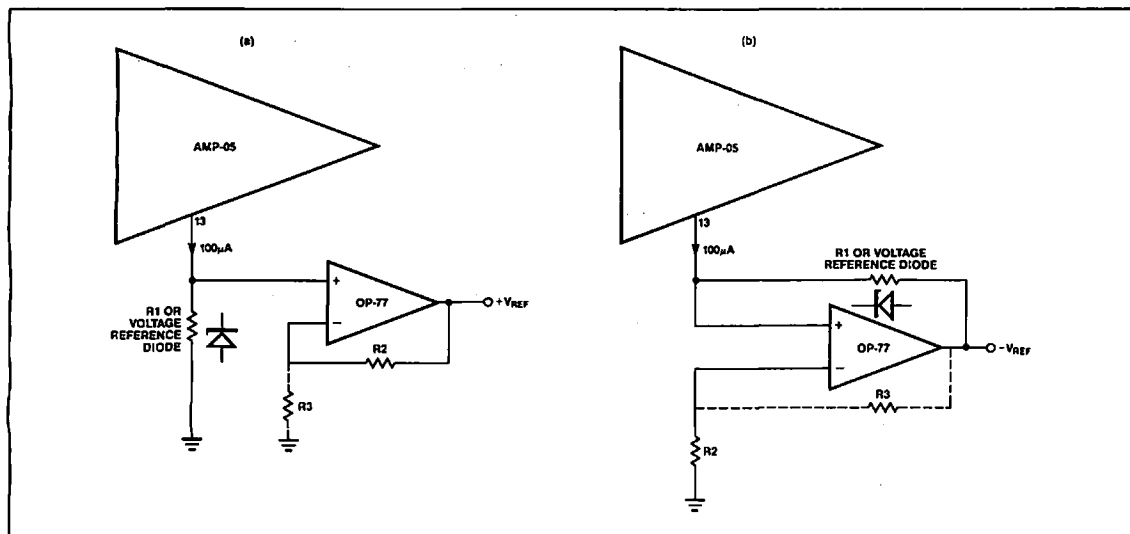
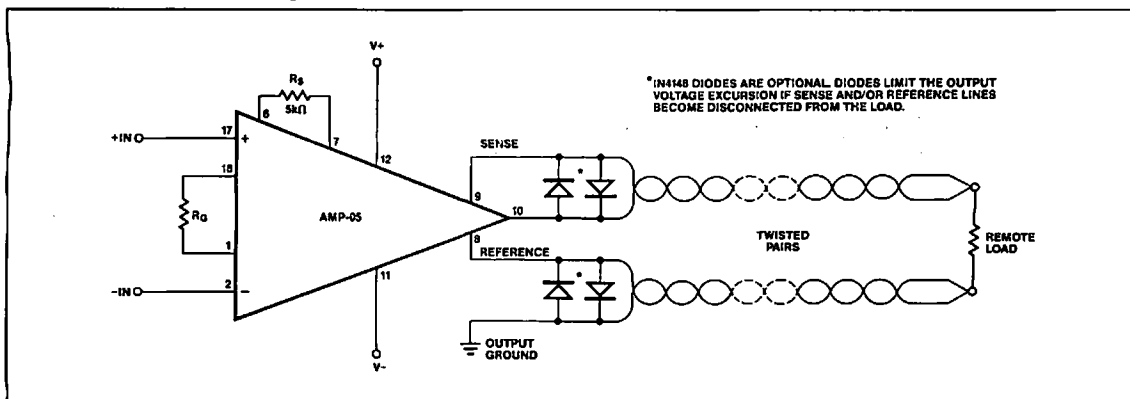


FIGURE 8: Remote Load Sensing



SENSE AND REFERENCE TERMINALS

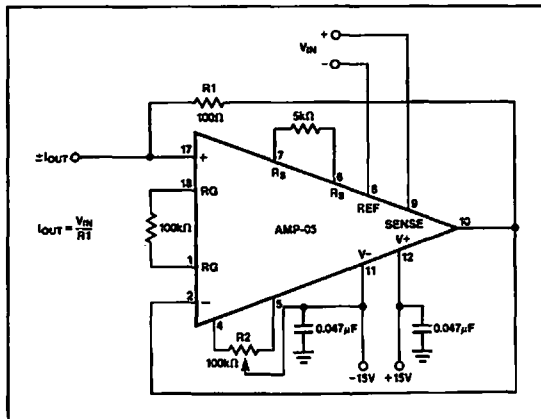
The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the output. The output signal is specified with respect to the reference terminal, which is normally connected to analog ground.

If high output currents are expected and/or the load is situated some distance from the amplifier, voltage drops due to trace or wire resistance will cause errors. Under these conditions, the sense and reference terminals can be used to "remote sense" the load as shown in Figure 8. This method of connection puts the $I \times R$ drops inside the feedback loop and virtually eliminates the error. An unbalance in the lead resistances from the sense and reference pins does not degrade CMR, but will change the output offset voltage. For example, a large unbalance of 3Ω will change the output offset by only $1mV$.

HIGH-COMPLIANCE CURRENT SOURCE

The inputs and outputs of the AMP-05 can be transposed to make a precision bipolar current source (refer to Figure 9). Reference and sense pins become differential inputs and the "old" input now monitors the voltage across a precision

FIGURE 9: High-Compliance Current Source With 16-Bit Linearity



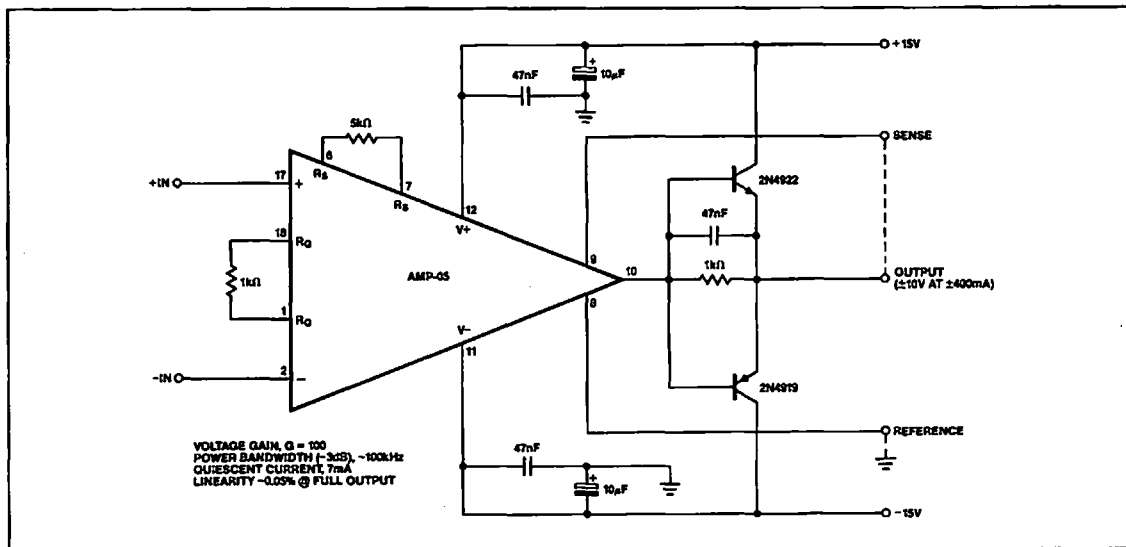
current-sense resistor, R1. Voltage gain is set at unity, so the transfer function is simply $I_{OUT} = V_{IN(differential)}/R1$. Using a 100 Ω resistor for R1 and limiting output current to ± 10 mA, a reasonable limit for power dissipation reasons, gives a ± 1 V input requirement for full-scale output. Voltage compliance for ± 10 mA output is ± 10 V with a typical output resistance of 50M Ω . Linearity is better than 16-bits at this current level. Potentiometer R2 will trim the output current to zero with the two inputs grounded, and fine gain adjustment is accomplished by trimming R3 or R4.

If the class B output stage shown in Figure 10 is added to the basic current-source, then the output current capability is increased to over 100mA with excellent linearity.

SERVO AMPLIFIER

The AMP-05's output power can be boosted by adding a simple class B output stage without increasing the amplifier's quiescent current of 7mA (refer to Figure 10). The 47nF capacitor connected across the transistor's base-emitter junctions prevents instability at V_{OUT} near ground, and reduces high-frequency crossover distortion. DC linearity is typically 0.05% when driving ± 10 V at ± 400 mA.

FIGURE 10: Adding two transistors increases output current to ± 400 mA without affecting the quiescent current of 7mA. Power bandwidth is 100kHz.



ANALOG-MULTIPLEXED DATA ACQUISITION SYSTEMS

For conditioning and digitizing multiple analog signals, there are two traditional system approaches. One dedicates an instrumentation amplifier to condition each input signal, then the high-level outputs are multiplexed and fed to an analog-to-digital converter (ADC). This system is expensive on a "per-channel" basis. A more economical approach is to multiplex unconditioned analog signals and feed them to a programmable-gain instrumentation amplifier, which conditions them before conversion. The per-channel cost drops as the number of channels increases. For this system to have a scan rate comparable to the first, the amplifier's settling-time should be less than the ADC's conversion time. The AMP-05, with its fast settling-time of 15 μ s maximum to 12 bits, is ideal for this single IA data acquisition system.

A digitally-controlled gain network can easily be added to the AMP-05 as described below.

PROGRAMMABLE-GAIN INSTRUMENTATION AMPLIFIER (PGIA)

Figure 11 shows a programmable gain instrumentation amplifier with digitally selectable gains of 1, 10, 100, and 1000. Each gain set resistor has two MOSFET switches connected back-to-back to prevent all but leakage current from flowing when a switch is OFF. In the high gain positions of 100 and 1000, the calculated values of gain resistor, R_G , are reduced to compensate for the switch ON resistance. The nonlinear switch resistance introduces a slight gain nonlinearity at high gain settings. The PGIA

selects gain values in 20 μ s, including the amplifier settling-time. Gain temperature coefficient depends on R_S , R_G , and on the temperature coefficient of the MOSFET's ON resistance. Values of 15 and 30ppm/ $^{\circ}$ C can be achieved at gains of 1 and 1000, respectively, despite the effect of the high tempco switches.

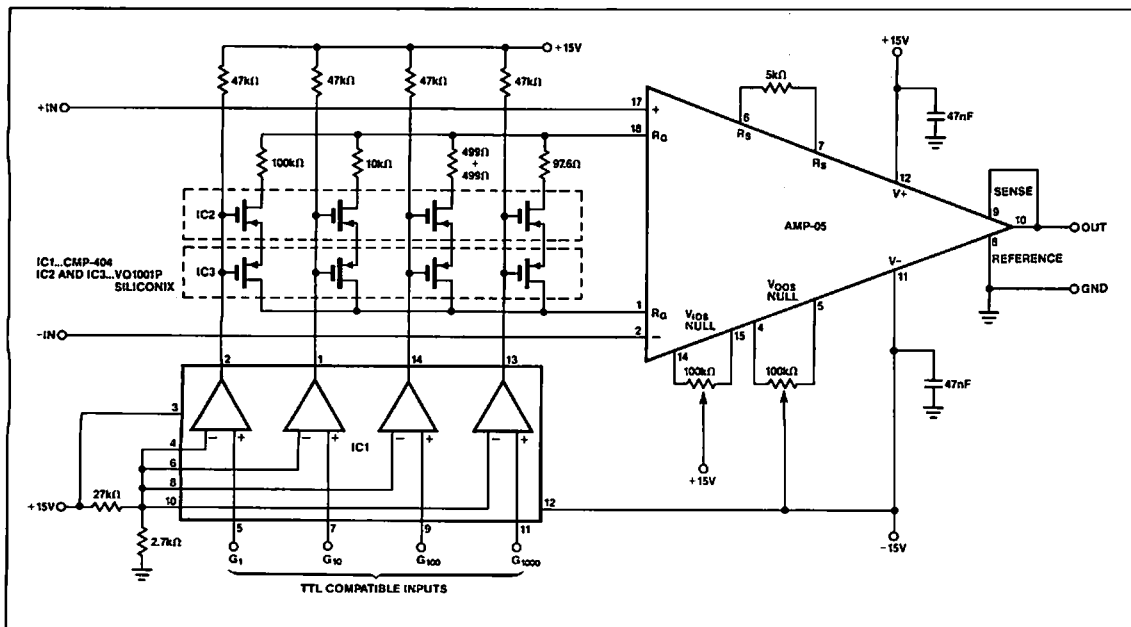
Where fast gain switching is not required, reed relays can substitute for the MOSFET switches. Reed relays have lower ON resistance and OFF leakage current errors. For gains of 100 and 1000, the values of R_G should be increased to 1k Ω and 100 Ω respectively, because of lower switch ON resistance. Gain linearity is improved over the original circuit.

AUTO-ZERO SYSTEMS

Offset voltage and drift can be a major error source in high-accuracy systems of 12 bits and above. To minimize initial offset voltage and its associated temperature drift, an auto-zero system can be employed. The technique can potentially keep offset errors well below 1 LSB on a 12-bit system over wide variations in ambient temperature.

For example, consider an instrumentation amplifier set to a gain of 1000 and driving a 12-bit analog-to-digital converter. The input offset voltage drift is 2.5 μ V/ $^{\circ}$ C, and the output offset voltage drift is negligible. The equivalent output drift is $1000 \times 2.5\mu\text{V}/^{\circ}\text{C}$, or 2.5mV/ $^{\circ}$ C—more than 1 LSB/ $^{\circ}$ C for a 10V full-scale range. An ambient temperature change from 25 $^{\circ}$ C to 125 $^{\circ}$ C would produce 102 LSBs of drift, excluding the ADC's drift.

FIGURE 11: The AMP-05 makes an excellent programmable-gain instrumentation amplifier. Combined gain-switching and settling-time to 12 bits falls below 20 μ s. Linearity is better than 12 bits over a gain range 1 to 1000.

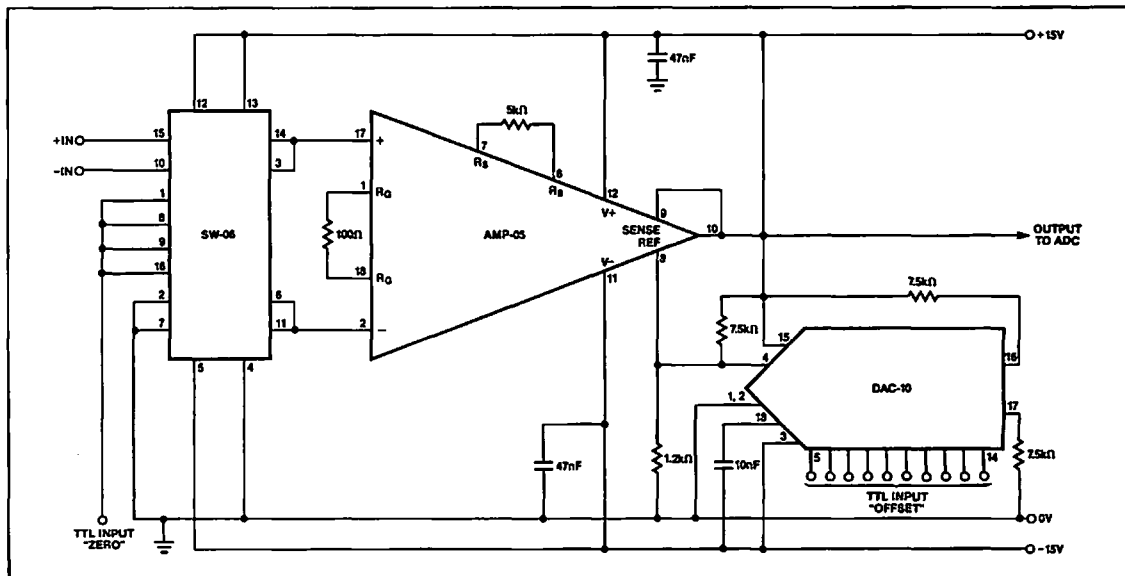


Obviously, to limit drift to 1 LSB or less over temperature demands some means of offset correction. Usually both hardware and software are employed to generate an error correction signal which is fed into the reference input of the instrumentation amplifier. Software alone could remove the system's offset error, but at the expense of the full-scale range for very large errors. Part of a typical auto-zero system is shown in Figure 12.

The sequence of events for auto-zeroing a system starts with switching the multiplexer so that the amplifier's two inputs are grounded. The amplifier is given time to settle, and the ADC (not shown) digitizes any system offset. The computer reads the offset and feeds a digital correction to the digital-to-analog converter. To verify that the offset is nulled, a second conversion may be performed, and the multiplexer then switches to measure the input signal.

For a system with a digitally programmable gain, the auto-zeroing process should be repeated for each gain setting. Each correction value can be stored in memory and recalled and refreshed as needed to correct for system drift with time and temperature.

FIGURE 12: Instrumentation Amplifier with Offset Correction System



SETTLING-TIME MEASUREMENT

Figure 13 is the test circuit used to measure settling-time. The circuit technique is similar to the "false sum-node" technique used to measure op amp settling-time. For simplicity, the connections for input and output offset nulling are not shown on the circuit, but null pots are required. Measurement set-up:

1. Set switches to $G = 1$, ground V_{IN} , and short-circuit R_G .
2. Adjust V_{IO} null pot for minimum output voltage on pin 10.
3. Remove short-circuit from R_G and adjust V_{OO} null pot for minimum output voltage on pin 10.
4. Apply a low frequency ($\sim 100\text{Hz}$) $20V_{p-p}$ square-wave to V_{IN} and adjust 200Ω pot for minimum square-wave on V_{OUT} .
5. Increase square-wave input frequency and monitor V_{OUT} with an oscilloscope. Settling-time to a 0.025% error band for a $20V$ input step is measured with limits of $\pm 2.5mV$ at V_{OUT} .
6. Change switch gain-positions and repeat settling-time measurements for $G = 10, 100$, and 1000 .

FIGURE 13: Settling-Time Test Circuit

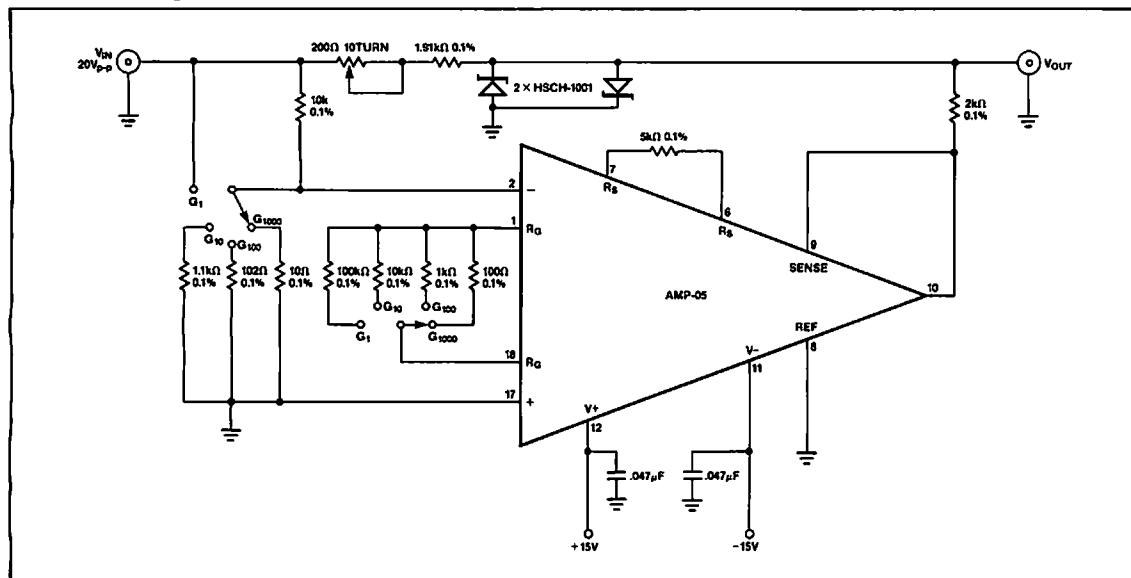


FIGURE 14: Burn-In Circuit

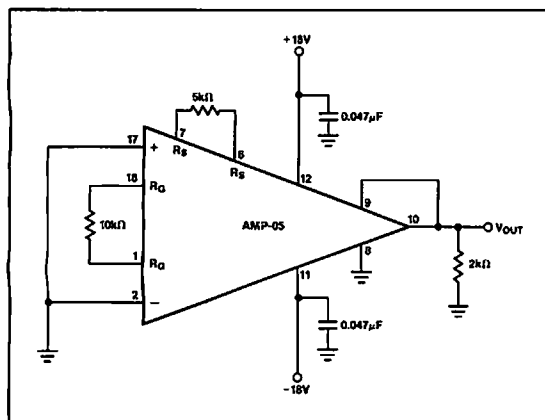


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VOLTAGE FOLLOWERS/BUFFERS

Precision Monolithics Inc.

Introduction 7-3

BUF-03

High-Speed Voltage Follower/Buffer 7-4



Precision Monolithics Inc.

VOLTAGE FOLLOWERS/BUFFERS

INTRODUCTION

The function of a unity-gain buffer is to accurately reproduce the input signal under widely-varying load conditions. To do this, buffers must have high input impedance, wide bandwidth, and high output drive. Offsets and gain error need to be minimized.

The buffer function can be implemented by use of general-purpose operational amplifiers connected as unity-gain voltage followers, but *higher performance* can be obtained by optimizing a circuit specifically for buffering. A design dedicated to unity-gain buffering and using no

feedback can provide better frequency response. In addition, output current can be increased substantially beyond that of conventional IC operational amplifiers.

The BUF-03 is a high-speed, unity-gain IC that is optimized for the buffer function. A FET input provides high input impedance. On-chip zener-zap trimming is used to reduce the offset voltage. The output stage is designed to supply approximately 70mA of peak current. These features combine to make the BUF-03 an IC analog buffer of unique capability.



BUF-03

HIGH-SPEED VOLTAGE FOLLOWER/BUFFER

Precision Monolithics Inc.

FEATURES

- Very High Slew Rate 220V/ μ s Min
- Wide Bandwidth 63MHz
- Load Drive Current 70mA Peak
- Easily Drives Large Capacitive Loads Without Oscillation
- High Input Resistance $5 \times 10^{11}\Omega$
- Low Output Resistance 2 Ω
- Very Low Bias Current (Warmed-Up) 400pA Max
- Low Offset Voltage 6mV Max
- Unity Gain 0.997V/V
- Excellent Gain Linearity 0.015%

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	OPERATING TEMPERATURE RANGE
6	BUF03AJ*	MIL
6	BUF03EJ	COM
15	BUF03BJ*	MIL
15	BUF03FJ	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

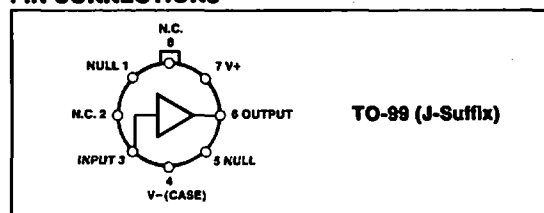
GENERAL DESCRIPTION

The BUF-03 is the first very high-speed monolithic voltage follower. Featuring performance previously unobtainable in a monolithic unit, it offers a combination of both exceptional speed and excellent input/output specifications. Implemented

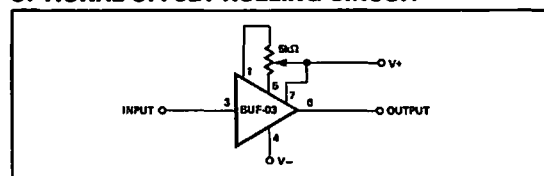
in an open-loop circuit employing source followers and emitter followers, the BUF-03 utilizes a quasi-quad FET input structure to optimize both speed and D.C. input characteristics. On-chip zener-zap trimming is used to achieve low offset voltage while careful biasing throughout results in excellent gain linearity over the full input voltage range.

Applications for which the BUF-03 is well-suited include high-speed line drivers, isolation amplifiers for driving reactive loads, and high-speed sample-hold circuits.

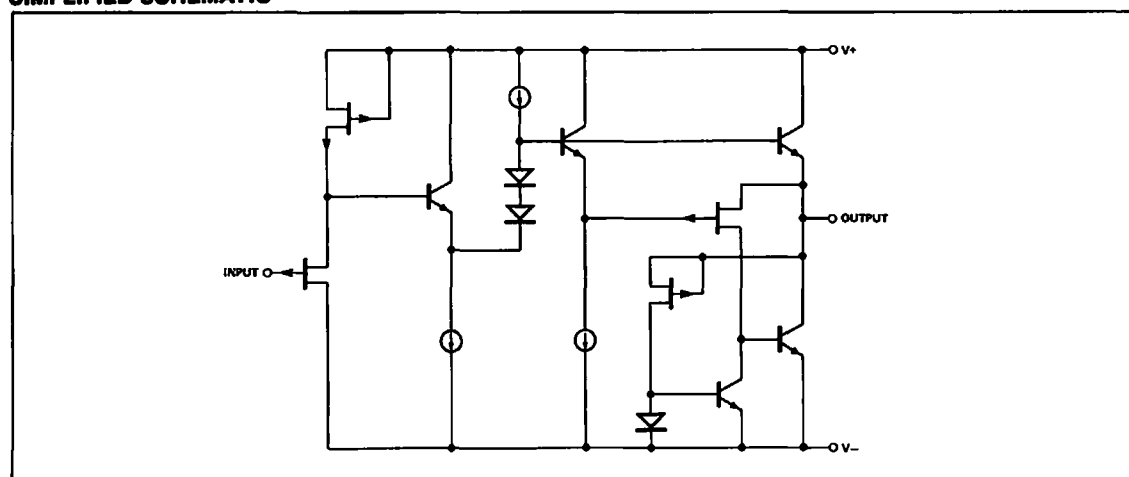
PIN CONNECTIONS



OPTIONAL OFFSET NULLING CIRCUIT



SIMPLIFIED SCHEMATIC




ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (P_d)	In Still Air Without Heat Sink (Note 1) 1.00W
Input Voltage (Note 2)	±18V
Continuous Output Current (Note 3)	70mA
Peak Output Current (Note 3)	100mA
Short Circuit Protection (Note 3)	Indefinite (Note 4)
Maximum Junction Temperature (T_j)	175°C
Storage Temperature Range	-65°C to +175°C
Operating Temperature Range (Note 5)	-55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

Dice Junction Temperature (T_j)	-65°C to +175°C
Thermal Resistance θ_{JA} (Note 1)	150°C/W
Thermal Resistance θ_{JC} (Note 1)	40°C/W

NOTES:

- Based on MIL-STD-38510 published thermal resistance specification for 8 lead can-case outline C.
- When $V_{CC} \leq \pm 18V$, the maximum input voltage is equal to the supply voltage.
- The maximum P_d or T_j are not to be exceeded.
- At 80mA.
- When operating at $T_A > +25^\circ\text{C}$, heat sinking is required to insure $T_{jMAX} = +175^\circ\text{C}$ specification is not exceeded using the equation $T_{jMAX} = T_A + (P_d \times \theta_{JA})$ where θ_{JA} = sink to ambient thermal resistance. PMI recommends using either the Thermalloy 2227 or 1101 or equivalent when operating up to $T_A = +125^\circ\text{C}$.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $R_S = 0\Omega$, $T_A = T_j = 25^\circ\text{C}$, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	BUF-03A/E			BUF-03B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC SPECIFICATIONS									
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$, $T_A = T_J = 75^\circ C$	220	250	—	180	250	—	V/ μs
Power Bandwidth	PBW	$V_{IN} = 10V_{P-P}$, $R_L \geq 2k\Omega$	—	9	—	—	8	—	MHz
Bandwidth	BW	$\Delta V_{IN} = \leq 2V_{P-P}$	—	63	—	—	50	—	MHz
Settling Time	t_S	To 0.1%, $\pm 10V$ step	—	90	—	—	100	—	ns
Capacitive Load Capability	C_{LOAD}	No Oscillations	—	1	—	—	1	—	μF
Propagation Delay	t_d	Step Input	—	7	—	—	7	—	ns
Rise Time	t_r	$\Delta V = 0.5V$	—	7	—	—	7	—	ns
Wide Band Input Noise Voltage	V_n	DC to 50MHz	—	350	—	—	400	—	μV_{RMS}
Input Noise Voltage Density	e_n	$f = 10kHz$	—	50	—	—	60	—	nV/ $\sqrt{Hz}$
DC SPECIFICATIONS									
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$ (Note 2)	—	2	6	—	4	15	mV
Input Bias Current	I_B		—	150	400	—	180	700	pA
Input Resistance	R_{IN}		—	5×10^{11}	—	—	4×10^{11}	—	Ω
Voltage Gain ($V_{IN} = \pm 10V$)	A_{VO}	$R_L \geq 10k\Omega$	0.9960	0.9975	—	0.9940	0.9970	—	V/V
		$R_L \geq 2k\Omega$	0.9945	0.9960	—	0.9930	0.9950	—	
		$R_L \geq 1k\Omega$	0.9925	0.9945	—	0.9905	0.9930	—	
Nonlinearity (Note 2)	NL	$V_{IN} = \pm 10V$, $R_L \geq 2k\Omega$	—	0.015	0.023	—	0.017	0.03	%F.S.
		$V_{IN} = \pm 7V$, $R_L \geq 1k\Omega$ (Note 3)	—	0.013	0.023	—	0.015	0.03	
Maximum Output Error	OUT_{error}	$V_{IN} = +10V, 0V, -10V$ $R_S = 0$ to $20k\Omega$ (Note 2) $R_L \geq 2k\Omega$ in all combinations	—	40	60	—	50	85	mV
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6V$ to $\pm 18V$	—	0.10	0.71	—	0.15	1.42	mV/V
Supply Current	I_{SY}	No Load	—	19	25	—	19	25	mA
Peak Load Current	$I_{L(PK)}$		—	70	—	—	70	—	mA
Output Resistance	R_O		—	2	—	—	2	—	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	—	± 80	—	—	± 80	—	mV
Input Voltage Range (Reduced Accuracy)	IVR		—	± 11.5	—	—	± 11.5	—	V

NOTES:

- Electrical parameters are pulse tested on automated test equipment. Total test time at each temperature is limited to less than one second maximum to keep T_j approximately equal to T_A .
- Parameters specified with $R_S \leq 20k\Omega$ are tested at $R_S = 0\Omega$. Limits in test program are adjusted to take into account worst case voltage offset induced by $R_S = 20k\Omega$, i.e., $I_B \text{ max} \times 20k\Omega$.
- Nonlinearity is computed using linear regression techniques with data from five points (e.g., -10V, -5V, 0V, +5V, +10V for $\pm 10V$ full-scale linearity; -7V, -3.5V, 0V, +3.5V, and +7V for $\pm 7V$ full-scale linearity).

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$, $T_A = T_j$, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	BUF-03A			BUF-03B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	—	220	—	—	220	—	$V/\mu s$
Input Offset Voltage	V_{OS}	$R_S \leq 2k\Omega$	—	6	20	—	10	35	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 2k\Omega$, (Note 2)	—	50	100	—	90	170	$\mu V/^\circ C$
Input Bias Current	I_B	$T_A = +125^\circ C$	—	25	75	—	30	90	nA
Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_{IN} = \pm 10V$	0.9920	0.9955	—	0.9902	0.9942	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	$ppm/^\circ C$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.15	1.26	—	0.20	2.24	mV/V
Supply Current	I_{SY}	$T_A = +125^\circ C$	—	18	24	—	18	24	mA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$, $T_A = T_j$, unless otherwise noted.

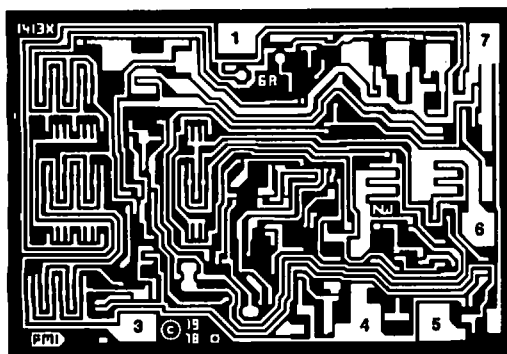
PARAMETER	SYMBOL	CONDITIONS	BUF-03E			BUF-03F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slew Rate	SR	$R_L \geq 2k\Omega$	—	240	—	—	240	—	$V/\mu s$
Input Offset Voltage	V_{OS}	$R_S \leq 2k\Omega$, $C_L = 50pF$	—	4	14	—	7	28	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S \leq 2k\Omega$, (Note 2)	—	40	90	—	80	150	$\mu V/^\circ C$
Input Bias Current	I_B	$T_A = +70^\circ C$	—	1.5	5	—	1.8	8	nA
Voltage Gain ($V_{IN} = \pm 10V$)	A_{VO}	$R_L \geq 2k\Omega$	0.9935	0.9958	—	0.9918	0.9946	—	V/V
Gain Drift with Temperature			—	5	—	—	8	—	$ppm/^\circ C$
Power Supply Rejection Ratio	PSRR	$V_S = \pm 7V$ to $\pm 15V$	—	0.12	1	—	0.16	1.78	mV/V
Supply Current	I_{SY}	$T_A = +70^\circ C$	—	19	25	—	19	25	mA

NOTES:

- In order to operate the device at an ambient temperature of $+125^\circ C$, more extensive heat sinking must be used to ensure that the chip temperature never exceeds the absolute maximum of $+175^\circ C$. The chip temperature of $+165^\circ C$ is achieved by reducing the case-to-ambient thermal resistance to $30^\circ C/W$ (e.g., Thermalloy 2227).
- Guaranteed by design.



DICE CHARACTERISTICS



DIE SIZE 0.071×0.049 inch, 3478 sq. mils
(1.80×1.24 mm, 2.23 sq. mm)

1. NULL
3. INPUT
4. NEGATIVE SUPPLY
5. NULL
6. OUTPUT
7. POSITIVE SUPPLY

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_J = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-03N LIMIT	BUF-03G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 20k\Omega$	6	15	mV MAX
Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_{IN} = \pm 10V$	0.9960	0.9940	V/V MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 6V$ to $\pm 18V$	0.71	1.42	mV/V MAX
Supply Current	I_{SY}	No Load	25	25	mA MAX

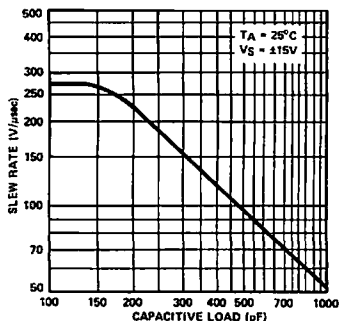
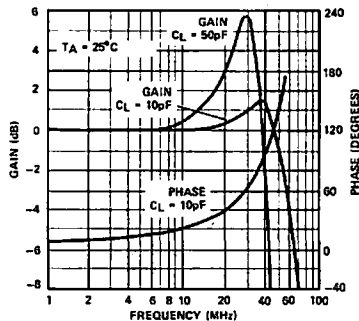
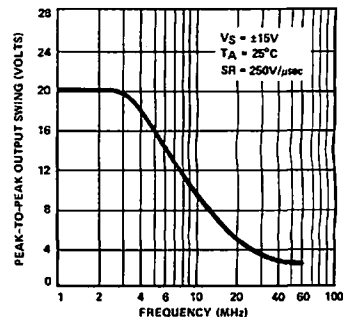
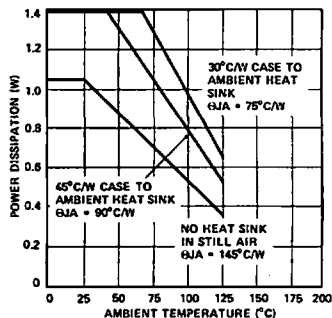
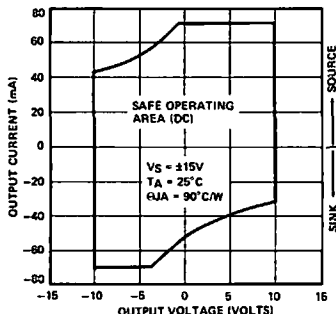
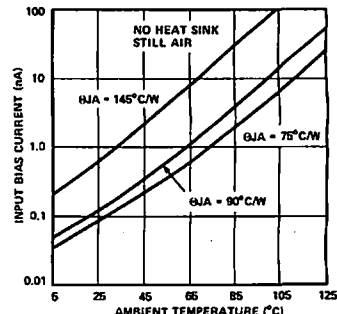
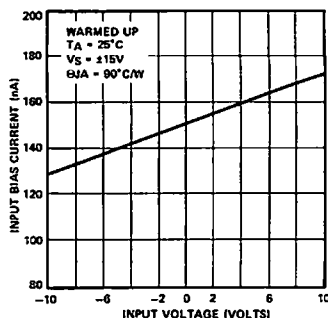
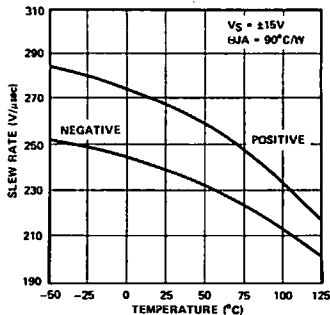
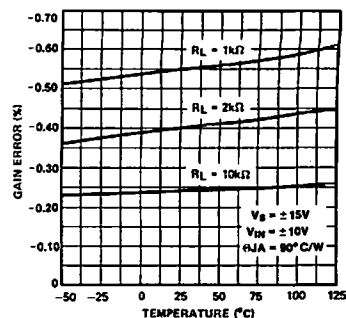
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

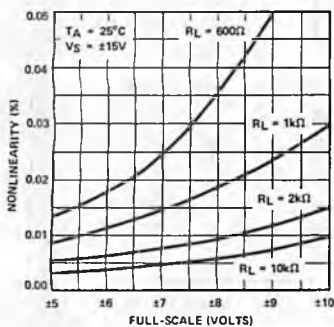
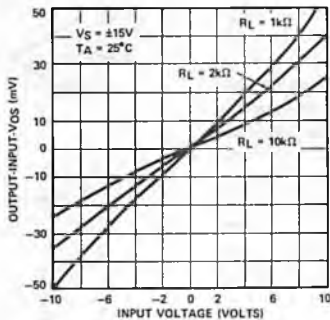
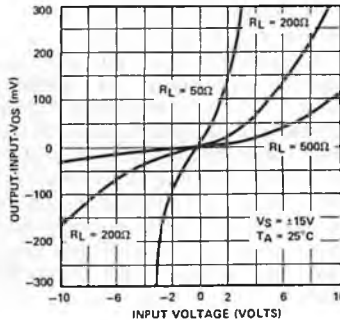
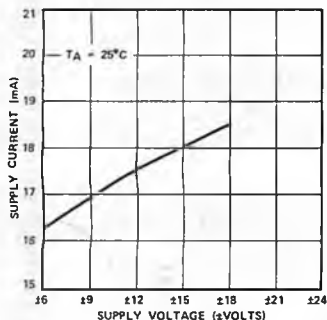
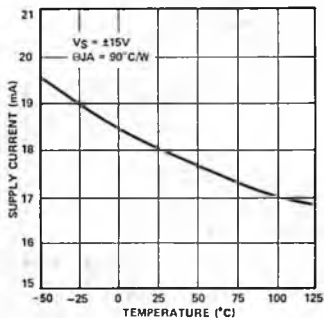
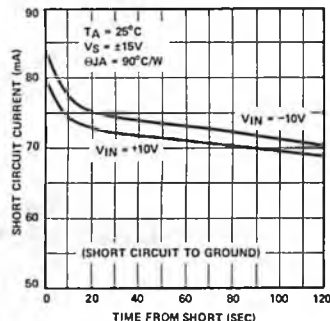
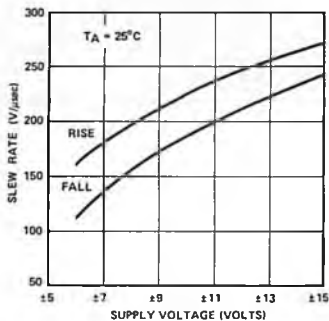
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_J = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	BUF-03N TYPICAL	BUF-03G TYPICAL	UNITS
Slew Rate	SR	$R_L \geq 2k\Omega$, $C_L = 50pF$	220	180	V/ μs
Peak Load Current	$I_L(PK)$		70	70	mA
Input Bias Current	I_B		40	60	pA
Input Resistance	R_{IN}		5×10^{11}	5×10^{11}	Ω
Output Resistance	R_O		2	2	Ω
Offset Voltage Nulling Range	ΔV_{OS}	$R_P \geq 1k\Omega$	± 80	± 80	mV
Input Voltage Range (Reduced Accuracy)	IVR		± 11.5	± 11.5	V
Power Bandwidth	PBW	$V_{IN} = 10V_{P-P}$, $R_L \geq 2k\Omega$	9	8	MHz
Bandwidth	BW	$\Delta V_{IN} \leq 2V_{P-P}$	63	55	MHz
Settling Time	t_S	To 0.1%, $\pm 10V$ step	90	100	ns
Capacitive Load Capacity	C_{LOAD}	No Oscillations	1	1	μF
Propagation Delay	t_d	Step Input	7	7	ns
Rise Time	t_r	$\Delta V_{IN} = 0.5V$	7	7	ns
Wide Band Input Noise Voltage	V_n	DC to 50MHz	350	400	μV_{RMS}
Input Noise Voltage Density	e_n	$f = 10kHz$	50	60	nV/ $\sqrt{Hz}$

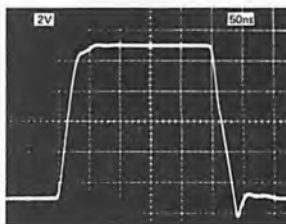
TYPICAL PERFORMANCE CHARACTERISTICS

 SLEW RATE vs
CAPACITIVE LOAD

 GAIN AND PHASE RESPONSE
vs FREQUENCY

 LARGE-SIGNAL
FREQUENCY RESPONSE

 MAXIMUM POWER
DISSIPATION vs
AMBIENT TEMPERATURE

 OUTPUT CURRENT
vs OUTPUT VOLTAGE

 INPUT BIAS CURRENT vs
TEMPERATURE (WARMED-UP)

 INPUT BIAS CURRENT
vs INPUT VOLTAGE

 SLEW RATE
vs TEMPERATURE

 GAIN ERROR
vs TEMPERATURE


TYPICAL PERFORMANCE CHARACTERISTICS

 NONLINEARITY vs
FULL-SCALE VOLTAGE

 GAIN ERROR vs
INPUT VOLTAGE

 GAIN ERROR vs
INPUT VOLTAGE

 SUPPLY CURRENT
vs SUPPLY VOLTAGE

 SUPPLY CURRENT
vs TEMPERATURE

 OUTPUT SHORT-CIRCUIT
CURRENT vs TIME

 SLEW RATE vs
SUPPLY VOLTAGE


SLEW RATE

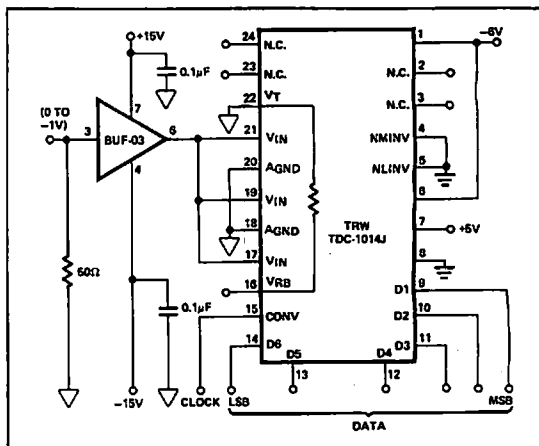


APPLICATIONS INFORMATION

OPERATING THE BUF-03 AT REDUCED POWER SUPPLIES

In most video applications the signal levels are significantly lower than the 20V peak-to-peak capability of the BUF-03. This suggests operating the BUF-03 at reduced power supplies; for example, at $\pm 6\text{V}$ supplies $\pm 2\text{V}$ signals can be handled. The obvious advantage of reduced supplies is the accompanying decrease in power dissipation: from a typical 540mW ($= 30\text{V} \times 18\text{mA}$) to 195mW ($= 12\text{V} \times 16.2\text{mA}$) at $\pm 6\text{V}$. At lower supply voltages heat sinking is no longer necessary. However, as shown on the slew rate vs supply voltage curve, slew rate does degrade at lower supplies. This occurs because of higher internal node capacitances at lower voltages and because of the slightly decreased operating current.

HIGH-SPEED 6-BIT A/D BUFFER



HIGH-SPEED SAMPLE/HOLD AMPLIFIER

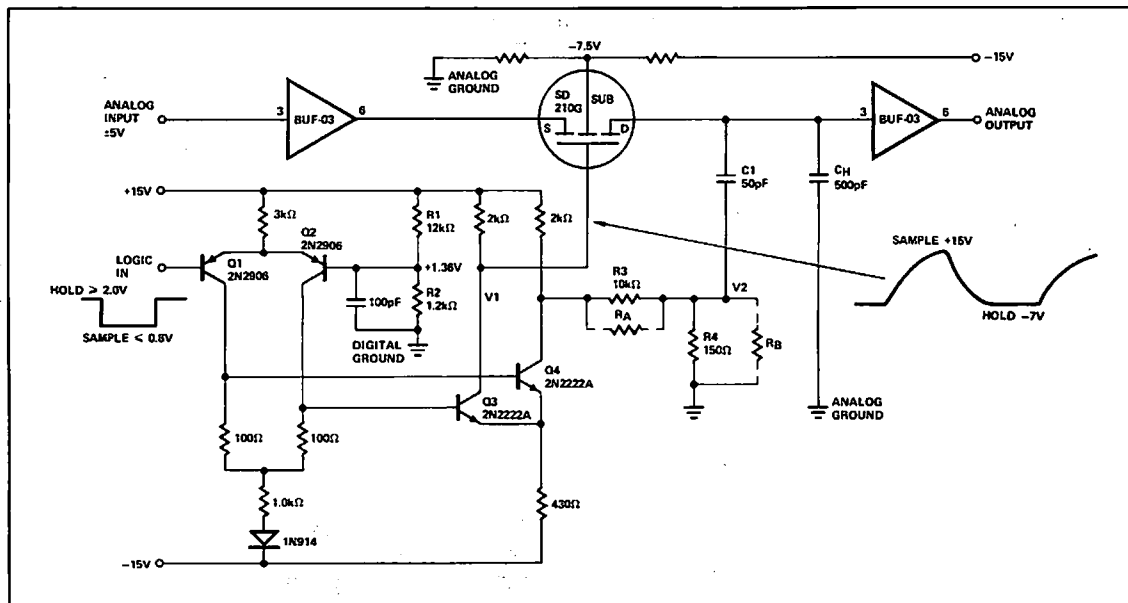


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VOLTAGE COMPARATORS

Precision Monolithics Inc.

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*Indicates new product or product whose data sheet has been finalized since the 1986 data book.



Precision Monolithics Inc.

VOLTAGE COMPARATORS

INTRODUCTION

A comparator provides a logic output indicating the amplitude relationship between two analog signal inputs.

When selecting a comparator, certain device parameters must be considered for proper design and application. These parameters are:

- V_{OS} (Input Offset Voltage)
- Response Time
- Slew Rate
- PSRR (Power Supply Rejection Ratio)
- I_B (Input Bias Current)
- CMVR (Common-Mode Voltage Range)
- Output Configuration
- Voltage Gain

The input offset voltage (V_{OS}) for a comparator should be as small as possible because in a high gain circuit it is the dominating factor that determines the exact threshold level. For this reason, comparators should be nulled or a Precision Comparator used so that the input differential voltage is as close to zero as practical when the output is at the logic switching threshold.

The voltage gain (A_V) determines the sensitivity and threshold accuracy of a comparator. For the ideal comparator, the gain could be considered infinite; and an extremely small voltage applied between the two inputs will cause a change in the output. In practice, some minimum voltage variation will be required at the input to effect a change in the output state. This minimum sensitivity will be determined from the voltage gain of the comparator. The relationship is as follows:

$$\Delta V_{IN(MIN)} = \frac{\Delta V_O}{A_V}$$

The quantity ΔV_O which is the difference between the high and low state of the output is generally chosen to be 2.5V to insure the matching of the comparator with the TTL load.

Precision Monolithics' comparator product line now spans high precision, low power and high speed comparators.

The CMP-01 is a fast precision comparator with low offset voltage. The CMP-02 offers the CMP-01's offset voltage performance along with lower input bias currents.

The quad CMP-04 offers both low power and low offset voltages. Existing "139" type applications can be upgraded by the pin compatible CMP-04. For very low power applications the CMP-04 drops into the "139" pinout, immediately reducing power consumption to 1.5 milliwatts. The PM-139/339 devices provide equal performance to "139/339" type comparators.

The CMP-05 brings together superior input specifications with very fast response times. This combination makes the CMP-05 the ideal choice in high-accuracy 10 and 12-bit data systems.

The latest addition to the PMI comparator line is the very high speed ECL output CMP-08 which offers 9.5 nanosecond response time in the space-saving 8-pin DIP package.

DEFINITIONS

Average Offset Current Drift (TC_{IOS}) — The ratio of the change in the input offset current to the change in temperature producing it.

Average Offset Voltage Drift (TC_{VOS}) — The ratio of the change in the input offset voltage to the change in temperature producing it.

Average Offset Voltage Drift With External Trimming (TC_{VOSN}) — The ratio of the change in the input offset voltage to the change in temperature producing it, with the input offset voltage trimmed to zero at room temperature.

Common-Mode Rejection Ratio (CMRR) — The ratio of differential voltage gain to common-mode voltage gain, expressed in dB. CMRR is measured as the ratio of the change in common-mode voltage divided by the change in input offset voltage.

$$CMRR = 20 \log \left(\frac{A_V(DIFF)}{A_V(CM)} \right) = 20 \log \left(\frac{\Delta CMV}{\Delta V_{OS}} \right)$$

Common-Mode Voltage Range (CMVR) — The range of common-mode voltage on the input terminals for which operation within specifications is assured.

VOLTAGE COMPARATORS

Differential Input Resistance (R_{IN}) — The resistance looking into either input terminal with the other grounded.

Differential Input Voltage — The range of voltage between the input terminals for which operation within specifications is assured.

Input Bias Current (I_B) — The average of the two input currents, with the inputs tied together.

Input Offset Current (I_{OS}) — The difference between the currents into the two input terminals when the output is within a specified voltage range.

Input Offset Voltage (V_{OS}) — The voltage applied between the input terminals to obtain a specified output voltage range.

Input Slew Rate — The maximum rate of change in differential and/or common-mode input voltage which the input stage can follow.

Input To Output High Propagation Delay (t_{pd+}) — The time measured between the input signal's V_{OS} crossing and the output voltage's 50% low-to-high transition point. Specified for a given input voltage step size and overdrive.

Input To Output Low Propagation Delay (t_{pd-}) — The time measured between the input signal's V_{OS} crossing and the output voltage's 50% high-to-low transition point. Specified for a given input voltage step size and overdrive.

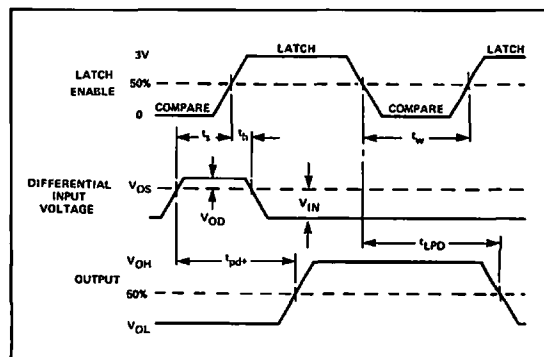
Latch Disable Propagation Delay (t_{LDD}) — The time measured between the 50% transition points of the latch enable signal and the output signal transition point.

Latch Hold Time (t_H) — The amount of time measured from 50% of the latch enable signal to the comparator-input trip-point crossing.

Latch Pulse Width (t_W) — The width of the latch enable pulse measured between the 50% points of the rising and falling pulse edges.

Latch Set-Up Time (t_S) — The amount of time measured from the comparator-input trip-point crossing to 50% of the latch enable control.

Switching Time Waveforms



Offset Voltage Adjustment Range — The change in offset voltage that can be obtained by adjusting a specified external nulling potentiometer.

Output Leakage Current (I_{LEAK}) — The current into the output terminal with a given output voltage and input drive equal to or greater than a specified value.

Output Sink Current (I_{SINK}) — The maximum negative current that can be delivered by the comparator.

Overdrive (V_{OD}) — The input step voltage (V_{IN}) of specified size drives the comparator from some initial input voltage to an input level just barely in excess of that required to bring the output from its high or low state to the logic threshold voltage. This excess is defined as the voltage overdrive.

Positive Output Voltage (V_{OH}) — The high output voltage level with a given load and an input drive equal to a specified value.

Power Supply Rejection Ratio (PSRR) — The ratio of the maximum change in input offset voltage to the specified change in power supply voltage.

Response Time (t_r) — The interval between the application of an input step function and the time when the output crosses the logic thresh-



VOLTAGE COMPARATORS

Precision Monolithics Inc.

old voltage. Logic threshold is defined as the voltage at the output of the comparator at which the loading logic circuitry changes its digital state, or, as 1.4V when the loading logic circuitry is not used.

Saturation Voltage (V_{OL}) — The low output voltage level with a given sink current and an input drive equal to a specified value.

Supply Currents — The currents required from the positive or negative supplies to operate the comparator without a load.

Voltage Gain (A_V) — The ratio of the change in output voltage (over a specified range) to the change in differential input voltage producing it.

VOLTAGE COMPARATOR SELECTION GUIDE

Quad Comparators

Product	V_{OS} mV	I_B nA	I_{OS} nA	A_V V/mV	t_r ns	I_{SY} mA	# of Comps	Features
CMP04	1	100	10	80	300	2.0	4	Low Power
CMP404	1	50	10	50	800	0.30	4	Low Power
PM139	2	100	25	50	1300	2.0	4	Low Power

High Speed Comparators

Product	V_{OS} mV	I_B nA	I_{OS} nA	A_V V/mV	t_r ns	I_{SY} mA	# of Comps	Features
CMP08	2.5	13000	1300	1.2	9.5	26	1	Very High Speed
CMP05	0.6	1200	80	8	55	11	1	High Speed
PM119/219	4.0	500	75	10	80	11.5	2	High Speed
CMP01	0.8	600	25	200	180	8.0	1	Fast

General Purpose Comparators

Product	V_{OS} mV	I_B nA	I_{OS} nA	A_V V/mV	t_r ns	I_{SY} mA	# of Comps	Features
PM111/211	3.0	50	5.0	75	180	5.0	1	General Purpose
CMP02	0.8	50	3.0	200	270	8.0	1	Low Input Current

VOLTAGE COMPARATORS

8

FEATURES

- Fast Response Time 180ns Max
- High Input Slew Rate 92V/ μ s
- Low Offset Voltage 0.3mV Typical, 0.8mV Max
- Low Offset Current 4nA Typical, 25nA Max
- Low Offset Drift 1 μ V/ $^{\circ}$ C, 30pA/ $^{\circ}$ C
- Standard Power Supplies +5V or $\pm$ 5V to $\pm$ 18V
- Guaranteed Operation from Single +5V Supply
- No Pull-Up Resistor Required for TTL Drive
- Wired OR Capability
- Fits 111, 106, 710 Sockets
- Easy Offset Nulling Single 2k Ω Potentiometer
- Easy to Use Free from Oscillations

ORDERING INFORMATION†

+25°C V _{OS} (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC			
	TO-99 8-PIN	DIP 8-PIN	PLASTIC DIP 8-PIN	
0.8	CMP01J*	CMP01Z*	—	MIL
0.8	CMP01EJ	CMP01EZ	CMP01EP	COM
2.8	CMP01CJ	CMP01CZ	CMP01CP	COM

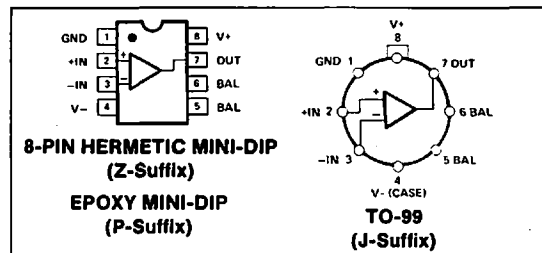
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

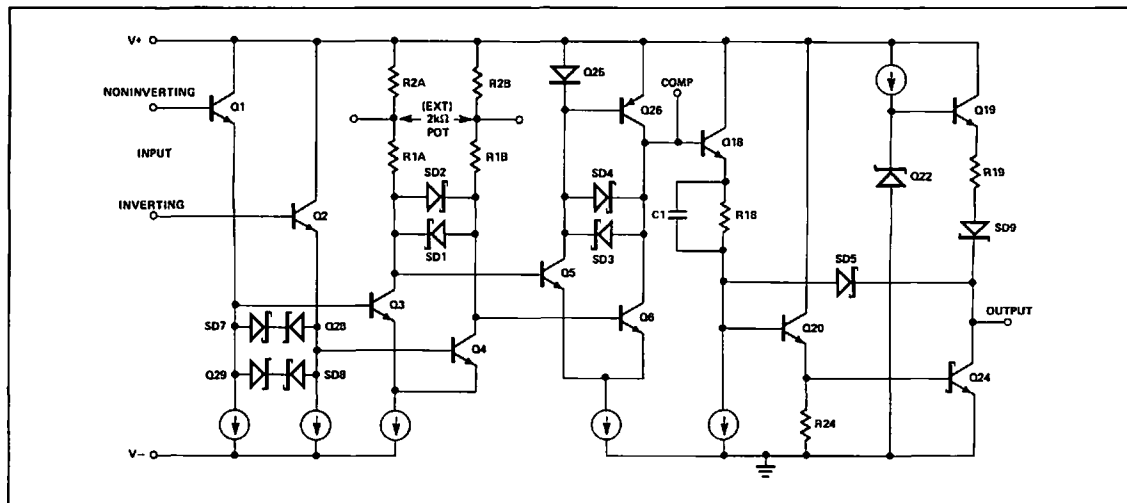
GENERAL DESCRIPTION

The CMP-01 is a monolithic fast precision voltage comparator using an advanced NPN-Schottky Barrier Diode process. It features fast response time to both large and small input signals, while maintaining excellent input characteristics. The CMP-01 is capable of operating over a wide range of supply voltages including single ended 5 volt supply. The large output current sinking and high output voltage capability assure good application flexibility, while the combination of fast response, high accuracy, and freedom from oscillation assure performance in precision level detectors and 12 and 13-bit A/D converters. The CMP-01 is pin-compatible to earlier 111, 106, and 710 types. For applications requiring lower input offset and bias currents, refer to the CMP-02 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ELECTRICAL CHARACTERISTICS** at $V_{S+} = 5V$, $V_{S-} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01 CMP-01E			CMP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	3	21	—	4	65	nA
Input Bias Current	I_B		—	250	500	—	300	720	nA
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	—	50	—	—	50	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive	—	150	—	—	150	—	ns
		5k Ω to 5V (Pull-Up) TTL Fan-Out = 4, 5k Ω to 5V (Pull-Up)	—	150	—	—	150	—	
Input Voltage Range	CMVR		1.8	1.7-3.8	3.5	1.8	1.7-3.8	3.5	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I_+	$V_{IN} \leq -10mV$	—	2.3	3.2	—	2.4	3.8	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	11.5	18	—	12	19	mW

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-01			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.5	1.6	mV
		$V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.6	2.8	
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	$\mu V/^\circ C$
Without External Trim			—	1	—	
Input Offset Current	I_{OS}	$T_A = +125^\circ C$, (Note 1)	—	4	25	nA
		$T_A = -55^\circ C$, (Note 1)	—	5	45	
Average Input Offset Current Drift	TCI_{OS}	$+25^\circ C \leq T_A \leq +125^\circ C$	—	12	—	$pA/^\circ C$
		$-55^\circ C \leq T_A \leq +25^\circ C$	—	35	—	
Input Bias Current	I_B	$T_A = +125^\circ C$	—	330	600	nA
		$T_A = -55^\circ C$	—	550	1400	
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive, (Note 2)	—	220	—	ns
		$T_A = +125^\circ C$, No Load $T_A = -55^\circ C$, No Load	—	100	—	
Input Voltage Range	CMVR		± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR		88	106	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	75	96	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0mA$	—	0.20	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.32	0.5	

NOTES:

- These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
- Guaranteed by design.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

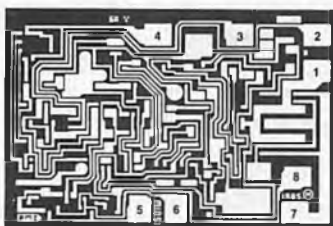
PARAMETER	SYMBOL	CONDITIONS	CMP-01E			CMP-01C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1) $V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.4	1.4	—	0.5	3.5	mV
			—	0.5	2.4	—	0.8	4.3	
Average Input Offset Voltage Drift Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	$\mu V/^\circ C$
With External Trim	TCV_{OSn}		—	1.0	—	—	1.2	—	
Input Offset Current	I_{OS}	$T_A = +70^\circ C$, (Note 1) $T_A = 0^\circ C$, (Note 1)	—	4	25	—	5	80	nA
			—	5	45	—	6	120	
Average Input Offset Current Drift	TCI_{OS}	$+25^\circ C \leq T_A \leq +70^\circ C$ $0^\circ C \leq T_A \leq +25^\circ C$	—	12	—	—	12	—	$pA/^\circ C$
			—	35	—	—	40	—	
Input Bias Current	I_B	$T_A = +70^\circ C$ $T_A = 0^\circ C$	—	330	600	—	340	900	nA
			—	400	850	—	450	1200	
Voltage Gain	A_V	$V_O = 0.4V$ to $2.4V$, (Notes 1, 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive $T_A = +70^\circ C$, No Load $T_A = 0^\circ C$, No Load	—	150	—	—	150	—	ns
			—	100	—	—	100	—	
Input Voltage Range	CMVR		± 12.0	± 13.3	—	± 12.0	± 13.3	—	V
Common-Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{slink} = 0$ $V_{IN} \leq -10mV$, $I_{slink} = 8.4mA$	—	0.17	0.4	—	0.17	0.4	V
			—	0.3	0.5	—	0.31	0.5	

NOTES:

- These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
- Guaranteed by design.



DICE CHARACTERISTICS



DIE SIZE 0.065×0.043 inch, 2730 sq. mils
(1.651×1.092 mm, 1.803 sq. mm)

1. GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	0.8	2.8	mV MAX
Input Offset Current	I_{OS}	(Note 1)	25	80	nA MAX
Input Bias Current	I_B		600	900	nA MAX
Differential Input Resistance	R_{IN}	(Note 2)	150	100	k Ω MIN
Input Voltage Range	CMVR		± 12.5	± 12.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S \leq 18V$ $-18V \leq V_S \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4	—	V MIN
Saturation Voltage	V_{OL}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	2	8	μA MAX
Positive Supply Current	I_+	$V_{IN} \leq -10mV$	8.0	8.5	mA MAX
Negative Supply Current	I_-	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

NOTES:

1. These parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to

+5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

2. Guaranteed by design.

WAFER TEST LIMITS at $V_S + = 5V$ and $V_S - = 0V$, $T_A = 25^\circ C$.

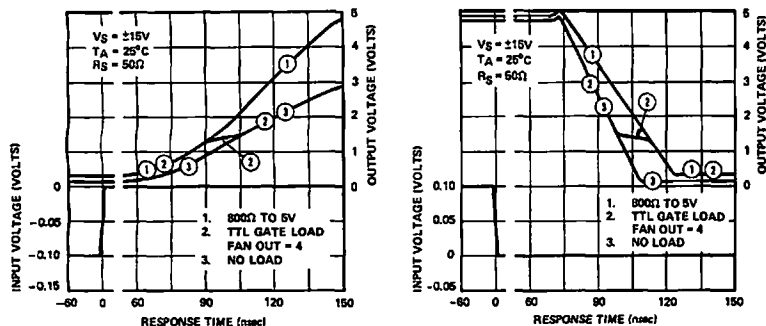
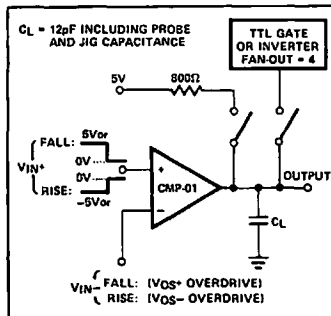
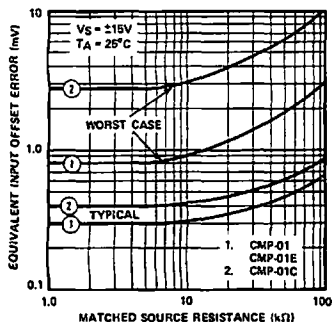
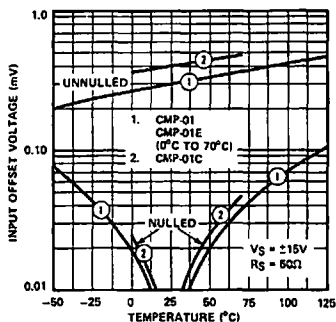
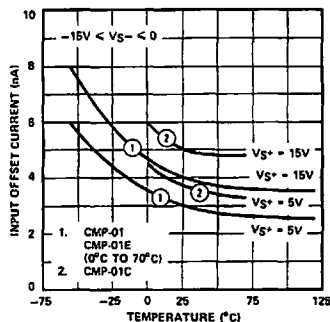
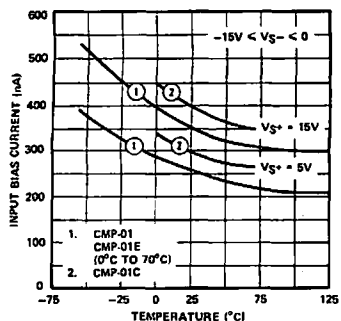
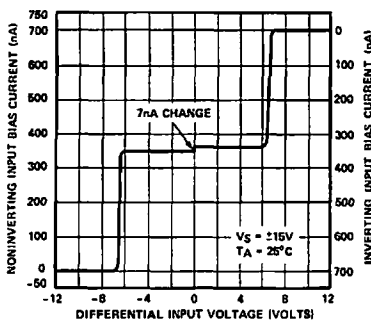
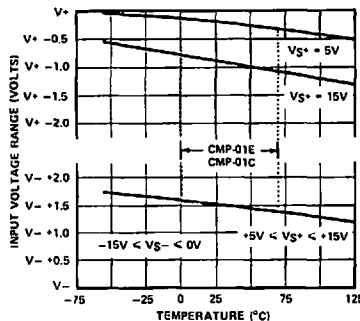
PARAMETER	SYMBOL	CONDITIONS	CMP-01N LIMIT	CMP-01GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		21	65	nA MAX

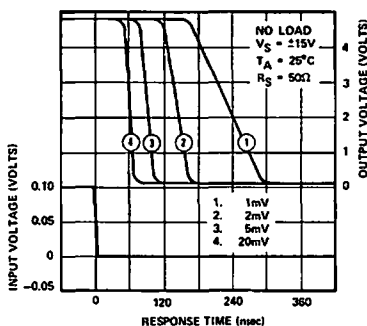
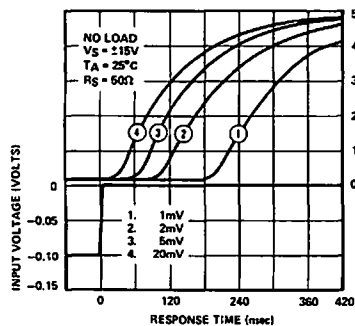
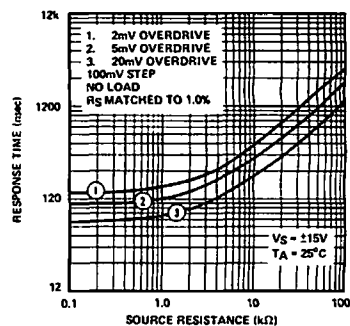
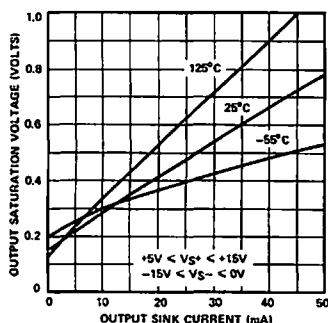
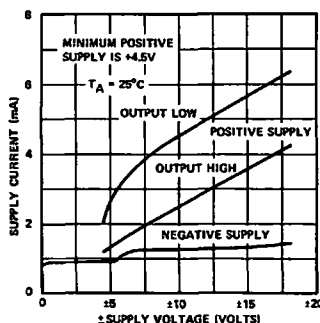
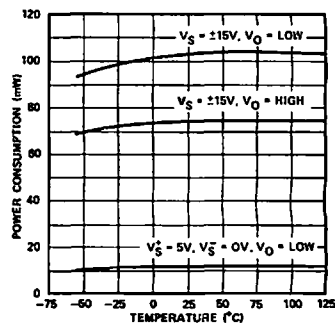
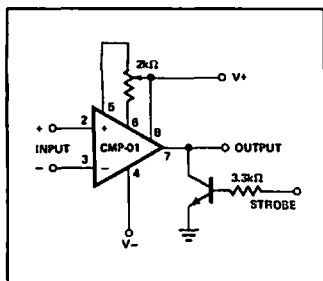
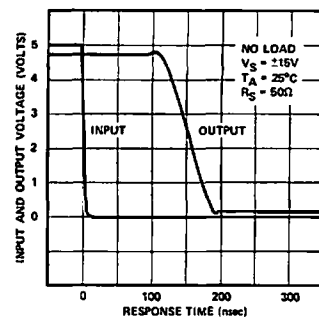
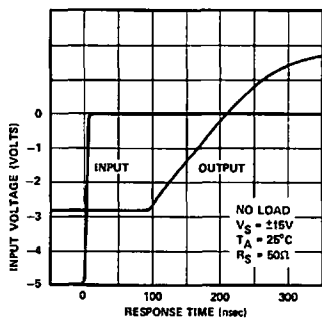
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-01N TYPICAL	CMP-01GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	1.5	1.8	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		35	40	pA/°C
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up), $T_A = 25^\circ C$	110	110	ns

TYPICAL PERFORMANCE CHARACTERISTICS
**RESPONSE TIME,
100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS**

RESPONSE TIME TEST CIRCUIT

**INPUT OFFSET ERROR vs
SOURCE RESISTANCE**

**OFFSET VOLTAGE vs
TEMPERATURE**

**INPUT OFFSET CURRENT
vs TEMPERATURE**

**INPUT BIAS CURRENT
vs TEMPERATURE**

**INPUT BIAS CURRENT
vs DIFFERENTIAL
INPUT VOLTAGE**

**INPUT VOLTAGE RANGE
vs TEMPERATURE**


TYPICAL PERFORMANCE CHARACTERISTICS
**RESPONSE TIME
FOR 100mV STEP AND VARIOUS INPUT OVERDRIVES**

**RESPONSE TIME vs
SOURCE RESISTANCE**

**SATURATION VOLTAGE
vs SINK CURRENT**

**SUPPLY CURRENT vs
SUPPLY VOLTAGE**

**POWER CONSUMPTION
vs TEMPERATURE**

**OFFSET TRIMMING
AND STROBE CIRCUIT**

**RESPONSE TIME
FOR 5V STEP AND 5mV OVERDRIVE**


APPLICATIONS INFORMATION

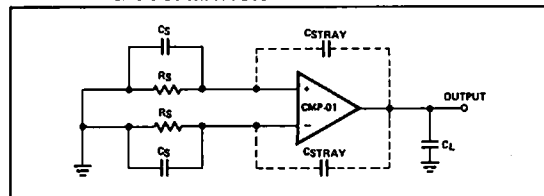
The CMP-01 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-01 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading (C_L). The capacitive loading techniques will eliminate the oscillations, but result in slower response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

and if $C_S \geq 20\text{pF}$ $\left(\frac{\text{maximum step size}}{\text{minimum overdrive}} \right)$

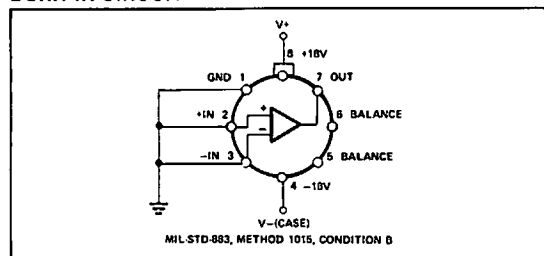
the response time will approximate the response time for low values of R_S . It should be noted that the offset nulling terminals do not require bypassing for stability. As with all

wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

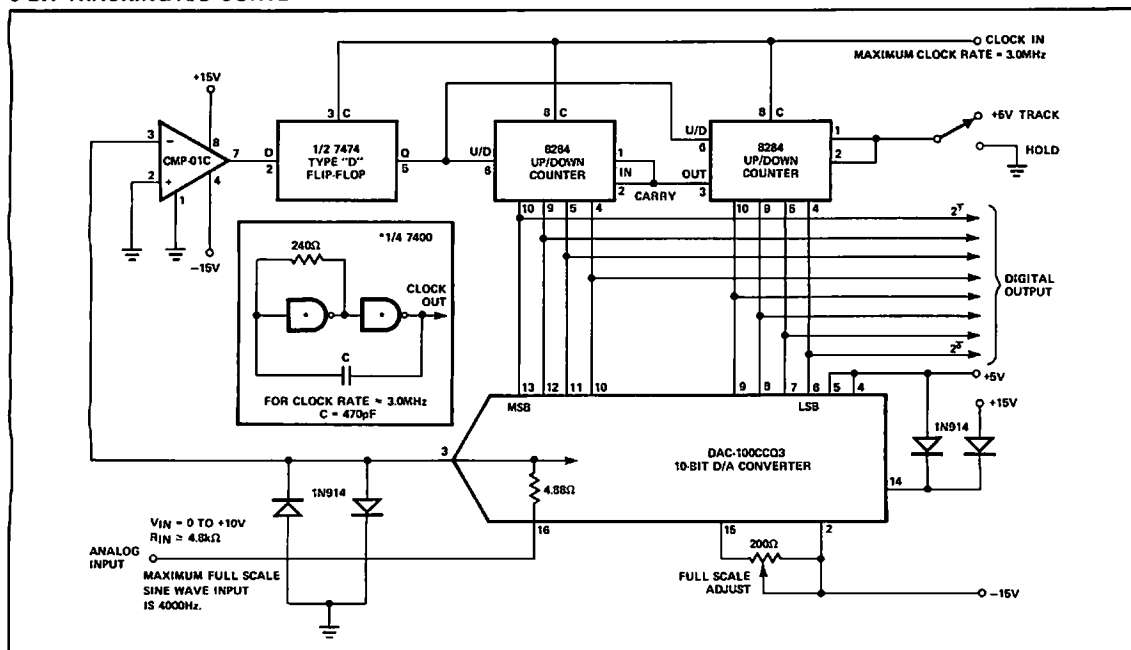
MINIMIZING OSCILLATION



BURN-IN CIRCUIT



8-BIT TRACKING A/D CONVERTER





CMP-02

LOW-INPUT-CURRENT
PRECISION COMPARATOR

Precision Monolithics Inc.

FEATURES

- Low Offset Voltage 0.3mV Typ, 0.8mV Max
- Low Offset Current 0.3nA Typ, 3nA Max
- Low Bias Current 28nA Typ, 50nA Max
- Low Offset Drift $1\mu\text{V}/^\circ\text{C}$, 4pA/ $^\circ\text{C}$
- High Gain 200,000 Min
- High CMRR 110dB Typ, 94dB Min
- High Input Impedance 16M Ω
- Fast Response Time 180ns Typ, 270ns Max
- Standard Power Supplies +5V or $\pm 5\text{V}$ to $\pm 18\text{V}$
- Guaranteed Operation from Single +5V
- No Pull-Up Resistor Required for TTL Drive
- Wired OR Capability
- Fits 111, 108, 710 Sockets
- Easy Offset Nulling Single 2k Ω Potentiometer
- Easy to Use Free from Oscillations

ORDERING INFORMATION†

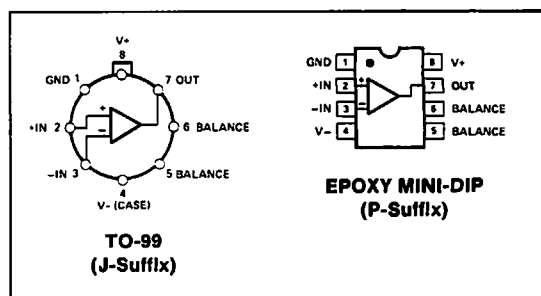
+25°C V _{OS} (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC TO-99 8-PIN	PLASTIC DIP 8-PIN	
0.8	—	CMP02EP	COM
2.8	CMP02CJ	CMP02CP	COM

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

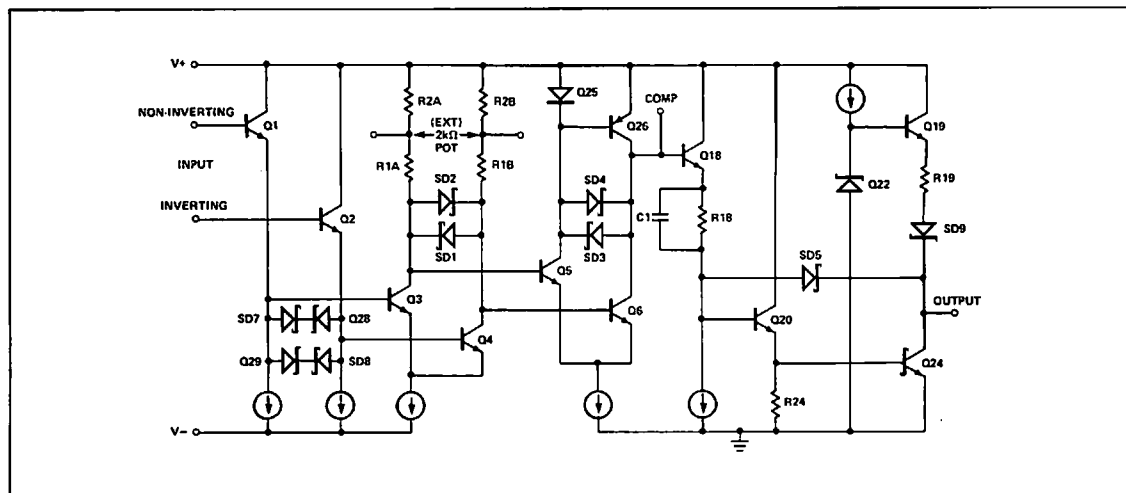
GENERAL DESCRIPTION

The CMP-02 is a monolithic low input current comparator using an advanced NPN-Schottky Barrier Diode process. It features superior input characteristics with extremely low offset voltage, offset current, bias current and temperature drift. High common-mode and power supply rejection plus good response time contribute to excellent performance in the most demanding applications. The balanced offset nulling, large output drive, and wired-OR capability combined with internal pull-up maximize application convenience. The CMP-02 is capable of operating over a wide range of supply voltages, including single plus 5 volt supply operation, and is pin-compatible to earlier 111, 108, and 710 types. For applications requiring faster response time, please refer to the CMP-01 fast precision comparator data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 2)

Total Supply Voltage, V+ to V-	36V
Output to Ground	-5V to +32V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Positive Supply Voltage to Ground	30V
Positive Supply Voltage to Offset Null	0 to 2V
Power Dissipation (See Note 1)	500mW
Differential Input Voltage	±11V
Input Voltage (V _S = ±15V)	±15V
Output Sink Current (Continuous Operation)	75mA
Operating Temperature Range	
CMP-02E, CMP-02C	0°C to +70°C
DICE Junction Temperature (T _j)	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
P-Suffix	-65°C to +125°C

[illegible]

NOTES:

1. Maximum package power dissipation vs. ambient temperature.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
Mini-DIP (P)	38° C	5.6mW/° C

2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02E			CMP-02C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.3	0.8	—	0.4	2.8	mV
Input Offset Voltage	V_{OS}	$R_S \leq 50k\Omega$, (Note 1)	—	0.3	0.9	—	0.4	3	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	3.0	—	0.4	15	nA
Input Bias Current	I_B		—	28	50	—	35	100	nA
Differential Input Resistance	R_{IN}	(Note 2)	1.7	3	—	0.9	2	—	M Ω
Voltage Gain	A_V	$V_O = 1$ to 3V, (Note 2)	200	500	—	100	500	—	V/mV
Response Time (Note 3)	t_r	100mV step, 5mV Overdrive	—	190	270	—	190	270	ns
		No Load (No Pull-Up)	—	190	—	—	190	—	
		5k Ω to 5V (Pull-Up)	—	190	—	—	190	—	
		TTL Fan-Out = 4, No Pull-Up	—	190	—	—	190	—	
Input Slew Rate			—	15	—	—	15	—	V/ μ s
Input Voltage Range	CMVR		± 12.5	± 13.0	—	± 12.5	± 13.0	—	V
Common-Mode Rejection Ratio	CMRR		94	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 18V$, $-18V \leq V_{S-} \leq 0V$	80	100	—	74	98	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$	2.4	3.2	—	—	—	—	V
		$V_{IN} \geq 3mV$, $I_O = 240\mu A$	—	—	—	2.4	3.4	—	
		$V_{IN} \geq 3mV$, $I_O = 0mA$	2.4	4.8	—	2.4	4.8	—	
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{SINK} = 0mA$	—	0.18	0.40	—	0.18	0.40	V
		$V_{IN} \leq -10mV$, $I_{SINK} \leq 6.4mA$	—	0.3	0.45	—	0.31	0.45	
		$V_{IN} \leq -10mV$, $I_{SINK} \leq 12mA$ (CMP-02 only)	—	0.38	0.5	—	—	—	
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = +30V$	—	0.03	2.0	—	0.05	8.0	μA
Positive Supply Current	I+	$V_{IN} \leq -10mV$	—	5.5	8.0	—	5.6	8.5	mA
Negative Supply Current	I-	$V_{IN} \leq -10mV$	—	1.1	2.2	—	1.2	2.2	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	99	153	—	102	181	mW
Offset Voltage Adjustment Range		Nulling Pot $\geq 2k\Omega$	—	± 5	—	—	± 5	—	mV

NOTES:

1. These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into

- account the worst case effects of voltage gain and input impedance.
- 2. Guaranteed by design.
- 3. Sample tested.

**ELECTRICAL CHARACTERISTICS** at $V_S = 5V$, $V_{S-} = 0V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-02E			CMP-02C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1)	—	0.4	1.5	—	0.5	3.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.25	3	—	0.35	14	nA
Input Bias Current	I_B		—	24	45	—	30	90	nA
Voltage Gain	A_V	$V_O = 1$ to $3V$	—	50	—	—	50	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive	—	250	—	—	250	—	ns
		5k Ω to 5V (Pull-Up) TTL Fan-Out = 4, 5k Ω to 5V	—	250	—	—	250	—	
Input Voltage Range	CMVR		1.8-3.5	1.7-3.8	—	1.8-3.5	1.7-3.8	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -3.5mV$, $I_{sink} \leq 6.4mA$	—	0.3	0.45	—	0.3	0.45	V
Positive Supply Current	I_+	$V_{IN} \leq -10mV$	—	2.2	3	—	2.3	3.6	mA
Power Dissipation	P_d	$V_{IN} \leq -10mV$	—	11	15	—	11.5	18	mW

NOTE:

- These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

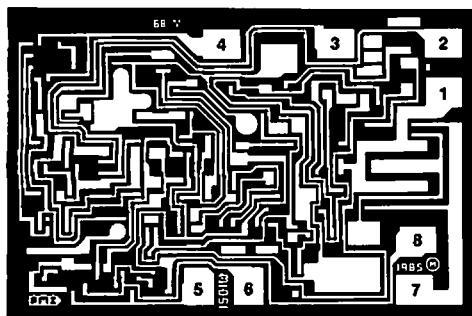
PARAMETER	SYMBOL	CONDITIONS	CMP-02E			CMP-02C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$, (Note 1) $V_{S+} = 5V$, $V_{S-} = 0V$, (Note 1)	—	0.4	1.4	—	0.5	3.5	mV
			—	0.5	2.4	—	0.6	4.3	
Average Input Offset Voltage Drift									
Without External Trim	TCV_{OS}	$R_S = 50\Omega$	—	1.5	—	—	1.8	—	$\mu V/^\circ C$
With External Trim	TCV_{OSn}	$R_S = 50\Omega$	—	1	—	—	1.2	—	
Input Offset Current	I_{OS}	$T_A = +70^\circ C$, (Note 1)	—	0.3	3	—	0.4	15	nA
		$T_A = 0^\circ C$, (Note 1)	—	0.4	6	—	0.5	25	
Average Input Offset Current Drift	TCI_{OS}	$+25^\circ C \leq T_A \leq +70^\circ C$	—	2	—	—	3	—	$pA/^\circ C$
		$0^\circ C \leq T_A \leq +25^\circ C$	—	4	—	—	5	—	
Input Bias Current	I_B	$T_A = +70^\circ C$	—	26	50	—	33	100	nA
		$T_A = 0^\circ C$	—	34	80	—	42	160	
Voltage Gain	A_V	$V_O = 1$ to $3V$, (Note 2)	100	500	—	70	500	—	V/mV
Response Time	t_r	100mV Step, 5mV Overdrive	—	225	—	—	225	—	ns
		$T_A = +70^\circ C$, No Load $T_A = 0^\circ C$, No Load	—	180	—	—	180	—	
Input Voltage Range	CMVR		± 12.0	± 13	—	± 12	± 13	—	V
Common-Mode Rejection Ratio	CMRR		90	108	—	86	108	—	dB
Power Supply Rejection Ratio	PSRR	$5V \leq V_{S+} \leq 15V$, $-15V \leq V_{S-} \leq 0V$	77	98	—	70	88	—	dB
Positive Output Voltage	V_{OH}	$V_{IN} \geq 4mV$, $I_O = 200\mu A$	2.4	3.2	—	2.4	3.2	—	V
Saturation Voltage	V_{OL}	$V_{IN} \leq -10mV$, $I_{sink} = 0$	—	0.17	0.4	—	0.17	0.4	V
		$V_{IN} \leq -10mV$, $I_{sink} = 6.4mA$	—	0.30	0.5	—	0.31	0.5	

NOTES:

- These Parameters are specified as the maximum values required to drive the output between the logic levels of 0.4V and 2.4V with a 1k Ω load tied to +5V; thus, these parameters define an error band which takes into account the worst case effects of voltage gain and input impedance.
- Guaranteed by design.



DICE CHARACTERISTICS



DIE SIZE 0.065×0.043 Inch, 2730 sq. mils
(1.651×1.094 mm, 1.806 sq. mm)

1. GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
5. BALANCE
6. BALANCE
7. OUTPUT
8. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$ $R_S \leq 50k\Omega$	0.8 0.9	2.8 3	mV MAX
Input Offset Current	I_{OS}		3	15	nA MAX
Input Bias Current	I_B		50	100	nA MAX
Differential Input Resistance	R_{IN}		1.7	0.9	M Ω MIN
Input Voltage Range	CMVR		± 12.5	± 12.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm CMVR$	94	90	dB MIN
Power Supply Rejection Ratio	PSRR	$5V \leq V_S \leq 18V$ $-18V \leq V_S \leq 0V$	80	74	dB MIN
Positive Output Voltage	V_{OH}	$V_{IN} \geq 3mV$, $I_O = 320\mu A$ $V_{IN} \geq 3mV$, $I_O = 240\mu A$	2.4 —	— 2.4	V MIN
Saturation Voltage	V_{OL}	$I_{sink} = 6.4mA$	0.45	0.45	V MAX
Output Leakage Current	I_{LEAK}	$V_{IN} \geq 10mV$, $V_O = 30V$	2	8	μA MAX
Positive Supply Current	I_+	$V_{IN} \leq -10mV$	8	8.5	mA MAX
Negative Supply Current	I_-	$V_{IN} \leq -10mV$	2.2	2.2	mA MAX
Power Consumption	P_d	$V_{IN} \leq -10mV$	153	161	mW MAX

WAFER TEST LIMITS at $V_{S+} = 5V$ and $V_{S-} = 0V$, $T_A = 25^\circ C$.

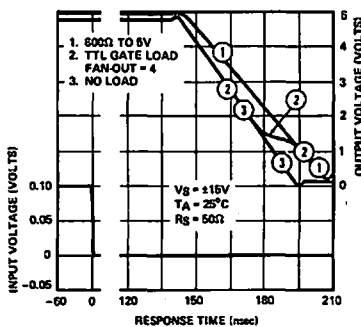
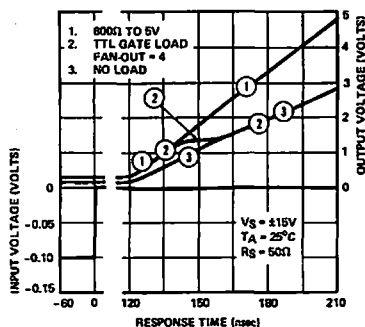
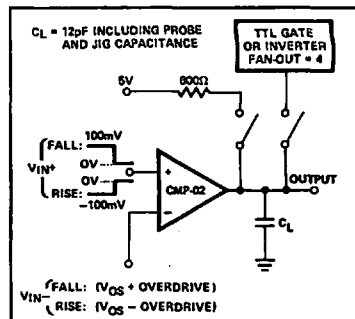
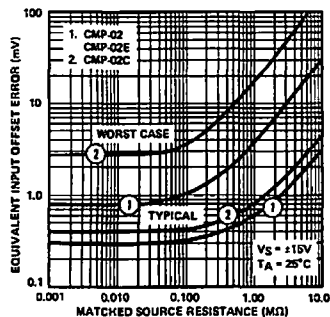
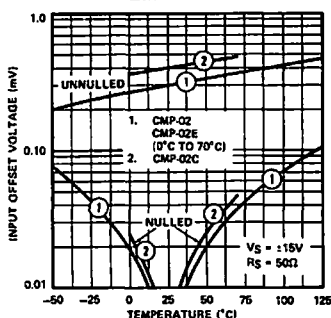
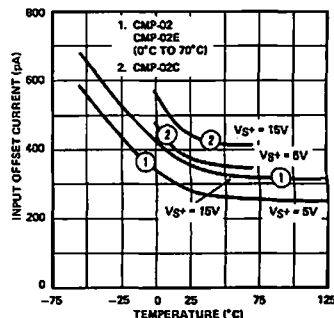
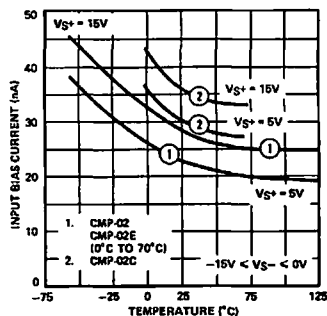
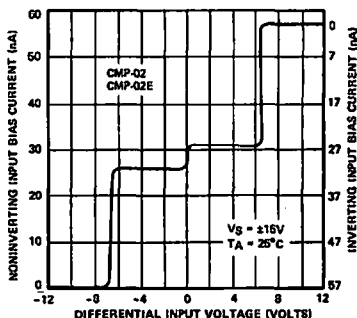
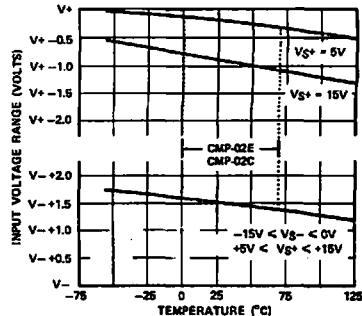
PARAMETER	SYMBOL	CONDITIONS	CMP-02N LIMIT	CMP-02GR LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$	1.5	3.5	mV MAX
Input Offset Current	I_{OS}		3	14	nA MAX

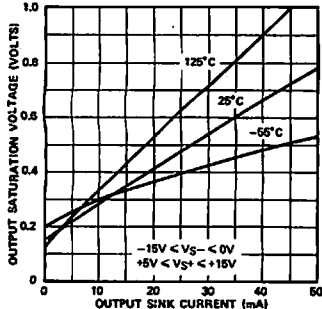
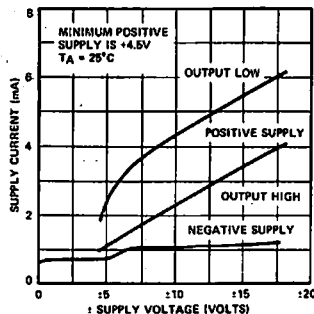
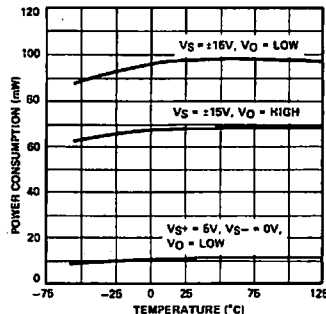
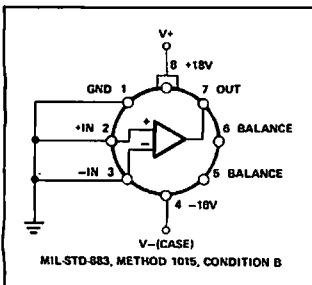
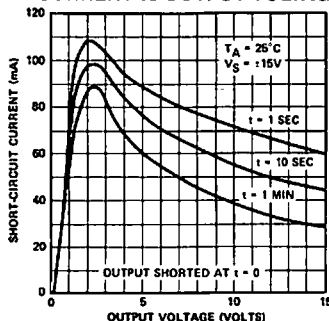
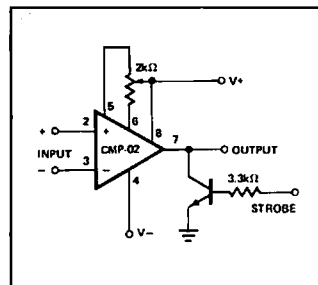
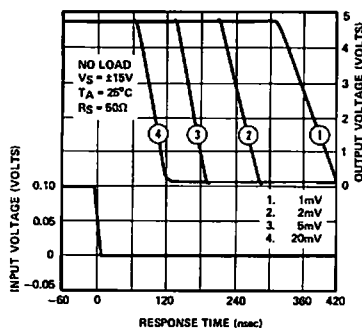
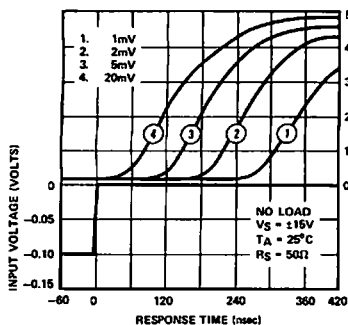
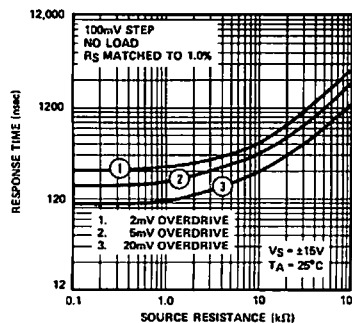
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$.

PARAMETER	SYMBOL	CONDITIONS	CMP-02N TYPICAL	CMP-02GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	1.5	1.8	$\mu V/^\circ C$
Average Input Offset Current Drift	TCI_{OS}		4	5	pA/°C
Response Time	t_r	100mV Step, 5mV Overdrive No Load (No Pull-Up), $T_A = 25^\circ C$	190	190	ns

TYPICAL PERFORMANCE CHARACTERISTICS
**RESPONSE TIME,
100mV STEP, 5mV OVERDRIVE, VARIOUS LOADS**

RESPONSE TIME TEST CIRCUIT

**INPUT OFFSET ERROR vs
SOURCE RESISTANCE**

**OFFSET VOLTAGE vs
TEMPERATURE**

**INPUT OFFSET CURRENT
vs TEMPERATURE**

**INPUT BIAS CURRENT
vs TEMPERATURE**

**INPUT BIAS CURRENT
vs DIFFERENTIAL
INPUT VOLTAGE**

**INPUT VOLTAGE RANGE
vs TEMPERATURE**


TYPICAL PERFORMANCE CHARACTERISTICS
**SATURATION VOLTAGE
vs SINK CURRENT**

**SUPPLY CURRENT vs
SUPPLY VOLTAGE**

**POWER CONSUMPTION
vs TEMPERATURE**

STANDARD BURN-IN CIRCUIT

**OUTPUT SHORT-CIRCUIT
CURRENT vs OUTPUT VOLTAGE**

**OFFSET TRIMMING AND
STROBE CIRCUITS**

**RESPONSE TIME,
100mV STEP AND VARIOUS INPUT OVERDRIVES**

**RESPONSE TIME vs
SOURCE RESISTANCE**


APPLICATIONS INFORMATION

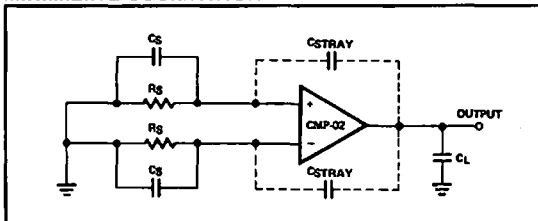
The CMP-02 provides fast response times even with small overdrives; to achieve this performance requires very high gain at high frequencies. The CMP-02 is completely free of oscillations; however, small values of stray capacitance from output to input when combined with high-source resistances can cause an unstable condition. DC characteristics are not affected, but when the input is within a few microvolts of the transition level, certain conditions can create an oscillation region. The width of this oscillatory region and the size of source resistance where oscillations begin is a strong function of the stray coupling present. The following suggestions are offered as a guide towards minimizing the conditions for oscillation: matched source resistors, minimized stray capacitances (e.g., a ground plane between output and input), or capacitive output loading (C_L). The capacitive loading techniques will eliminate the oscillations, but result in slower

response time. Matched bypass capacitors across the input resistors also can eliminate the instability,

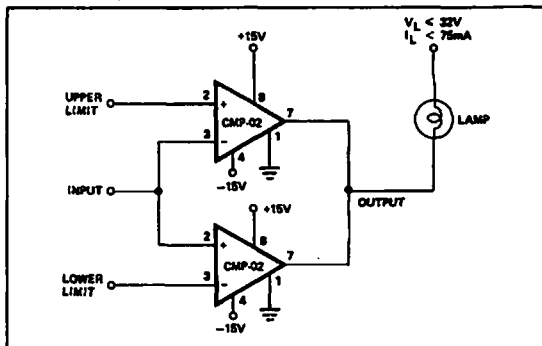
$$\text{and if } C_S \geq 20\text{pF} \left(\frac{\text{maximum step size}}{\text{minimum overdrive}} \right)$$

the response time will approximate the response time for low values of R_S . It should be noted that the offset nulling terminals do not require bypassing for stability. As with all wideband circuits, it is recommended that the supplies be bypassed near the socket of the device.

MINIMIZING OSCILLATION



PRECISION, DUAL LIMIT, GO/NO GO TESTER





Precision Monolithics Inc.

CMP-04

QUAD LOW-POWER PRECISION COMPARATOR

FEATURES

- High Gain 200V/mV Typ
- Single or Dual Supply Operation
- Input Voltage Range Includes Ground
- Low Power Consumption (1.5mW/Comparator)
- Low Input Bias Current 100nA Max
- Low Input Offset Current 10nA Max
- Low Offset Voltage 1mV Max
- Low Output Saturation Voltage 250mV @ 4mA
- Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS
- Directly Replaces LM139/239/339 Comparators

ORDERING INFORMATION†

25°C V _{OS} (mV)	DIP PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC 14-PIN	PLASTIC 14-PIN	
1	CMP04BY*	—	MIL
1	CMP04FY	—	IND
1	—	CMP04FP	COM

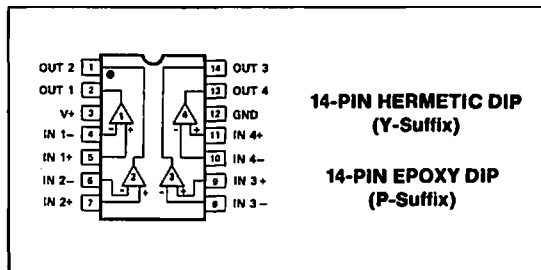
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

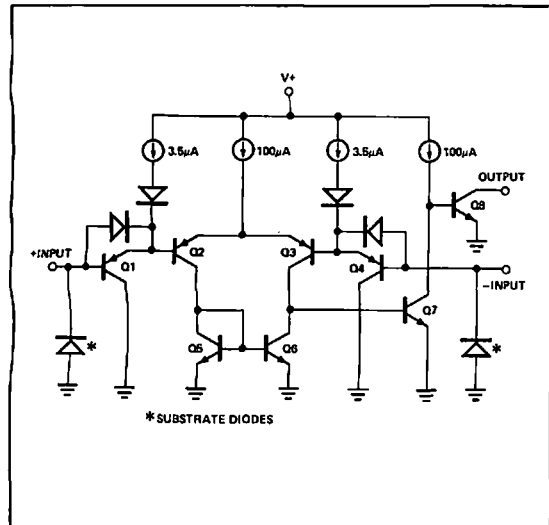
GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP-04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V₋ for split supplies. A low power supply current of 2mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

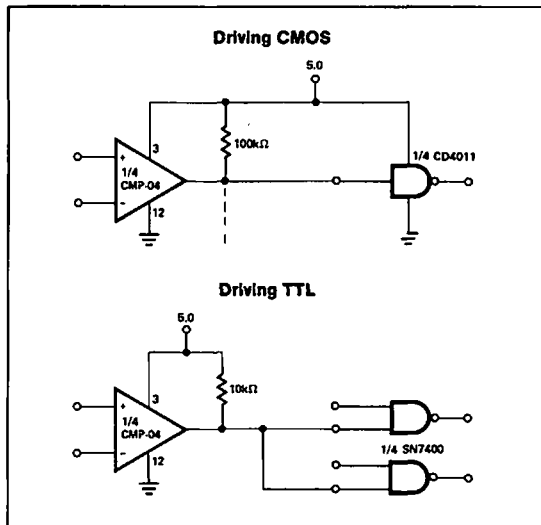
PIN CONNECTIONS



SIMPLIFIED SCHEMATIC (1/4 CMP-04)



TYPICAL INTERFACE



VOLTAGE COMPARATORS

8

**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Supply Voltage	36V or $\pm 18V$
Differential Input Voltage	36V _{DC}
Input Voltage	-0.3V to +36V
Power Dissipation (Note 1)	500mW
Operating Temperature Range	
CMP-04FY	-25°C to +85°C
CMP-04BY	-55°C to +125°C
CMP-04FP	0°C to +70°C
DICE Junction Temperature (T _J)	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
P-Suffix	-65°C to +125°C

Input Current (V _{IN} < -3.0V)	50mA
Output Short-Circuit to GND	Continuous
Lead Temperature (Soldering, 60 sec)	300°C

NOTES:

- See table for maximum ambient temperature rating and derating factor.
- Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
Hermetic DIP (Y)	100°C	10mW/°C
Plastic DIP (P)	50°C	8mW/°C

ELECTRICAL CHARACTERISTICS at V₊ = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04B/F			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	R _S = 0Ω, R _L = 5.1kΩ V _O = 1.4V, (Note 1)	—	0.4	1	mV
Input Offset Current	I _{OS}	I _{IN} (+) - I _{IN} (-) R _L = 5.1kΩ V _O = 1.4V	—	2	10	nA
Input Bias Current	I _B	I _{IN} (+) or I _{IN} (-)	—	25	100	nA
Voltage Gain	A _V	R _L ≥ 15kΩ, V ₊ = 15V, (Note 5)	80	200	—	V/mV
Large-Signal Response Time	t _r	V _{IN} = TTL Logic Swing V _{REF} = 1.4V, (Note 4) V _{RL} = 5V, R _L = 5.1kΩ	—	300	—	ns
Small-Signal Response Time	t _r	V _{IN} = 100mV Step, (Note 4) 5mV Overdrive V _{RL} = 5V, R _L = 5.1kΩ	—	1.3	—	μs
Input Voltage Range	CMVR	(Note 2)	0	—	V ₊ - 1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	80	100	—	dB
Power Supply Rejection Ratio	PSRR	V ₊ = +5V to 18V, (Note 5)	80	100	—	dB
Saturation Voltage	V _{OL}	V _{IN} (-) ≥ 1V, V _{IN} (+) = 0, I _{SINK} ≤ 4mA	—	250	400	mV
Output Sink Current	I _{SINK}	V _{IN} (-) ≥ 1V, V _{IN} (+) = 0, V _O ≤ 1.5V	6	16	—	mA
Output Leakage Current	I _{LEAK}	V _{IN} (+) ≥ 1V, V _{IN} (-) = 0, V _O = 30V	—	0.1	100	nA
Supply Current	I ₊	R _L = ∞, All Comps V ₊ = 30V	—	0.8	2.0	mA

NOTES:

- At output switch point, V_O = 1.4V, R_S = 0Ω with V₊ from 5V; and over the full input common-mode range (0V to V₊ - 1.5V).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V₊ - 1.5V, but either or both inputs can go to +30V without damage.
- R_L ≥ 15kΩ, V₊ = 15V, V_{CM} = 1.5V to 13.5V.
- Sample tested.
- Guaranteed by design.

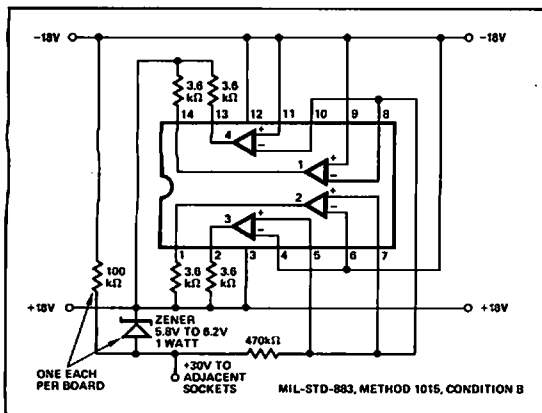


ELECTRICAL CHARACTERISTICS at $V+ = +5V$. For CMP-04BY, $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$. For CMP-04FY, $-25^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$. For CMP-04FP, $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04B/F (Note 3)			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	—	1	2	mV
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	—	4	20	nA
Input Bias Current	I_B	$I_{IN(+)} \text{ or } I_{IN(-)}$	—	40	200	nA
Voltage Gain	A_V	$R_L \geq 15k\Omega$, $V+ = 15V$, (Note 5)	70	125	—	V/mV
Large-Signal Response Time	t_r	$V_{IN} = \text{TTL Logic Swing}$ $V_{REF} = 1.4V$, (Note 4) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	300	—	ns
Small-Signal Response Time	t_r	$V_{IN} = 100\text{mV Step}$, (Note 4) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	—	1.3	—	μs
Input Voltage Range	CMVR	(Note 2)	0	—	$V+ - 1.5$	V
Common-Mode Rejection Ratio	CMRR	(Notes 3, 5)	60	100	—	dB
Power Supply Rejection Ratio	PSRR	$V+ = +5V \text{ to } 18V$	80	100	—	dB
Saturation Voltage	V_{OL}	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\text{mA}$	—	250	700	mV
Output Sink Current	I_{SINK}	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $V_O \leq 1.5V$	5	16	—	mA
Output Leakage Current	I_{LEAK}	$V_{IN(+)} \geq 1V$, $V_{IN(-)} = 0$, $V_O = 30V$	—	0.1	200	nA
Supply Current	$I+$	$R_L = \infty$, All Comps $V+ = 30V$	—	1.2	3.0	mA

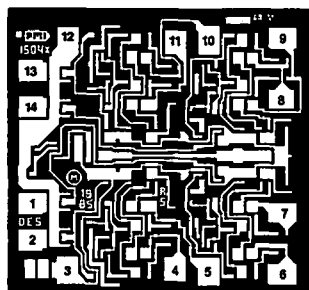
NOTES:

- At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with $V+$ from 5V; and over the full input common-mode range (0V to $V+ - 1.5V$).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V+ - 1.5V$, but either or both inputs can go to +30V without damage.
- $R_L \geq 15k\Omega$, $V+ = 15V$, $V_{CM} = 1.5V \text{ to } 13.5V$.
- Sample tested.
- Guaranteed by design.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.058 × 0.055 inch, 3190 sq. mils
(1.47 × 1.40 mm, 2.058 sq. mm)

- | | |
|---------------------------|----------------------------|
| 1. OUTPUT (2) | 8. INVERTING INPUT (3) |
| 2. OUTPUT (1) | 9. NONINVERTING INPUT (3) |
| 3. POSITIVE SUPPLY | 10. INVERTING INPUT (4) |
| 4. INVERTING INPUT (1) | 11. NONINVERTING INPUT (4) |
| 5. NONINVERTING INPUT (1) | 12. GROUND (SUBSTRATE) |
| 6. INVERTING INPUT (2) | 13. OUTPUT (4) |
| 7. NONINVERTING INPUT (2) | 14. OUTPUT (3) |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = +5V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04N LIMIT	CMP-04G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	1	2	mV MAX
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	10	25	nA MAX
Input Bias Current	I_B	$I_{IN(+)}$ or $I_{IN(-)}$, (Note 1)	100	100	nA MAX
Voltage Gain	A_V	$R_L \geq 15k\Omega$, $V_+ = 15V$, (Note 3)	80	50	V/mV MIN
Input Voltage Range	CMVR	(Notes 2, 3)	$V_+ - 1.5$	$V_+ - 1.5$	V MAX
Common-Mode Rejection Ratio	CMRR	(Note 4)	80	80	dB MIN
Power Supply Rejection Ratio	PSRR	$V_+ = 5V$ to $+18V$	80	80	dB MIN
Saturation Voltage	V_{OL}	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$	400	400	mV MAX
Output Sink Current	I_{SINK}	$V_{IN(-)} \geq 1V$, $V_{IN(+)} = 0$, $V_O \leq 1.5V$	6	6	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN(+)} \geq 1V$, $V_{IN(-)} = 0$, $V_O = 30V$	100	100	nA MAX
Supply Current	I_+	$R_L = \infty$, All Comps $V_+ = 30V$	2	2	mA MAX

NOTES:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = +5V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-04N TYPICAL	CMP-04G TYPICAL	UNITS
Large-Signal Response Time	t_r	$V_{IN} = \text{TTL Logic Swing}$ $V_{REF} = 1.4V$, (Note 5) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	600	600	ns
Small-Signal Response Time	t_r	$V_{IN} = 100mV \text{ Step}$, (Note 5) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	1.3	1.3	μs

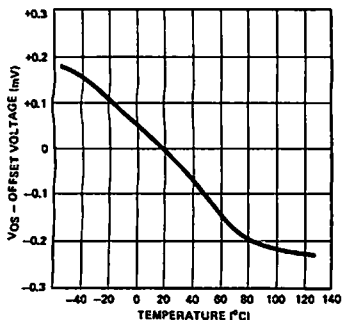
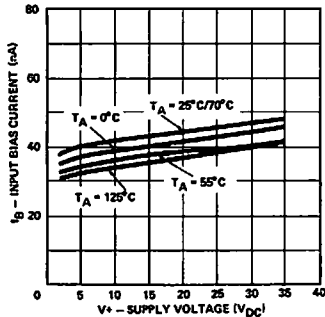
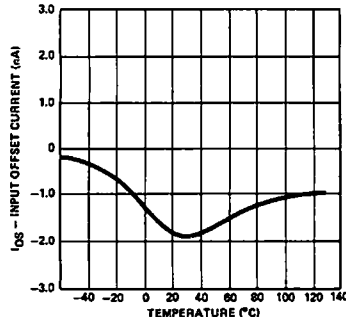
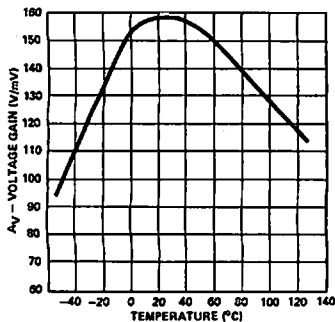
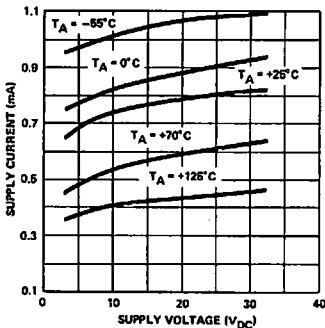
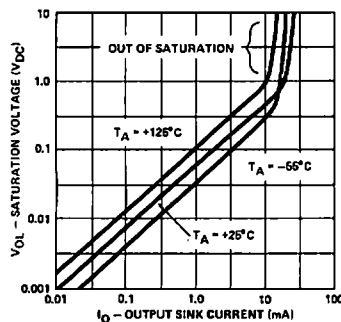
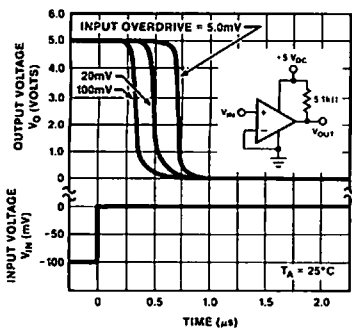
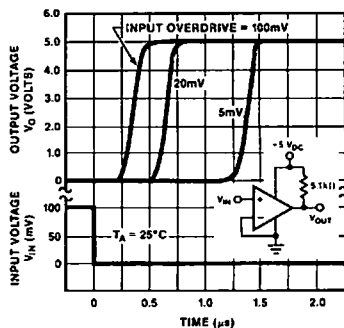
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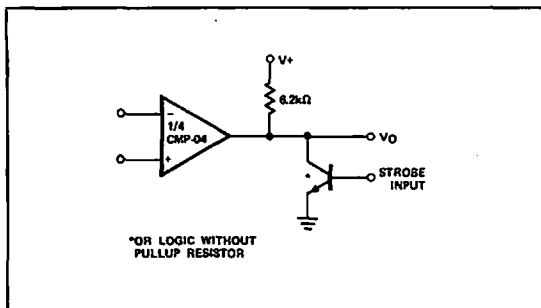
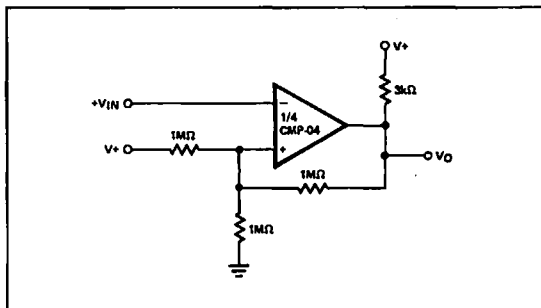
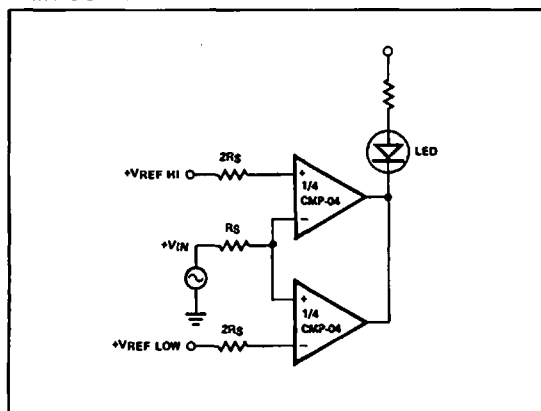
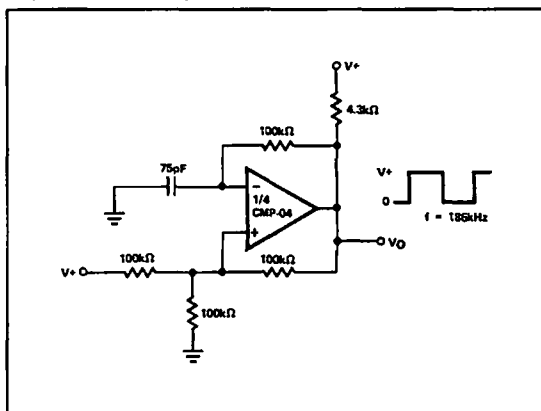
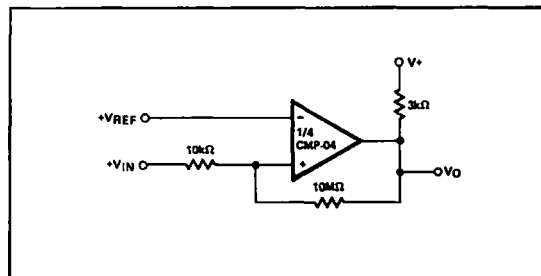
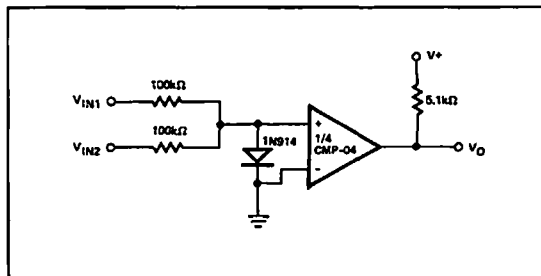
- At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V_+ from 5V; and over the full input common-mode range (0V to $V_+ - 1.5V$).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the

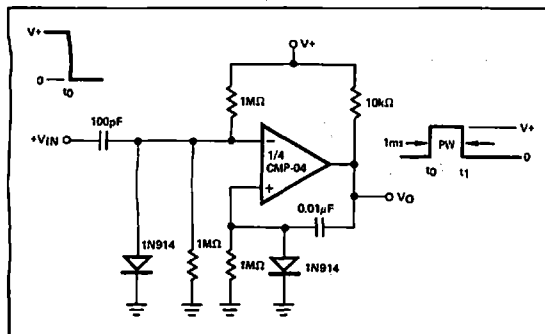
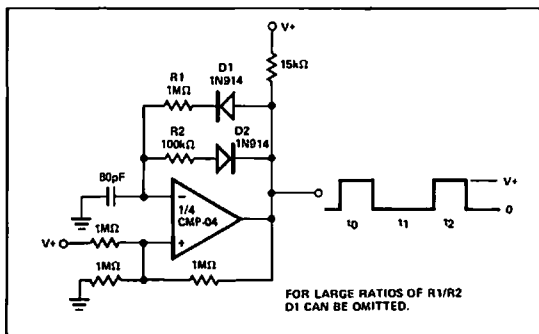
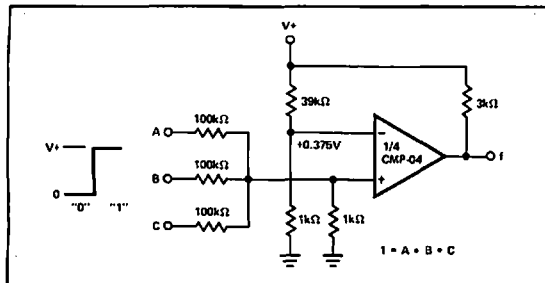
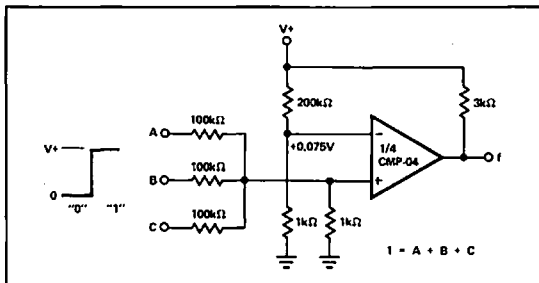
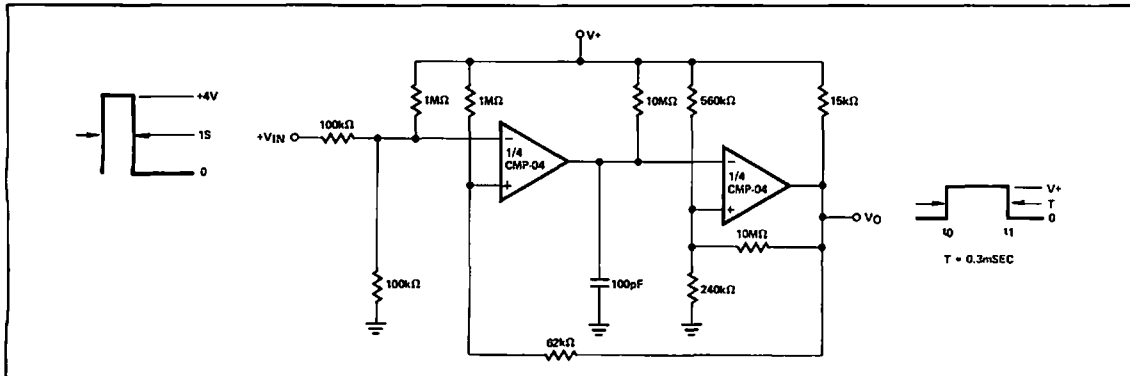
common-mode voltage range is $V_+ - 1.5V$, but either or both inputs can go to $+30V$ without damage.

- Guaranteed by design.
- $R_L \geq 15k\Omega$, $V_{CM} = 1.5V$ to $13.5V$.
- Sample tested.

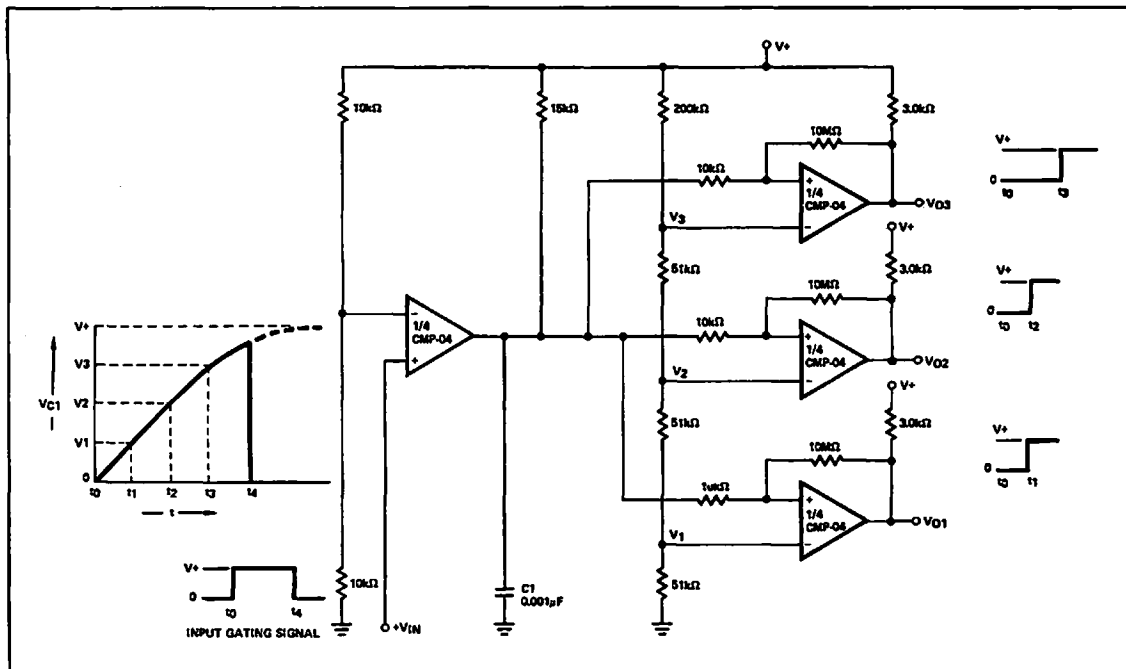
TYPICAL PERFORMANCE CHARACTERISTICS

 OFFSET VOLTAGE
vs TEMPERATURE

 INPUT BIAS CURRENT
vs V_+ AND TEMPERATURE

 INPUT OFFSET CURRENT
vs TEMPERATURE

 VOLTAGE GAIN
vs TEMPERATURE

 SUPPLY CURRENT
vs SUPPLY VOLTAGE

 OUTPUT VOLTAGE vs
OUTPUT CURRENT AND
TEMPERATURE

 RESPONSE TIME FOR
VARIOUS INPUT
OVERDRIVES — NEGATIVE
TRANSITION

 RESPONSE TIME FOR
VARIOUS INPUT
OVERDRIVES — POSITIVE
TRANSITION


TYPICAL APPLICATIONS
OUTPUT STROBING

INVERTING COMPARATOR WITH HYSTERESIS

LIMIT COMPARATOR

SQUAREWAVE OSCILLATOR

NONINVERTING COMPARATOR WITH HYSTERESIS

COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY


ONE-SHOT MULTIVIBRATOR

PULSE GENERATOR

AND GATE

OR GATE

ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT


TIME DELAY GENERATOR





Precision Monolithics Inc.

CMP-05

HIGH-SPEED PRECISION COMPARATOR
(WITH LATCH CIRCUIT)

FEATURES

- Precision Input Stage
 - Input Offset Voltage 150 μ V
 - Input Offset Current 15nA
- Fast Response Time (5mV Overdrive) 38ns
- High Voltage Gain 16,000V/V
- Latch Function with TTL Compatible Input
- TTL Compatible Output
- Available in Hermetic Mini-DIP Package

ORDERING INFORMATION†

25°C V _{OS} (μ V)	PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC		PLASTIC	
	TO-99 8-PIN	DIP 8-PIN	DIP 8-PIN	
600	CMP05BJ*	CMP05BZ*	—	MIL
600	CMP05FJ	CMP05FZ	—	IND
1000	CMP05CJ*	CMP05CZ*	—	MIL
1000	CMP05GJ	CMP05GZ	—	IND
1000	—	—	CMP05GP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-In is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

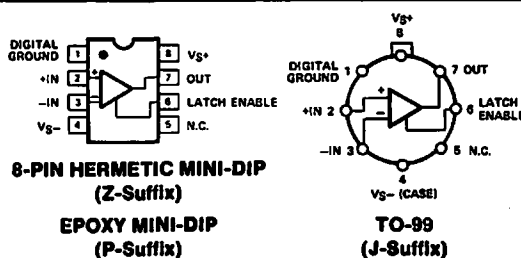
GENERAL DESCRIPTION

The CMP-05's very high speed and precision input specifications make it the ideal comparator in systems needing 12-bit

accuracy along with high speed. An exceptionally fast response time of 60nsec is possible with only 1/2 LSB overdrive (12-bit, 10-volt system).

The CMP-05 design makes it the ideal component in systems requiring high speed with excellent low-level analog signal resolution. High-speed 12-bit successive approximation A/D converters, zero crossing detectors and logic threshold detectors are typical system applications.

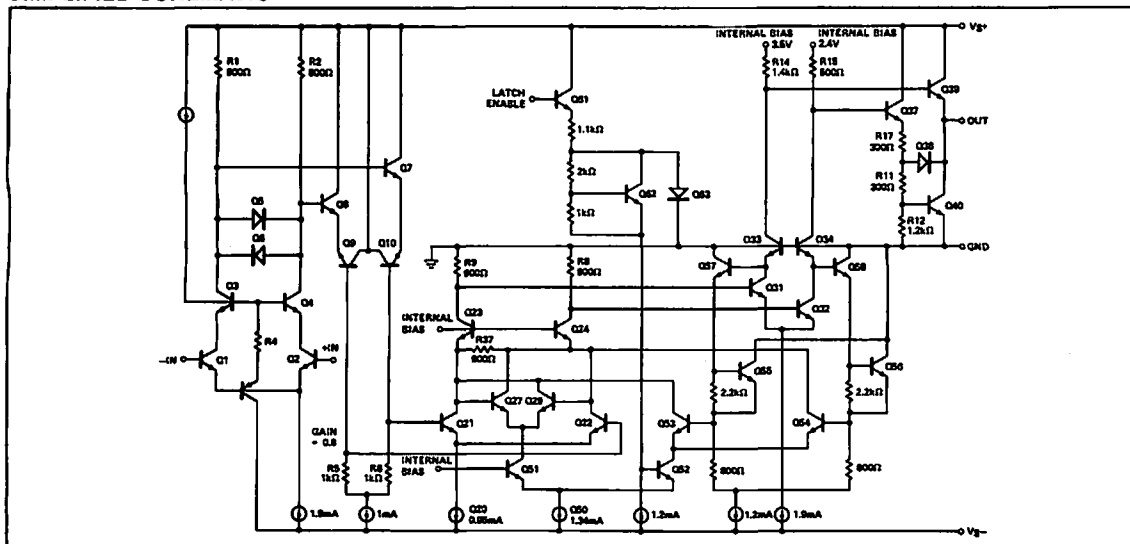
PIN CONNECTIONS



LOGIC TABLE

LATCH ENABLE	OUT
0 or NC	Comparing
1	Latched

SIMPLIFIED SCHEMATIC



VOLTAGE COMPARATORS

**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Positive Supply Voltage	 +6V
Negative Supply Voltage	 -18V
Power Dissipation (Note 1)	 500mW
Differential Input Voltage	 $\pm 5V$
Latch Enable Input Voltage	 -0.5V to V+ Supply
Operating Temperature Range	
CMP-05B/C (J or Z Package)	
(Note 3)	 -55°C to +125°C
CMP-05F/G (J or Z Package)	 -25°C to +85°C
CMP-05G (P Package)	 0°C to +70°C
DICE Junction Temperature (T_J)	 -65°C to +150°C
Storage Temperature Range	 -65°C to +150°C
P-Suffix	 -65°C to +125°C
Lead Temperature (Soldering, 60 sec)	 300°C

Output Short-Circuit Duration — to ground Indefinite
 — to V+ = 5.0V ... 1 Minute

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
Epoxy Mini-DIP (P)	35°C	5.6mW/°C
Hermetic Mini-DIP (Z)	75°C	6.7mW/°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.
2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
3. Latch is functional for -55°C $\leq T_A \leq$ +85°C.

ELECTRICAL CHARACTERISTICS at $V_S^+ = 5.0V$, $V_S^- = -5.0V$, $T_A = 25^\circ C$ and Latch Enable grounded, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05B/F			CMP-05C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	150	600	—	400	1000	μV
Input Offset Current	I_{OS}		—	15	80	—	30	150	nA
Input Bias Current	I_B		—	0.6	1.2	—	0.8	1.8	μA
Voltage Gain	A_{VO}	(Note 1)	8	16	—	7	14	—	V/mV
Input Voltage Range	CMVR	(Note 1)	± 3.0	± 3.3	—	± 3.0	± 3.3	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 3.0V$, (Note 1)	86	91	—	84	89	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.75V$ to $V_S = \pm 5.25V$	—	51	126	—	64	126	$\mu V/V$
		P Package	—	—	—	—	120	360	
		$V_S^+ = 5V$, $V_S^- = -5V$ to -15V	—	15	51	—	18	63	
		P Package	—	—	—	—	38	180	
Output High Voltage	V_{OH}	$V_{IN} \geq 10mV$, $I_O = 0\mu A$	2.4	2.9	—	2.4	2.9	—	V
		$V_{IN} \geq 10mV$, $I_O = 320\mu A$	2.4	2.9	—	—	—	—	
		$V_{IN} \geq 10mV$, $I_O = 200\mu A$	—	—	—	2.4	2.9	—	
			—	—	—	—	—	—	
Saturation Voltage	V_{SAT}	$V_{IN} \leq -10mV$, $I_{SINK} = 0mA$	—	0.13	0.40	—	0.13	0.40	V
		$V_{IN} \leq -10mV$, $I_{SINK} = 8mA$	—	—	—	—	0.28	0.40	
		$V_{IN} \leq -10mV$, $I_{SINK} = 12.8mA$	—	0.32	0.40	—	—	—	
			—	—	—	—	—	—	
Positive Supply Current	I_{S^+}	$V_O \leq 2.4V$, (Note 1)	—	7.5	11	—	8.0	12	mA
		$V_O \leq 0.4V$	—	10	15	—	11	16	
Negative Supply Current	I_{S^-}	$V_O \leq 0.4V$	—	11	16	—	12	18	mA
Power Dissipation	P_d	$V_O \leq 0.4V$	—	105	155	—	115	170	mW
Latch Input Voltage									
Logic 1	V_{LH}	Over Operating Temp. Range Latch Enabled, (Note 1)	2.0	—	—	2.0	—	—	V
Logic 0	V_{LL}	Over Operating Temp. Range Latch Disabled, (Note 1)	—	—	0.8	—	—	0.8	
Latch Input Current									
Logic 1	I_{LH}	$V_{LH} = 3.0V$, (Note 1)	—	10	45	—	10	45	μA
Logic 0	I_{LL}	$V_{LL} = 0.8V$, (Note 1)	—	6	25	—	6	25	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Note 2)	—	60	—	—	60	—	ns
		$V_{OD} = 5.0mV$, (Note 2)	—	41	55	—	41	55	
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Note 2)	—	60	—	—	60	—	ns
		$V_{OD} = 5.0mV$, (Note 2)	—	37	55	—	37	55	
Latch Disable Time	t_{LPD}	(Note 3)	—	50	65	—	50	65	ns

NOTES:

1. Guaranteed by design.
2. Times are for 100mV step inputs. See switching time waveforms.
3. See switching time waveforms.



ELECTRICAL CHARACTERISTICS at $V_{S+} = 5.0V$, $V_{S-} = -5.0V$, and Latch Enable grounded. For CMP-05B/C, $-55^{\circ}C \leq T_A \leq 125^{\circ}C$. For CMP-05F/G, $-25^{\circ}C \leq T_A \leq 85^{\circ}C$ (J, Z Packages) and $0^{\circ}C \leq T_A \leq 70^{\circ}C$ (P Package), unless otherwise noted.

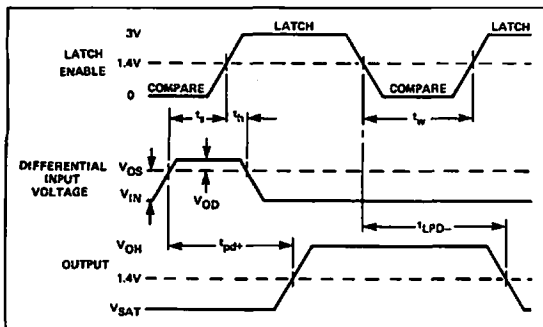
PARAMETER	SYMBOL	CONDITIONS	CMP-05B/F			CMP-05C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	—	0.3	1.5	—	0.55	2.0	mV
Input Offset Voltage Drift	TCV_{OS}		—	1.5	7.5	—	2.5	15	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}		—	40	250	—	70	400	nA
Input Bias Current	I_B		—	1.1	2.5	—	1.5	3.8	μA
Voltage Gain	A_{VO}	(Note 1)	6	11	—	5	10	—	V/mV
Input Voltage Range	CMVR	(Note 1)	± 2.9	± 3.2	—	± 2.9	± 3.2	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$, (Note 1)	83	90	—	80	88	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 4.75V \leq V_S \leq \pm 5.25V$ P Package	—	63	178	—	80	252	$\mu V/V$
Output High Voltage	V_{OH}	$V_{IN} \geq 10mV$, $I_O = 0\mu A$	2.4	—	—	2.4	—	—	V
		$V_{IN} \geq 10mV$, $I_O = 240\mu A$	2.4	—	—	—	—	—	
		$V_{IN} \geq 10mV$, $I_O = 160\mu A$	—	—	—	2.4	—	—	
Saturation Voltage	V_{SAT}	$V_{IN} \leq -10mV$, $I_{SINK} = 0mA$	—	0.18	0.40	—	0.20	0.40	V
		$V_{IN} \leq -10mV$, $I_{SINK} = 9.6mA$	—	0.2	0.40	—	—	—	
		$V_{IN} \leq -10mV$, $I_{SINK} = 6.4mA$	—	—	—	—	0.30	0.40	
Positive Supply Current	I_{S+}	$V_O \leq 0.4V$	—	11	16	—	12	17	mA
Negative Supply Current	I_{S-}	$V_O \leq 0.4V$	—	12	17	—	13	19	mA
Power Dissipation	P_d	$V_O \leq 0.4V$	—	115	165	—	125	180	mW
Latch Input Current									
Logic 1	I_{LH}	$V_{LH} = 3V$, (Notes 1, 4)	—	16	90	—	18	90	μA
Logic 0	I_{LL}	$V_{LL} = 0.8V$, (Notes 1, 4)	—	10	50	—	10	50	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Note 2) $V_{OD} = 5.0mV$, (Note 2)	—	125	—	—	125	—	ns
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Note 2) $V_{OD} = 5.0mV$, (Note 2)	—	92	—	—	92	—	
Latch Disable Time	t_{LPD+}	(Notes 2, 4)	—	115	—	—	115	—	ns
	t_{LPD-}		—	88	—	—	88	—	
Latch Disable Time	t_{LPD+}	(Notes 2, 4)	—	56	—	—	56	—	ns
	t_{LPD-}		—	30	—	—	30	—	

NOTES:

- Guaranteed by design.
- Times are for 100mV step inputs. See switching time waveforms.
- A high on the latch enable input will cause the latch to assume the state

of the comparator and not follow subsequent inputs.

- Latch is functional for $-55^{\circ}C \leq T_A \leq +85^{\circ}C$.

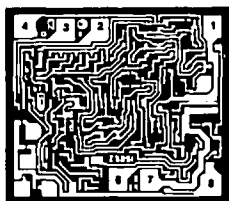
SWITCHING TIME WAVEFORMS**Minimum Input Timing Requirements***

Parameter	Minimum Limit	Units
t_s Setup Time	35	ns
t_h Hold Time	10	
t_w Latch Pulse Width	25	

* t_s , t_h , t_w are tested with $V_{IN} = 100mV$ and $V_{OD} = 5mV$.



DICE CHARACTERISTICS



DIE SIZE 0.052 × 0.046 inch, 2392 sq. mils
(1.321 × 1.168mm, 1.543 sq. mm)

1. DIGITAL GROUND
2. NONINVERTING INPUT
3. INVERTING INPUT
4. NEGATIVE SUPPLY (SUBSTRATE)
6. LATCH ENABLE
7. OUTPUT
8. POSITIVE SUPPLY

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 5V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-05G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	1000	μV MAX
Input Offset Current	I_{OS}		150	nA MAX
Input Bias Current	I_B		1.8	μA MAX
Voltage Gain	A_{VO}	(Note 1)	7	V/mV MIN
Input Voltage Range	CMVR	(Note 1)	± 3.0	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 2.9V$ (Note 1)	80	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 4.75 \leq V_S \leq \pm 5.25$	178	$\mu V/V$ MAX
		$V_{S+} = 5V, V_{S-} = -5V$ to $-15V$	63	
Positive Output Voltage	V_{OH}	$V_{IN} \geq 10mV, I_O = 0\mu A$	2.4	V MIN
Saturation Voltage	V_{SAT}	$V_{IN} \leq 10mV, I_O = 0\mu A$	0.4	V MAX
Positive Supply Current	I_+	$V_O \leq 0.4V$	16	mA MAX
Negative Supply Current	I_-	$V_O \leq 0.4V$	18	mA MAX
Negative Supply Current	I_-	$V_- = -15V, V_O \leq 0.4V$	20	mA MAX
Latch Input Voltage	Logic 1 Logic 0	V_{LH} Latch Enabled	2.0	V MIN
		V_{LL} Latch Disabled	0.8	V MAX
Latch Input Current	Logic 1 Logic 0	I_{LH} $V_{LH} = 3.0V$, (Notes 1, 4)	45	μA MAX
		I_{LL} $V_{LL} = 0.8V$, (Notes 1, 4)	25	
Input to Output High Response Time	t_{pd+}	$V_{OD} = 5.0mV$, (Notes 1, 2)	60	ns MAX
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 5.0mV$, (Notes 1, 2)	60	ns MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 5V$, $T_A = 25^\circ C$, unless otherwise noted.

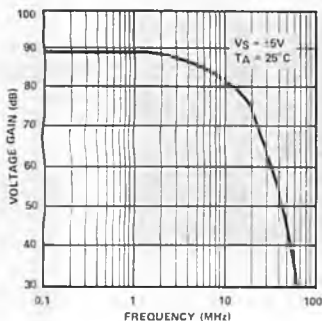
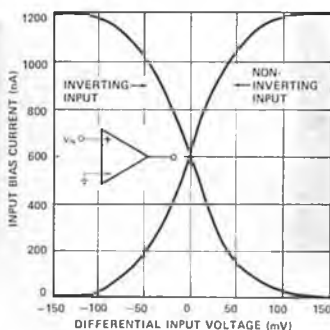
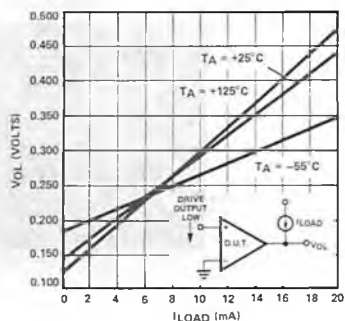
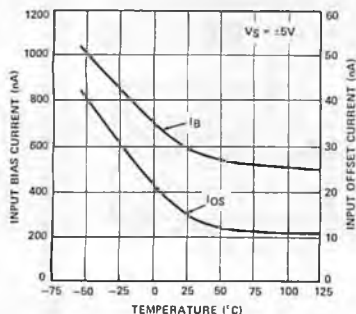
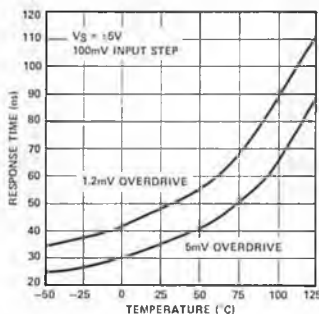
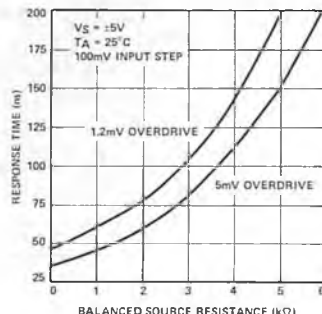
PARAMETER	SYMBOL	CONDITIONS	CMP-05G TYPICAL	UNITS
Input to Output High Response Time	t_{pd+}	$V_{OD} = 1.2mV$, (Note 2)	41	ns
Input to Output Low Response Time	t_{pd-}	$V_{OD} = 1.2mV$, (Note 2)	37	ns
Latch Disable Time	t_{LPD}	(Notes 3, 4)	50	ns

NOTES:

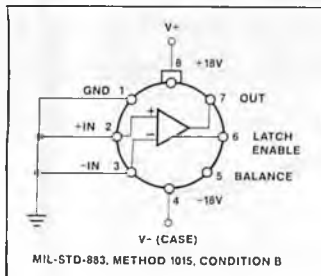
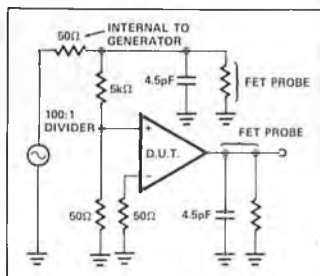
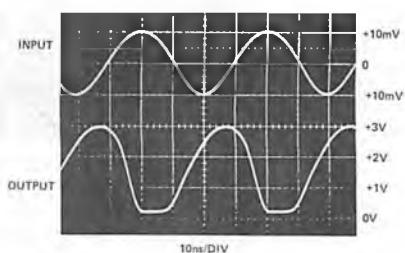
1. Guaranteed by design.
2. Times are for 100mV step inputs.

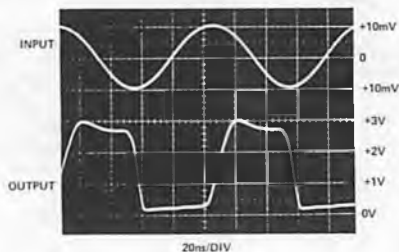
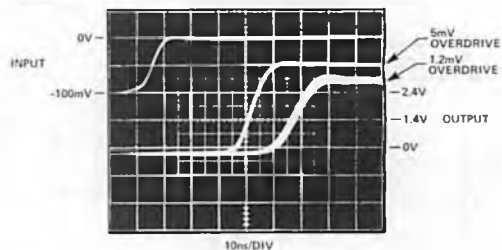
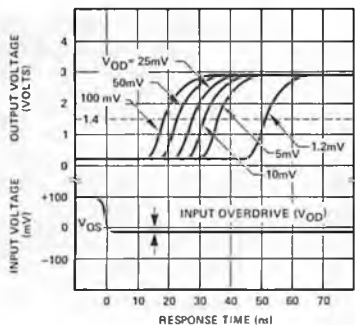
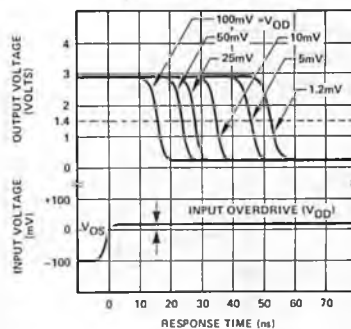
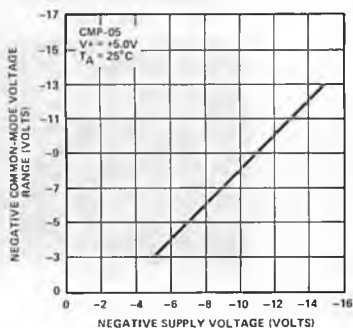
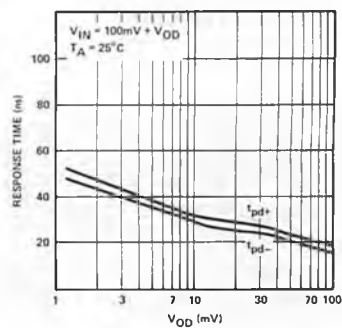
3. See switching time waveforms.
4. Latch is functional for $-55^\circ C \leq T_A \leq 85^\circ C$.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE GAIN
vs FREQUENCY

INPUT BIAS CURRENT
vs DIFFERENTIAL
INPUT VOLTAGE

 V_{SAT} vs LOAD CURRENT

INPUT CURRENTS vs
TEMPERATURE

RESPONSE TIME vs
TEMPERATURE

RESPONSE TIME vs BALANCED
SOURCE RESISTANCE


STANDARD BURN-IN CIRCUIT


RESPONSE PHOTOGRAPH
TEST SET-UP

RESPONSE TO 25MHz
SINE WAVE


TYPICAL PERFORMANCE CHARACTERISTICS
**RESPONSE TO 10MHz
SINE WAVE**

**RESPONSE TIME
TO 5mV AND 1.2mV
(= 1/2 LSB) OVERDRIVES**

 t_{pd+} RESPONSE TIME

 t_{pd-} RESPONSE TIME

**CMP-05 NEGATIVE COMMON-
MODE INPUT RANGE vs
NEGATIVE SUPPLY**

**RESPONSE TIME vs
OVERDRIVE VOLTAGE**


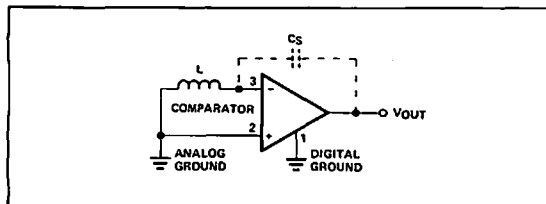
APPLICATION INFORMATION

The CMP-05 is a very accurate device providing fast response time even with small—Microvolt level—overdrives. To achieve this performance requires high gain at high frequencies. As shown in the voltage gain versus frequency curve, the gain—bandwidth product of the CMP-05 is 1.5×10^{11} Hz. It maintains its full gain to approximately 8MHz and rolls off at a very fast rate beyond that frequency due to the fact that five poles occur in the 30 to 60MHz range. At 30MHz the gain of the comparator is still 2000. Therefore, in the transition region small values of source lead inductance and stray feedback capacitance can cause an oscillatory condition.

For example (in the figure below) with $L = 0.1 \mu\text{H}$, $C_S = 0.15 \text{pF}$, the closed-loop gain of the circuit at 30MHz is:

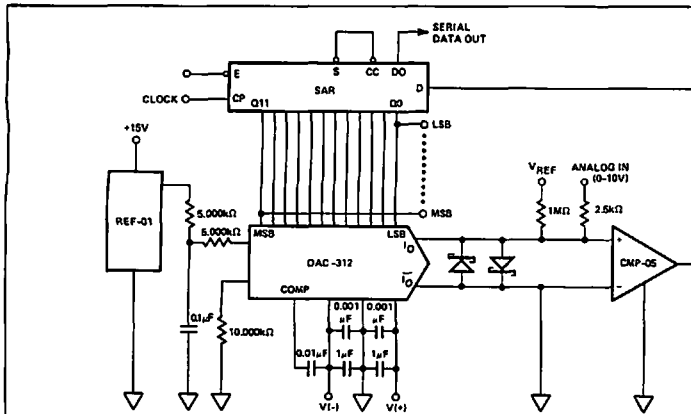
$$A_V = \frac{1}{LC_S \omega^2} = \frac{1}{10^{-7} \times 0.15 \times 10^{-12} \times (2\pi \times 30 \times 10^6)^2} = 1880$$

POTENTIAL FEEDBACK SOURCES



With the open-loop gain at 2000 oscillation will occur since the phase shift exceeds 180° . To minimize these problems power supplies should be decoupled, lead lengths should be kept as short as possible, and a ground plane should be used to reduce the stray feedback capacitance. In addition, a ground plane substantially diminishes the possibility of the output current spike coupling back to the inputs through the ground lead. Keeping a separate digital ground (pin 1) and analog ground (to which the inputs are referenced) also reduces the magnitude of the problem.

12-BIT FAST A/D CONVERTER



NOTE:
DEVICE(S) CONNECTED TO ANALOG INPUT MUST BE CAPABLE OF SOURCING 4.0mA.
A BUFFER (eg. BUF-03) MAY BE REQUIRED.

Fortunately, in high-speed circuitry the comparator inputs will be driven at a fast rate, in which case no transition region oscillations will occur. As the minimum slew rate versus source resistance curve indicates, if the input is driven at a rate exceeding $6 \text{mV}/\mu\text{sec}$, no oscillations will occur with source resistors of less than $1 \text{k}\Omega$. Examples of "clean" transitions can be observed in the photographs of the response time with 5mV and 1.2mV overdrives, and the response to the 10 and 25MHz input signals.

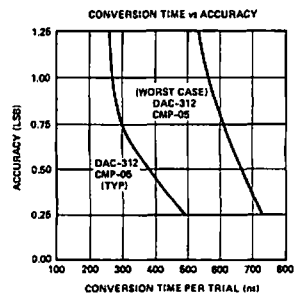
In order to not degrade its speed the CMP-05's inputs are not internally clamped. If large differential voltages are present it is recommended that the inputs be clamped with high speed, low capacitance diodes such as the H.P. 5082-2835, which is a Schottky Diode.

As in all high-speed devices, it is to the user's advantage to keep the source impedances low and matched.

LATCH

The CMP-05 has a latch feature which functions over -55°C to $+85^\circ\text{C}$. When the latch is enabled, the output stays in its existing logic state regardless of the input signal. The input timing requirements of the latch are presented in the Switching Time Waveforms. The latch opens up a broader applications area at no sacrifice in total system speed. Effectively, the latch allows high speed sampling of comparison decisions. This is important in automatic test equipment limit comparators, in measuring pods used in logic analyzers and other similar synchronous measurement circuitry needing fast clocking frequencies. The latch pulse width t_w allows sampling of input signals to take place in 25nsec.

The latch prevents self oscillation (due to positive feedback) from taking place when slowly-moving high-source-impedance signals pass thru the linear amplification region of the comparator. This is successfully accomplished by rapidly strobing the comparator near its minimum t_w time which prevents self oscillation from making a complete cycle since t_w is shorter than the total response time t_{pd} through the comparator.



CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
CMP-05	82	125
TOTAL	375ns	680ns
$\times 13$	4.9 μs	8.8 μs



CMP-08

HIGH-SPEED COMPARATOR WITH ECL OUTPUTS

Precision Monolithics Inc.

FEATURES

- Complementary Emitter-Coupled-Logic Outputs
- 50 Ω Line Driving Capability
- Excellent Stability; Resists Oscillation
- Propagation Delay at 5mV Overdrive,
Over Full Operating Temperature Range:
 - Industrial Temperature Range 9.5ns Max
 - Military Temperature Range 12.0ns Max
- Over 100MHz Output Bandwidth
- Space-Saving 8-Pin DIP
- High Performance, Low Price

ORDERING INFORMATION†

PACKAGE	OPERATING TEMPERATURE RANGE
CERDIP	
CMP08BZ*	MIL
CMP08FZ	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The CMP-08 is a very high-speed voltage comparator which provides complementary Emitter-Coupled-Logic (ECL) outputs. It is particularly suitable for level-crossing detection and sinewave-squaring applications with input amplitude as low as 2 millivolts.

Fiber-optics and communications circuits will find the CMP-08 attractive. Its high sensitivity, low drift, stability, and wide-

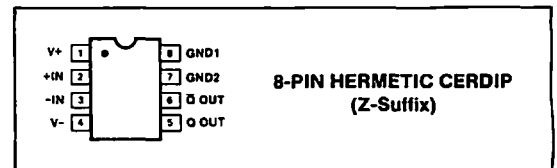
band operation make CMP-08 excellent for signal recovery and pulse-shaping applications. With its ECL-logic outputs and bandwidth over 100MHz, the performance of CMP-08 is double that of comparable TTL-output devices.

The CMP-08 offers consistent delay, with low delay variation as a function of temperature or overdrive. This provides excellent timing resolution in 10-30MHz computer peripheral applications. If necessary, conversion to TTL levels can be easily performed after initial processing with ECL logic.

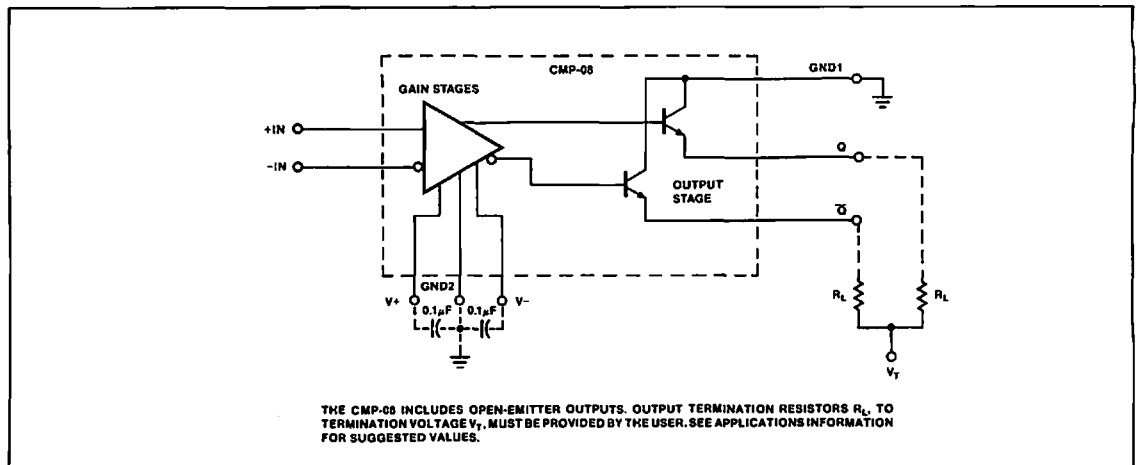
The CMP-08 is specified for operation using +5V and -5.2V supplies. With 5% supply tolerance, input voltage range includes -3.0V to +2.7V over all operating temperatures. In applications such as video systems, the CMP-08 input voltage range and sensitivity permit a dynamic range of over 60dB to be achieved. For added flexibility, the positive input voltage limit may be extended by using a +6V positive supply rather than +5V. It is also possible to use a -5V supply, when the -5.2V supply is not available.

When AC system layout rules are used, the excellent stability of CMP-08 eliminates the need for an on-chip latch. If needed, the latch function may be performed within digital logic. With its space-saving 8-pin DIP and low price, the CMP-08 provides an excellent alternative to Am685-type devices.

PIN CONNECTIONS



CONNECTION DIAGRAM



**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Positive Supply Voltage	+6.5V
Negative Supply Voltage	-6.0V
Input Voltage	±4V
Differential Input Voltage	±6V
Output Current	30mA
Power Dissipation (Note 2)	500mW
Operating Temperature Range (Note 3)	
CMP-08B	-55°C to +125°C
CMP-08F	-30°C to +85°C

Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature (T _J)	-65°C to +165°C

NOTES:

- Beyond which the useful life may be impaired.
- Derate by 9mW/°C above +105°C ambient.
- Device in thermal equilibrium with 500 LFPM transverse airflow.

ELECTRICAL CHARACTERISTICS at V₊ = +5V, V₋ = -5.2V, V_T = -2V, R_L = 50Ω; -55°C ≤ T_A ≤ +125°C for CMP-08B; -30°C ≤ T_A ≤ +85°C for CMP-08F, unless otherwise noted.

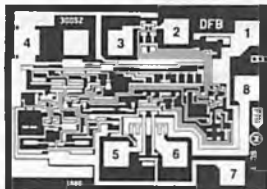
PARAMETER	SYMBOL	CONDITIONS	CMP-08F			CMP-08B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V _{OS}	R _S = 50Ω	-2.5	—	+2.5	-3.0	—	+3.0	mV
Average Input Offset Voltage Drift	TCV _{OS}	R _S = 50Ω	—	5	—	—	5	—	μV/°C
Input Offset Current	I _{OS}		-1.3	—	+1.3	-1.6	—	+1.6	μA
Input Bias Current	I _B		—	—	13	—	—	16	μA
Input Voltage Range	CMVR	(Note 3)	-3.0	—	+2.7	-3.0	—	+2.7	V
Common-Mode Rejection Ratio	CMRR		80	—	—	80	—	—	dB
Power Supply Rejection Ratio	PSRR	(Note 1)	80	—	—	80	—	—	dB
Small Signal Gain, Linear Region	A _V	T _A = 25°C	800	1200	—	800	1200	—	V/V
Input Resistance	R _{IN}	T _A = 25°C	6	—	—	6	—	—	kΩ
Input Capacitance	C _{IN}	T _A = 25°C	—	3	—	—	3	—	pF
Output HIGH Voltage (Note 2)	V _{OH}	T _A = 25°C	-0.960	—	-0.810	-0.960	—	-0.810	V
		T _A = T _A (MIN)	-1.060	—	-0.890	-1.100	—	-0.920	
		T _A = T _A (MAX)	-0.890	—	-0.700	-0.850	—	-0.620	
Output LOW Voltage (Note 2)	V _{OL}	T _A = 25°C	-1.950	—	-1.650	-1.950	—	-1.650	V
		T _A = T _A (MIN)	-1.950	—	-1.660	-1.950	—	-1.660	
		T _A = T _A (MAX)	-1.950	—	-1.625	-1.950	—	-1.575	
V ₊ Supply Current	I ₊		—	—	15	—	—	15	mA
V ₋ Supply Current	I ₋		—	—	26	—	—	26	mA
SWITCHING CHARACTERISTICS									
Propagation Delay	t _{PD}	(Notes 4, 6)	—	6.5	9.5	—	6.5	12	ns
Output Edge Rate	t _H , t _F	T _A = 25°C (Note 5)	—	2	—	—	2	—	ns

NOTES:

- Tested with a ±5% supply variation.
- Specifications apply when the device is in thermal equilibrium with 500 LFPM transverse airflow. Actual test limits must be corrected for thermal offset between test conditions and airflow equilibrium.
- Specified input voltage range is for V₊ = +5V ±5% and for V₋ = -5.2V ±5%. CMVR will change if other supply voltages are used. Recommended supply limits are V₊ = +4.75V to +6.3V, V₋ = -4.7V to -5.7V. CMVR is guaranteed by I_B and CMRR tests.
- Propagation delay is specified for 100mV input voltage step, 5mV overdrive beyond the offset voltage.
- Output rise/fall time 20%–80% with input amplitude 20mV peak-to-peak, 2ns input rise/fall time.
- This parameter is sample tested at 25°C. Typical number represents 25°C operation.



DICE CHARACTERISTICS



DIE SIZE: 0.056×0.041 inch, 2296 sq. mils
(1.42×1.04 mm, 1.48 sq. mm)

- 1. V+ Positive Supply
- 2. +IN NonInverting Input
- 3. -IN Inverting Input
- 4. V- Negative Supply
- 5. Q True Output
- 6. $\bar{Q}$ Complement Output
- 7. GND2 Circuit Ground
- 8. GND1 Output Ground

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V+ = +5V$, $V- = -5.2V$, $V_T = -2V$, $R_L = 50\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

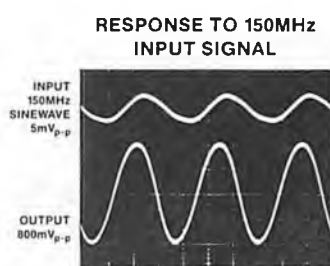
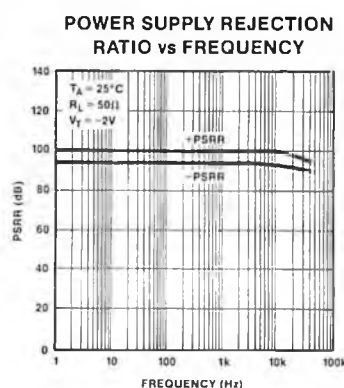
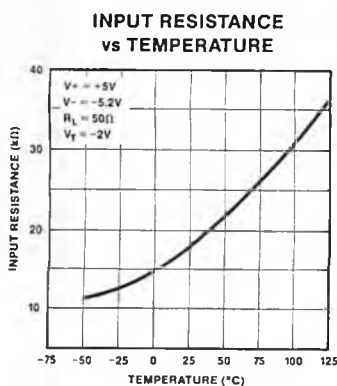
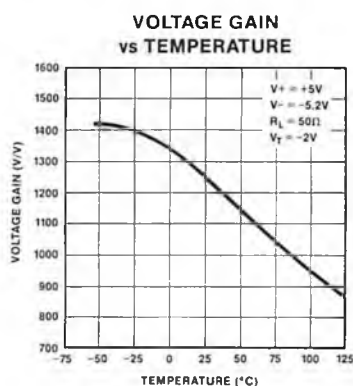
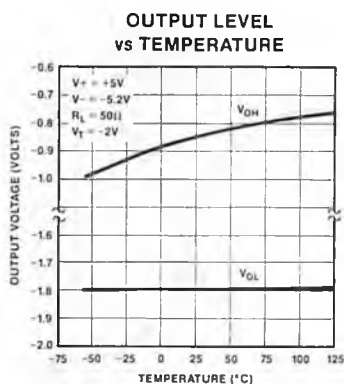
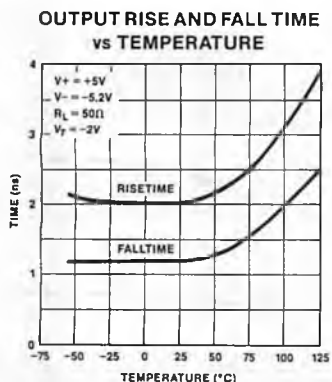
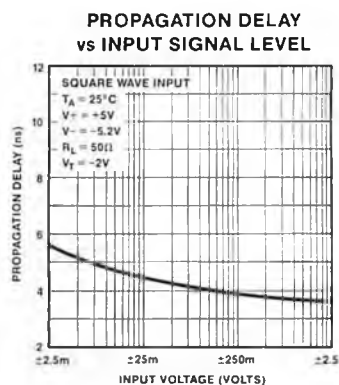
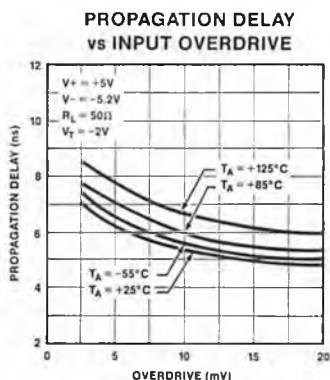
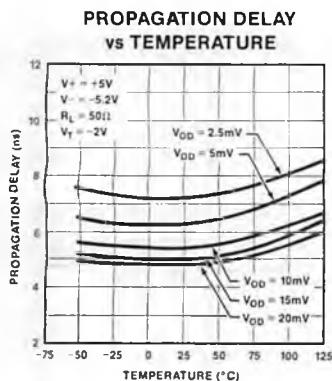
PARAMETER	SYMBOL	CONDITIONS	CMP-08N		UNITS
			MIN	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	-2.2	+2.2	mV
Input Offset Current	I_{OS}		-1.0	+1.0	μA
Input Bias Current	I_B		—	10	μA
Input Voltage Range	CMVR	(Note 1)	-3.0	+2.7	V
Common-Mode Rejection Ratio	CMRR		80	—	dB
Power Supply Rejection Ratio	PSRR	$V+ = +4.75V$ to $+5.25V$, $V- = -4.94V$ to $-5.46V$	80	—	dB
Small-Signal Gain, Linear Region	A_V		800	—	V/V
Input Resistance	R_{IN}		6	—	k Ω
Output HIGH Voltage	V_{OH}	(Note 2)	-0.960	-0.810	V
Output LOW Voltage	V_{OL}	(Note 2)	-1.950	-1.650	V
V+ Supply Current	$I+$		—	15	mA
V- Supply Current	$I-$		—	26	mA

NOTES:

- CMVR is measured using $V+ = +4.75V$, $V- = -4.94V$ (worst-case).
- The V_{OH} and V_{OL} specifications are temperature sensitive. Since $T_A = 25^\circ C$ at wafer sort does not correspond to the same junction temperature as $T_A = 25^\circ C$ for packaged units, the actual test limits are corrected to allow for temperature offset.

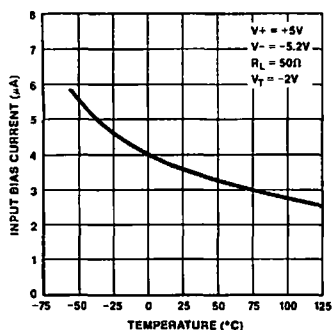
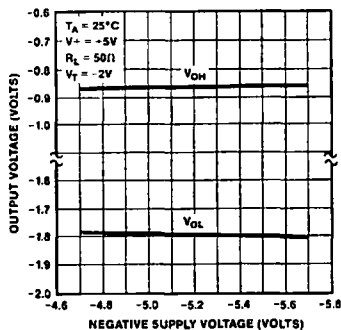
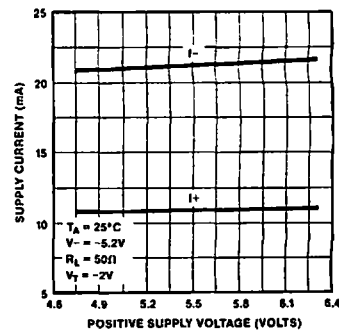
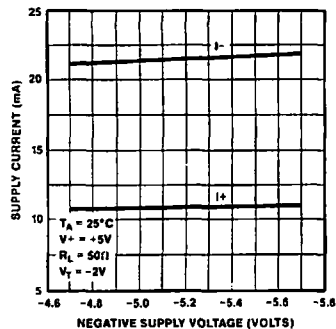
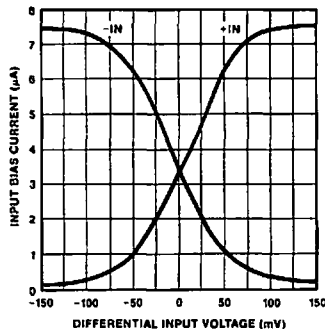
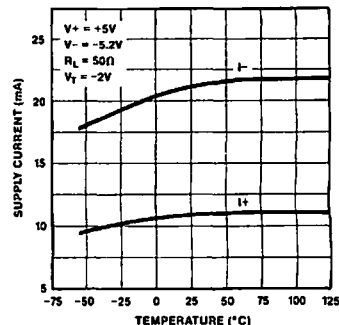
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

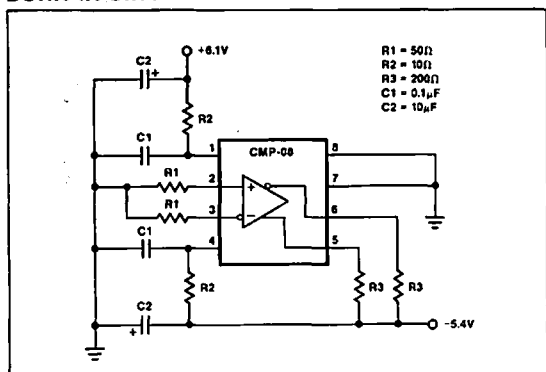




TYPICAL PERFORMANCE CHARACTERISTICS

INPUT BIAS CURRENT
vs TEMPERATUREOUTPUT LEVEL vs
NEGATIVE SUPPLY VOLTAGESUPPLY CURRENT vs
POSITIVE SUPPLY VOLTAGESUPPLY CURRENT vs
NEGATIVE SUPPLY VOLTAGEINPUT CURRENT
vs DIFFERENTIAL
INPUT VOLTAGESUPPLY CURRENT
vs TEMPERATURE

BURN-IN CIRCUIT



APPLICATIONS INFORMATION

POWER SUPPLIES

The CMP-08 uses a $V+$ positive supply, $V-$ negative supply, and GND. Recommended operating limits for $V+$ are +4.75V to +6.3V. Recommended operating limits for $V-$ are -4.7V to -5.7V.

The GND2 pin is the circuit ground for internal bias and logic level reference. The GND1 pin is output signal return ground for the output transistor collectors.

OUTPUT TERMINATION AND LOADING

The CMP-08 outputs are ECL logic open-emitter transistors. Each output requires a pulldown resistor, which must be provided on the circuit board. Output logic level DC limits are specified for pulldown $R_L = 50\Omega$ to termination voltage $V_T = -2V$.

When the -2V termination voltage is available, the practical pulldown resistor range is 50Ω to 100Ω . If the user does not wish to provide a -2V supply, then pulldown may be to -5.2V with 200Ω to 300Ω resistors. Alternatively, each output may be loaded with 82Ω to GND and 130Ω to -5.2V, to generate the Thevenin equivalent of 50Ω to -2V.

The effect of various termination values on output logic levels may be estimated by assuming 7Ω as the output source resistance. There are AC effects as well. The CMP-08 is a high-gain broadband device, with stability dependent to some extent on output loading.

Optimum damping is achieved when both outputs are equally terminated with 50Ω to -2V or the Thevenin equivalent, with capacitive load below $10pF$ per output, and less than $5pF$ load mismatch. Avoid the use of only one output. Some loss of input resolution may occur when termination resistance exceeds 50Ω , or with greater capacitive loading.

INPUT RESOLUTION

All comparators have input resolution limited by gain and noise. Fast, broadband devices generally have less input resolution than traditional, slow comparators. The CMP-08 offers a good combination of input resolution and performance.

To obtain "hard" output logic voltage swing over the full operating temperature range, a minimum input voltage increment of about $1.5mV$ is required. Smaller input increments can be resolved if the CMP-08 outputs are used differentially, or if the CMP-08 drives the data input to a latch or flip-flop.

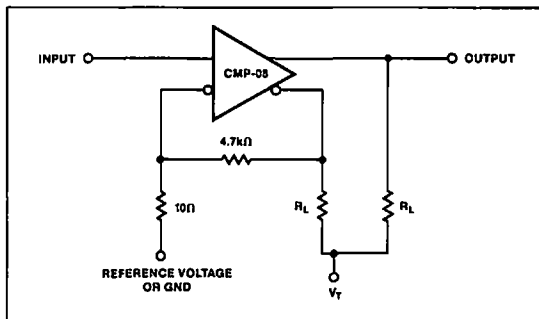
In the linear transfer region, the CMP-08 broadband noise is approximately $0.1mV$ RMS, or $0.5mV$ peak-to-peak. This provides a limit to the repeatability of any comparison decision.

ADDING HYSTERESIS

With its excellent stability, the CMP-08 will not require hysteresis in most applications. Hysteresis may be beneficial if the input voltage may come to rest within $2mV$ of threshold, or if the input slew rate is below $0.5V/ns$ through threshold. The use of hysteresis will provide sharp output transitions even when inputs are slow, and will reduce the likelihood of invalid output transitions due to noise.

Figure 1 shows hysteresis added to a CMP-08 circuit, with single-ended input and output signals. Pulldown resistors R_L to termination voltage V_T are required as usual. With the illustrated values of $4.7k\Omega$ to output and 10Ω to ground, switching points at $-1.1mV$ and $-3.9mV$ are typically obtained. In most DC-coupled applications, the hysteresis trip points must be offset to other values. This may be accomplished by connecting the 10Ω resistor to a reference voltage other than ground, provided that the reference voltage is carefully decoupled. In small-signal applications, variations in switching points due to output voltage variations, resistance tolerance, and offset voltage must be taken into account. Note that the source resistance seen at the feedback node has been kept small, to avoid excessive phase shift due to RC time constants.

FIGURE 1: Optional Hysteresis Circuit



INPUT VOLTAGE RANGE

The CMP-08 positive common-mode input voltage range extends at least to $2.05V$ below the $V+$ supply. The negative common-mode range extends at least to $1.94V$ above the $V-$ supply.

The application of either input signal above the positive common-mode range may cause undesirable operation. On the negative end, the CMP-08 will function properly if one or the other input is outside the common-mode range (but within the absolute maximum limits), provided that the other input is within the common-mode range.

In all cases, the maximum differential signal between $+IN$ and $-IN$ must be kept within the $\pm 6V$ absolute maximum rating.



CIRCUIT BOARD DESIGN

The CMP-08 is a high-gain broadband device. The circuit board must use RF design practices for proper operation. Wire-wrap techniques are unlikely to be successful.

The V+ and V- supplies must be decoupled to ground using low inductance capacitors installed adjacent to the CMP-08 supply pins. The use of 0.1 μ F ceramic capacitors with closely trimmed leads (or leadless) is recommended.

The circuit board should include a solid ground plane, at least in the neighborhood of the CMP-08 and overlying its input and output signal traces. When a -2V termination

supply is used, it should be decoupled to ground adjacent to the CMP-08 output pulldown resistors.

Best operation is obtained when the CMP-08 is soldered directly to the circuit board. Successful operation is also obtained with the use of low-profile machined-contact sockets, which are designed for high-speed applications.

ECL-TO-TTL TRANSLATION

The MC10125 or MC10H125 quad ECL-to-TTL translator devices may be used to convert the CMP-08 ECL outputs to a TTL-compatible signal.



Precision Monolithics Inc.

CMP-404

QUAD LOW-POWER PRECISION COMPARATOR

FEATURES

- Very Low Power Consumption 1.5mW Max
- Low Input Offset Voltage 1mV Max
- Very Low Drift $3\mu\text{V}/^\circ\text{C}$ Typ
- High Output-Drive Current 25mA Typ
- Single or Dual Supply Operation
- Ideal for CMOS Logic Interface
- LM139 Pinout

ORDERING INFORMATION†

25°C V_{OS} (mV)	HERMETIC DIP PACKAGE	OPERATING TEMPERATURE RANGE
1	CMP404AY*	MIL
2	CMP404BY*	MIL
1	CMP404EY	IND
2	CMP404FY	IND

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

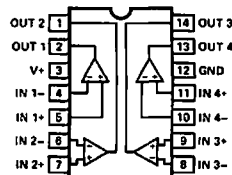
GENERAL DESCRIPTION

Four precision-input comparators provide excellent speed with low power consumption through use of a novel Schottky-clamped design. These open-collector output comparators only consume 365 microwatts each, yet they make accurate 5mV decisions in only four microseconds. In addition, they can drive load currents of 25mA. This output stage is ideal for driving relays, lamps, and LEDs.

The low input-offset-voltage makes the CMP-404 an ideal companion to CMOS logic when the stability and accuracy of a bipolar technology is needed along with low power consumption. The open-collector outputs with pull-up resistors provide CMOS interface with excellent noise immunity. Improved isolation between comparators was achieved by use of an independent bias circuit for each comparator. This is especially important when one comparator is detecting low-level signals while an adjacent comparator is being driven by a high-level signal. In single-supply operation, the inputs can operate at ground. The CMP-404 can operate from 5 to 30 volts single supply or ± 2.5 to ± 15 volts dual supply.

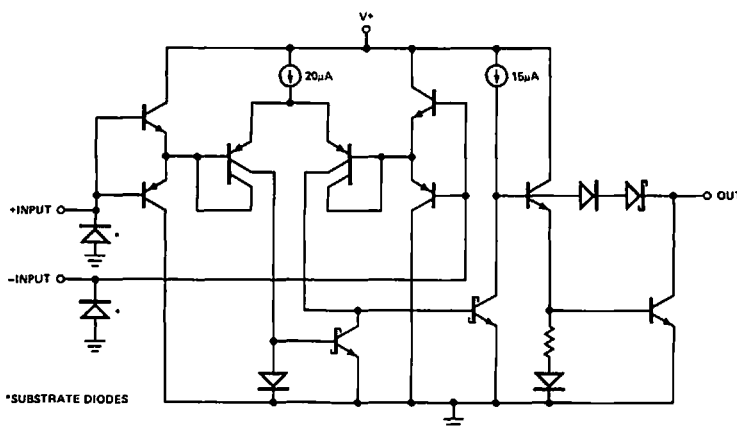
Window comparators, limit comparators, multivibrators, one shots, voltage-controlled oscillators, and set-point detectors are common applications.

PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)

SIMPLIFIED SCHEMATIC (1/4 OF CMP-404)



VOLTAGE COMPARATORS

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage	36V or $\pm 18V$
Input Voltage	$-0.3V$ to $V+$
Output Voltage	$-0.3V$ to $36V$
Power Dissipation	500mW
Derate Above $100^{\circ}C$ by	$10mW/^{\circ}C$
Thermal Resistance (θ_{JA})	$100^{\circ}C/W$
Operating Temperature Range	
CMP-404EY/FY	$-25^{\circ}C$ to $+85^{\circ}C$
CMP-404AY/BY	$-55^{\circ}C$ to $+125^{\circ}C$
DICE Junction Temperature (T_J)	$-65^{\circ}C$ to $+150^{\circ}C$

Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Input Current (Note 2)	20mA
Output Short-Circuit to $V+$ (Note 3)	50mA
Lead Temperature (Soldering, 60 sec)	$300^{\circ}C$

NOTE:

1. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.
2. Limit for input current that flows when input voltage signals exceed $V+$ or GND forward biasing internal junctions.
3. Short circuits to $V+$ can cause excessive heating and eventual destruction. The maximum output current is 50mA.

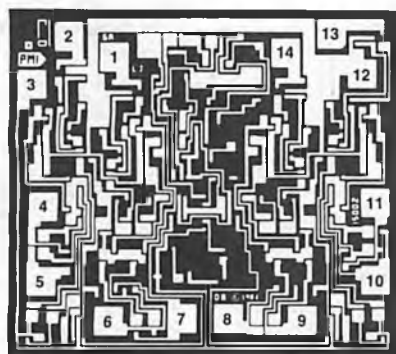
ELECTRICAL CHARACTERISTICS at $V+ = 5V$, $R_L = 5.1k\Omega$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ for CMP-404AY/BY; $-25^{\circ}C \leq T_A \leq 85^{\circ}C$ for CMP-404 EY/FY, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-404A/E			CMP-404B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$, $T_A = 25^{\circ}C$	—	—	1	—	—	2	mV
		$R_S = 50\Omega$, Full Temp	—	—	2	—	—	3	mV
Average Input Offset Voltage Drift	TCV_{OS}	$R_S = 50\Omega$	—	3	—	—	3	—	$\mu V/^{\circ}C$
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25^{\circ}C$	—	3	10	—	3	25	nA
		$I_{IN(+)} - I_{IN(-)}$, Full Temp	—	—	50	—	—	100	nA
Input Bias Current	I_B	$I_{IN(+)} \text{ or } I_{IN(-)}$, $T_A = 25^{\circ}C$	—	10	50	—	10	100	nA
		$I_{IN(+)} \text{ or } I_{IN(-)}$, Full Temp	—	—	100	—	—	200	nA
Voltage Gain	A_V	$R_L = 15k\Omega$	50	400	—	50	400	—	V/mV
Small-Signal Response Time	t_r	$V_{OD} = 5mV$, $V_{STEP} = 100mV$ $R_L = 5.1k\Omega$, $T_A = 25^{\circ}C$ (Note 4)	—	3.5	5	—	3.5	5	μs
Large-Signal Response Time	t_r	$V_{IN} = TTL$ Logic Swing $V_{REF} = 1.4V$, $R_L = 5.1k\Omega$	—	0.8	—	—	0.8	—	μs
Input Voltage Range	CMVR	$T_A = 25^{\circ}C$	0	—	$V+ - 1.5$	0	—	$V+ - 1.5$	V
		$T_A = \text{Full Temp}$	0	—	$V+ - 2$	0	—	$V+ - 2$	V
Common-Mode Rejection Ratio	CMRR	$R_L = 15k\Omega$, (Note 6)	75	85	—	75	85	—	dB
Saturation Voltage	V_{OL}	$T_A = 25^{\circ}C$, (Note 2)	—	0.32	0.4	—	0.32	0.4	V
		Full Temp, (Note 2)	—	—	0.5	—	—	0.5	V
Output Sink Current	I_{SINK}	$V_{IN(-)} = 1V$ $V_{IN(+)} = 0V$, $V_O = 2V$, (Note 5)	10	25	—	10	25	—	mA
Output Leakage Current	I_{LEAK}	$T_A = 25^{\circ}C$, (Note 3)	—	0.01	0.1	—	0.01	0.1	μA
		Full Temp, (Note 3)	—	—	0.4	—	—	0.4	μA
Power Supply Rejection Ratio	PSRR	$V+ = 5V$ to $30V$, $R_L = 15k\Omega$	75	100	—	65	100	—	dB
Supply Current	$I+$	$R_L = \infty$	—	220	300	—	220	350	μA

NOTES:

1. Typical values are reported for $T_A = 25^{\circ}C$.
2. $I_{SINK} = 1mA$, $V_{IN(-)} = 1V$, $V_{IN(+)} = 0V$
3. $V_{IN(-)} = 0V$, $V_{IN(+)} = 1V$, $V_O = 30V$
4. Guaranteed by design. See response-time test circuit.
5. Output Sink Current should be limited to 50mA by external resistance.
6. Applies over the CMVR range.

DICE CHARACTERISTICS



DIE SIZE 0.069 × 0.077 inch, 5313 sq. mils
(1.753 × 1.956 mm, 3.43 sq. mm)

- | | |
|---------------------------|----------------------------|
| 1. OUTPUT (2) | 8. INVERTING INPUT (3) |
| 2. OUTPUT (1) | 9. NONINVERTING INPUT (3) |
| 3. POSITIVE SUPPLY | 10. INVERTING INPUT (4) |
| 4. INVERTING INPUT (1) | 11. NONINVERTING INPUT (4) |
| 5. NONINVERTING INPUT (1) | 12. GROUND |
| 6. INVERTING INPUT (2) | 13. OUTPUT (4) |
| 7. NONINVERTING INPUT (2) | 14. OUTPUT (3) |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = 5V$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	CMP-404G LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 50\Omega$	2	mV MAX
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$	25	nA MAX
Input Bias Current	I_B	$I_{IN(+)} \text{ or } I_{IN(-)}$	100	nA MAX
Voltage Gain	A_V	$R_L = 15k\Omega$	50	V/mV MIN
Input Voltage Range	CMVR		$V_+ - 1.5$	V MAX
Common-Mode Rejection Ratio	CMRR	$R_L = 15k\Omega$	75	dB MIN
Power Supply Rejection Ratio	PSRR	$V_+ = 5V \text{ to } 30V$, $R_L = 15k\Omega$	65	dB MIN
Saturation Voltage	V_{OL}	$I_{SINK} = 1mA$	0.4	V MAX
Output Sink Current	I_{SINK}	$V_{IN(-)} = 1V$ $V_{IN(+)} = 0V$, $V_O = 2V$	10	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN(-)} = 0V$ $V_{IN(+)} = 1V$, $V_O = 30V$	0.1	μA MAX
Supply Current	I_+	$R_L = \infty$	300	μA MAX

NOTE:

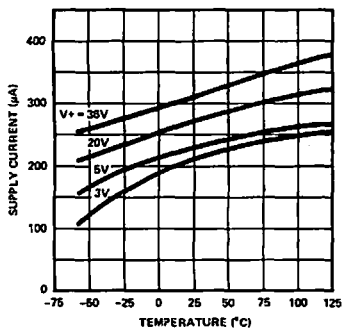
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = 5V$, unless otherwise noted.

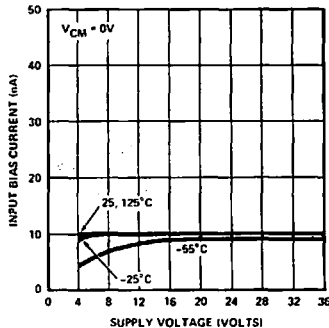
PARAMETER	SYMBOL	CONDITIONS	CMP-404G TYPICAL	UNITS
Large-Signal Response Time	t_r	$V_{IN} = \text{TTL Logic Swing}$ $V_{REF} = 1.4V$, $R_L = 5.1k\Omega$	0.8	μs
Small-Signal Response Time	t_r	$V_{OD} = 5mV$, $V_{STEP} = 100mV$ $R_L = 5.1k\Omega$	3.5	μs

TYPICAL PERFORMANCE CHARACTERISTICS

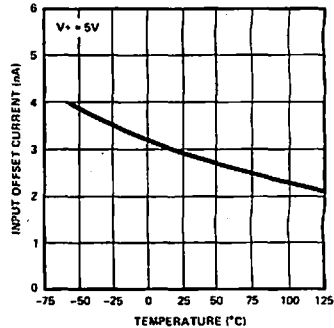
**SUPPLY CURRENT
vs TEMPERATURE**



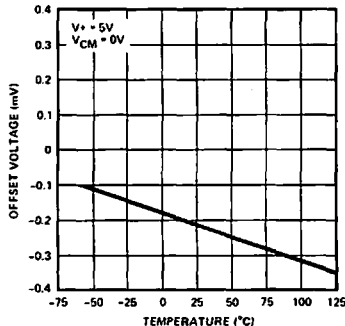
**INPUT BIAS CURRENT
vs SUPPLY VOLTAGE**



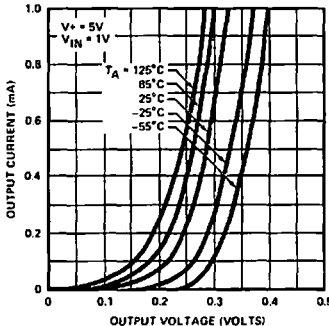
**INPUT OFFSET CURRENT
vs TEMPERATURE**



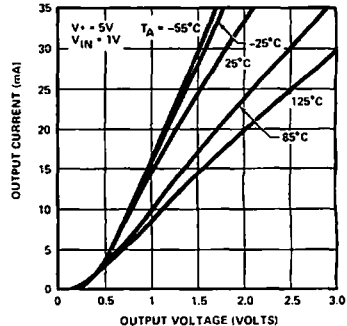
**OFFSET VOLTAGE
vs TEMPERATURE**



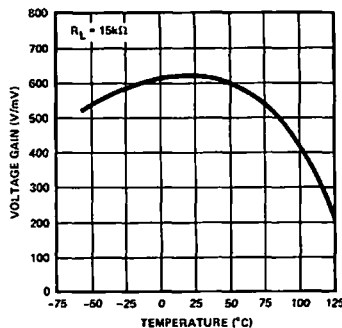
**OUTPUT CURRENT
vs OUTPUT VOLTAGE**



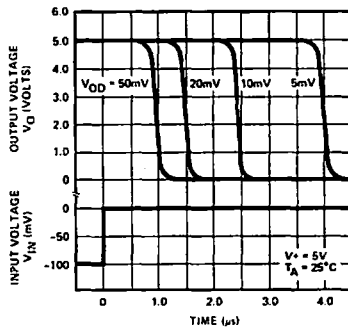
**OUTPUT CURRENT
vs OUTPUT VOLTAGE**



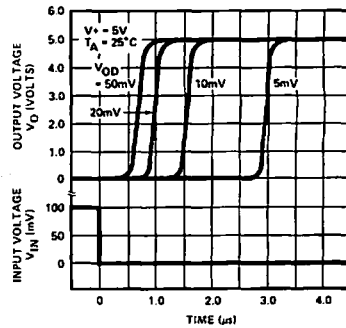
**OPEN-LOOP GAIN
vs TEMPERATURE**



**NEGATIVE RESPONSE TIME
vs OVERDRIVE**

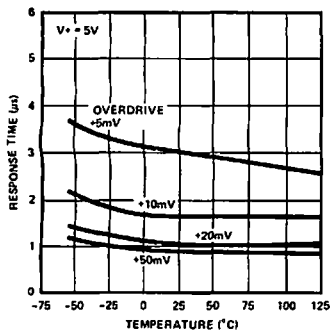
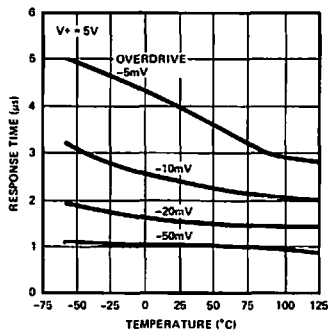
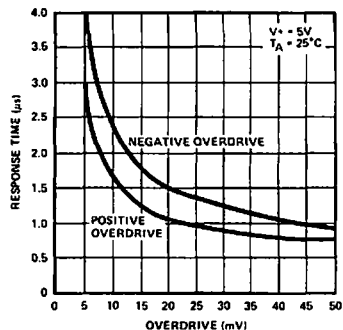
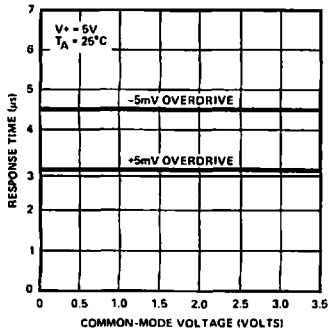
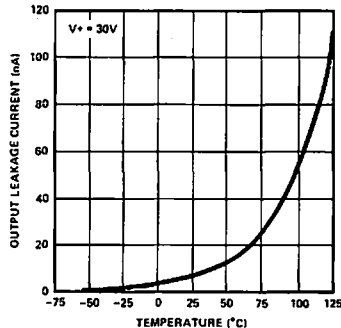
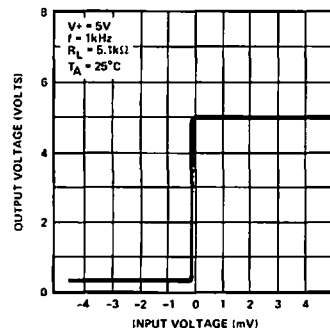


**POSITIVE RESPONSE TIME
vs OVERDRIVE**

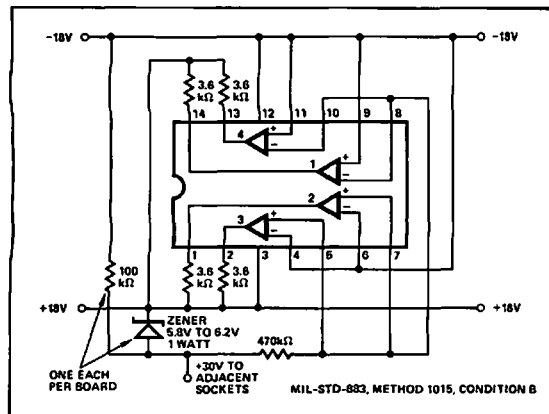




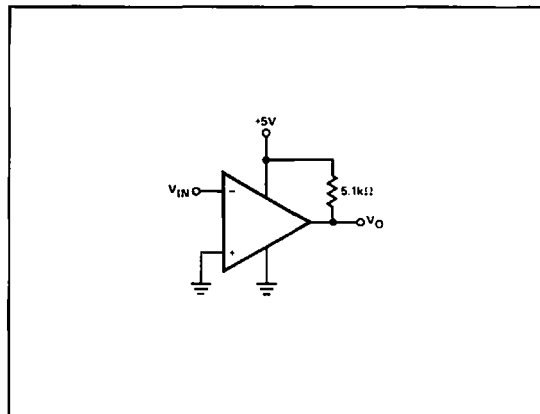
TYPICAL PERFORMANCE CHARACTERISTICS

POSITIVE RESPONSE TIME
vs TEMPERATURENEGATIVE RESPONSE TIME
vs TEMPERATURERESPONSE TIME
vs OVERDRIVERESPONSE TIME
vs COMMON-MODE VOLTAGEOUTPUT LEAKAGE
vs TEMPERATUREINPUT-OUTPUT
TRANSFER CHARACTERISTIC

BURN-IN CIRCUIT



RESPONSE-TIME TEST CIRCUIT



APPLICATIONS INFORMATION

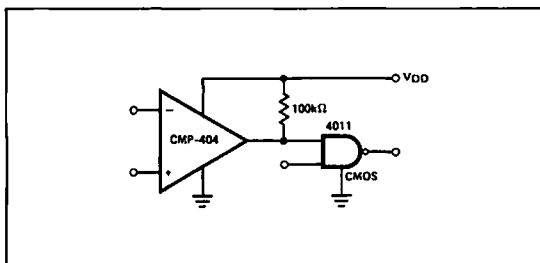
The use of non-saturated switching within the CMP-404 design results in optimized response time. The high-gain output stage drives large load currents with a minimum saturation voltage (V_{OL}). This provides excellent noise margin when driving LSTTL loads. An independent bias network for each comparator inside the CMP-404 minimizes crosstalk between comparators. This proves especially important when one comparator is detecting low-level signals while adjacent comparators are making transitions.

Input signals should be confined to between the power supply rails. Input signals exceeding either V_+ or GND will forward-bias internal junctions. Input current during forward bias should be limited to 20mA.

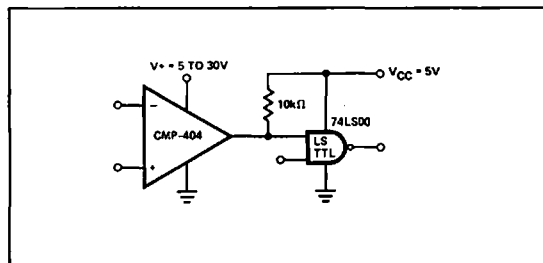
Exceeding the positive end of the common-mode input-voltage-range will cause the comparator output transistor to turn on, thus resulting in a continuous logic-low output state.

The open-collector output stage can be easily wire-OR-ed to make window comparators. The open-collector output also simplifies shifting of logic levels between different supply levels. The output transistors easily drive high-current loads, which is especially useful in fault-detector circuits for driving high-level enunciators (piezo horns, relays, lamps, or red LEDs).

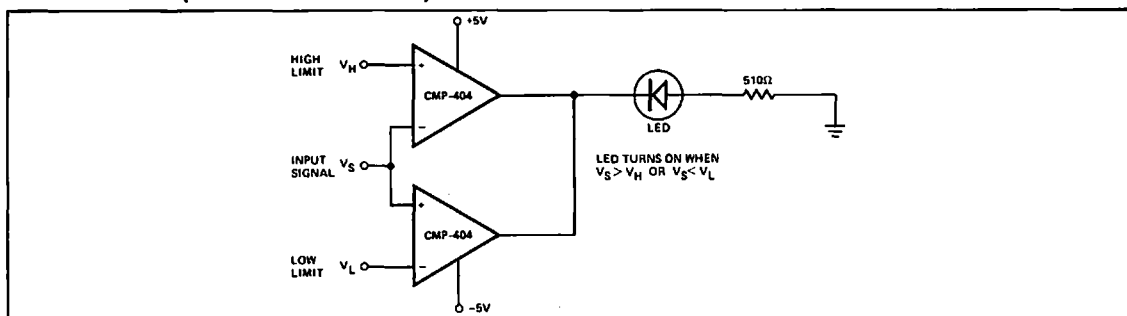
CMOS INTERFACING



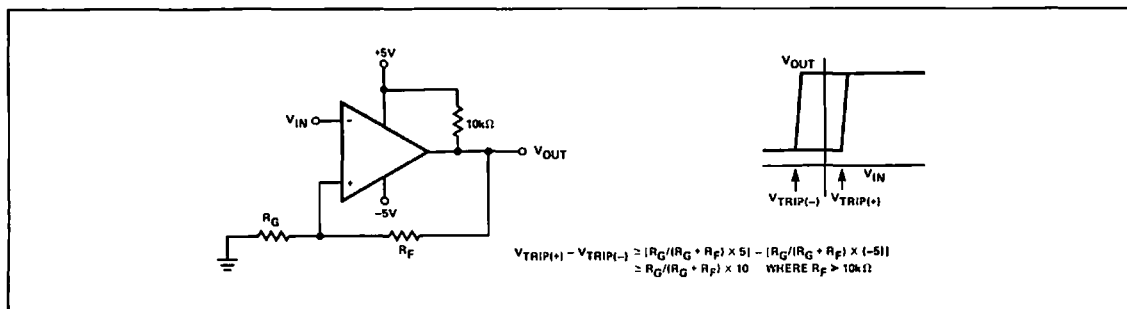
TTL INTERFACING



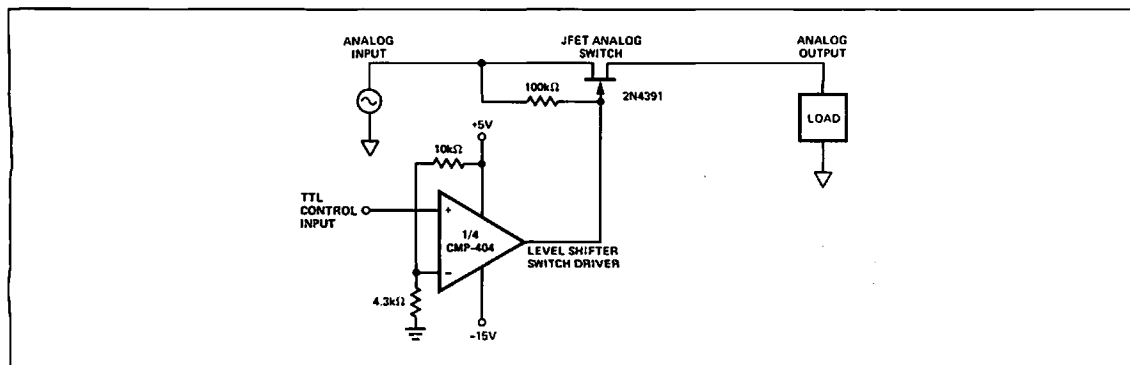
LIMIT DETECTOR (WINDOW COMPARATOR)



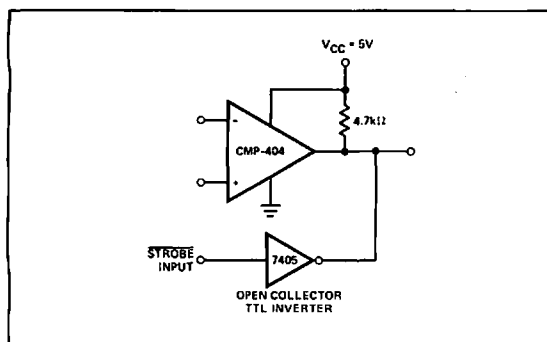
SETTING UP HYSTERESIS



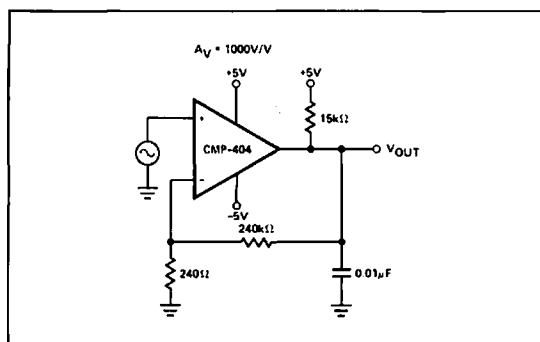
TTL-COMPATIBLE ANALOG SWITCH



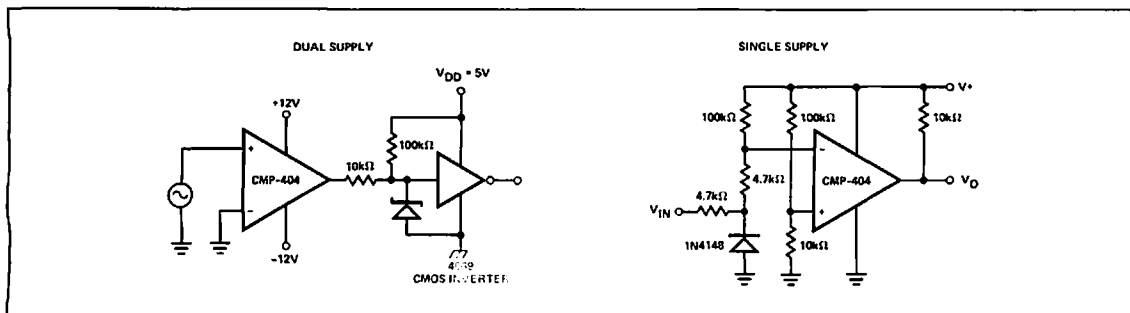
OUTPUT STROBING



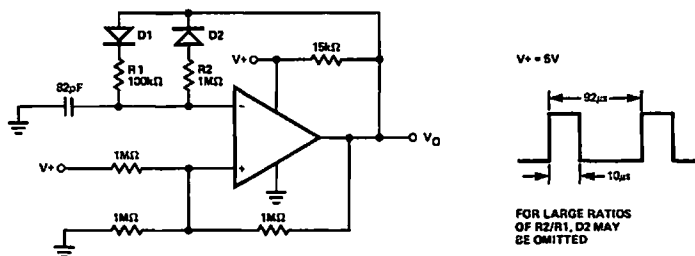
LOW-FREQUENCY OPERATIONAL AMPLIFIER



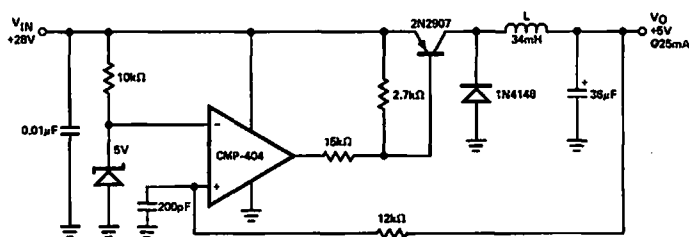
ZERO-CROSSING DETECTOR CIRCUITS



PULSE GENERATOR



REGULATED DC-TO-DC CONVERTER



NOTE:
OPERATING FREQUENCY OF 2.4kHz IS DETERMINED PRIMARILY BY VALUE OF L. THE INDUCTOR MUST HAVE A SATURATION CURRENT HIGHER THAN ITS PEAK OPERATING CURRENT.



PM-111/PM-211

PRECISION VOLTAGE
COMPARATORS

Precision Monolithics Inc.

FEATURES

- High Output Drive 50mA
- Low Input Bias Current 50nA Max
- Low Offset Voltage 3mV Max
- Differential Input Voltage Range $\pm 30V$
- Logic Outputs Compatible with Bipolar and CMOS
- Fully-Specified at All Temperatures

ORDERING INFORMATION†

V _{OS} MAX (mV)	PACKAGE				OPERATING TEMPERATURE RANGE
	TO-99 8-PIN	HERMETIC DIP 14-PIN	HERMETIC DIP 8-PIN	LCC 20-PIN	
3.0	PM111J*	PM111Y*	PM111Z*	PM111RC/883	MIL
3.0	PM211J	PM211Y	PM211Z	—	IND

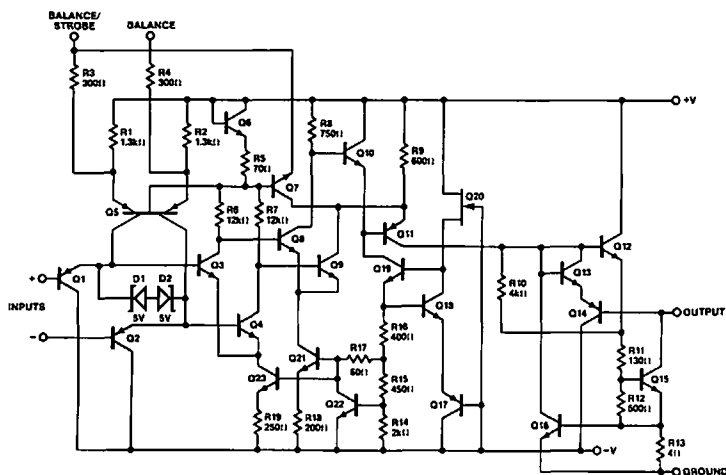
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

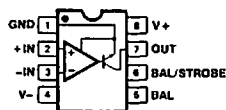
GENERAL DESCRIPTION

The PM-111/PM-211 are voltage comparators featuring low input bias and offset currents, high-differential voltage ranges, and wide-supply voltage ranges. The inputs and outputs can be isolated from system ground, and the output can drive loads referred to ground or either supply voltage. Strobing and offset balancing are available and the outputs can be wire OR'ed.

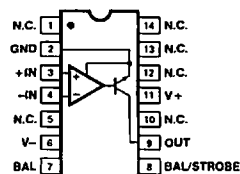
SIMPLIFIED SCHEMATIC



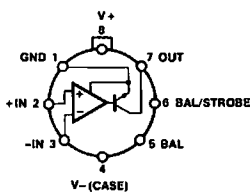
PIN CONNECTIONS



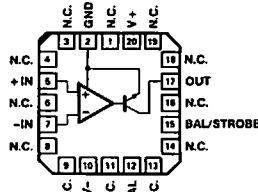
HERMETIC MINI-DIP
(Z-Suffix)



14-PIN HERMETIC DIP
(Y-Suffix)



TO-99
(J-Suffix)



PM-111RC/883
LCC
(RC-Suffix)

VOLTAGE COMPARATORS

**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

Total Supply Voltage, V_+ to V_-	36V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Strobe Pin Voltage	$V^+ - 5V$
Differential Input Voltage	$\pm 30V$
Input Voltage (Note 2)	$\pm 15V$
Power Dissipation (Note 3)	500mW
Output Short-Circuit Duration	10s
Operating Temperature Range	
PM-111	-55°C to $+125^\circ\text{C}$
PM-211	-25°C to $+85^\circ\text{C}$
DICE Junction Temperature (T_j)	-65°C to $+150^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering, 10 sec)	300°C

NOTES:

1. Absolute Maximum Ratings apply to both packaged parts and DICE, unless otherwise noted.
2. Rating applies to $V_S = \pm 15V$. The positive input-voltage limit is 30V above the negative supply. The negative input-voltage limit is equal to the negative supply or 30V below the positive supply, whichever is less.
3. Maximum package power-dissipation vs. ambient temperature.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	75°C	$6.8\text{mW}/^\circ\text{C}$
Hermetic DIP (Z)	75°C	$6.7\text{mW}/^\circ\text{C}$
Hermetic DIP (Y)	85°C	$9.0\text{mW}/^\circ\text{C}$
LCC (RC)	88°C	$8.1\text{mW}/^\circ\text{C}$

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pin at ground and $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-111/PM-211			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	0.75	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	5.0	nA
Input Bias Current	I_B	(Note 1)	—	25	50	nA
Voltage Gain (Emitter)	A_{VE}	(Note 2)	—	75	—	V/mV
Voltage Gain (Collector)	A_{VC}		—	200	—	V/mV
Response Time	t_r	$R_L = 500\Omega$ (tied to V_+) $V_{OD} = 5\text{mV}$ (Note 3)	—	160	—	ns
Saturation Voltage	V_{OL}	$V_{IN} \leq -5\text{mV}$ $I_{OUT} = 50\text{mA}$	—	0.68	1.0	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq +5\text{mV}$ $V_{OUT} = 50V$	—	5	15	nA
Positive Supply Current	I_{SV^+}		—	3.3	5	mA
Negative Supply Current	I_{SV^-}		—	2.4	4	mA
Input Voltage Range	IVR		-14.5 +13	-14.8 +14	—	V

NOTES:

1. The offset voltage, offset current, and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a $7.5k\Omega$ load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
2. Average of A_{V^+} and A_{V^-} over a $\pm 10V$ output range measured at the emitter.
3. The response time specified is for a 100mV input step with a 5mV overdrive and is the time required for the slowest edge. The slowest response occurs at the highest temperature of operation.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pin at ground and $-25^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-211			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	0.8	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	7	nA
Input Bias Current	I_B	(Note 1)	—	25	100	nA
Voltage Gain (Emitter)	A_{VE}	(Note 2)	—	35	—	V/mV
Response Time	t_r	$R_L = 500\Omega$ (tied to $V+$) $V_{OD} = 5mV$ (Note 3)	—	240	—	ns
Saturation Voltage	V_{OL}	$V_{IN} \leq -5mV$ $I_{OUT} = 50mA$	—	0.8	1.5	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq +5mV$ $V_{OUT} = 50V$	—	10	100	nA
Positive Supply Current	I_{SY+}		—	4	6	mA
Negative Supply Current	I_{SY-}		—	2.8	5	mA
Input Voltage Range	IVR		-14.5 13	-14.8 14	—	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pin at ground and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

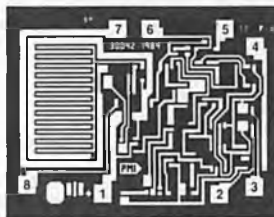
PARAMETER	SYMBOL	CONDITIONS	PM-111			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	0.8	3.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	0.3	10	nA
Input Bias Current	I_B	(Note 1)	—	25	100	nA
Voltage Gain (Emitter)	A_{VE}	(Note 2)	—	20	—	V/mV
Response Time	t_r	$R_L = 500\Omega$ (tied to $V+$) $V_{OD} = 5mV$ (Note 3)	—	420	—	ns
Saturation Voltage	V_{OL}	$V_{IN} \leq -5mV$ $I_{OUT} = 50mA$	—	0.82	1.5	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq +5mV$ $V_{OUT} = 50V$	—	145	500	nA
Positive Supply Current	I_{SY+}		—	4.2	6	mA
Negative Supply Current	I_{SY-}		—	3	5	mA
Input Voltage Range	IVR		-14.8 +13	-14.8 +14	—	V

NOTES:

1. The offset voltage, offset current, and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5k Ω load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
2. Average of A_{V+} and A_{V-} over a $\pm 10V$ output range measured at the emitter.
3. The response time specified is for a 100mV input step with a 5mV overdrive and is the time required for the slowest edge. The slowest response occurs at the highest temperature of operation.



DICE CHARACTERISTICS



DIE SIZE 0.066 × 0.050 inch, 3300 sq. mils
(1.68 × 1.27mm, 2.13 sq. mm)

1. GROUND
2. +IN
3. -IN
4. V-
5. BALANCE
6. BALANCE/STROBE
7. OUTPUT
8. V+

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ and ground pin at ground for PM-111GBC, $T_A = 125^\circ C$ for PM-111GTBC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-111GTBC	PM-111GBC	UNITS
			LIMIT	LIMIT	
Input Offset Voltage	V_{OS}	(Note 1)	3	3	mV MAX
Input Offset Current	I_{OS}	(Note 1)	10	5	nA MAX
Input Bias Current	I_B	(Note 1)	100	50	nA MAX
Saturation Voltage	V_{OL}		1.5	1.0	V MAX
Output Leakage Current	I_{CEX}	$V_{IN} \geq +5mV$ $V_{OUT} = 50V$	500	15	nA MAX
Input Voltage Range	IVR		± 13	—	V MIN
Positive Supply Current	I_{SV+}		6	5	mA MAX
Negative Supply Current	I_{SV-}		5	4	mA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

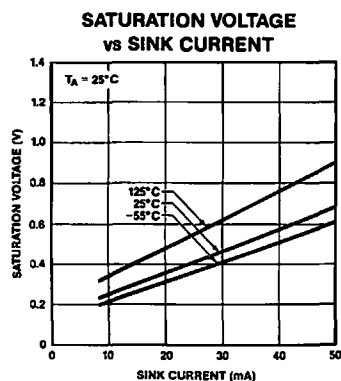
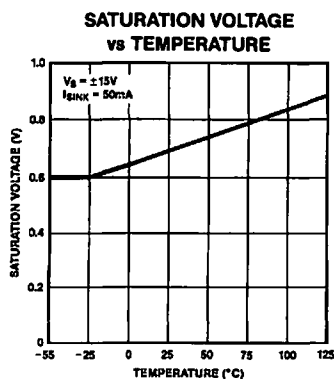
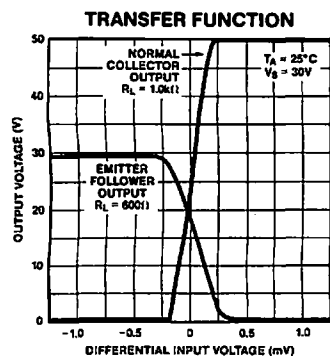
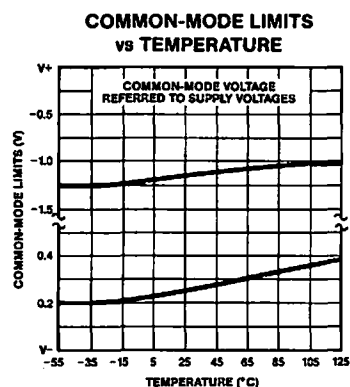
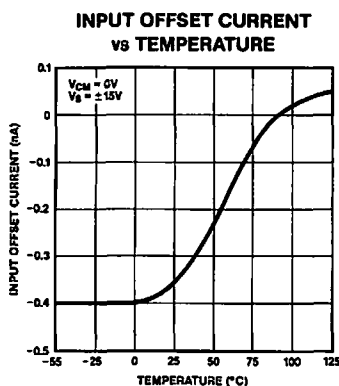
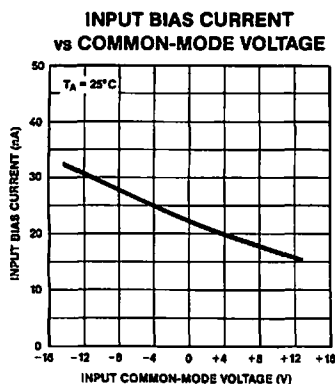
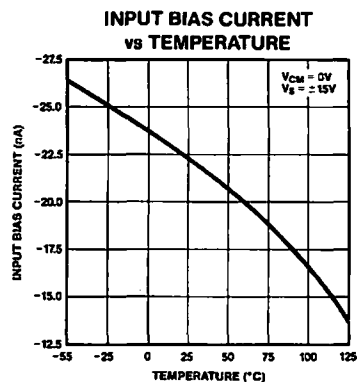
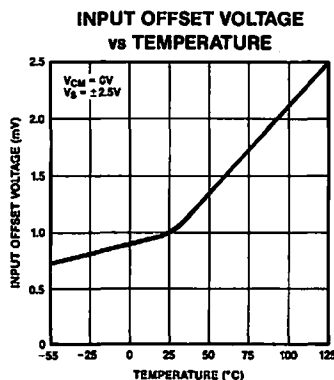
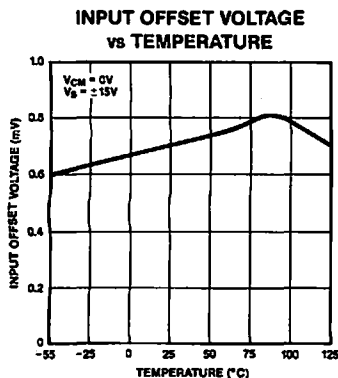
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25^\circ C$ and ground pin at ground for PM-111GBC, $T_A = 125^\circ C$ for PM-111GTBC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-111GTBC	PM-111GBC	UNITS
			TYPICAL	TYPICAL	
Voltage Gain (Emitter)	A_{VE}	(Note 2)	20	75	V/mV
Response Time	t_r	(Note 3)	420	180	ns

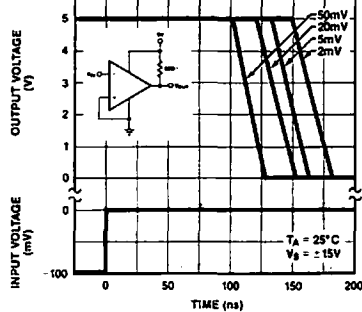
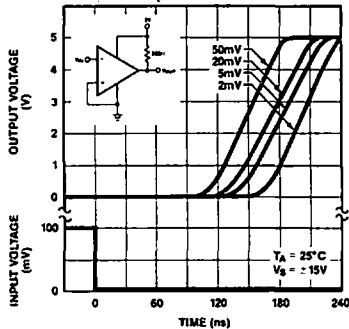
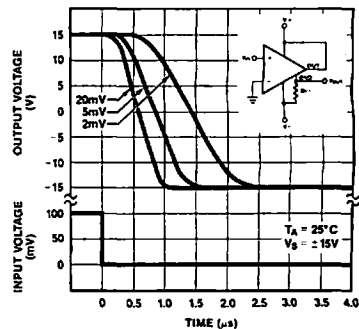
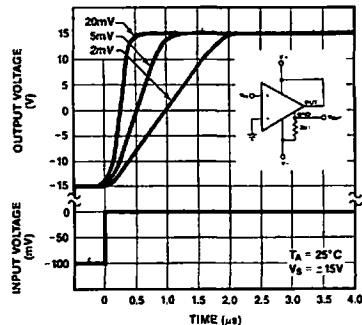
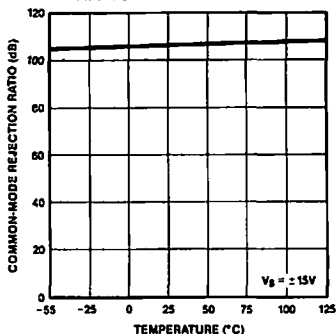
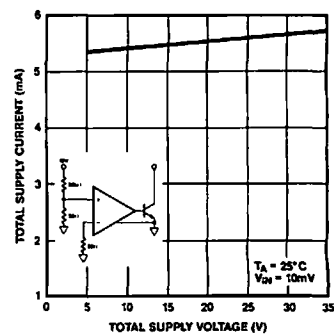
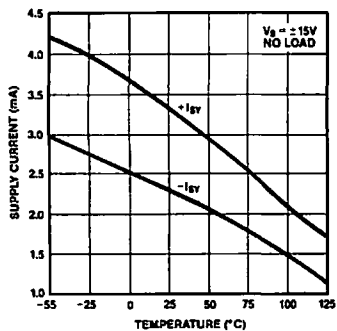
NOTES:

1. The offset voltage, offset current, and bias current given are the maximum values required to drive the collector output to within 1V of the supplies with a 7.5k Ω load. These parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
2. Average of A_{V+} and A_{V-} over a $\pm 10V$ output range measured at the emitter.
3. The response time specified is for a 100mV input step with a 5mV overdrive and is the time required for the slowest edge. The slowest response occurs at the highest temperature of operation.

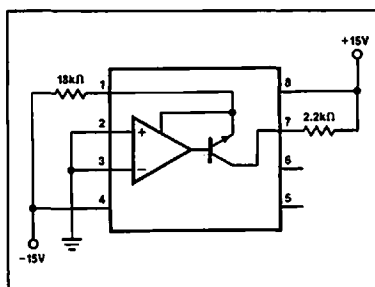
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS

 RESPONSE TIME FOR
VARIOUS INPUT OVERDRIVES

 RESPONSE TIME FOR
VARIOUS INPUT OVERDRIVES

 RESPONSE TIME FOR
VARIOUS INPUT OVERDRIVES

 RESPONSE TIME FOR
VARIOUS INPUT OVERDRIVES

 COMMON-MODE REJECTION
RATIO vs TEMPERATURE

 TOTAL SUPPLY CURRENT
vs TOTAL SUPPLY VOLTAGE

 SUPPLY CURRENT
vs TEMPERATURE


BURN-IN CIRCUIT





PM-119/PM-219

PRECISION HIGH-SPEED
DUAL COMPARATORS

Precision Monolithics Inc.

FEATURES

- Two Independent Comparators
- Operates from a Single 5V Supply
- Response Time 80ns Typ at $\pm 15V$
- High Output Drive Current 25mA
- Pin for Pin Replacement for LM119 with Improved Electrical Specifications
 - Input Offset Voltage 2.5mV Max
 - Input Offset Current 50nA Max
 - Voltage Gain 100V/mV Min
 - Positive Supply Current 10mA Max
 - Negative Supply Current 4mA Max
- Minimum Fan Out of 2 Each Side
- Inputs and Outputs Isolated from System Ground

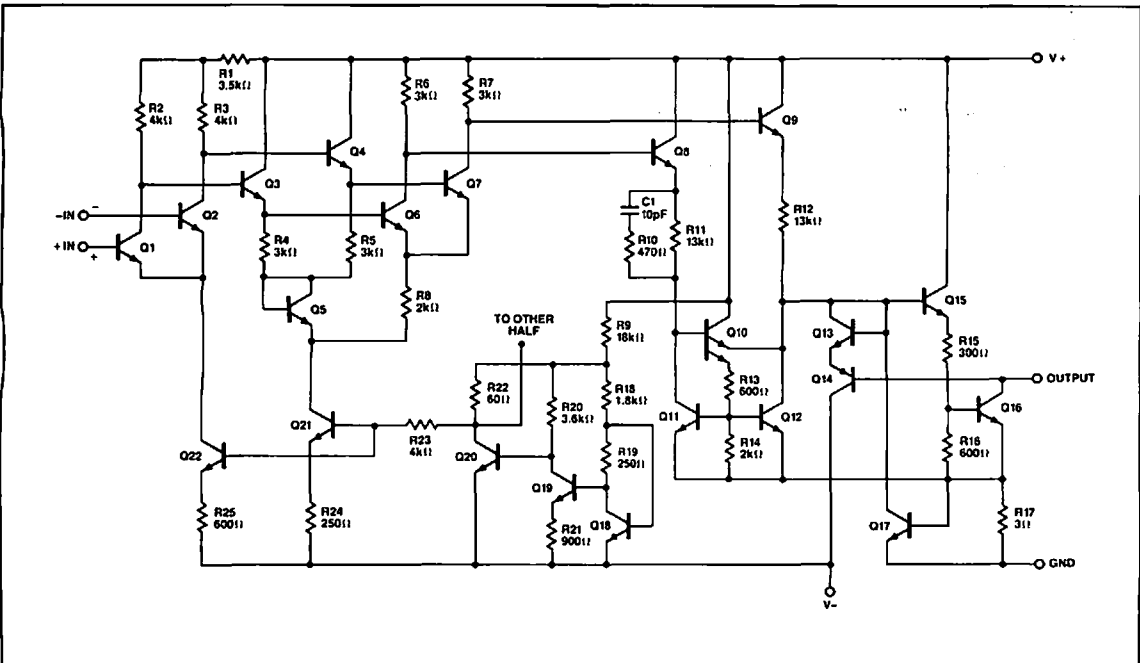
ORDERING INFORMATION†

V_{OS} MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
2.5	PM-119Y*	MIL
2.5	PM-219Y	IND

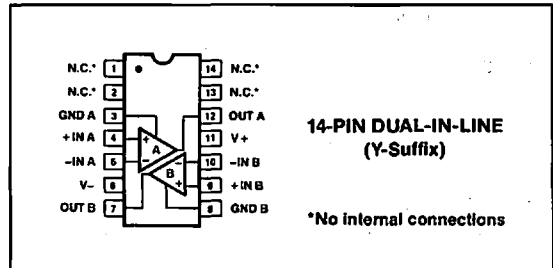
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cardip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

SIMPLIFIED SCHEMATIC



PIN CONNECTIONS



GENERAL DESCRIPTION

The PM-119/PM-219 is PMI's improved version of the industry-standard LM119 series dual high-speed voltage comparator (see Features section). It is designed to operate from a single +5V supply up to $\pm 15V$ dual supplies. Open-collector outputs are provided for logic interface flexibility, allowing output swings of up to +35V. High output drive capability facilitates RTL, DTL, and TTL interfacing, as well as relay and lamp driving at currents up to 25mA. Typical response time of 80ns with $\pm 15V$ power supplies makes the PM-119/PM-219 ideal for application in fast A/D converters, level shifters, oscillators, and multivibrators.

VOLTAGE COMPARATORS

**ABSOLUTE MAXIMUM RATINGS**

Total Supply Voltage	36V
Out to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	
PM-119	-55°C to +125°C
PM-219	-25°C to +85°C

Storage Temperature Range -65°C to +150°C
 Lead Temperature (Soldering, 10 sec) 300°C

NOTES:

- For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- The maximum junction temperature of the PM-119 is 150°C, while that of the PM-219 is 110°C. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pins at ground and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-119/PM-219			UNITS
			MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	$R_B \leq 5k\Omega$	—	0.2	2.5	mV
Input Offset Current	I_{OS}	(Note 1)	—	10	50	nA
Input Bias Current	I_B	(Note 1)	—	250	500	nA
Voltage Gain	A_{VO}		100	1000	—	V/mV
Response Time	t_r	(Note 2)	—	80	—	ns
Saturation Voltage	V_{SAT}	$V_{IN} \leq -5mV, I_{OUT} = 25mA$	—	0.6	1.2	V
Saturation Voltage	V_{SAT}	$V+ \geq 4.5V, V- = 0$ $V_{IN} \leq -8mV, I_{SINK} \leq 3.2mA$	—	0.23	0.4	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq 5mV, V_{OUT} = 35V$	—	0.1	2.0	μA
Positive Supply Current	I_{S+}		—	7.0	10.0	mA
Negative Supply Current	I_{S-}		—	3.0	4.0	mA
Positive Supply Current	I_{S+}	$V+ = 5V, V- = 0$	—	3.5	—	mA
Input Voltage Range	IVR		-12	±13	+12	V

NOTES:

- The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
- The response time specified is for a 100mV input step with 5mV overdrive.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pins at ground and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	PM-119		UNITS
				TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$	—	2.0	5.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	20	100	nA
Input Bias Current	I_B	(Note 1)	—	400	1000	nA
Positive Supply Current	I_S^+		—	8.0	11.5	mA
Negative Supply Current	I_S^-		—	3.0	4.5	mA
Positive Supply Current	I_S^+	$V^+ = 5V, V^- = 0$	—	3.5	—	mA
Saturation Voltage	V_{SAT}	$V^+ \geq 4.5V, V^- = 0$ $V_{IN} \leq -6mV, I_{SINK} \leq 3.2mA$	—	0.3	0.6	V
Differential Input Voltage			—	—	± 5	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq 5mV, V_{OUT} = 35V$	—	1.5	10.0	μA

NOTE:

1. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, ground pins at ground and $-25^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

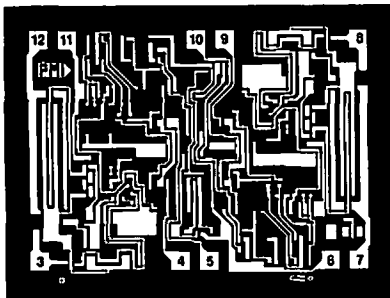
PARAMETER	SYMBOL	CONDITIONS	MIN	PM-219		UNITS
				TYP	MAX	
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$	—	0.5	5.0	mV
Input Offset Current	I_{OS}	(Note 1)	—	15	100	nA
Input Bias Current	I_B	(Note 1)	—	350	1000	nA
Positive Supply Current	I_S^+		—	8.0	11.5	mA
Negative Supply Current	I_S^-		—	3.0	4.5	mA
Positive Supply Current	I_S^+	$V^+ = 5V, V^- = 0$	—	3.5	—	mA
Saturation Voltage	V_{SAT}	$V^+ \geq 4.5V, V^- = 0$ $V_{IN} \leq -6mV, I_{SINK} \leq 3.2mA$	—	0.3	0.6	V
Differential Input Voltage			—	—	± 5	V
Output Leakage Current	I_{CEX}	$V_{IN} \geq 5mV, V_{OUT} = 35V$	—	0.2	10.0	μA

NOTE:

1. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.



DICE CHARACTERISTICS



DIE SIZE 0.079×0.059 inch, 4661 sq. mils
(1.98×1.48 mm, 2.93 sq. mm)

- | | |
|-------------------|--------------------|
| 1. N.C.* | 8. GND B |
| 2. N.C.* | 9. + INPUT B |
| 3. GND A | 10. - INPUT B |
| 4. + INPUT A | 11. V ⁺ |
| 5. - INPUT A | 12. OUTPUT A |
| 6. V ⁻ | 13. N.C.* |
| 7. OUTPUT B | 14. N.C.* |

*No internal connection

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, ground pins at ground and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-119GBC LIMIT	PM-119GTBC LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 5k\Omega$	5.0	5.0	mV MAX
Input Offset Current	I_{OS}	(Note 1)	100	100	nA MAX
Input Bias Current	I_B	(Note 1)	1000	1000	nA MAX
Saturation Voltage	V_{SAT}	$V_{IN} \leq -5mV$, $I_{OUT} = 25mA$	1.2	—	V MAX
Saturation Voltage		$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6mV$, $I_{SINK} \leq 3.2mA$	0.4	0.6	V MAX
Output Leakage Current	I_{CEX}	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$	2.0	10.0	μA MAX
Positive Supply Current	I_S^+		11.5	11.5	mA MAX
Negative Supply Current	I_S^-		4.5	4.5	mA MAX

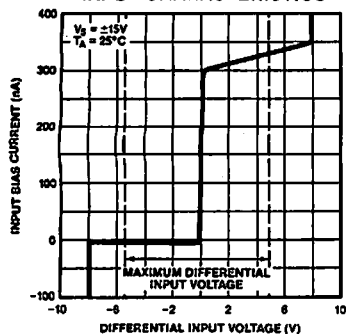
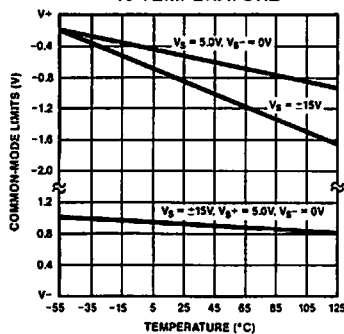
NOTES:

1. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

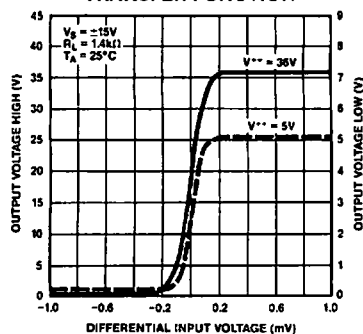
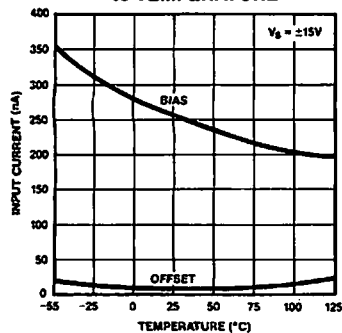
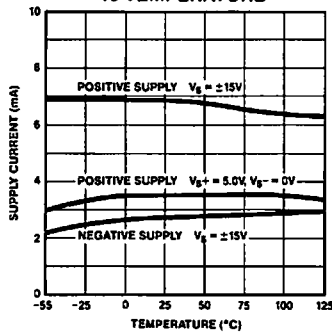
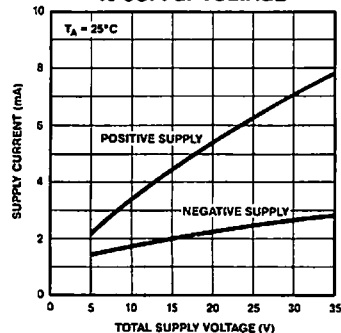
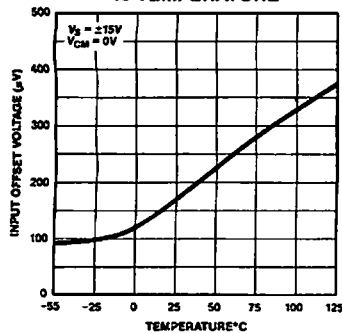
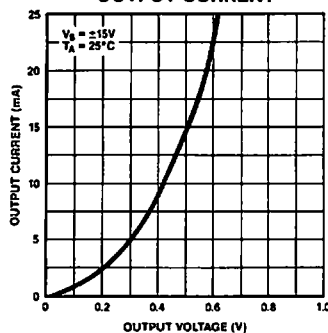
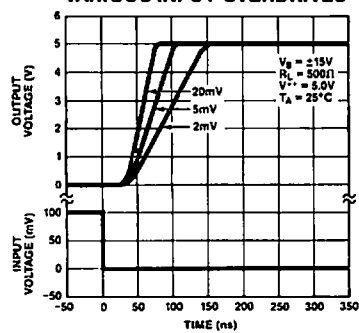
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

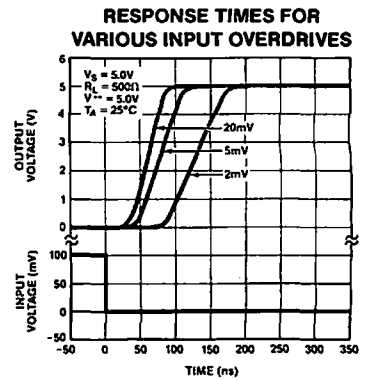
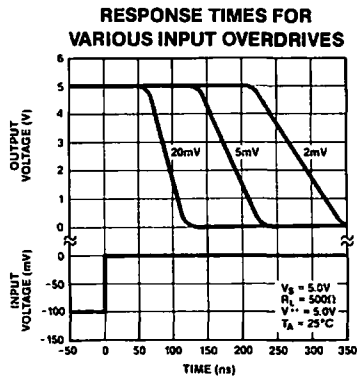
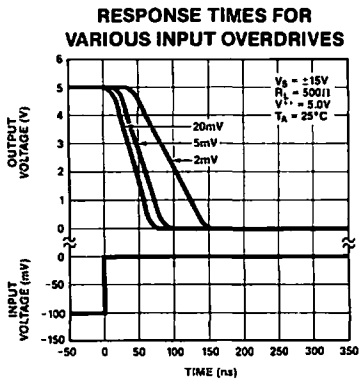
INPUT CHARACTERISTICS


COMMON-MODE LIMITS
vs TEMPERATURE


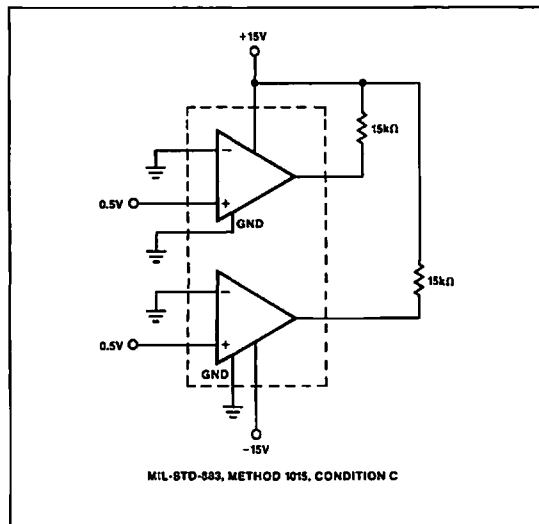
TRANSFER FUNCTION


INPUT CURRENTS
vs TEMPERATURE

SUPPLY CURRENTS
vs TEMPERATURE

SUPPLY CURRENTS
vs SUPPLY VOLTAGE

INPUT OFFSET VOLTAGE
vs TEMPERATURE

OUTPUT SATURATION
VOLTAGE vs
OUTPUT CURRENT

RESPONSE TIMES FOR
VARIOUS INPUT OVERDRIVES


TYPICAL PERFORMANCE CHARACTERISTICS



BURN-IN CIRCUIT





PM-139/PM-139A

QUAD LOW-POWER
VOLTAGE COMPARATORS

Precision Monolithics Inc.

FEATURES

- Single or Dual Supply Operation
- Input Voltage Range Includes Ground
- Low Power Consumption (2mW/Comparator)
- Low Input Bias Current 25nA
- Low Input Offset Current ± 5 nA
- Low Offset Voltage ± 2 mV
- Low Output Saturation Voltage (250mV @ 4mA)
- Logic Outputs Compatible with TTL, DTL, ECL, MOS, and CMOS
- Directly Replaces LM139 and LM139A Comparators

ORDERING INFORMATION†

+25°C V _{OS} (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	14-PIN HERMETIC DIP	LCC	
$\pm 2^*$	PM139AY*	PM139ARC/883	MIL
$\pm 5^*$	PM139Y*		MIL

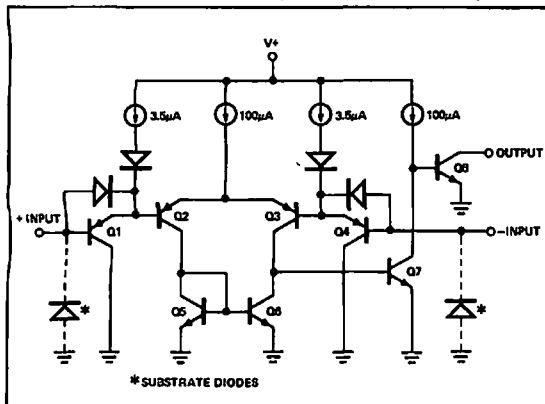
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

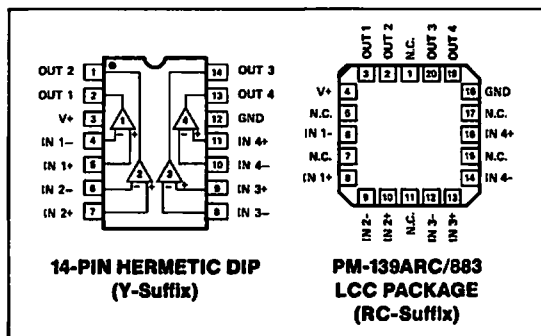
The PM-139 has four independent voltage comparators, each with precision DC specifications. Low offset voltage, bias current, power consumption and output saturation voltage

SIMPLIFIED SCHEMATIC (ONE COMPARATOR)

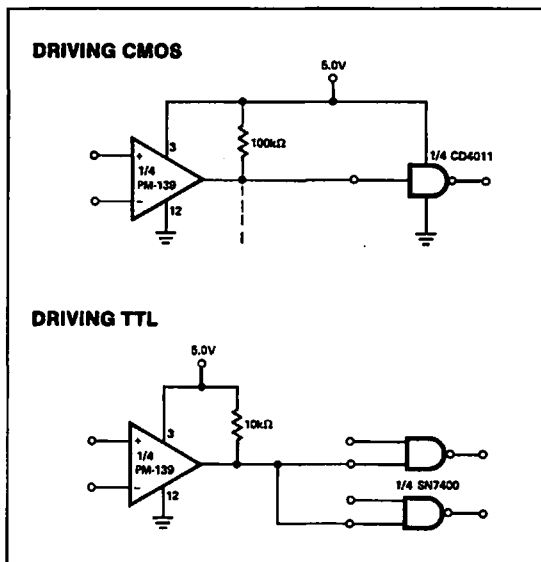


are offered in a design that features single power supply operation. The input voltage range includes ground for convenient single supply operation. The 2mA power supply current, independent of supply voltage — coupled with the single supply operation, makes this comparator ideal for low power applications. Open collector outputs allow maximum applications flexibility.

PIN CONNECTIONS



TYPICAL INTERFACE



VOLTAGE COMPARATORS

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V+$ 36V or $\pm 18V$
 Differential Input Voltage 36V
 Input Voltage $-0.3V$ to $+36V$
 Power Dissipation Hermetic DIP 500mW
 Derate Above $100^{\circ}C$ 10mW/ $^{\circ}C$
 Output Short-Circuit to Ground Continuous

Input Current ($V_{IN} < -0.3V$) 50mA
 Operating Temperature Range
 PM-139A/139/139ARC $-55^{\circ}C$ to $+125^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temperature (Soldering, 60 sec) $300^{\circ}C$

ELECTRICAL CHARACTERISTICS at $V+ = +5V$, $T_A = 25^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-139A			PM-139			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	1	2	—	2	5	mV
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range	—	25	100	—	25	100	nA
Input Offset Current	I_{OS}	$I_{IN}(+)$ or $I_{IN}(-)$	—	3	25	—	3	25	nA
Input Common-Mode Voltage Range	CMVR	(Notes 2, 5, 6)	0	—	3.5	0	—	3.5	V
Supply Current	I_S	$R_L = \infty$ on all Comparators $V+ = 30V$	—	0.8	2	—	0.8	2	mA
Voltage Gain	A_{VO}	$R_L \geq 15k\Omega$, $V+ = 15V$ (To support large V_O swing) (Note 5)	50	200	—	50	200	—	V/mV
Large-Signal Response Time	t_r	$V_{IN} = TTL$ Logic Swing, $V_{REF} = 1.4V$, $V_{RL} = 5V$, $R_L = 5.1k\Omega$, (Note 4)	—	300	—	—	300	—	ns
Response Time	t_r	$V_{RL} = 5V$, $R_L = 5.1k\Omega$ (Notes 3, 4)	—	1.3	—	—	1.3	—	μs
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$	6	16	—	6	16	—	mA
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	—	250	400	—	250	400	mV
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, $V_O = 30V$	—	0.1	—	—	0.1	—	nA

ELECTRICAL CHARACTERISTICS at $V+ = +5V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, unless otherwise noted.

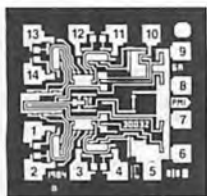
PARAMETER	SYMBOL	CONDITIONS	PM-139A			PM-139			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}	(Note 1)	—	—	4	—	—	9	mV
Input Offset Current	I_{OS}	$I_{IN}(+)$ or $I_{IN}(-)$	—	—	100	—	—	100	nA
Input Bias Current	I_B	$I_{IN}(+)$ OR $I_{IN}(-)$ with Output in Linear Range	—	—	300	—	—	300	nA
Input Common-Mode Voltage Range	CMVR	(Notes 3, 5)	0	—	$V+ - 2$	0	—	$V+ - 2$	V
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4mA$	—	—	700	—	—	700	mV
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1V$, $V_{IN}(-) = 0$, $V_O = 30V$	—	—	1	—	—	1	μA
Differential Input Voltage		Keep All $V_{INs} \geq 0V$	—	—	36	—	—	36	V

NOTES:

- At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with $V+$ from 5V, and over the full input common-mode range (0V to $V+ - 1.5V$).
- The input common-mode voltage or either input voltage signal should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V+ - 1.5V$, but either or both inputs can go to $+30V$ without damage.
- The response time specified is for a 100mV input step with 5mV overdrive. For larger overdrive signals 300ns can be obtained. See characteristics section.
- Sample tested.
- Guaranteed by design.
- Positive CMVR limit equals $V+ - 1.5V$ for supply voltages other than 5V.



DICE CHARACTERISTICS



DIE SIZE 0.051×0.048 inch, 2448 sq. mils
(1.295×1.220 mm, 1.58 sq. mm)

- | | |
|---------------------------|----------------------------|
| 1. OUTPUT (2) | 8. INVERTING INPUT (3) |
| 2. OUTPUT (1) | 9. NONINVERTING INPUT (3) |
| 3. POSITIVE SUPPLY | 10. INVERTING INPUT (4) |
| 4. INVERTING INPUT (1) | 11. NONINVERTING INPUT (4) |
| 5. NONINVERTING INPUT (1) | 12. GROUND (SUBSTRATE) |
| 6. INVERTING INPUT (2) | 13. OUTPUT (4) |
| 7. NONINVERTING INPUT (2) | 14. OUTPUT (3) |

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = +5V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-139N LIMIT	UNITS
Input Offset Voltage	V_{OS}	$R_S = 0\Omega$, $R_L = 5.1k\Omega$ $V_O = 1.4V$, (Note 1)	2	mV MAX
Input Offset Current	I_{OS}	$I_{IN(+)} - I_{IN(-)}$ $R_L = 5.1k\Omega$ $V_O = 1.4V$	25	nA MAX
Input Bias Current	I_B	$I_{IN(+)}$ or $I_{IN(-)}$, (Note 1)	100	nA MAX
Voltage Gain	A_V	$R_L \geq 15k\Omega$, $V_+ = 15V$, (Note 3)	50	V/mV MIN
Input Voltage Range	CMVR	(Notes 2, 3)	$V_+ - 1.5$	V MAX
Common-Mode Rejection Ratio	CMRR	(Note 4)	60.5	dB MIN
Power Supply Rejection Ratio	PSRR	$V_+ = 5V$ to $+18V$	60.5	dB MIN
Saturation Voltage	V_{OL}	$V_{IN(+)} \geq 1V$, $V_{IN(-)} = 0$, $I_{SINK} \leq 4mA$	400	mV MAX
Output Sink Current	I_{SINK}	$V_{IN(+)} \geq 1V$, $V_{IN(-)} = 0$, $V_O \leq 1.5V$	6	mA MIN
Output Leakage Current	I_{LEAK}	$V_{IN(+)} \geq 1V$, $V_{IN(-)} = 0$, $V_O = 30V$	500	nA MAX
Supply Current	I_+	$R_L = \infty$, All Comps $V_+ = 30V$	2	mA MAX

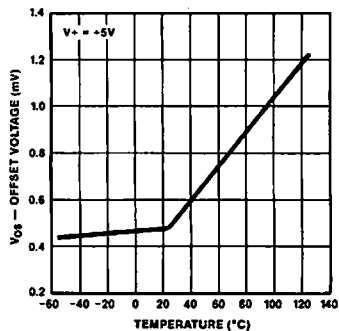
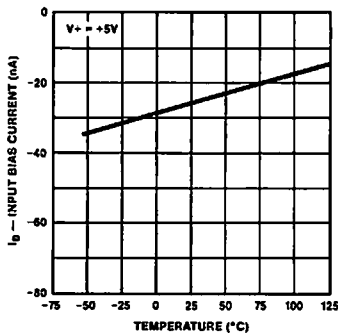
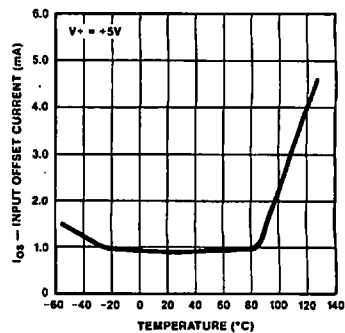
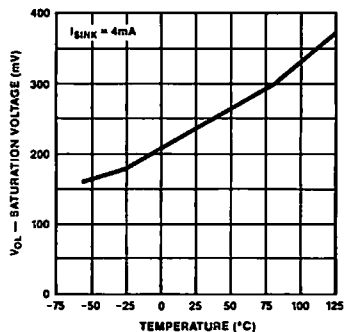
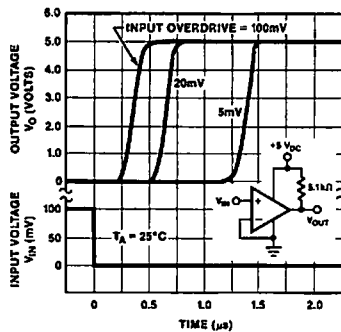
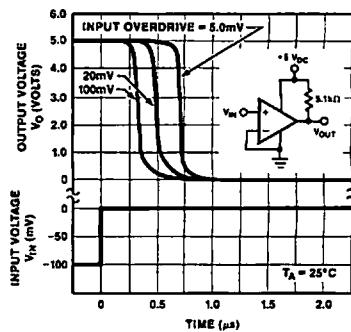
NOTES:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = +5V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-139N TYPICAL	UNITS
Large-Signal Response Time	t_r	$V_{IN} = \text{TTL Logic Swing}$ $V_{REF} = 1.4V$, (Note 5) $V_{RL} = 5V$, $R_L = 5.1k\Omega$	600	ns
Small-Signal Response Time	t_r	$V_{IN} = 100mV \text{ Step}$, (Note 5) 5mV Overdrive $V_{RL} = 5V$, $R_L = 5.1k\Omega$	1.3	μs

NOTES:
1. At output switch point, $V_O = 1.4V$, $R_S = 0\Omega$ with V_+ from 5V; and over the full input common-mode range $-0V$ to $V_+ - 1.5V$.
2. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_+ - 1.5V$, but either or both inputs can go to $-4.30V$ without damage.
3. Guaranteed by design.
4. $R_L \geq 15k\Omega$, $V_{CM} = 1.5V$ to $13.5V$, $V_+ = 15V$
5. Sample tested.

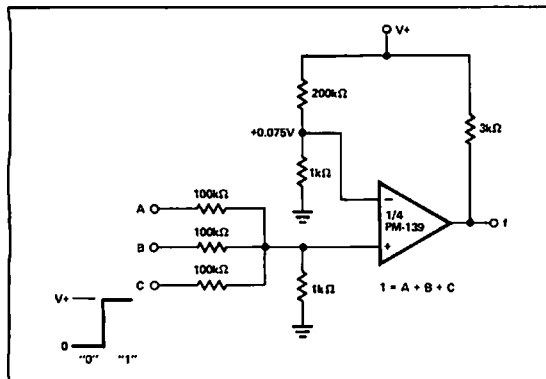
TYPICAL PERFORMANCE CHARACTERISTICS

 OFFSET VOLTAGE
vs TEMPERATURE

 INPUT BIAS CURRENT
vs TEMPERATURE

 INPUT OFFSET CURRENT
vs TEMPERATURE

 SATURATION VOLTAGE
vs TEMPERATURE

 RESPONSE TIME FOR
VARIOUS INPUT OVERDRIVES —
POSITIVE TRANSITION

 RESPONSE TIME FOR
VARIOUS INPUT OVERDRIVES —
NEGATIVE TRANSITION


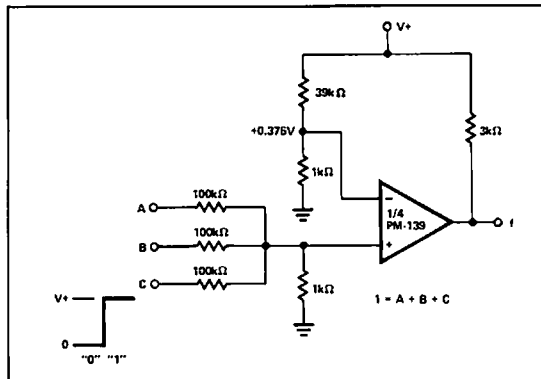


TYPICAL APPLICATIONS

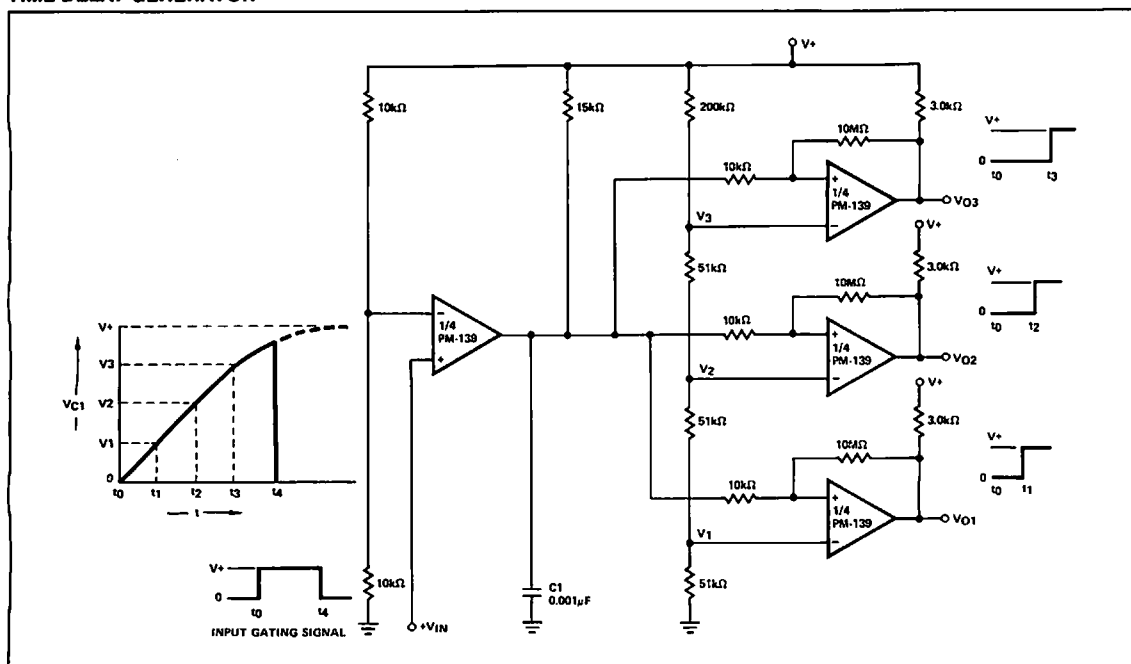
OR GATE



AND GATE

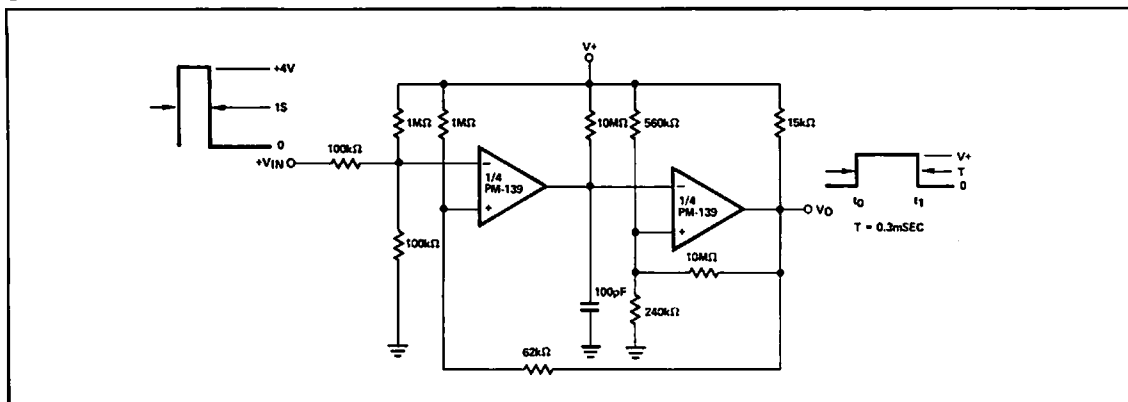


TIME DELAY GENERATOR

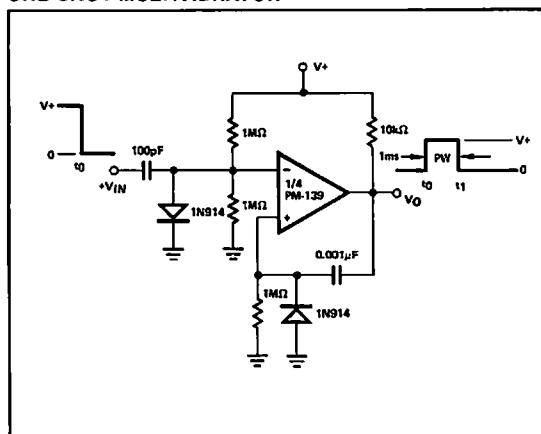


TYPICAL APPLICATIONS

ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK-OUT



ONE-SHOT MULTIVIBRATOR



BURN-IN CIRCUIT

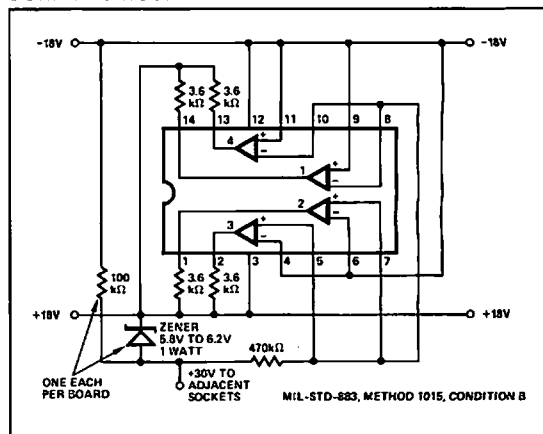


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MATCHED TRANSISTOR ARRAYS

Precision Monolithics Inc.

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*MAT-04	
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*Indicates new product or product whose data sheet has been finalized since the 1986 data book.

MATCHED DUAL NPN TYPES**Parameter Comparison Table ($I_C = 10\mu A$) for MAT-02**

Product	BV_{CEO} Min (V)	V_{OS} Max (mV)	TCV_{OS} Max ($\mu V/^{\circ}C$)	h_{FE} Min	I_{OS} Max (nA)	TCI_{OS} Max (pA/ $^{\circ}C$)
MAT-02A/E**	40	0.05	0.3	400	0.5	90
MAT-02B/F**	40	0.15	1	300	1.3	150
LM194	40	0.05	0.3	300	0.7	N.C.
LM394	40	0.15	1	200	2.0	N.C.
MAT-01AH	45	0.1	0.5	500	0.6	90
MAT-01GH	45	0.5	1.8	250	3.2	150
LM114A	45	0.5	2.0	500	2.0	—
LM114	45	2.0	10	250	10	—
LM115A	60	0.5	2.0	250	2.0	—
LM115	60	2.0	10	250	10	—
AD810*	35	3.0	15	100	2.0	600
AD811*	45	1.5	7.5	200	10	300
AD812*	35	1.0	5.0	400	2.5	300
AD813*	45	0.5	2.5	200	5	300
AD818*	20	1.0	5.0	200	10	300

*Discontinued

Temperature range for A-grade and B-grade is $-55^{\circ}C$ to $+125^{\circ}C$; temperature range for E-grade and F-grade is $-25^{\circ}C$ to $+85^{\circ}C$.Parameter Comparison Table ($I_C = 10\mu A$) for MAT-01 to 2N-Types**

Product	BV_{CEO} Min (V)	V_{OS} Max (mV)	TCV_{OS} Max ($\mu V/^{\circ}C$)	h_{FE} Min	% h_{FE} Match Max	I_{OS} Max (nA)	TCI_{OS} Max (pA/ $^{\circ}C$)
MAT-01GH	45	0.5	1.8	250	8	3.2	150
2N2639	45	5.0	10	50	10	20	1000
2N2640	45	10	20	50	20	40	2000
2N2642	45	5.0	10	100	10	10	500
2N2643	45	10	20	100	20	20	375
2N2915	45	3.0	10	60	10	17	600
2N2915A	45	2.0	5.0	60	15	26	900
2N2916	45	5.0	10	150	10	7	N.C.
2N2916A	45	2.0	5.0	150	15	10	300
2N2917	45	10	20	60	20	17	1450
2N2918	45	5.0	20	150	20	7	750
2N2919	60	3.0	10	60	10	17	600
2N2919A	60	1.5	5.0	60	10	17	600
2N2920	60	3.0	10	150	10	7	N.C.
2N2920A	60	1.5	5.0	150	10	7	300
2N2060	60	5.0	10	25	10	40	N.C.
2N2060A	60	3.0	5.0	25	10	40	N.C.
2N2060B	60	1.5	5.0	25	10	40	N.C.

NOTES:

1. TCI_{OS} Max and I_{OS} Max calculated from published data.
2. N.C. = Insufficient published data to calculate.
3. All of above are physically interchangeable pin-for-pin with MAT-01 and MAT-02 series.

INTRODUCTION

Monolithic dual and quad transistor arrays feature inherently close matching of electrical parameters and very low thermal differentials. In addition, PMI arrays are specifically designed for low offset voltage, low offset voltage drift, low noise, and high gain, specified over a wide range of collector currents. Monolithic duals are optimized for amplifier input use and provide the best possible input stage performance. The dual and quad transistors are excellent for use in high-performance audio systems, high-gain instrumentation amplifiers, and precision current mirrors. PMI offers both NPN and PNP type matched transistors.

Both the dual and quad transistors are also designed for minimal base-to-emitter resistance which makes log conformity excellent. For an ideal transistor, the base-to-emitter voltage is equal to $(kT/q) \ln(I_C/I_S)$. An added term, $I_C r_{BE}$, causes departure from this idealized logarithmic relationship. The NPN MAT-02 and MAT-04 and PNP MAT-03 have very low r_{BE} over a wide range of collector current. Circuits for squaring, RMS-to-DC conversion, and logarithmic amplification can be accurately implemented through use of these low- r_{BE} products. The MAT-03 advance data sheet is shown in this section.

The well-defined relationship between V_{BE} and collector current can also be used for temperature sensing or for generating bandgap-reference voltages. The low noise, low offsets, and high gain combined with a wide operating range for collector current make these monolithic arrays very useful for a diverse range of applications.

DEFINITIONS

Average Offset Current Drift (TCI_{OS}) — The ratio of the change in I_{OS} to the change in temperature producing it.

Average Offset Voltage Drift (TCV_{OS}) — The ratio of the change in V_{OS} to the change in temperature producing it.

current.

Broadband Noise Voltage (e_{nRMS}) — The root-mean-square noise voltage referred to the input over a specified bandwidth at a specified collector voltage and current.

Current Gain Match (Δh_{FE}) — The difference in h_{FE} between the transistors at a specified voltage and current, expressed as a percentage of the higher of the two h_{FE} 's.

$$\left(1 - \frac{h_{FE1}}{h_{FE2}}\right) \times 100$$

Excess Emitter Resistance (r_{BE}) — The effective resistance between the base and emitter terminals of each transistor.

Noise Voltage (e_{np-p}) — The peak-to-peak noise voltage referred to the input over a specified bandwidth at a specified collector voltage and current.

Noise Voltage Density (e_n) — The rms noise voltage referred to the input in a 1Hz band surrounding a specified frequency, measured at a specified collector voltage and current.

Offset Current (I_{OS}) — The difference between the base currents at a specified collector voltage and current.

Offset Current Change ($\Delta I_{OS}/\Delta V_{CB}$) — The ratio of the change in offset current to the change in collector-base voltage producing it.

Offset Voltage (V_{OS}) — The difference between the base-emitter voltages ($V_{BE1}-V_{BE2}$) at a specified collector voltage and current.



Precision Monolithics Inc.

MATCHED TRANSISTOR ARRAYS

INTRODUCTION

Monolithic dual and quad transistor arrays feature inherently close matching of electrical parameters and very low thermal differentials. In addition, PMI arrays are specifically designed for low offset voltage, low offset voltage drift, low noise, and high gain, specified over a wide range of collector currents. Monolithic duals are optimized for amplifier input use and provide the best possible input stage performance. The dual and quad transistors are excellent for use in *high-performance* audio systems, high-gain instrumentation amplifiers, and precision current mirrors. PMI offers both NPN and PNP type matched transistors.

Both the dual and quad transistors are also designed for minimal base-to-emitter resistance which makes *log* conformity excellent. For an ideal transistor, the base-to-emitter voltage is equal to $(kT/q) \ln(I_C/I_S)$. An added term, $I_C r_{BE}$, causes departure from this idealized logarithmic relationship. The NPN MAT-02 and MAT-04 and PNP MAT-03 have very low r_{BE} over a wide range of collector current. Circuits for squaring, RMS-to-DC conversion, and logarithmic amplification can be accurately implemented through use of these low- r_{BE} products. The MAT-03 advance data sheet is shown in this section.

The well-defined relationship between V_{BE} and collector current can also be used for temperature sensing or for generating bandgap-reference voltages. The low noise, low offsets, and high gain combined with a wide operating range for collector current make these monolithic arrays very useful for a diverse range of applications.

DEFINITIONS

Average Offset Current Drift (TCI_{OS}) — The ratio of the change in I_{OS} to the change in temperature producing it.

Average Offset Voltage Drift (TCV_{OS}) — The ratio of the change in V_{OS} to the change in temperature producing it.

Bias Current (I_B) — The average of the base currents at a specified collector voltage and current.

Broadband Noise Voltage (e_{nRMS}) — The root-mean-square noise voltage referred to the input over a specified bandwidth at a specified collector voltage and current.

Current Gain Match (Δh_{FE}) — The difference in h_{FE} between the transistors at a specified voltage and current, expressed as a percentage of the higher of the two h_{FE} 's.

$$\left(1 - \frac{h_{FE1}}{h_{FE2}}\right) \times 100$$

Excess Emitter Resistance (r_{BE}) — The effective resistance between the base and emitter terminals of each transistor.

Noise Voltage (e_{np-p}) — The peak-to-peak noise voltage referred to the input over a specified bandwidth at a specified collector voltage and current.

Noise Voltage Density (e_n) — The rms noise voltage referred to the input in a 1Hz band surrounding a specified frequency, measured at a specified collector voltage and current.

Offset Current (I_{OS}) — The difference between the base currents at a specified collector voltage and current.

Offset Current Change ($\Delta I_{OS}/\Delta V_{CB}$) — The ratio of the change in offset current to the change in collector-base voltage producing it.

Offset Voltage (V_{OS}) — The difference between the base-emitter voltages ($V_{BE1}-V_{BE2}$) at a specified collector voltage and current.



MATCHED TRANSISTOR ARRAYS

Precision Monolithics Inc.

MATCHED DUAL NPN TYPES

Parameter Comparison Table ($I_C = 10\mu A$) for MAT-02

Product	BV_{CEO} Min (V)	V_{OS} Max (mV)	TCV_{OS} Max ($\mu V/^{\circ}C$)	h_{FE} Min	I_{OS} Max (nA)	TCI_{OS} Max ($pA/^{\circ}C$)
MAT-02A/E**	40	0.05	0.3	400	0.5	90
MAT-02B/F**	40	0.15	1	300	1.3	150
LM194	40	0.05	0.3	300	0.7	N.C.
LM394	40	0.15	1	200	2.0	N.C.
MAT-01AH	45	0.1	0.5	500	0.6	90
MAT-01GH	45	0.5	1.8	250	3.2	150
LM114A	45	0.5	2.0	500	2.0	—
LM114	45	2.0	10	250	10	—
LM115A	60	0.5	2.0	250	2.0	—
LM115	60	2.0	10	250	10	—
AD810*	35	3.0	15	100	2.0	600
AD811*	45	1.5	7.5	200	10	300
AD812*	35	1.0	5.0	400	2.5	300
AD813*	45	0.5	2.5	200	5	300
AD818*	20	1.0	5.0	200	10	300

*Discontinued

**Temperature range for A-grade and B-grade is $-55^{\circ}C$ to $+125^{\circ}C$; temperature range for E-grade and F-grade is $-25^{\circ}C$ to $+85^{\circ}C$.

Parameter Comparison Table ($I_C = 10\mu A$) for MAT-01 to 2N-Types

Product	BV_{CEO} Min (V)	V_{OS} Max (mV)	TCV_{OS} Max ($\mu V/^{\circ}C$)	h_{FE} Min	% h_{FE} Match Max	I_{OS} Max (nA)	TCI_{OS} Max ($pA/^{\circ}C$)
MAT-01GH	45	0.5	1.8	250	8	3.2	150
2N2639	45	5.0	10	50	10	20	1000
2N2640	45	10	20	50	20	40	2000
2N2642	45	5.0	10	100	10	10	500
2N2643	45	10	20	100	20	20	375
2N2915	45	3.0	10	60	10	17	600
2N2915A	45	2.0	5.0	60	15	26	900
2N2916	45	5.0	10	150	10	7	N.C.
2N2916A	45	2.0	5.0	150	15	10	300
2N2917	45	10	20	60	20	17	1450
2N2918	45	5.0	20	150	20	7	750
2N2919	60	3.0	10	60	10	17	600
2N2919A	60	1.5	5.0	60	10	17	600
2N2920	60	3.0	10	150	10	7	N.C.
2N2920A	60	1.5	5.0	150	10	7	300
2N2060	60	5.0	10	25	10	40	N.C.
2N2060A	60	3.0	5.0	25	10	40	N.C.
2N2060B	60	1.5	5.0	25	10	40	N.C.

NOTES:

1. TCI_{OS} Max and I_{OS} Max calculated from published data.
2. N.C. = Insufficient published data to calculate.
3. All of above are physically interchangeable pin-for-pin with MAT-01 and MAT-02 series.



MAT-01

MATCHED MONOLITHIC
DUAL TRANSISTOR

Precision Monolithics Inc.

FEATURES

- Low V_{OS} (V_{BE} Match) $40\mu V$ Typ
..... $100\mu V$ Max
- Low TCV_{OS} $0.5\mu V/^{\circ}C$ Max
- High h_{FE} 500 Min
- Excellent h_{FE} Linearity from 10nA to 10mA
- Low Noise Voltage $0.23\mu V_{p-p}$ — 0.1Hz to 10Hz
- High Breakdown 45V Min

ORDERING INFORMATION†

$T_A = 25^{\circ}C$ V_{OS} MAX (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
0.1	MAT01AH*	MIL
0.5	MAT01GH*	MIL

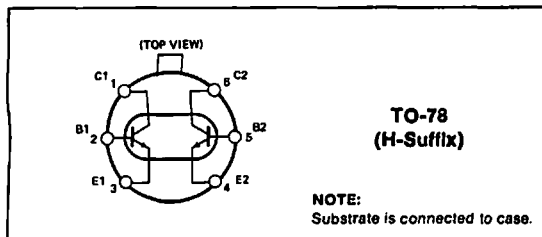
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The MAT-01 is a monolithic dual NPN transistor. An exclusive Silicon Nitride "Triple-Passivation" process provides excellent stability of critical parameters over both temperature and time. Matching characteristics include offset voltage of $40\mu V$, temperature drift of $0.15\mu V/^{\circ}C$, and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 at a collector current of only 10nA. The high gain at low collector current makes the MAT-01 ideal for use in low-power, low-level input stages.

PIN CONNECTIONS



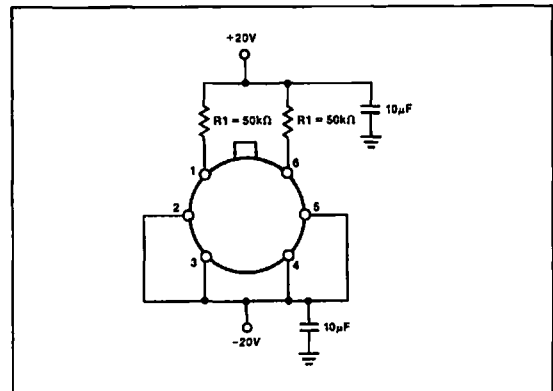
ABSOLUTE MAXIMUM RATINGS (Note 4)

Collector-Base Voltage (V_{CBO})	45V
MAT-01AH, GH, N	45V
Collector-Emitter Voltage (V_{CEO})	45V
MAT-01AH, GH, N	45V
Collector-Collector Voltage (V_{CC})	45V
MAT-01AH, GH, N	45V
Emitter-Emitter Voltage (V_{EE})	45V
MAT-01AH, GH, N	45V
Emitter-Base Voltage (V_{EB0}) (Note 1)	5V
Collector Current (I_C)	25mA
Emitter Current (I_E)	25mA
Total Power Dissipation	
Case Temperature $\leq 40^{\circ}C$ (Note 2)	1.8W
Ambient Temperature $\leq 70^{\circ}C$ (Note 3)	500mW
Operating Ambient Temperature	$-55^{\circ}C$ to $+125^{\circ}C$
Operating Junction Temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (Soldering, 60 sec)	$300^{\circ}C$
DICE Junction Temperature	$-65^{\circ}C$ to $+150^{\circ}C$

NOTES:

1. Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure V_{EB0} greater than the 5V rating shown.
2. Rating applies to applications using heat sinking to control case temperature. Derate linearly at $16.4mW/^{\circ}C$ for case temperatures above $40^{\circ}C$.
3. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at $6.3mW/^{\circ}C$ for ambient temperatures above $70^{\circ}C$.
4. Absolute maximum ratings apply to both DICE and packaged devices.

BURN-IN CIRCUIT



MATCHED TRANSISTORS

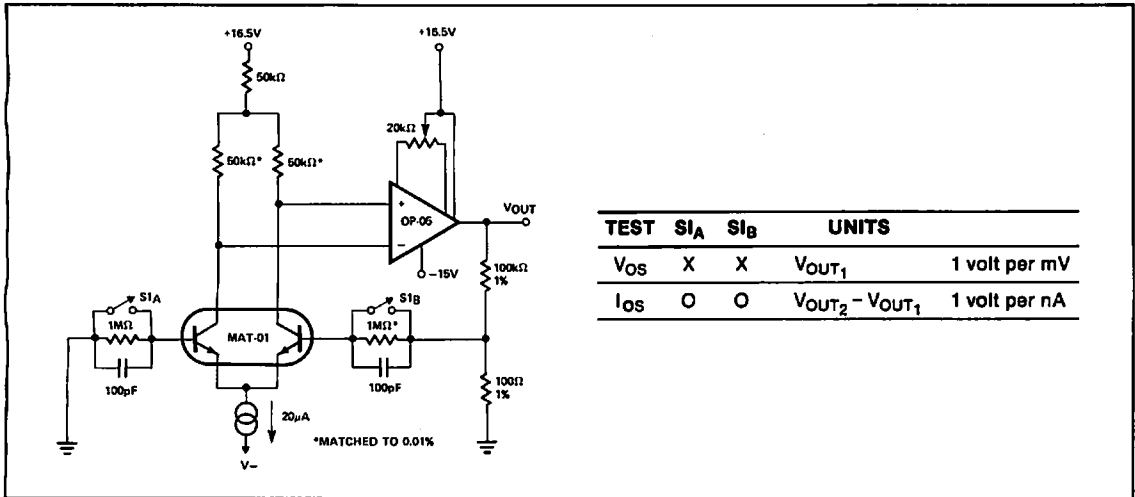
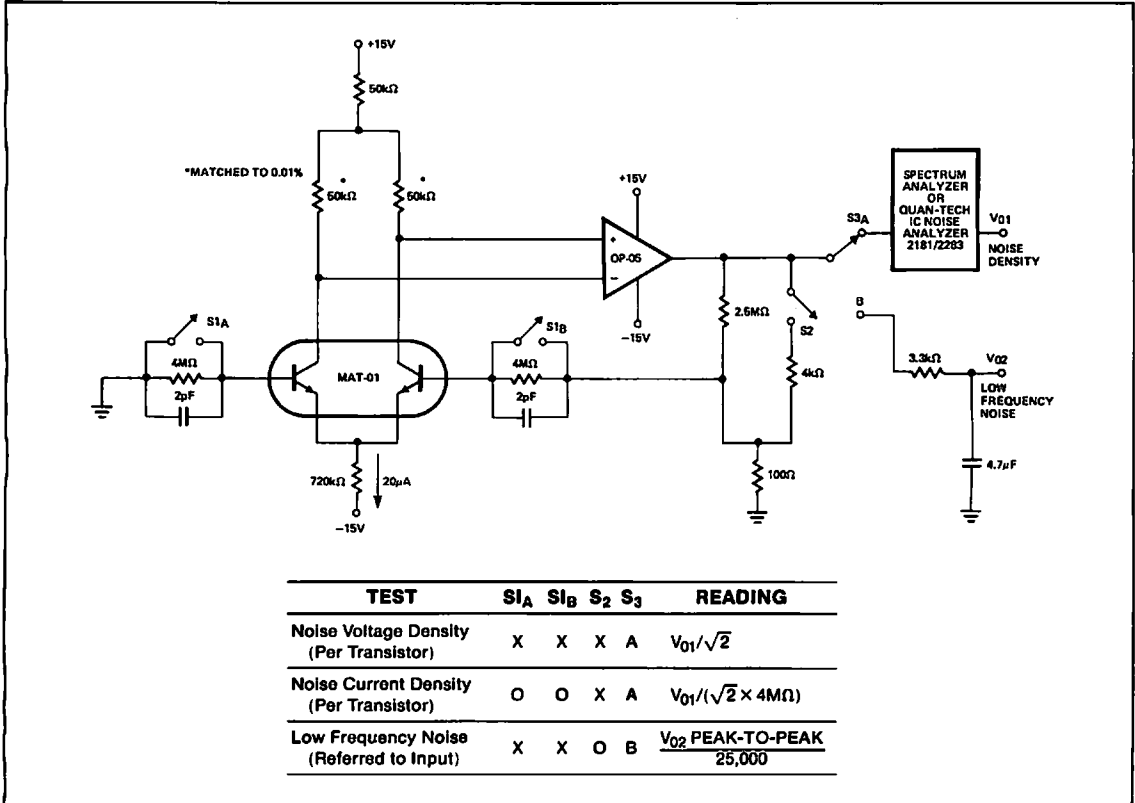
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**ELECTRICAL CHARACTERISTICS** at $V_{CB} = 15V$, $I_C = 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01AH			MAT-01GH			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Breakdown Voltage	BV_{CEO}	$I_C = 100\mu A$	45	—	—	45	—	—	V
Offset Voltage	V_{OS}		—	0.04	0.1	—	0.10	0.5	mV
Offset Voltage Stability	V_{OS}/Time	(Note 1)	—	2.0	—	—	2.0	—	$\mu V/\text{Mo}$
		(Note 2)	—	0.2	—	—	0.2	—	
Offset Current	I_{OS}		—	0.1	0.6	—	0.2	3.2	nA
Bias Current	I_B		—	13	20	—	18	40	nA
Current Gain	h_{FE}	$I_C = 10nA$	—	590	—	—	430	—	
		$I_C = 10\mu A$	500	770	—	250	560	—	
		$I_C = 10mA$	—	840	—	—	610	—	
Current Gain Match	Δh_{FE}	$I_C = 10\mu A$	—	0.7	3.0	—	1.0	8.0	%
		$100nA \leq I_C \leq 10mA$	—	0.8	—	—	1.2	—	
Low Frequency Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.23	0.4	—	0.23	0.4	μV_{p-p}
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	—	0.60	—	—	0.60	—	μV_{RMS}
Noise Voltage Density	e_n	$f_O = 10Hz$ (Note 3)	—	7.0	9.0	—	7.0	9.0	$nV/\sqrt{Hz}$
		$f_O = 100Hz$ (Note 3)	—	8.1	7.8	—	8.1	7.6	
		$f_O = 1000Hz$ (Note 3)	—	6.0	7.5	—	6.0	7.5	
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	—	0.5	3.0	—	0.8	8.0	$\mu V/V$
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30V$	—	2	15	—	3	70	pA/V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 30V$, $I_E = 0$ (Note 4)	—	15	50	—	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 30V$, $V_{BE} = 0$ (Notes 4, 6)	—	50	200	—	90	400	pA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = 30V$, (Note 6)	—	20	200	—	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 0.1mA$, $I_C = 1mA$	—	0.12	0.20	—	0.12	0.25	V
		$I_B = 1mA$, $I_C = 10mA$	—	0.8	—	—	0.8	—	
Gain-Bandwidth Product	f_T	$V_{CE} = 10V$, $I_C = 10mA$	—	450	—	—	450	—	MHz
Output Capacitance	C_{ob}	$V_{CB} = 15V$, $I_E = 0$	—	2.8	—	—	2.8	—	pF
Collector-Collector Capacitance	C_{CC}	$V_{CC} = 0$	—	8.5	—	—	8.5	—	pF

ELECTRICAL CHARACTERISTICS at $V_{CB} = 15V$, $I_C = 10\mu A$, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01AH			MAT-01GH			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}		—	0.06	0.15	—	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 7)	—	0.15	0.50	—	0.35	1.8	$\mu V/^\circ C$
Offset Current	I_{OS}		—	0.9	8.0	—	1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 5)	—	10	90	—	15	150	$pA/^\circ C$
Bias Current	I_B		—	28	60	—	36	130	nA
Current Gain	h_{FE}		187	400	—	77	300	—	
Collector-Base Leakage Current	I_{CBO}	$T_A = 125^\circ C$, $V_{CB} = 30V$, $I_E = 0$ (Note 4)	—	15	60	—	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	$T_A = 125^\circ C$, $V_{CE} = 30V$, $V_{BE} = 0$ (Notes 4, 6)	—	50	300	—	90	400	nA
Collector-Collector Leakage Current	I_{CC}	$T_A = 125^\circ C$, $V_{CC} = 30V$ (Note 6)	—	30	200	—	50	400	nA

MAT-01 TEST CIRCUITS
MAT-01 MATCHING MEASUREMENT CIRCUIT

MAT-01 NOISE MEASUREMENT CIRCUIT


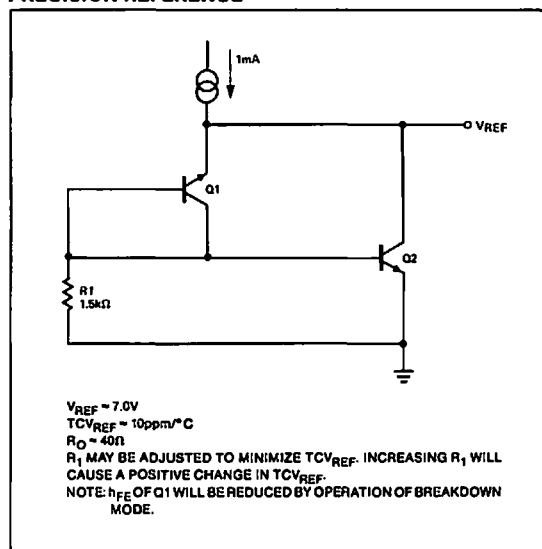
APPLICATION NOTES

Application of reverse bias voltages to the emitter-base junctions in excess of ratings (5V) may result in degradation of h_{FE} and h_{FE} matching characteristics. Circuit designs should be checked to ensure that reverse bias voltages above 5V cannot be applied during such transient conditions as at circuit turn-on and turn-off.

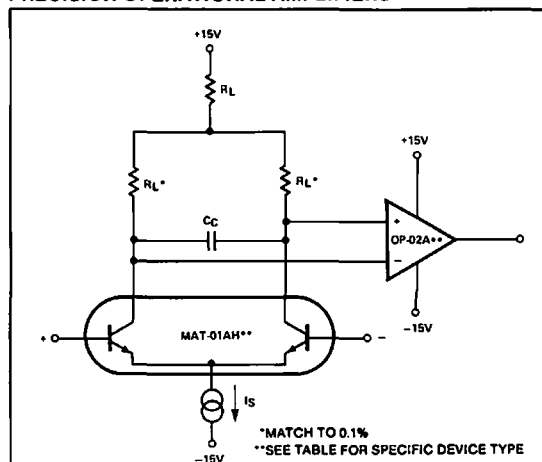
Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the predicted drift performance. Both input terminals should be maintained at the same temperature, preferably close to the temperature of the device's package.

TYPICAL APPLICATIONS

PRECISION REFERENCE



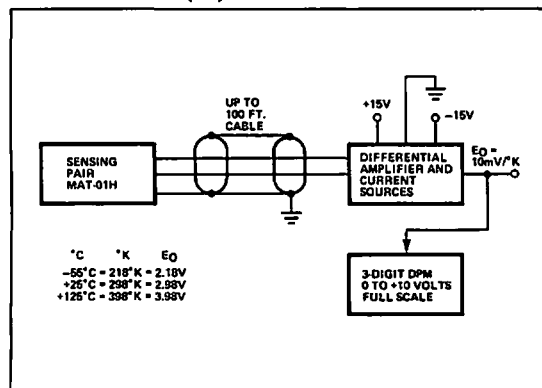
PRECISION OPERATIONAL AMPLIFIERS



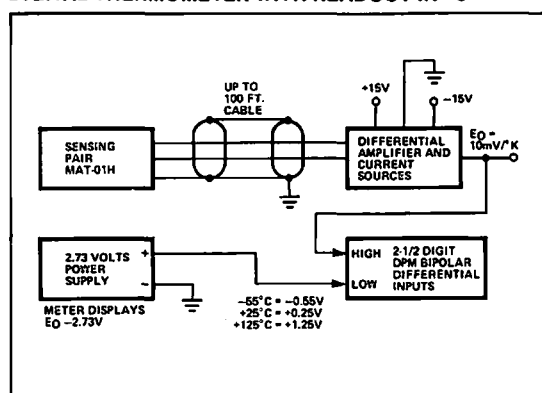
THIS CONFIGURATION CAN ALSO BE USED WITH THE LOW POWER OP-21 OR MICROPOWER OP-22 TO ACHIEVE A LOW NOISE AND LOW POWER PRECISION OP-AMP.

	MAT-01AH OP-02A	MAT-01AH OP-02A	MAT-01GH OP-02	MAT-01GH OP-02
V_{OS} Maximum	0.15mV	0.27mV	0.65mV	1.2mV
TCV_{OS} Maximum	0.6 μ V/ $^{\circ}C$	1 μ V/ $^{\circ}C$	2 μ V/ $^{\circ}C$	4 μ V/ $^{\circ}C$
I_{OS} Maximum	0.8nA	0.1nA	3.2nA	0.32nA
I_B Maximum	20nA	2nA	40nA	4nA
Gain Minimum	2,000,000	2,000,000	800,000	800,000
I_S	20 μ A	2 μ A	20 μ A	2 μ A
R_L	100k Ω	1M Ω	100k Ω	1M Ω

BASIC DIGITAL THERMOMETER READOUT IN DEGREES KELVIN ($^{\circ}K$)



DIGITAL THERMOMETER WITH READOUT IN $^{\circ}C$





Precision Monolithics Inc.

MAT-02

LOW-NOISE, MATCHED DUAL MONOLITHIC TRANSISTOR

FEATURES

- Low Offset Voltage $50\mu\text{V}$ Max
- Low Noise Voltage at 100Hz, 1mA ... $1.0\text{nV}/\sqrt{\text{Hz}}$ Max
- High Gain (h_{FE}) 500 Min at $I_C = 1\text{mA}$
..... 300 Min at $I_C = 1\mu\text{A}$
- Excellent Log Conformance $r_{BE} \approx 0.3\Omega$
- Low Offset Voltage Drift $0.1\mu\text{V}/^\circ\text{C}$ Max
- Improved Direct Replacement for LM194/394

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ V_{OS} Max (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-78 6-PIN	LCC	
50	MAT02AH*	—	MIL
50	MAT02EH	—	IND
150	MAT02BH*	MAT02BRC/883	MIL
150	MAT02FH	—	IND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

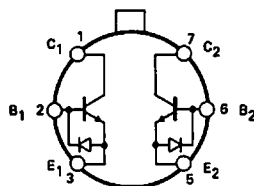
GENERAL DESCRIPTION

The design of the MAT-02 series of NPN dual monolithic transistors is optimized for very low noise, low drift, and low r_{BE} . Precision Monolithics' exclusive Silicon Nitride "Triple-Passivation" process stabilizes the critical device parameters over wide ranges of temperature and elapsed time. Also, the high current gain (h_{FE}) of the MAT-02 is maintained over a wide range of collector current. Exceptional characteristics of the MAT-02 include offset voltage of $50\mu\text{V}$ max (A/E grades) and $150\mu\text{V}$ max (B/F grades). Device performance is specified over the full military temperature range as well as at 25°C .

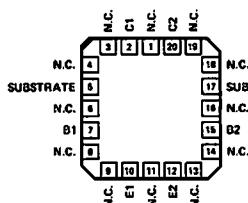
Input protection diodes are provided across the emitter-base junctions to prevent degradation of the device characteristics due to reverse-biased emitter current. The substrate is clamped to the most negative emitter by the parasitic isolation junction created by the protection diodes. This results in complete isolation between the transistors.

The MAT-02 should be used in any application where low noise is a priority. The MAT-02 can be used as an input stage to make an amplifier with noise voltage of less than $1.0\text{nV}/\sqrt{\text{Hz}}$ at 100Hz. Other applications, such as log/anti-log circuits, may use the excellent logging conformity of the MAT-02. Typical bulk resistance is only 0.3Ω to 0.4Ω . The MAT-02 electrical characteristics approach those of an ideal transistor when operated over a collector current range of $1\mu\text{A}$ to 10mA . For applications requiring multiple devices see MAT-04 Quad Matched Transistor data sheet.

PIN CONNECTIONS



TO-78
(H-Suffix)



MAT-02BRC/883
20-LEAD LCC
(RC-Suffix)

NOTE: Substrate is connected to case on TO-78 package. Substrate is normally connected to the most negative circuit potential, but can be floated.

ABSOLUTE MAXIMUM RATINGS (Note 3)

Collector-Base Voltage (BV_{CBO})	40V
Collector-Emitter Voltage (BV_{CEO})	40V
Collector-Collector Voltage (BV_{CC})	40V
Emitter-Emitter Voltage (BV_{EE})	40V
Collector Current (I_C)	20mA
Emitter Current (I_E)	20mA
Total Power Dissipation	
Case Temperature $\leq 40^\circ\text{C}$ (Note 1)	1.8W
Ambient Temperature $\leq 70^\circ\text{C}$ (Note 2)	500mW
Operating Temperature Range	
MAT-02A, B	-55°C to $+125^\circ\text{C}$
MAT-02E, F	-25°C to $+85^\circ\text{C}$
Operating Junction Temperature	-55°C to $+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to $+150^\circ\text{C}$

NOTES:

1. Rating applies to applications using heat sinking to control case temperature. Derate linearly at $16.4\text{mW}/^\circ\text{C}$ for case temperature above 40°C .
2. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at $6.3\text{mW}/^\circ\text{C}$ for ambient temperature above 70°C .
3. Absolute maximum ratings apply to both DICE and packaged devices.

MATCHED TRANSISTORS

**ELECTRICAL CHARACTERISTICS** at $V_{CB} = 15V$, $I_C = 10\mu A$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02A/E			MAT-02B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$I_C = 1mA$ (Note 1)	500	605	—	400	605	—	
		$I_C = 100\mu A$	500	590	—	400	590	—	
		$I_C = 10\mu A$	400	550	—	300	550	—	
		$I_C = 1\mu A$	300	485	—	200	485	—	
Current Gain Match	Δh_{FE}	$10\mu A \leq I_C \leq 1mA$, (Note 2)	—	0.5	2	—	0.5	4	%
Offset Voltage	V_{OS}	$V_{CB} = 0$ $1\mu A \leq I_C \leq 1mA$ (Note 7)	—	10	50	—	80	150	μV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq V_{MAX}$, (Note 6) $1\mu A \leq I_C \leq 1mA$ (Note 7)	—	10	25	—	10	50	μV
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	$V_{CB} = 0V$ $1\mu A \leq I_C \leq 1mA$ (Note 7)	—	5	25	—	5	50	μV
Offset Current Change vs V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq V_{MAX}$	—	30	70	—	30	70	pA/V
Bulk Resistance	r_{BE}	$10\mu A \leq I_C \leq 10mA$ (Note 3)	—	0.3	0.5	—	0.3	0.5	Ω
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$	—	25	200	—	25	400	pA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$, (Notes 3, 5)	—	35	200	—	35	400	pA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}$, (Notes 3, 5) $V_{BE} = 0$	—	35	200	—	35	400	pA
Noise Voltage Density	e_n	$I_C = 1mA$, $V_{CB} = 0$, (Note 4)	—	1.6	2	—	1.8	3	$nV/\sqrt{Hz}$
		$f_O = 10Hz$	—	0.9	1	—	0.9	2	
		$f_O = 100Hz$	—	0.85	1	—	0.85	2	
		$f_O = 10kHz$	—	0.85	1	—	0.85	2	
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1mA$ $I_B = 100\mu A$	—	0.05	0.1	—	0.05	0.2	V
Input Bias Current	I_B	$I_C = 10\mu A$	—	—	25	—	—	34	nA
Input Offset Current	I_{OS}	$I_C = 10\mu A$	—	—	0.8	—	—	1.3	nA
Breakdown Voltage	BV_{CEO}		40	—	—	40	—	—	V
Gain-Bandwidth Product	f_T	$I_C = 10mA$, $V_{CE} = 10V$	—	200	—	—	200	—	MHz
Output Capacitance	C_{OB}	$V_{CB} = 15V$, $I_E = 0$	—	23	—	—	23	—	pF
Collector-Collector Capacitance	C_{CO}	$V_{CC} = 0$	—	35	—	—	35	—	pF

NOTES:

- Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.
- Current Gain Match (Δh_{FE}) is defined as:

$$\Delta h_{FE} = \frac{100 (\Delta I_B) (h_{FE \min})}{I_C}$$

3. Guaranteed by design.

4. Sample tested.

5. I_{CC} and I_{CES} are verified by measurement of I_{CBO} .6. This is the maximum change in V_{OS} as V_{CB} is swept from 0V to 40V.7. Measured at $I_C = 10\mu A$ and guaranteed by design over the specified range of I_C .

**ELECTRICAL CHARACTERISTICS** $V_{CB} = 15V$, $-25^{\circ}C \leq T_A \leq +85^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02E			MAT-02F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}	$V_{CB} = 0$ $1\mu A \leq I_C \leq 1mA$ (Note 5)	—	—	70	—	—	220	μV
Average Offset Voltage Drift	TCV_{OS}	$10\mu A \leq I_C \leq 1mA$, $0 \leq V_{CB} \leq V_{MAX}$, (Note 1)	—	0.08	0.3	—	0.08	1	$\mu V/^{\circ}C$
		V_{OS} Trimmed to Zero, (Note 3)	—	0.03	0.1	—	0.03	0.3	
Input Offset Current	I_{OS}	$I_C = 10\mu A$	—	—	8	—	—	13	nA
Input Offset Current Drift	TCI_{OS}	$I_C = 10\mu A$, (Note 4)	—	40	90	—	40	150	$pA/^{\circ}C$
Input Bias Current	I_B	$I_C = 10\mu A$	—	—	45	—	—	50	nA
Current Gain	h_{FE}	$I_C = 1mA$, (Note 2)	325	—	—	300	—	—	
		$I_C = 100\mu A$	275	—	—	250	—	—	
		$I_C = 10\mu A$	225	—	—	200	—	—	
		$I_C = 1\mu A$	200	—	—	150	—	—	
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$	—	2	—	—	3	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}$, $V_{BE} = 0$	—	3	—	—	4	—	nA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$	—	3	—	—	4	—	nA

ELECTRICAL CHARACTERISTICS $V_{CB} = 15V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, unless otherwise noted.

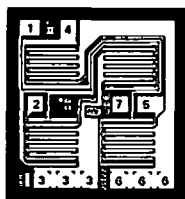
PARAMETER	SYMBOL	CONDITIONS	MAT-02A			MAT-02B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage	V_{OS}	$V_{CB} = 0$ $1\mu A \leq I_C \leq 1mA$ (Note 5)	—	—	80	—	—	250	μV
Average Offset Voltage Drift	TCV_{OS}	$10\mu A \leq I_C \leq 1mA$, $0 \leq V_{CB} \leq V_{MAX}$, (Note 1)	—	0.08	0.3	—	0.08	1	$\mu V/^{\circ}C$
		V_{OS} Trimmed to Zero, (Note 3)	—	0.03	0.1	—	0.03	0.3	
Input Offset Current	I_{OS}	$I_C = 10\mu A$	—	—	9	—	—	15	nA
Input Offset Current Drift	TCI_{OS}	$I_C = 10\mu A$, (Note 4)	—	40	90	—	40	150	$pA/^{\circ}C$
Input Bias Current	I_B	$I_C = 10\mu A$	—	—	60	—	—	70	nA
Current Gain	h_{FE}	$I_C = 1mA$, (Note 2)	275	—	—	250	—	—	
		$I_C = 100\mu A$	225	—	—	200	—	—	
		$I_C = 10\mu A$	175	—	—	150	—	—	
		$I_C = 1\mu A$	150	—	—	100	—	—	
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$ $T_A = 125^{\circ}C$	—	15	—	—	25	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = V_{MAX}$, $V_{BE} = 0$ $T_A = 125^{\circ}C$	—	50	—	—	50	—	nA
Collector-Collector Leakage Current	I_{CC}	$V_{CC} = V_{MAX}$ $T_A = 125^{\circ}C$	—	30	—	—	40	—	nA

NOTES:

- Guaranteed by V_{OS} test ($TCV_{OS} \approx \frac{V_{OS}}{T}$ for $V_{OS} < V_{BE}$) $T = 298K$ for $T_A = 25^{\circ}C$.
- Current gain is guaranteed with Collector-Base Voltage V_{CB} swept from 0 to V_{MAX} at the indicated collector current.
- The initial zero offset voltage is established by adjusting the ratio of I_{C1} to I_{C2} at $T_A = 25^{\circ}C$. This ratio must be held to 0.003% over the entire temperature range. Measurements are taken at the temperature extremes and $25^{\circ}C$.
- Guaranteed by design.
- Measured at $I_C = 10\mu A$ and guaranteed by design over the specified range of I_C .



DICE CHARACTERISTICS



1. COLLECTOR 1
2. BASE 1
3. EMITTER 1
4. COLLECTOR 2
5. BASE 2
6. EMITTER 2
7. SUBSTRATE

DIE SIZE 0.061×0.057 inch, 3,477 sq. mils
(1.549×1.448 mm, 224 sq. mm)

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at 25°C for $V_{CB} = 15\text{V}$ and $I_C = 10\mu\text{A}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}		40	V MIN
Offset Voltage	V_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ (Note 1)	150	μV MAX
Input Offset Current	I_{OS}		1.2	nA MAX
Input Bias Current	I_B	$V_{CB} = 0\text{V}$	34	nA MAX
Current Gain	h_{FE}	$I_C = 1\text{mA}$, $V_{CB} = 0\text{V}$ $I_C = 10\mu\text{A}$, $V_{CB} = 0\text{V}$	400 300	MIN
Current Gain Match	Δh_{FE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$, $V_{CB} = 0\text{V}$	4	% MAX
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$0\text{V} \leq V_{CB} \leq 40\text{V}$ $10\mu\text{A} \leq I_C \leq 1\text{mA}$ (Note 1)	50	μV MAX
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	$V_{CB} = 0$ $10\mu\text{A} \leq I_C \leq 1\text{mA}$ (Note 1)	50	μV MAX
Bulk Resistance	r_{BE}	$100\mu\text{A} \leq I_C \leq 10\text{mA}$	0.5	Ω MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1\text{mA}$ $I_B = 100\mu\text{A}$	0.2	V MAX

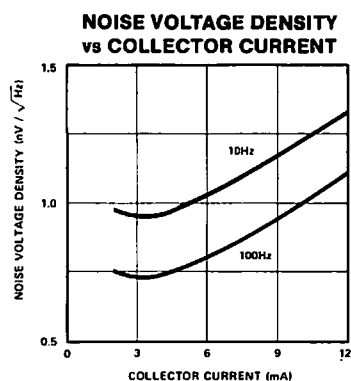
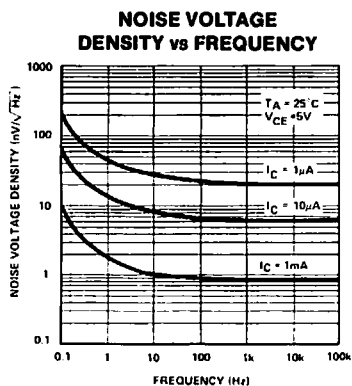
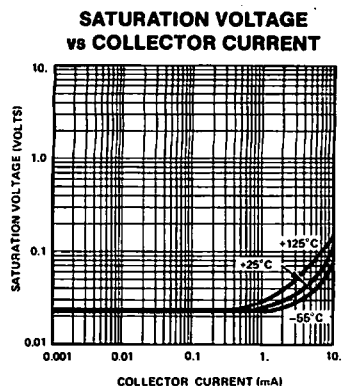
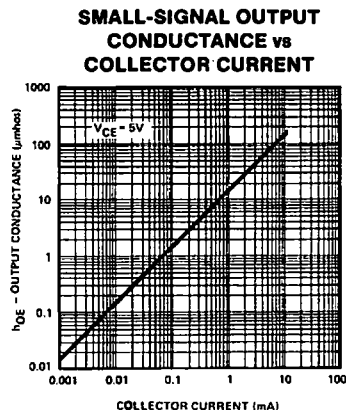
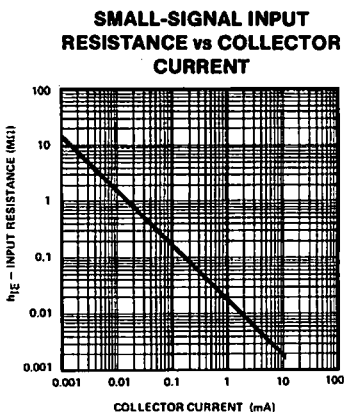
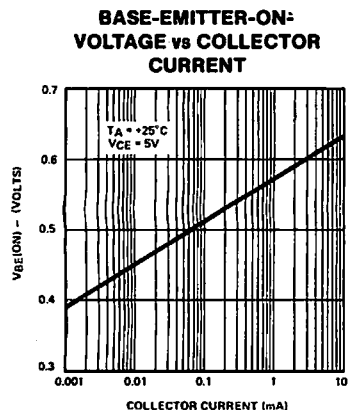
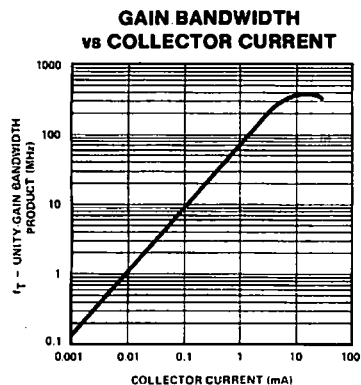
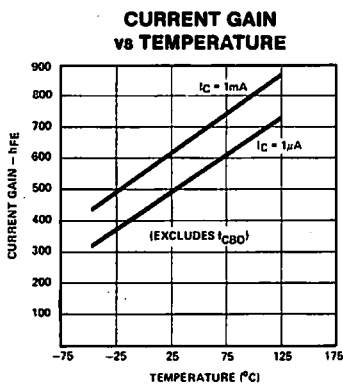
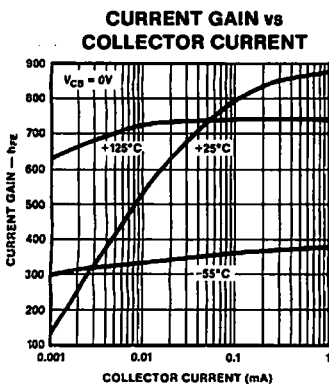
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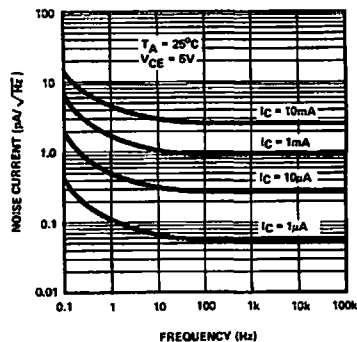
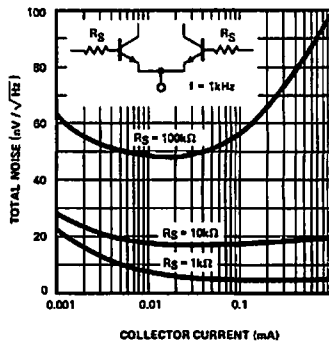
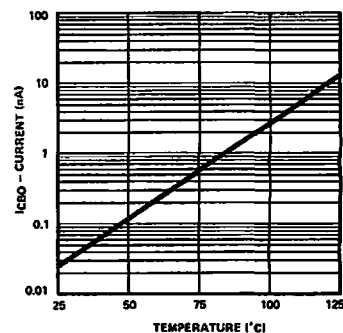
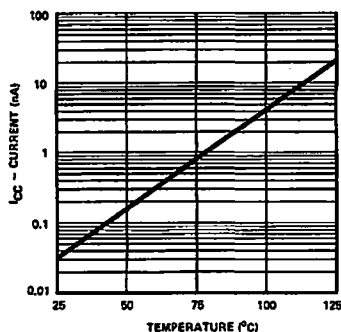
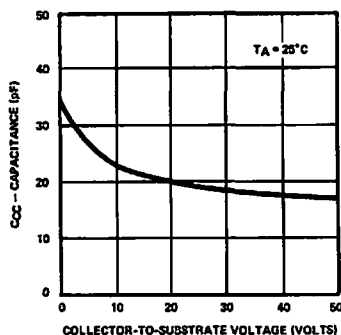
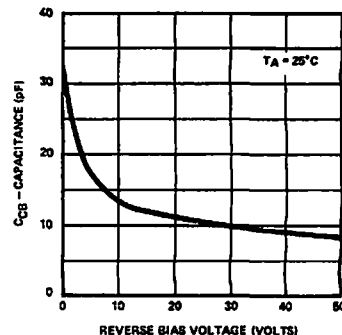
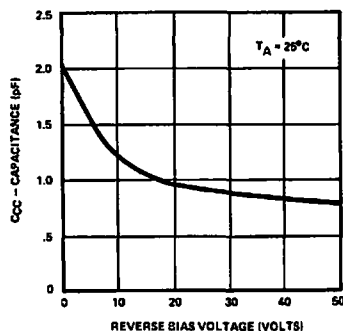
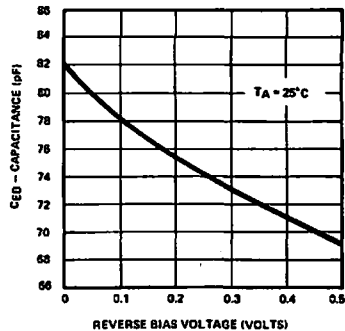
1. Measured at $I_C = 10\mu\text{A}$ and guaranteed by design over the specified range of I_C .

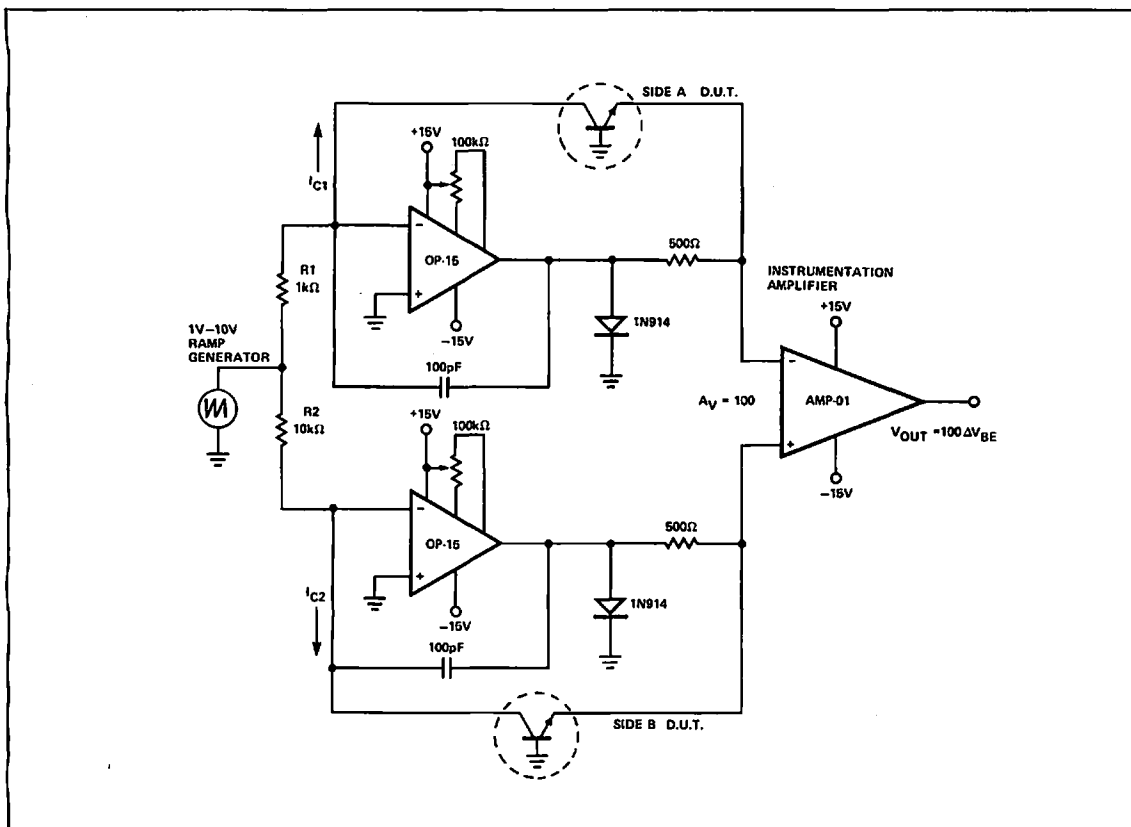
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS $V_{CB} = 15\text{V}$, $I_C = 10\mu\text{A}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02N TYPICAL	UNITS
Average Offset Voltage Drift	TCV_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0 \leq V_{CB} \leq V_{MAX}$	0.08	$\mu\text{V}/^{\circ}\text{C}$
Average Offset Current Drift	TCI_{OS}	$I_C = 10\mu\text{A}$	40	$\text{pA}/^{\circ}\text{C}$
Gain-Bandwidth Product	f_T	$V_{CE} = 10\text{V}$, $I_C = 10\text{mA}$	200	MHz
Offset Current Change vs V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 40\text{V}$	70	pA/V

TYPICAL PERFORMANCE CHARACTERISTICS


TYPICAL PERFORMANCE CHARACTERISTICS
NOISE CURRENT DENSITY vs FREQUENCY

TOTAL NOISE vs COLLECTOR CURRENT

COLLECTOR-TO-BASE LEAKAGE vs TEMPERATURE

COLLECTOR-TO-COLLECTOR LEAKAGE vs TEMPERATURE

COLLECTOR-TO-COLLECTOR CAPACITANCE vs COLLECTOR-TO-SUBSTRATE VOLTAGE

COLLECTOR-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE

COLLECTOR-TO-COLLECTOR CAPACITANCE vs REVERSE BIAS VOLTAGE

EMITTER-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE


LOG CONFORMANCE TEST CIRCUIT

LOG CONFORMANCE TESTING

The log conformance of the MAT-02 is tested using the circuit shown above. The circuit employs a dual transdiode logarithmic converter operating at a fixed ratio of collector currents that are swept over a 10:1 range. The output of each transdiode converter is the V_{BE} of the transistor plus an error term which is the product of the collector current and r_{BE} , the bulk emitter resistance. The difference of the V_{BE} is amplified at a gain of $\times 100$ by the AMP-01 instrumentation amplifier. The differential emitter-base voltage (ΔV_{BE}) consists of a temperature-dependent DC level plus an AC error voltage which is the deviation from true log conformity as the collector currents vary.

The output of the transdiode logarithmic converter comes from the idealized intrinsic transistor equation (for silicon):

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} \quad \text{where} \quad (1)$$

k = Boltzmann's Constant ($1.38062 \times 10^{-23} \text{ J/}^\circ\text{K}$)

q = Unit Electron Charge ($1.60219 \times 10^{-19} \text{ C}$)

T = Absolute Temperature, $^\circ\text{K}$ ($= ^\circ\text{C} + 273.2$)

I_S = Extrapolated Current for $V_{BE} = 0$

I_C = Collector Current

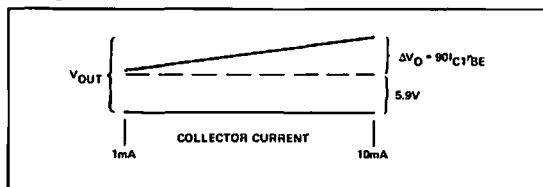
An error term must be added to this equation to allow for the bulk resistance (r_{BE}) of the transistor. Error due to the op amp input current is limited by use of the OP-15 BIFET-input op amp. The resulting AMP-01 input is:

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{I_{C1}}{I_{C2}} + I_{C1} r_{BE1} - I_{C2} r_{BE2} \quad (2)$$

A ramp function which sweeps from 1V to 10V is converted by the op amps to a collector current ramp through each transistor. Because I_{C1} is made equal to $10 I_{C2}$, and assuming $T_A = 25^\circ\text{C}$, the previous equation becomes:

$$\Delta V_{BE} = 59\text{mV} + 0.9 I_{C1} r_{BE} \quad (\Delta r_{BE} = 0)$$

As viewed on an oscilloscope, the change in ΔV_{BE} for a 10:1 change in I_C is then displayed as shown below:



With the oscilloscope AC coupled, the temperature dependent term becomes a DC offset and the trace represents the deviation from true log conformity. The bulk resistance can be calculated from the voltage deviation ΔV_O and the change in collector current (9mA):

$$r_{BE} = \frac{\Delta V_O}{9\text{mA}} \times \frac{1}{100} \quad (3)$$

This procedure finds r_{BE} for Side A. Switching R_1 and R_2 will provide the r_{BE} for Side B. Differential r_{BE} is found by making $R_1 = R_2$.

APPLICATIONS: NONLINEAR FUNCTIONS

MULTIPLIER/DIVIDER CIRCUIT

The excellent log conformity of the MAT-02 over a very wide range of collector current makes it ideal for use in log-antilog circuits. Such nonlinear functions as multiplying, dividing, squaring, and square-rooting are accurately and easily implemented with a log-antilog circuit using two MAT-02 pairs (see Figure 1). The transistor circuit accepts three input currents (I_1 , I_2 , and I_3) and provides an output current I_O according to $I_O = I_1 I_2 / I_3$. All four currents must be positive in the log-antilog circuit, but negative input voltages can be

easily accommodated by various offsetting techniques. Protective diodes across each base-to-emitter junction would normally be needed, but these diodes are built into the MAT-02. External protection diodes are therefore not needed.

For the circuit shown in Figure 1, the operational amplifiers make $I_1 = V_X / R_1$, $I_2 = V_Y / R_2$, $I_3 = V_Z / R_3$, and $I_O = V_O / R_O$. The output voltage for this one-quadrant, log-antilog multiplier/divider is ideally:

$$V_O = \frac{R_3 R_O}{R_1 R_2} \frac{V_X V_Y}{V_Z} \quad (V_X, V_Y, V_Z > 0) \quad (4)$$

If all the resistors (R_O , R_1 , R_2 , R_3) are made equal, then $V_O = V_X V_Y / V_Z$. Resistor values of 50k Ω to 100k Ω are recommended assuming an input range of 0.1V to +10V.

ERROR ANALYSIS

The base-to-emitter voltage of the MAT-02 in its forward-active operation is:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} + r_{BE} I_C, V_{CB} \sim 0 \quad (5)$$

The first term comes from the idealized intrinsic transistor equation previously discussed (see equation (1)).

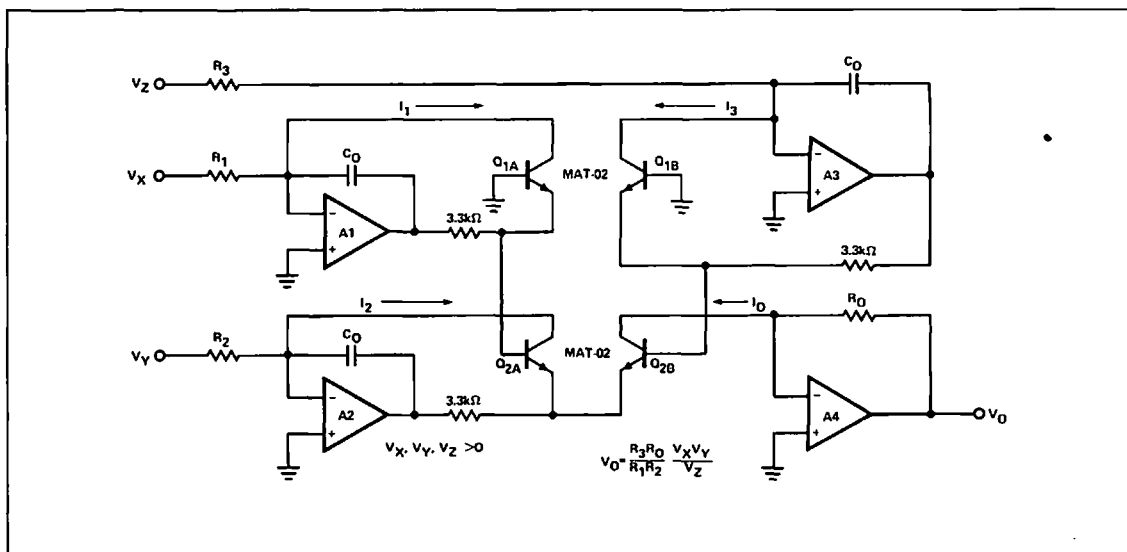


Figure 1. One-Quadrant Multiplier/Divider

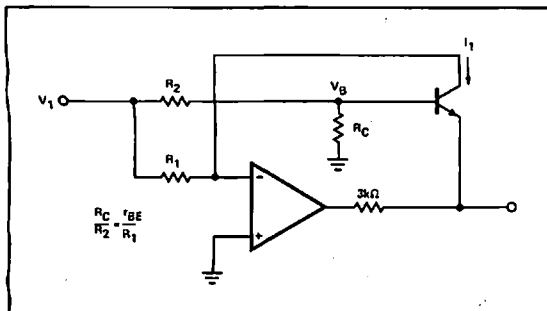


Figure 2. Compensation of Bulk Resistance Error

Extrinsic resistive terms and the Early effect cause departure from the ideal logarithmic relationship. For small V_{CB} , all of these effects can be lumped together as a total effective bulk resistance r_{BE} . The r_{BE}/C term causes departure from the desired logarithmic relationship. The r_{BE} term for the MAT-02 is less than 0.5Ω and Δr_{BE} between the two sides is negligible.

Returning to the multiplier/divider circuit of Figure 1 and using Equation (4):

$$V_{BE1A} + V_{BE2A} - V_{BE2B} - V_{BE1B} + (I_1 + I_2 - I_O - I_3) r_{BE} = 0$$

If the transistor pairs are held to the same temperature, then:

$$\frac{kT}{q} \ln \frac{I_1 I_2}{I_3 I_O} = \frac{kT}{q} \ln \frac{I_{S1A} I_{S2A}}{I_{S1B} I_{S2B}} + (I_1 + I_2 - I_O - I_3) r_{BE} \quad (6)$$

If all the terms on the right-hand side were zero, then we would have $\ln(I_1 I_2 / I_3 I_O)$ equal to zero which would lead directly to the desired result:

$$I_O = \frac{I_1 I_2}{I_3}, \text{ where } I_1, I_2, I_3, I_O > 0 \quad (7)$$

Note that this relationship is temperature independent. The right-hand side of Equation (6) is near zero and the output current I_O will be approximately $I_1 I_2 / I_3$. To estimate error, define ϕ as the right-hand side terms of Equation (6):

$$\phi = \ln \frac{I_{S1A} I_{S2A}}{I_{S1B} I_{S2B}} + \frac{q}{kT} (I_1 + I_2 - I_O - I_3) r_{BE} \quad (8)$$

For the MAT-02, $\ln(I_{SA}/I_{SB})$ and $I_C r_{BE}$ are very small. For small ϕ , $e^\phi \sim 1 + \phi$ and therefore:

$$\begin{aligned} \frac{I_1 I_2}{I_3 I_O} &= 1 + \phi \\ I_O &\sim \frac{I_1 I_2}{I_3} (1 - \phi) \end{aligned} \quad (9)$$

The $\ln(I_{SA}/I_{SB})$ terms in ϕ cause a fixed gain error of less than $\pm 0.6\%$ from each pair when using the MAT-02, and this gain error is easily trimmed out by varying R_O . The $I_C r_{BE}$ terms are more troublesome because they vary with signal levels and are multiplied by absolute temperature. At 25°C , kT/q is

approximately 26mV and the error due to an r_{BE}/C term will be $r_{BE}/C/26\text{mV}$. Using an r_{BE} of 0.4Ω for the MAT-02 and assuming a collector-current range of up to $200\mu\text{A}$, then a peak error of 0.3% could be expected for an r_{BE}/C error term when using the MAT-02. Total error is dependent on the specific application configuration (multiply, divide, square, etc.) and the required dynamic range. An obvious way to reduce $I_C r_{BE}$ error is to reduce the maximum collector current, but then op amp offsets and leakage currents become a limiting factor at low input levels. A design range of no greater than $10\mu\text{A}$ to 1mA is generally recommended for most nonlinear function circuits.

A powerful technique for reducing error due to $I_C r_{BE}$ is shown in Figure 2. A small voltage equal to $I_C r_{BE}$ is applied to the transistor base. For this circuit:

$$V_B = \frac{R_C}{R_2} V_1 \text{ and } I_C r_{BE} = \frac{r_{BE}}{R_1} V_1 \quad (10)$$

The error from r_{BE}/C is cancelled if R_C/R_2 is made equal to r_{BE}/R_1 . Since the MAT-02 bulk resistance is approximately 0.39Ω , an R_C of 3.9Ω and R_2 of $10R_1$ will give good error cancellation.

In more complex circuits, such as the circuit in Figure 1, it may be inconvenient to apply a compensation voltage to each individual base. A better approach is to sum all compensation to the bases of Q1. The "A" side needs a base voltage of $(V_O/R_O + V_Z/R_3) r_{BE}$ and the "B" side needs a base voltage of $(V_X/R_1 + V_Y/R_2) r_{BE}$. Linearity of better than $\pm 0.1\%$ is readily achievable with this compensation technique.

Operational amplifier offsets are another source of error. In Figure 2, the input offset voltage and input bias current will cause an error in collector current of $(V_{OS}/R_1) + I_B$. A low offset op amp, such as the OP-07 with less than $75\mu\text{V}$ of V_{OS} and I_B of less than $\pm 3\text{nA}$, is recommended. The OP-22/32, a programmable micropower op amp, should be considered if low power consumption or single-supply operation is needed. The value of frequency-compensating capacitor (C_O) is dependent on the op amp frequency response and peak collector current. Typical values for C_O range from 30pF to 300pF .

FOUR-QUADRANT MULTIPLIER

A simplified schematic for a four-quadrant log/antilog multiplier is shown in Figure 3. As with the previously discussed one-quadrant multiplier, the circuit makes $I_O = I_1 I_2 / I_3$. The two input currents, I_1 and I_2 , are each offset in the positive direction. This positive offset is then subtracted out at the output stage. Assuming ideal op amps, the currents are:

$$I_1 = \frac{V_X}{R_1} + \frac{V_R}{R_2}, \quad I_2 = \frac{V_Y}{R_1} + \frac{V_R}{R_2} \quad (11)$$

$$I_O = \frac{V_X}{R_1} + \frac{V_Y}{R_1} + \frac{V_R}{R_2} + \frac{V_O}{R_O}, \quad I_3 = \frac{V_R}{R_2}$$

From $I_O = I_1 I_2 / I_3$, the output voltage will be:

$$V_O = \frac{R_O R_2}{R_1^2} \frac{V_X V_Y}{V_R} \quad (12)$$

Collector-current range is the key design decision. The inherently low r_{BE} of the MAT-02 allows the use of a relatively high collector current. For input scaling of $\pm 10V$ full-scale and using a 10V reference, we have a collector-current range for I_1 and I_2 of:

$$\left(\frac{-10}{R_1} + \frac{10}{R_2}\right) \leq I_C \leq \left(\frac{10}{R_1} + \frac{10}{R_2}\right) \quad (13)$$

Practical values for R_1 and R_2 would range from 50k Ω to 100k Ω . Choosing an R_1 of 82k Ω and R_2 of 62k Ω provides a collector-current range of approximately 39 μA to 283 μA . An R_O of 108k Ω will then make the output scale factor 1/10 and $V_O = V_X V_Y / 10$. The output, as well as both inputs, are scaled for $\pm 10V$ full-scale.

Linear error for this circuit is substantially improved by the small correction voltage applied to the base of Q1 as shown in Figure 3. Assuming an equal bulk emitter resistance for each MAT-02 transistor, then the error is nulled if:

$$(I_1 + I_2 - I_3 - I_O) r_{BE} + \rho V_O = 0$$

The currents are known from the previous discussion, and the relationship needed is simply:

$$V_O = \frac{r_{BE}}{R_O} V_O \quad (14)$$

The output voltage is attenuated by a factor of r_{BE}/R_O and applied to the base of Q1 to cancel the summation of voltage drops due to $r_{BE}I_C$ terms. This will make $\ln(I_1 I_2 / I_3 I_O)$ more nearly zero which will thereby make $I_O = I_1 I_2 / I_3$ a more accurate relationship. Linearity of better than 0.1% is readily achievable with this circuit if the MAT-02 pairs are carefully kept at the same temperature.

MULTIFUNCTION CONVERTER

The multifunction converter circuit provides an accurate means of squaring, square rooting, and of raising ratios to arbitrary powers. The excellent log conformity of the MAT-02 allows a wide range of exponents. The general transfer function is:

$$V_O = V_Y \left(\frac{V_Z}{V_X} \right)^m \quad (15)$$

V_X , V_Y , and V_Z are input voltages and the exponent "m" has a practical range of approximately 0.2 to 5. Inputs V_X and V_Y are often taken from a fixed reference voltage. With a REF-01 providing a precision $\pm 10V$ to both V_X and V_Y , the transfer function would simplify to:

$$V_O = 10 \left(\frac{V_Z}{10} \right)^m \quad (16)$$

As with the multiplier/divider circuits, assume that the transistor pairs have excellent matching and are at the same temperature. The $\ln I_{SA}/I_{SB}$ will then be zero. In the circuit of Figure 4, the voltage drops across the base-emitter junctions of Q1 provide:

$$\frac{R_B}{R_B + KR_A} V_A = \frac{kT}{q} \ln \frac{I_Z}{I_X} \quad (17)$$

I_Z is V_Z/R_1 and I_X is V_X/R_1 . Similarly, the relationship for Q2 is:

$$\frac{R_B}{R_B + (1-K)R_A} V_A = \frac{kT}{q} \ln \frac{I_O}{I_Y} \quad (18)$$

I_O is V_O/R_O and I_Y is V_Y/R_1 . These equations for Q1 and Q2 can then be combined.

$$\frac{R_B + KR_A}{R_B + (1-K)R_A} \ln \frac{I_Z}{I_X} = \ln \frac{I_O}{I_Y} \quad (19)$$

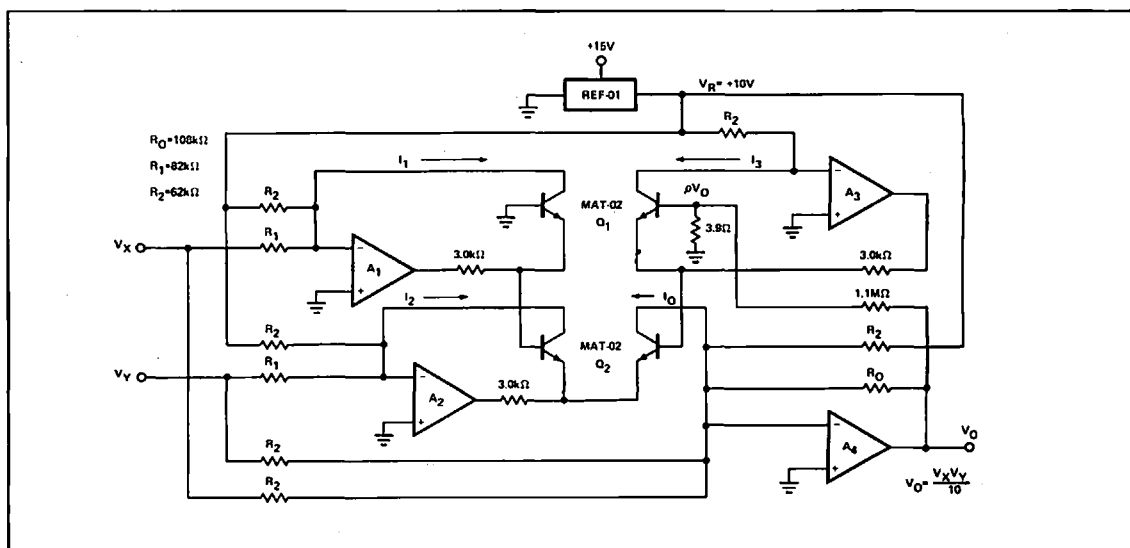


Figure 3. Four-Quadrant Multiplier

Substituting in the voltage relationships and simplifying leads to:

$$V_O = \frac{R_O}{R_1} V_Y \left(\frac{V_Z}{V_X} \right)^m, \text{ where} \quad (20)$$

$$m = \frac{R_B + KR_A}{R_B + (1-K)R_A}$$

The factor "K" is a potentiometer position and varies from zero to 1.0, so "m" ranges from $R_B/(R_A + R_B)$ to $(R_B + R_A)/R_B$. Practical values are 125Ω for R_B and 500Ω for R_A ; these values will provide an adjustment range of 0.2 to 5.0. A value of $100k\Omega$ is recommended for the R_1 resistors assuming a full-scale input range of 10V. As with the one-quadrant multiplier/divider circuit previously discussed, the V_X , V_Y , and V_Z inputs must all be positive.

The op amps should have the lowest possible input offsets. The OP-07 is recommended for most applications, although such programmable micropower op amps as the OP-22 or OP-32 offer advantages in low-power or single-supply circuits. The micropower op amps also have very low input-bias-current drift, an important advantage in log/antilog circuits. External offset nulling may be needed, particularly for applications requiring a wide dynamic range. Frequency-compensating capacitors, on the order of 50pF, may be required for A2 and A3. Amplifier A1 is likely to need a larger capacitor, typically $0.0047\mu F$, to assure stability.

Accuracy is limited at the higher input levels by bulk emitter resistance, but this is much lower for the MAT-02 than for other transistor pairs. Accuracy at the lower signal levels primarily depends on the op amp offsets. Accuracies of

better than 1% are readily achievable with this circuit configuration and can be better than $\pm 0.1\%$ over a limited operating range.

FAST LOGARITHMIC AMPLIFIER

The circuit of Figure 5 is a modification of a standard logarithmic amplifier configuration. Running the MAT-02 at 2.5mA per side (full-scale) allows a fast response with wide dynamic range. The circuit has a 7 decade current range, a 5' decade voltage range, and is capable of $2.5\mu\text{sec}$ settling time to 1% with a 1 to 10V step.

The output follows the equation:

$$V_O = \frac{R_3 + R_2}{R_2} \frac{kT}{q} \ln \frac{V_{REF}}{V_{in}} \quad (21)$$

The output is inverted with respect to the input, and is nominally $-1V/\text{decade}$ using the component values indicated.

LOW-NOISE $\times 1000$ AMPLIFIER

The MAT-02 noise voltage is exceptionally low, only $1nV/\sqrt{\text{Hz}}$ at 10Hz when operated over a collector-current range of 1 to 4mA. A single-ended $\times 1000$ amplifier that takes advantage of this low MAT-02 noise level is shown in Figure 6. In addition to low noise, the amplifier has very low drift and high CMRR. An OP-32 programmable low-power op amp is used for the second stage to obtain good speed with minimal power consumption. Small-signal bandwidth is 1MHz, slew-rate is $2.4V/\mu\text{s}$, and total supply current is approximately 2.8mA.

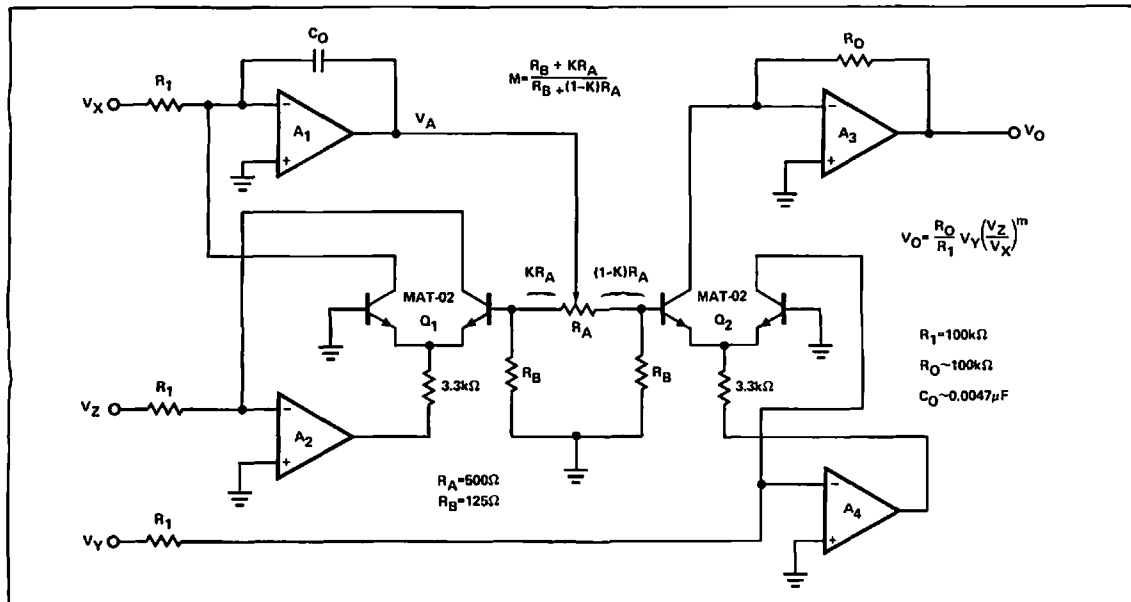


Figure 4. Multifunction Converter

Transistors Q2 and Q3 form a 2mA current source (0.65V/330Ω ~ 2mA). Each collector of Q1 operates at 1mA. The OP-32 inputs are 3V below the positive supply voltage ($R_L C \sim 3V$). The OP-32's low input offset current, typically less than 1nA, and low offset voltage of 1mV cause negligible error when referred to the amplifier input. Input stage gain is $9mR_L$, which is approximately 100 when operating at I_C of 1mA with R_L of 3kΩ. Since the OP-32 has a minimum open-loop gain of 500,000, total open-loop gain for the composite amplifier is over 50 million. Even at closed-loop gain of 1000, the gain error due to finite open-loop gain will be negligible. The OP-32 features excellent symmetry of slew-rate and very linear gain. Signal distortion is minimal.

Frequency compensation is very easy with this circuit; just vary the set-resistor R_S for the desired frequency response. Gain-bandwidth of the OP-32 varies directly with the supply current. A set resistor of 549kΩ was found to provide the best step response for this circuit. The resultant supply current is found from:

$$R_{SET} = \frac{(V+) - (V-) - (2V_{BE})}{I_{SET}}, I_{SY} = 15 I_{SET} \quad (22)$$

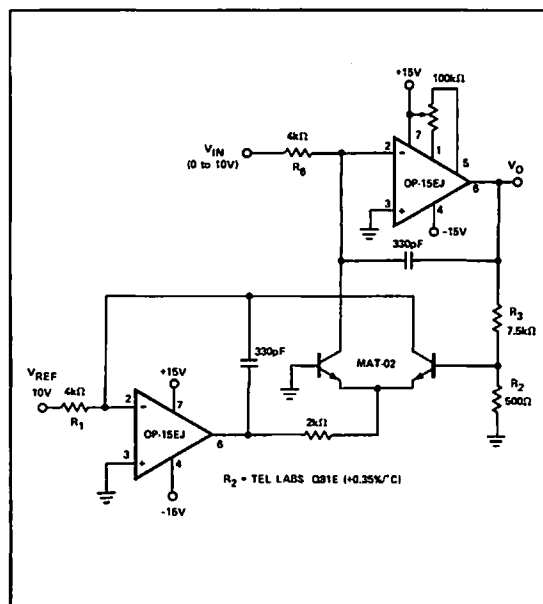


Figure 5. Fast Logarithmic Amplifier

The I_{SET} , using $\pm 15V$ supplies and an R_{SET} of 549kΩ, is approximately 52μA which will result in supply current of 784μA.

Dynamic range of this amplifier is excellent; the OP-32 has an output voltage swing of $\pm 14V$ with a $\pm 15V$ supply.

Input characteristics are outstanding. The MAT-02B/F has offset voltage of less than 150μV at 25°C and a maximum offset drift of 1μV/°C. Nulling the offset will further reduce offset drift. This can be accomplished by slightly unbalancing the collector load resistors. This adjustment will reduce the drift to less than 0.1μV/°C.

Input bias current is relatively low due to the high current gain of the MAT-02. The minimum β of 400 at 1mA for the MAT-02B/F implies an input bias current of approximately 2.5μA. This circuit should be used with signals having relatively low source impedance. A high source impedance will degrade offset and noise performance.

This circuit configuration provides exceptionally low input noise voltage and low drift. Noise can be reduced even further by raising the collector currents from 1mA to 3mA, but power consumption is then increased.

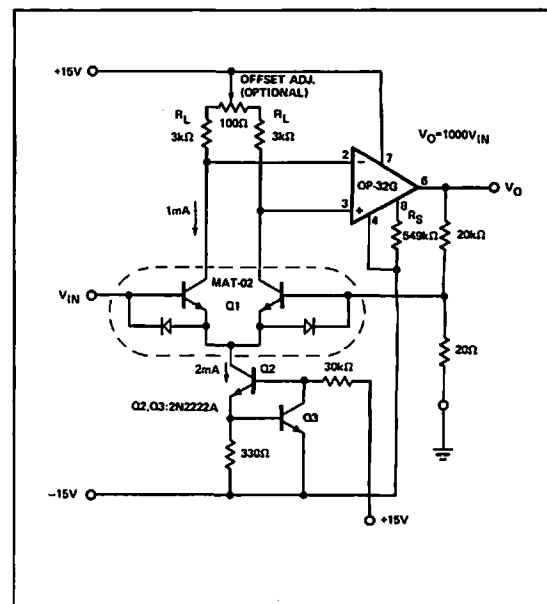


Figure 6. Low-Noise, Single-Ended X1000 Amplifier



Precision Monolithics Inc.

MAT-03

LOW-NOISE, MATCHED
DUAL PNP TRANSISTOR

ADVANCE PRODUCT INFORMATION

FEATURES

- Low Offset Voltage $50\mu\text{V}$ Max
- High Gain Bandwidth 150MHz Typ
- High Gain 100 Min
- Tight Gain Matching 2% Max
- Low Noise $1\text{nV}/\sqrt{\text{Hz}}$ @ 1kHz Max
- Outstanding Log Conformance $r_{\text{BE}} = 0.5\Omega$ Max

ORDERING INFORMATION†

$T_A = +25^\circ\text{C}$ V_{OS} MAX (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-78	LCC	
50	MAT03EH	—	XIND
150	MAT03AH*	MAT03ARC/883	MIL
150	MAT03FH	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip and TO-can packages. For ordering information see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

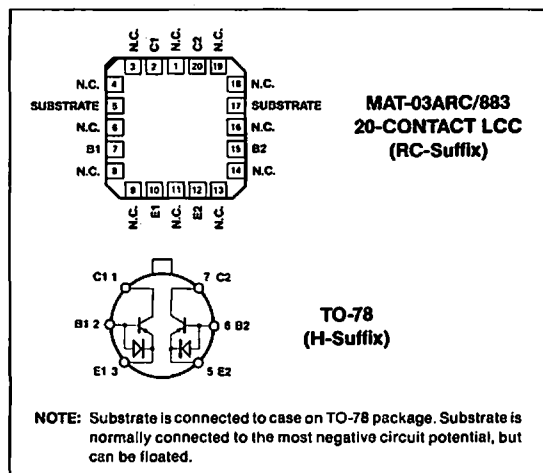
The MAT-03 is a monolithic dual PNP transistor that features outstanding parametric matching and high frequency performance. Offset voltage is under $50\mu\text{V}$ with gain matching better than 2%. Gain of the MAT-03 exceeds 100 with a high gain-bandwidth product of 150MHz . The MAT-03 also features extremely low noise, under $1\text{nV}/\sqrt{\text{Hz}}$ @ 1kHz , and excellent logarithmic conformance.

The tight parametric matching and superior logarithmic conformance of the MAT-03 makes it an ideal choice in current

sources and log-antilog circuits. The low noise of the MAT-03 also makes it ideal for low noise amplifiers.

The long-term stability of the MAT-03's matching parameters is guaranteed by the protection diodes across the base-emitter junction of each transistor. These diodes prevent degradation of the gain and matching characteristics of the MAT-03 due to excessive reverse bias base-emitter current.

PIN CONNECTIONS



MATCHED TRANSISTORS

This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Collector-Base Voltage (V_{CB0})	36V
Collector-Emitter Voltage (V_{CEO})	36V
Collector-Collector Voltage (V_{CC})	36V
Emitter-Emitter Voltage (V_{EE})	36V
Collector Current (I_C)	20mA
Emitter Current (I_E)	20mA
Total Power Dissipation	
Ambient Temperature $\leq 70^\circ\text{C}$ (Note 2)	500mW
Operating Temperature Range	
MAT-03A	-55°C to $+125^\circ\text{C}$
MAT-03E/F	-40°C to $+85^\circ\text{C}$

Operating Junction Temperature	-55°C to $+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C
DICE Junction Temperature	-65°C to $+150^\circ\text{C}$

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged devices.
2. Rating applies to TO-78 not using a heat sink and LCC; devices in free air only. For TO-78 derate linearly at $8.3\text{mW}/^\circ\text{C}$ above 70°C ambient temperature; for LCC derate at $7.8\text{mW}/^\circ\text{C}$.

ELECTRICAL CHARACTERISTICS at $V_{CB} = 15\text{V}$, $I_C = 10\mu\text{A}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-03E			MAT-03A/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$I_C = 1\text{mA}$ (Note 1)	100	—	—	80	—	—	
		$I_C = 10\mu\text{A}$	80	—	—	65	—	—	
Current Gain Match	Δh_{FE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$, (Note 2)	—	—	2	—	—	4	%
Offset Voltage	V_{OS}	$V_{CB} = 0$ $10\mu\text{A} \leq I_C \leq 1\text{mA}$	—	—	50	—	—	150	μV
Offset Voltage Change vs. V_{CB}	$\Delta V_{OS} / \Delta V_{CB}$	$0 \leq V_{CB} \leq V_{MAX}$, (Note 3) $10\mu\text{A} \leq I_C \leq 1\text{mA}$	—	—	25	—	—	50	μV
Offset Voltage Change vs. Collector Current	$\Delta V_{OS} / \Delta I_C$	$V_{CB} = 0\text{V}$ $10\mu\text{A} \leq I_C \leq 1\text{mA}$	—	—	25	—	—	50	μV
Offset Current Change vs. V_{CB}	$\Delta I_{OS} / \Delta V_{CB}$	$0 \leq V_{CB} \leq V_{MAX}$	—	—	70	—	—	70	pA/V
Bulk Resistance	r_{BE}	$10\mu\text{A} \leq I_C \leq 10\text{mA}$	—	0.3	0.5	—	0.3	0.5	Ω
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = V_{MAX}$	—	—	200	—	—	400	pA
Noise Voltage Density	e_n	$I_C = 1\text{mA}$, $V_{CB} = 0$, (Note 4)	—	—	2	—	—	3	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 10\text{Hz}$	—	—	1	—	—	2	
		$f_O = 100\text{Hz}$	—	—	1	—	—	2	
		$f_O = 1\text{kHz}$	—	—	1	—	—	2	
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1\text{mA}$ $I_B = 100\mu\text{A}$	—	—	0.1	—	—	0.2	V
Breakdown Voltage	V_{CEO}		36	—	—	36	—	—	V
Gain-Bandwidth Product	f_T	$I_C = 10\text{mA}$, $V_{CE} = 10\text{V}$	—	150	—	—	150	—	MHz

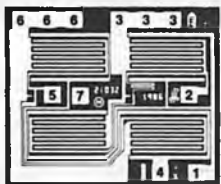
NOTES:

1. Current gain is measured with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.
2. Current Gain Match (Δh_{FE}) is defined as:
3. This is the maximum change in V_{OS} as V_{CB} is swept from 0V to 36V.
4. Sample tested.

$$\Delta h_{FE} = \frac{100 (\Delta I_B) (h_{FE \text{ min}})}{I_C}$$



DICE CHARACTERISTICS



DIE SIZE 0.070×0.060 inch, 4,200 sq. mils
(1.78×1.52 mm, 2.70 sq. mm)

1. COLLECTOR 1
2. BASE 1
3. EMITTER 1
4. COLLECTOR 2
5. BASE 2
6. EMITTER 2
7. SUBSTRATE

For additional DICE ordering information, refer to
1988 Data Book, Section 2.

WAFER TEST LIMITS at 25°C for $V_{CB} = 15\text{V}$ and $I_C = 10\mu\text{A}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}		36	V MIN
Offset Voltage	V_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$	150	μV MAX
Current Gain	h_{FE}	$I_C = 1\text{mA}, V_{CB} = 0\text{V}$	80	MIN
		$I_C = 10\mu\text{A}, V_{CB} = 0\text{V}$	65	
Current Gain Match	Δh_{FE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}, V_{CB} = 0\text{V}$	4	% MAX
Offset Voltage Change vs. V_{CB}	$\Delta V_{OS} / \Delta V_{CB}$	$0\text{V} \leq V_{CB} \leq 36\text{V}$	50	μV MAX
		$10\mu\text{A} \leq I_C \leq 1\text{mA}$		
Offset Voltage Change vs. Collector Current	$\Delta V_{OS} / \Delta I_C$	$V_{CB} = 0$	50	μV MAX
		$10\mu\text{A} \leq I_C \leq 1\text{mA}$		
Bulk Resistance	r_{BE}	$100\mu\text{A} \leq I_C \leq 10\text{mA}$	0.5	Ω MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 0.1\text{mA}$	0.2	V MAX
		$I_B = 10\mu\text{A}$		

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

FEATURES

- Low Offset Voltage 200 μ V Max
- High Current Gain 400 Min
- Excellent Current Gain Match 2% Max
- Low Noise Voltage at 100Hz, 1mA 2.5nV/ $\sqrt{\text{Hz}}$ Max
- Excellent Log Conformance $r_{BE} = 0.6\Omega$ Max
- Matching Guaranteed for All Transistors

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ $V_{OS} \text{ MAX}$ (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	HERMETIC DIP 14-PIN	PLASTIC 14-PIN	
200	MAT04AY*	—	MIL
200	MAT04EY	—	IND
400	MAT04BY*	—	MIL
400	MAT04FY	MAT04FP	IND
400	—	MAT04GS††	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cer-dip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

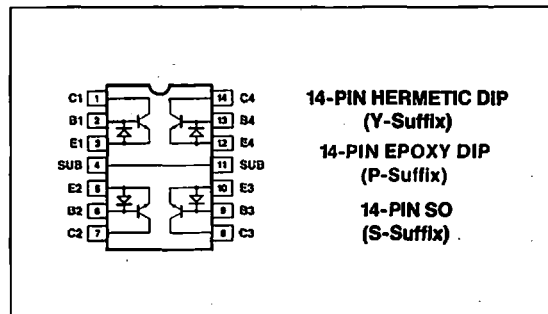
GENERAL DESCRIPTION

The MAT-04 is a quad monolithic NPN transistor that offers excellent parametric matching for precision amplifier and non-linear circuit applications. Performance characteristics of the MAT-04 include high gain (400 minimum) over a wide range of collector current, low noise (2.5nV/ $\sqrt{\text{Hz}}$ maximum at 100Hz, $I_C = 1\text{mA}$) and excellent logarithmic conformance. The MAT-04 also features a low offset voltage of 200 μV and tight current gain matching, to within 2%. Each transistor of the MAT-04 is individually tested to data sheet specifications. For matching parameters (offset voltage, input offset current, and gain match), each of the dual transistor combinations are verified to meet stated limits. Device performance is guaranteed at 25°C and over the industrial and military temperature ranges.

The long-term stability of matching parameters is guaranteed by the protection diodes across the base-emitter junction of each transistor. These diodes prevent degradation of beta and matching characteristics due to reverse bias base-emitter current.

The superior logarithmic conformance and accurate matching characteristics of the MAT-04 makes it an excellent choice for use in log and antilog circuits. The MAT-04 is an ideal choice in applications where low noise and high gain are required.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS (Note 1)

Collector-Base Voltage (BV_{CBO})	40V
Collector-Emitter Voltage (BV_{CEO})	40V
Collector-Collector Voltage (BV_{CC})	40V
Emitter-Emitter Voltage (BV_{EE})	40V
Collector Current	30mA
Emitter Current	30mA
Substrate (Pin-4 to Pin-11) Current	30mA
Total Power Dissipation (Note 2)	500mW
Operating Temperature Range	
MAT-04AY, BY	-55°C to +125°C
MAT-04EY, FY, FP	-25°C to +85°C
MAT-04GS	0°C to +70°C
Storage Temperature	
Y Package	-65°C to +150°C
P Package	-65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged devices.
2. The table below lists maximum ambient temperature ratings and derating factors.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin Hermetic DIP (Y)	100°C	10mW/°C
14-Pin Epoxy DIP (P)	42°C	6mW/°C



ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS} , I_{OS} , Δh_{FE}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04A/E			MAT-04B/F/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 1)	400	800	—	300	600	—	
Current Gain Match	Δh_{FE}	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 2)	—	0.5	2	—	1	4	%
Offset Voltage	V_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 4)	—	50	200	—	100	400	μV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0\text{V}$ (Note 4)	—	5	25	—	10	50	μV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 4)	—	50	100	—	100	200	μV
Bulk Emitter Resistance	r_{BE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0\text{V}$ (Note 5)	—	0.4	0.6	—	0.4	0.6	Ω
Input Bias Current	I_B	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	125	250	—	165	330	nA
Input Offset Current	I_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	0.6	5	—	2	13	nA
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu\text{A}$	40	—	—	40	—	—	V
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 100\mu\text{A}$ $I_C = 1\text{mA}$	—	0.03	0.06	—	0.03	0.06	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40\text{V}$	—	5	—	—	5	—	pA
Noise Voltage Density	e_n	$V_{CB} = 0\text{V}$ $f_O = 10\text{Hz}$ $I_C = 1\text{mA}$ $f_O = 100\text{Hz}$ (Note 3) $f_O = 1\text{kHz}$	—	2	3	—	2	4	$\text{nV}/\sqrt{\text{Hz}}$
Gain Bandwidth Product	f_T	$I_C = 1\text{mA}$ $V_{CE} = 10\text{V}$	—	300	—	—	300	—	MHz
Output Capacitance	C_{OBO}	$V_{CB} = 15\text{V}$ $I_E = 0$ $f = 1\text{MHz}$	—	10	—	—	10	—	pF
Input Capacitance	C_{EBO}	$V_{BE} = 0\text{V}$ $I_C = 0$ $f = 1\text{MHz}$	—	40	—	—	40	—	pF

NOTES:

- Current gain measured at $I_C = 10\mu\text{A}$, $100\mu\text{A}$ and 1mA .
- Current gain match is defined as: $\Delta h_{FE} = \frac{100 (\Delta I_B) (h_{FE \text{ min}})}{I_C}$
- Sample tested.
- Measured at $I_C = 10\mu\text{A}$ and guaranteed by design over the specified range of I_C .
- Guaranteed by design.

9

MATCHED TRANSISTORS



ELECTRICAL CHARACTERISTICS at $-25^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ for MAT-04E and F, $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for MAT-04G, unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS} , I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04E			MAT-04F/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 1)	225	625	—	200	500	—	
Offset Voltage	V_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 3)	—	60	260	—	120	520	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$ (Note 2)	—	0.2	1	—	0.4	2	$\mu\text{V}/^{\circ}\text{C}$
Input Bias Current	I_B	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	160	445	—	200	500	nA
Input Offset Current	I_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	4	20	—	8	40	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	50	—	—	100	—	$\text{pA}/^{\circ}\text{C}$
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu\text{A}$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40\text{V}$	—	0.5	—	—	0.5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40\text{V}$	—	5	—	—	5	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40\text{V}$	—	0.7	—	—	0.7	—	nA

ELECTRICAL CHARACTERISTICS at $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS} , I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

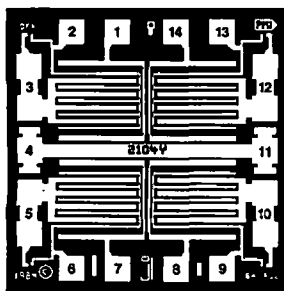
PARAMETER	SYMBOL	CONDITIONS	MAT-04A			MAT-04B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Current Gain	h_{FE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 1)	175	475	—	125	425	—	
Offset Voltage	V_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$ (Note 3)	—	70	300	—	140	600	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$ (Note 2)	—	0.2	1	—	0.4	2	$\mu\text{V}/^{\circ}\text{C}$
Input Bias Current	I_B	$I_C = 100\mu\text{A}$ $0\text{V} \leq V_{CB} \leq 30\text{V}$	—	210	570	—	235	800	nA
Input Offset Current	I_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	6	30	—	12	60	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0\text{V}$	—	50	—	—	100	—	$\text{pA}/^{\circ}\text{C}$
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu\text{A}$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40\text{V}$	—	5	—	—	5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40\text{V}$	—	100	—	—	100	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40\text{V}$	—	7	—	—	7	—	nA

NOTES:

- Current gain measured at $I_C = 10\mu\text{A}$, $100\mu\text{A}$ and 1mA .
- Guaranteed by V_{OS} test ($TCV_{OS} \leq V_{OS}/T$ for $V_{OS} \ll V_{BE}$) $T = 293^{\circ}\text{K}$ for $T_A = 25^{\circ}\text{C}$.
- Measured at $I_C = 10\mu\text{A}$ and guaranteed by design over the specified range of I_C .



DICE CHARACTERISTICS



DIE SIZE 0.060 × 0.060 inch, 3600 sq. mils
(1.52 × 1.52 mm, 2.31 sq. mm)

1. Q1 COLLECTOR
2. Q1 BASE
3. Q1 EMITTER
4. SUBSTRATE
5. Q2 EMITTER
6. Q2 BASE
7. Q2 COLLECTOR
8. Q3 COLLECTOR
9. Q3 BASE
10. Q3 EMITTER
11. SUBSTRATE
12. Q4 EMITTER
13. Q4 BASE
14. Q4 COLLECTOR

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS} , I_{OS} , Δh_{FE}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04N LIMITS	UNITS
Current Gain	h_{FE}	$I_C = 100\mu\text{A}$ $0V \leq V_{CB} \leq 30V$	300	MIN
Current Gain Match	Δh_{FE}	$I_C = 100\mu\text{A}$, $V_{CB} = 0V$	4	% MAX
Offset Voltage	V_{OS}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0V \leq V_{CB} \leq 30V$ (Note 1)	400	μV MAX
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0V$ (Note 1)	50	μV MAX
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $0V \leq V_{CB} \leq 30V$ (Note 1)	200	μV MAX
Bulk Emitter Resistance	r_{BE}	$10\mu\text{A} \leq I_C \leq 1\text{mA}$ $V_{CB} = 0V$ (Note 2)	0.6	Ω MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 100\mu\text{A}$ $I_C = 1\text{mA}$	0.06	V MAX
Input Bias Current	I_B	$I_C = 100\mu\text{A}$ $0V \leq V_{CB} \leq 30V$	330	nA MAX
Input Offset Current	I_{OS}	$I_C = 100\mu\text{A}$ $V_{CB} = 0V$	13	nA MAX
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu\text{A}$	40	V MIN

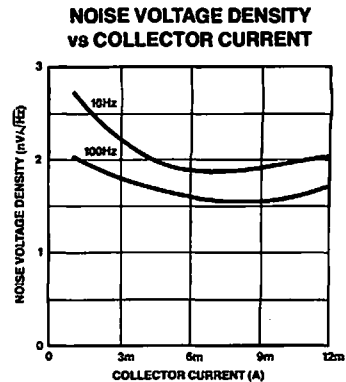
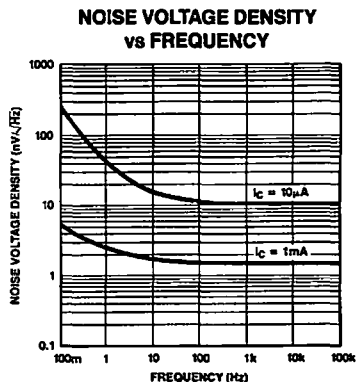
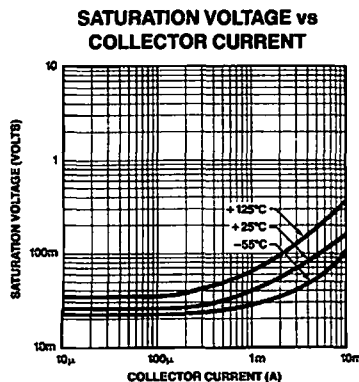
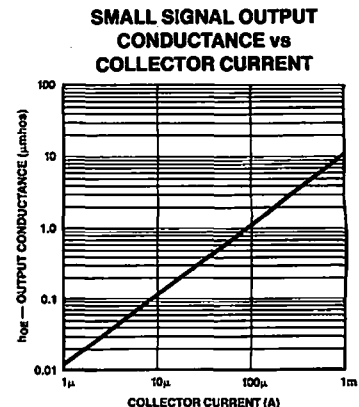
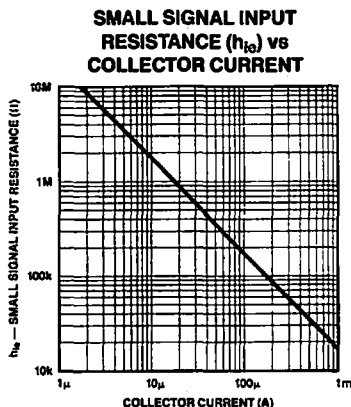
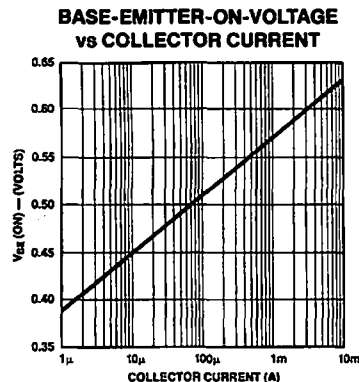
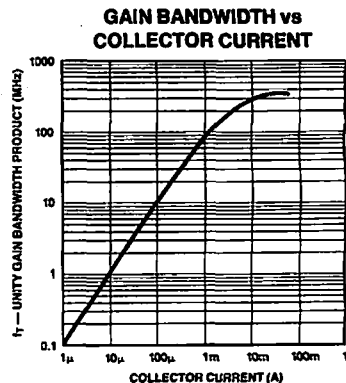
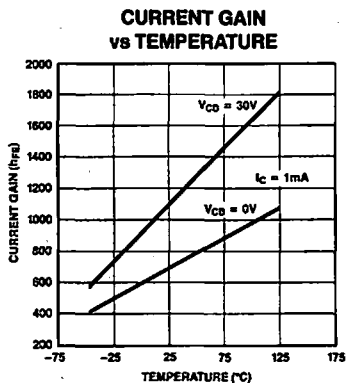
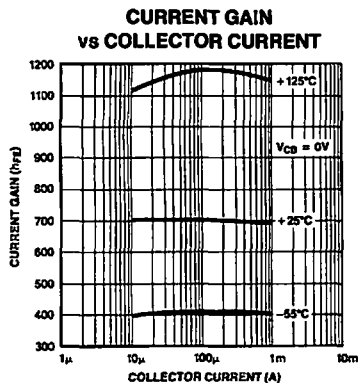
NOTES:

1. Measured at $I_C = 10\mu\text{A}$ and guaranteed by design over the specified range of I_C .

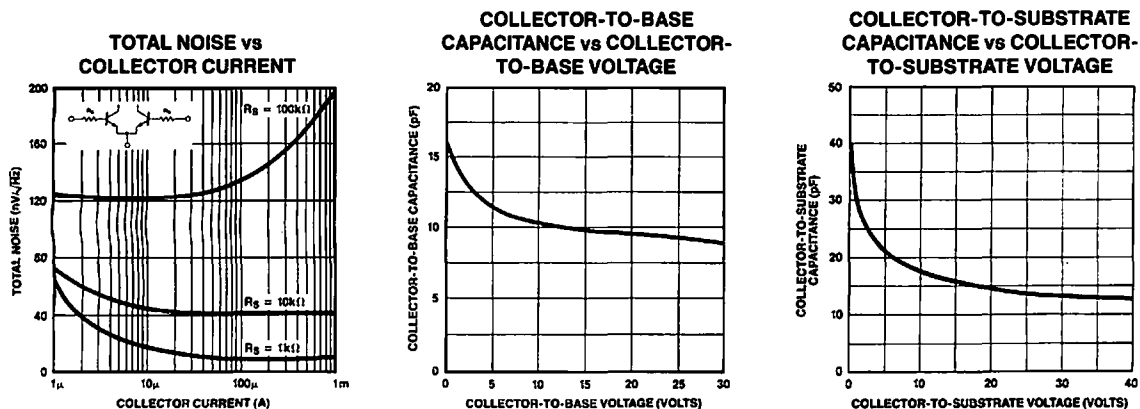
2. Guaranteed by design.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATION NOTES

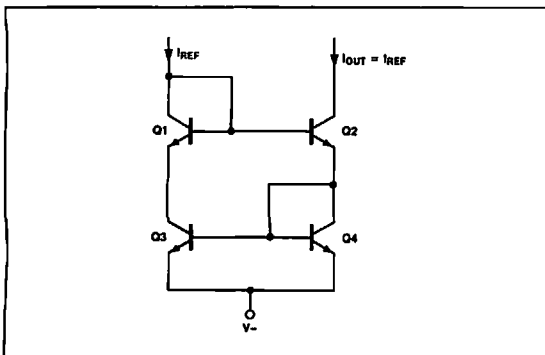
It is recommended that one of the substrate pins (Pins 4 and 11) be tied to the most negative circuit potential to minimize coupling between devices. Pins 4 and 11 are internally connected.

APPLICATIONS

CURRENT SOURCES

The MAT-04 can be used to implement a variety of high impedance current mirrors as shown in Figures 1, 2, and 3. These current mirrors can be used as biasing elements and load devices for amplifier stages.

FIGURE 1: Unity Gain Current Mirror, $I_{OUT} = I_{REF}$



The unity-gain current mirror of Figure 1, using a MAT-04AY, has an accuracy of better than 1% and an output impedance of over $100M\Omega$ at $100\mu A$. Figures 2 and 3 show modified current mirrors designed for a current gain of two, and one-half respectively. The accuracy of these mirrors is reduced from that of the unity-gain source due to base current errors but is still better than 2%.

FIGURE 2: Current Mirror, $I_{OUT} = 2(I_{REF})$

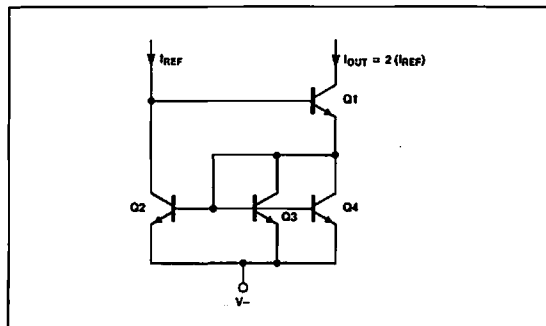


FIGURE 3: Current Mirror, $I_{OUT} = 1/2(I_{REF})$

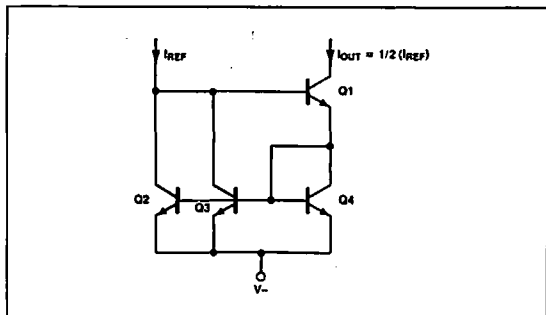
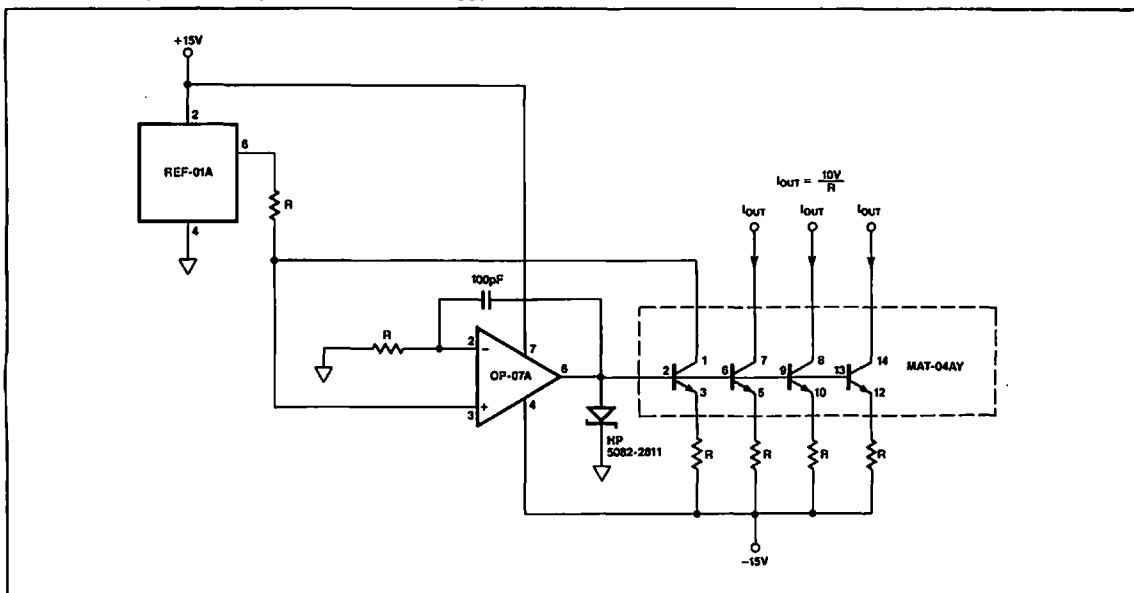


Figure 4 is a temperature independent current sink that has an accuracy of better than 1% over the military temperature range at an output current of $100\mu A$ to $1mA$. The Schottky diode acts as a clamp to insure correct circuit start-up at power on. The resistors used in this circuit should be 1% metal-film type.

FIGURE 4: Temperature Independent Current Sink, $I_{OUT} = 10V/R\Omega$ **NONLINEAR FUNCTIONS**

An application where precision matched-transistors are a powerful tool is in the generation of nonlinear functions. These circuits are based on the transistor's logarithmic property which takes the following idealized form:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S}$$

The MAT-04, with its excellent logarithmic conformance, maintains this idealized function over many decades of collector current. This, in addition to the stringent parametric matching of the MAT-04, enables the implementation of extremely accurate log/antilog circuits.

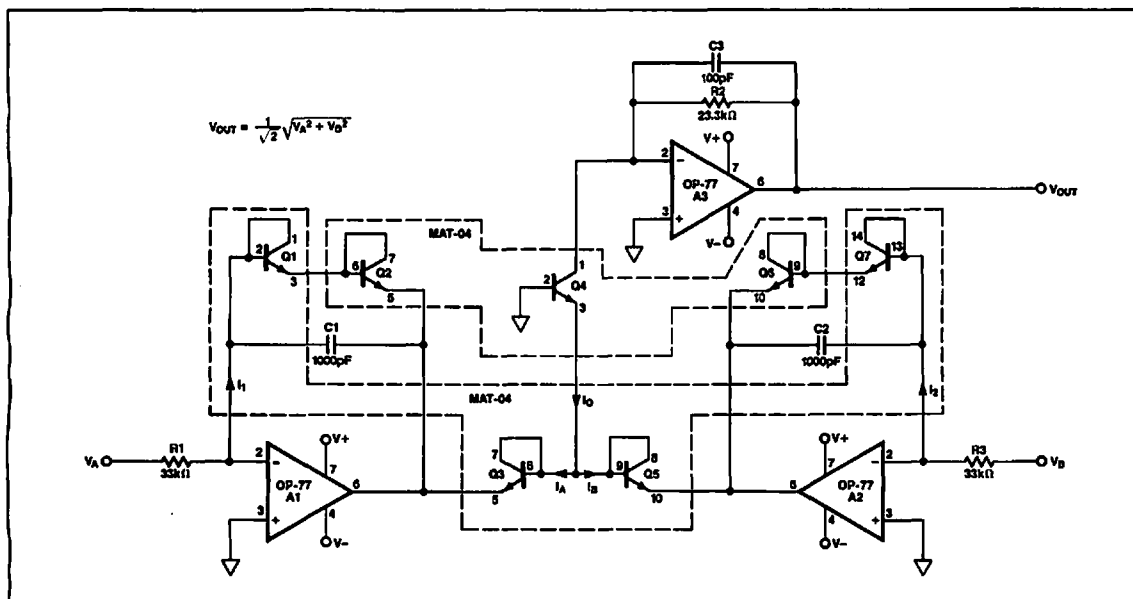
The circuit of Figure 5 is a vector summer that adds and subtracts logged inputs to generate the following transfer function:

$$V_{OUT} = \frac{1}{\sqrt{2}} \sqrt{V_A^2 + V_B^2}$$

This circuit uses two MAT-04AYs and maintains an accuracy of better than 0.5% over an input range of 10mV to 10V. The layout of the MAT-04s reduces errors due to matching and temperature differences between the two precision quad matched-transistors.

Op amps A1 and A2 translate the input voltages into logarithmic valued currents (I_A and I_B in Figure 5) that flow through transistor Q_3 and Q_5 . These currents are summed by transistor Q_4 ($I_O = I_A + I_B = \sqrt{I_1^2 + I_2^2}$) which feeds the current-to-voltage converter consisting of op amp A3. To maintain accuracy, 1% metal-film resistors should be used.

FIGURE 5: Vector Summer



LOW NOISE, HIGH SPEED INSTRUMENTATION AMPLIFIER

The circuit of Figure 6 is a very low noise, high speed amplifier, ideal for use in precision transducer and professional audio applications. The performance of the amplifier is summarized in Table I. Figure 7 shows the input referred spot noise over the 0-25kHz bandwidth to be flat at 1.2nV/√Hz. Figure 8 highlights the low 1/f noise corner at 2Hz.

The circuit uses a high speed op amp, the OP-17, preceded by an input amplifier. This consists of a precision dual matched-transistor, the MAT-02, and a feedback V-to-I converter, the MAT-04. The arrangement of the MAT-04 is known as a "linearized cross quad" which performs the voltage-to-current conversion. The OP-17 acts as an overall nulling amplifier to complete the feedback loop. Resistors R1, R2, and R3, R4 form voltage dividers that attenuate the output voltage swing since the "cross quad" arrangement has a limited input range. Biasing for the input stage is set by zener diode Z1. At low currents the effective zener voltage is about 3.3V due to the soft knee characteristic of the zener diode. This results in a bias current of 530μA per side for the input stage. The gain of this amplifier with the values shown in Figure 6 is:

$$\frac{V_{out}}{V_{in}} = \frac{33000}{R_G}$$

TABLE I: Instrumentation Amplifier Characteristics

Input Noise Voltage Density	G = 1000	1.2nV/√Hz
	G = 100	3.6nV/√Hz
	G = 10	30nV/√Hz
Bandwidth	G = 500	400kHz
	G = 100	1MHz
	G = 10	1.2MHz
Slew Rate		40V/μs
Common-Mode Rejection	G = 1000	130dB
	G = 100	
Distortion	f = 20Hz to 20kHz	0.03%
Settling Time	G = 1000	10μs
Power Consumption		350mW



FIGURE 6: Low Noise, High Speed Instrumentation Amplifier

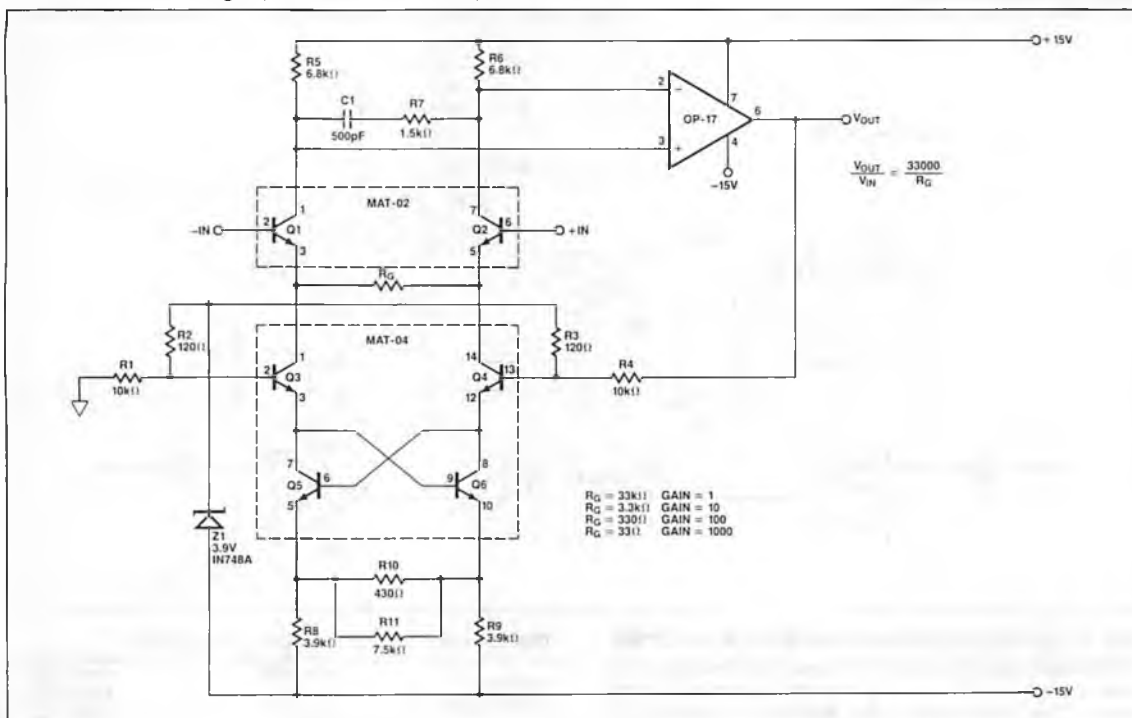


FIGURE 7: Spot Noise of the Instrumentation Amplifier from 0-25kHz at a Gain of 1000

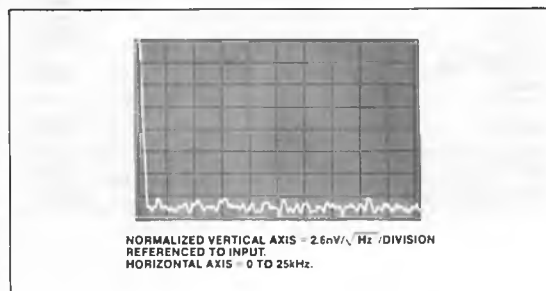


FIGURE 8: Low Frequency Noise Spectrum Showing Low 2Hz Noise Corner. Gain = 1000.

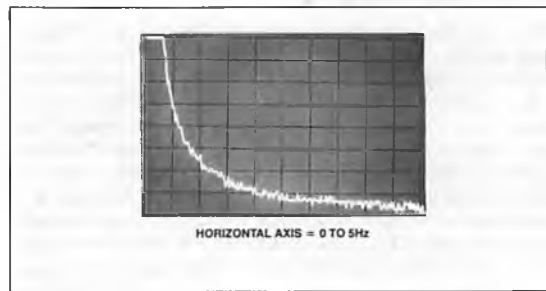
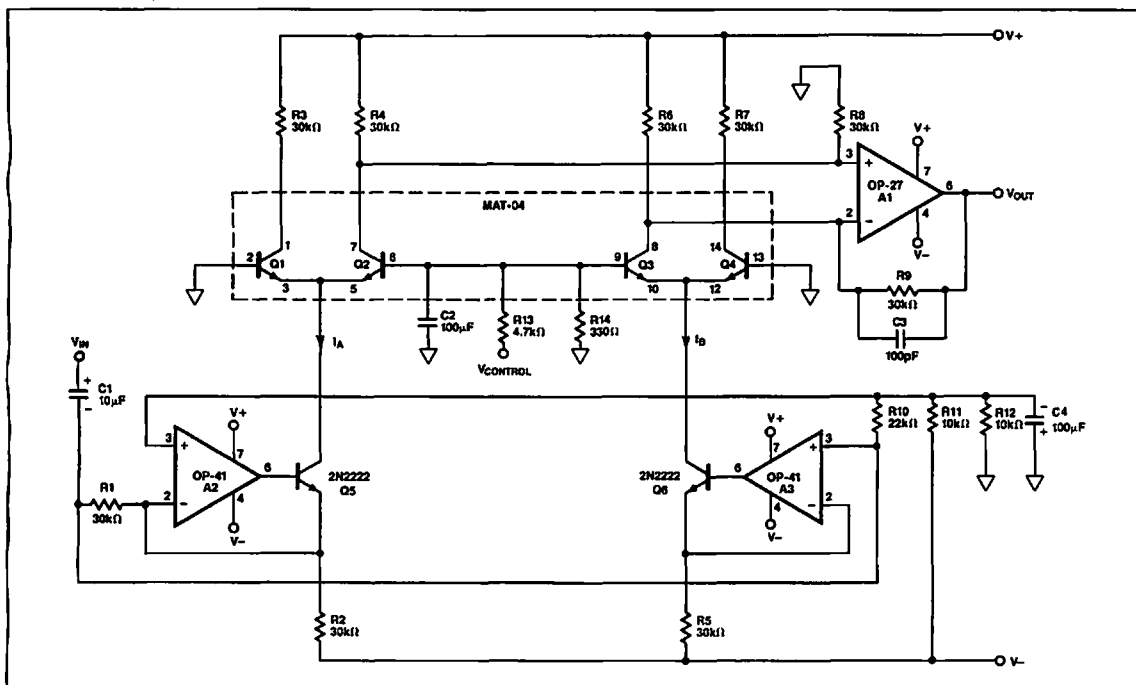


FIGURE 9: Voltage-Controlled Attenuator



VOLTAGE-CONTROLLED ATTENUATOR

The voltage-controlled attenuator (VCA) of Figure 9, widely used in professional audio circles, can easily be implemented using a MAT-04. The excellent matching characteristics of the MAT-04 enables the VCA to have a distortion level of under 0.03% over a wide range of control voltages. The VCA accepts a 3V RMS input and easily handles the full 20Hz-20kHz audio bandwidth as shown in Figure 10. Noise level for the VCA is more than 110dB below maximum output.

In the voltage-controlled attenuator, the input signal modulates the stage current of each differential pair. Op amps A2 and A3 in conjunction with transistors Q5 and Q6 form voltage-to-current converters that transform a single input voltage into differential currents which form the stage currents of each differential pair. The control voltage shifts the current between each side of the two differential pairs, regulating the signal level reaching the output stage which consists of op amp A1. Figure 11 shows the increase in signal attenuation as the control voltage becomes more negative.

The ideal transfer function for the voltage-controlled attenuator is:

$$V_{OUT}/V_{IN} = \frac{2}{1 + \exp \left((-V_{CONTROL}) \left(\frac{R_{14}}{R_{13} + R_{14}} \right) \left(\frac{kT}{q} \right) \right)}$$

Where k = Boltzmann constant $1.38 \times 10^{-23} \text{ J/}^\circ\text{K}$

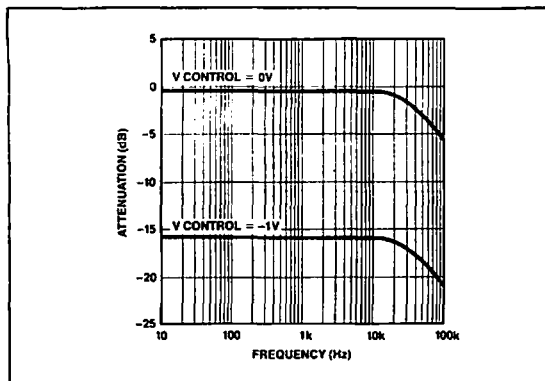
T = temperature in $^\circ\text{K}$

q = electronic charge = $1.602 \times 10^{-19} \text{ C}$

From the transfer function it can be seen that the maximum gain of the circuit is 2 (6dB).

To insure best performance, resistors R2 through R7 should be 1% metal film resistors. Since capacitor C2 can see small amounts of reverse bias when the control voltage is positive, it may be prudent to use a nonpolarized tantalum capacitor.

**FIGURE 10: Voltage-Controlled Attenuator,
Attenuation vs Frequency**



**FIGURE 11: Voltage-Controlled Attenuator,
Attenuation vs Control Voltage**

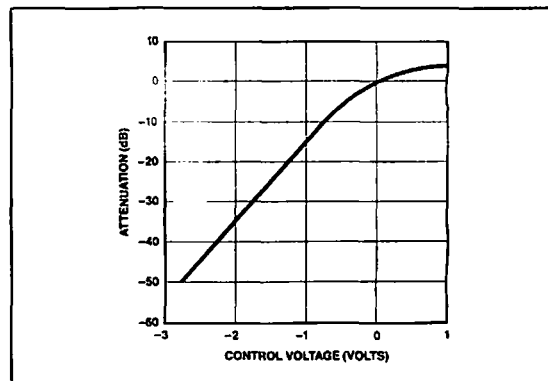


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*Indicates new product or product whose data sheet has been finalized since the 1986 data book.



Precision Monolithics Inc.

VOLTAGE REFERENCES

INTRODUCTION

Voltage references provide a constant output voltage irrespective of changes in input voltage, output current, or temperature. References are needed in such diverse equipment as power supplies, panel meters, calibration standards, precision current sources, data conversion systems, and control set-point circuits.

PMI references are fabricated using either a bandgap cell or a buried zener. The first method sums voltages with negative and positive temperature coefficients to yield a stable output voltage over temperature. A transistor base-emitter junction voltage (V_{BE}) exhibits a negative temperature coefficient, while the differential junction voltage of two transistors operating at unequal current densities (ΔV_{BE}) will exhibit a positive tempco. ΔV_{BE} is amplified and summed with V_{BE} to form a 1.23V bandgap cell which has a near-zero overall temperature coefficient. The 1.23V level is then amplified to the desired output voltage. Buried-zener references utilize a subsurface zener to produce a stable voltage, which is then amplified and buffered. Both methods may be trimmed for absolute tolerance and temperature coefficients using either zener-zap or laser trimming techniques.

A variety of output voltages are available. The REF-01, REF-02 and REF-03 are bandgap references producing +10V, +5V and +2.5V outputs respectively. The REF-02 provides an additional output voltage having a linear temperature dependence.

The REF-43 is a high-performance +2.5V bandgap reference, having a 5ppm/°C maximum drift with 0.05% initial output tolerance. 2.5V references are of value in systems operating from a 5V supply voltage.

Many data-converter ICs require a negative reference voltage, which in the past required an additional op amp to invert the output of a positive reference. The REF-08 serves this function, providing a stable -10V output. This reference is produced using a buried-zener diode.

The REF-05 and REF-10 are premium versions of the REF-01 and REF-02 that have guaranteed long-term stability and MIL-STD-883 process-

ing. Extensive testing over a long period of time, combined with tight control of processing, has enabled PMI to specify limits on output change with time.

DEFINITIONS

Line Regulation — The ratio of the change in output voltage to the change in input (line) voltage producing it. It includes the effects of self-heating.

Load Regulation — The ratio of the change in output voltage to the change in load current. It includes the effects of self-heating.

Output Change With Temperature (ΔV_{OT}) — The absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of the typical output voltage.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{V_O \text{ (Typical)}} \right| \times 100$$

Output Temperature Coefficient (TCV_O) — The ratio of output change with temperature variation to the specified temperature range expressed in ppm/°C. For example, TCV_O is defined as ΔV_{OT} divided by the temperature range; i.e.,

$$TCV_O(0^\circ\text{C to } +70^\circ\text{C}) = \frac{\Delta V_{OT}(0^\circ\text{C to } +70^\circ\text{C})}{70^\circ\text{C}}$$

$$\text{and } TCV_O(-55^\circ\text{C to } +125^\circ\text{C}) = \frac{\Delta V_{OT}(-55^\circ\text{C to } +125^\circ\text{C})}{180^\circ\text{C}}$$

Output Turn-On Settling Time (t_{ON}) — The time required for the output voltage to reach its final value within a specified error band after application of V_{IN} .

Output Voltage Noise (e_{np-p}) — The peak-to-peak output noise voltage within a specified frequency band.

Quiescent Supply Current (I_{SQ}) — The current required from the supply to operate the device with no load.



VOLTAGE REFERENCES

Precision Monolithics Inc.

VOLTAGE REFERENCE SELECTION GUIDE

Product	V_O	e_{np-p}	Line Regulation	Load Regulation	I_{SY}	TCV_O
REF01	+10V	$30\mu V_{p-p}$	0.01%/V	0.008%/mA	1.4mA	8.5ppm/°C
REF02	+5V	$15\mu V_{p-p}$	0.01%/V	0.010%/mA	1.4mA	8.5ppm/°C
REF03	+2.5V	$7.5\mu V_{p-p}$	0.01%/V	0.008%/mA	1.4mA	65ppm/°C
REF05*	+5V	$15\mu V_{p-p}$	0.01%/V	0.010%/mA	1.4mA	8.5ppm/°C
REF08	-10V	$10\mu V_{p-p}$	10ppm/V	10ppm/mA	2.0mA	10ppm/°C
REF10*	+10V	$30\mu V_{p-p}$	0.01%/V	0.008%/mA	1.4mA	8.5ppm/°C
REF43	+2.5V	$8\mu V_{RMS}$	2-5ppm/V	20ppm/mA	350 μ A	5ppm/°C

*Guaranteed long-term stability

Precision Monolithics Inc.

FEATURES

- 10 Volt Output $\pm 0.3\%$ Max
- Adjustment Range $\pm 3\%$ Min
- Excellent Temperature Stability $8.5\text{ppm}/^\circ\text{C}$ Max
- Low Noise $30\mu\text{V}_{\text{p-p}}$ Max
- Low Supply Current 1.4mA Max
- Wide Input Voltage Range 12V to 40V
- High Load-Driving Capability 20mA
- No External Components
- Short-Circuit Proof
- MIL-STD-883 Screening Available

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ $\Delta V_O \text{ MAX}$ (mV)	PACKAGE				OPERATING TEMPERATURE RANGE
	TO-99	CERDIP	PLASTIC	LCC	
± 30	REF01AJ*	REF01AZ*	—	—	MIL
± 30	REF01EJ	REF01EZ	—	—	COM
± 50	REF01J*	REF01Z*	—	REF01RC/883	MIL
± 50	REF01HJ	REF01HZ	REF01HP	—	COM
± 100	REF01CJ	REF01CZ	REF01CP	—	COM
± 100	—	—	REF01CS††	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

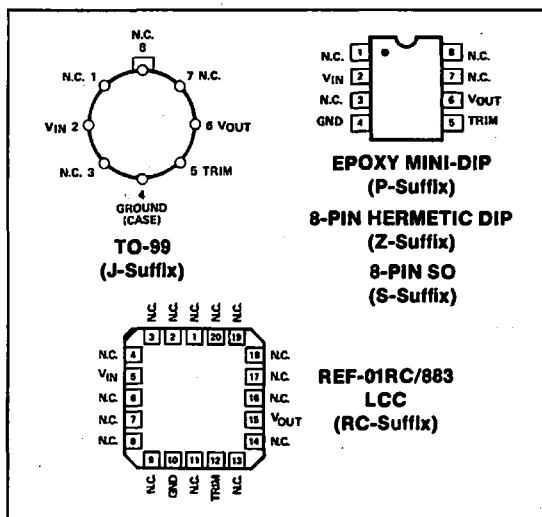
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

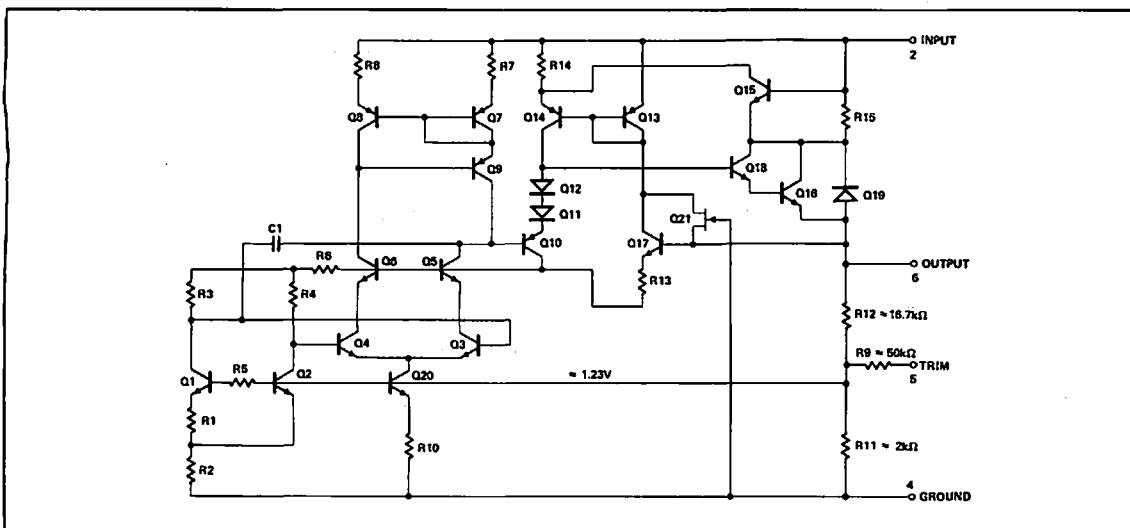
The REF-01 precision voltage reference provides a stable +10V output which can be adjusted over a $\pm 3\%$ range with minimal effect on temperature stability. Single-supply opera-

tion over an input voltage range of 12V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-01 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. Full military temperature range devices with screening to MIL-STD-883 are available. For guaranteed long-term drift see the REF-10 data sheet.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Input Voltage

REF-01, A, E, H, RC, All DICE 40V

REF-01C 30V

Power Dissipation (Note 1) 500mW

Output Short-Circuit Duration
(to Ground or V_{IN}) Indefinite

Storage Temperature Range

J, RC, and Z Packages -65° C to +150° C

P Package -65° C to +125° C

Operating Temperature Range

REF-01A, REF-01, REF-01RC -55° C to +125° C

REF-01E, REF-01H, REF-01C 0° C to +70° C

DICE Junction Temperature (T_J) -65° C to +150° C

Lead Temperature (Soldering, 60 sec.) 300° C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80° C	7.1mW/° C
8-Pin Hermetic DIP (Z)	75° C	6.7mW/° C
8-Pin Plastic DIP (P)	38° C	5.6mW/° C
LCC (RC)	72° C	7.8mW/° C

2. Absolute maximum ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25° C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01A/E			REF-01/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0$	0.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	± 3.0	± 3.3	—	± 3.0	± 3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 8)	—	20	30	—	20	30	μV_{p-p}
Line Regulation (Note 4)		$V_{IN} = 13V$ to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		$I_L = 0$ to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{on}	To $\pm 0.1\%$ of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SQ}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S	(Note 7)	-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55° C \leq T_A \leq +125° C$ and $I_L = 0mA$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01A/E			REF-01/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 1, 2)	ΔV_{OT}	$0° C \leq T_A \leq +70° C$ $-55° C \leq T_A \leq +125° C$	—	0.02	0.06	—	0.07	0.17	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	—	10.0	25.0	ppm/° C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 13V$ to 33V) (Note 4)		$0° C \leq T_A \leq +70° C$ $-55° C \leq T_A \leq +125° C$	—	0.007	0.012	—	0.007	0.012	%/V
Load Regulation ($I_L = 0$ to 8mA) (Note 4)		$0° C \leq T_A \leq +70° C$ $-55° C \leq T_A \leq +125° C$	—	0.006	0.010	—	0.007	0.012	%/mA

NOTES:1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

2. ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O (0° \text{ to } +70° C) = \frac{\Delta V_{OT} (0° \text{ to } +70° C)}{70° C}$$

$$\text{and } TCV_O (-55° \text{ to } +125° C) = \frac{\Delta V_{OT} (-55° \text{ to } +125° C)}{180° C}$$

4. Line and Load Regulation specifications include the effect of self heating.
5. Guaranteed by design.
6. Sample tested.
7. During sink current test the device meets the output voltage specified.

**ELECTRICAL CHARACTERISTICS** at $V_{IN} = +15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C			UNITS
			MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0mA$	9.90	10.00	10.10	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	± 2.7	± 3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 8)	—	25	35	μV_{p-p}
Line Regulation (Note 4)		$V_{IN} = 13V$ to $30V$	—	0.009	0.015	%/V
Load Regulation (Note 4)		$I_L = 0$ to $8mA$	—	0.006	0.015	%/mA
Turn-on Settling Time	t_{ON}	To $\pm 0.1\%$ of final value	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	mA
Load Current	I_L		8	21	—	mA
Sink Current	I_S	(Note 7)	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	mA

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01C			UNITS
			MIN	TYP	MAX	
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	—	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	20	65	ppm/ $^\circ C$
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	ppm/%
Line Regulation (Note 4)		$V_{IN} = 13V$ to $30V$	—	0.011	0.018	%/V
Load Regulation (Note 4)		$I_L = 0$ to $5mA$	—	0.008	0.018	%/mA

NOTES:

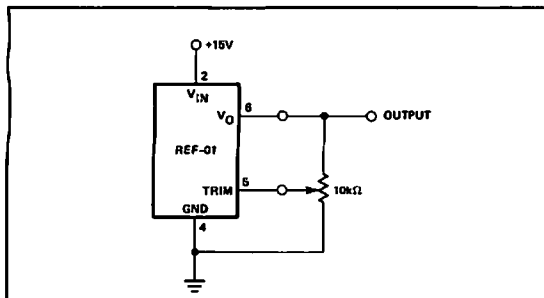
1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

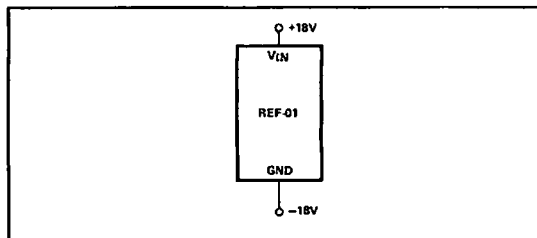
2. ΔV_{OT} specification applies trimmed to $\pm 10.000V$ or untrimmed.
3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70^\circ C}$$

4. Line and Load Regulation specifications include the effect of self heating.
5. Guaranteed by design.
6. Sample tested.
7. During sink current test the device meets the output voltage specified.

OUTPUT ADJUSTMENT

The REF-01 trim terminal can be used to adjust the output voltage over a $10V \pm 300mV$ range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can

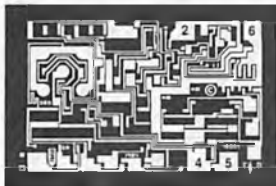
BURN-IN CIRCUIT

also be set to exactly 10.000V, or to 10.240V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7 ppm/ $^\circ C$ for 100mV of output adjustment.



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.074 × 0.048 Inch, 3552 sq. mils
(1.88 × 1.22 mm, 2.29 sq. mm)

2. INPUT VOLTAGE (V_{IN})
4. GROUND
5. TRIM
6. OUTPUT VOLTAGE (V_{OUT})

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{IN} = +15V$, $T_A = 25^\circ C$ for REF-01N and REF-01G devices; $T_A = 125^\circ C$ for REF-01NT and REF-01GT devices, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	REF-01NT LIMIT	REF-01N LIMIT	REF-01GT LIMIT	REF-01G LIMIT	UNITS
Output Voltage	V_O	$I_L = 0$	10.05 9.95	10.03 9.97	10.10 9.90	10.05 9.95	V MAX V MIN
Output Adjustment Range	V_{Trim}	$R_P = 10k\Omega$	—	±3.0	—	±3.0	% MIN
Line Regulation		$V_{IN} = 13V$ to 33V	0.015	0.01	0.015	0.01	%/V MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

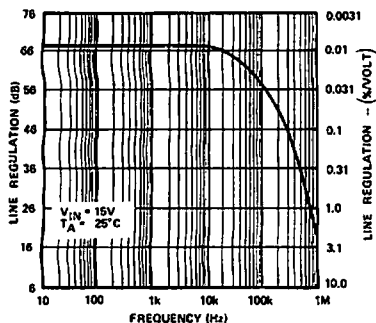
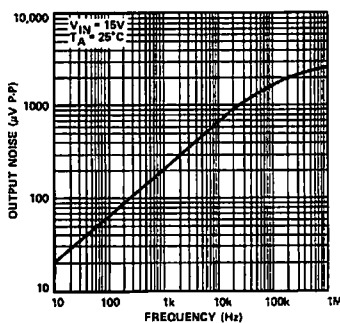
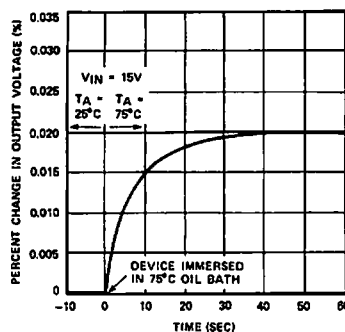
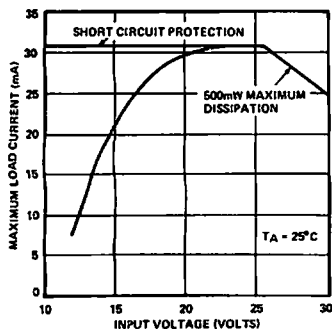
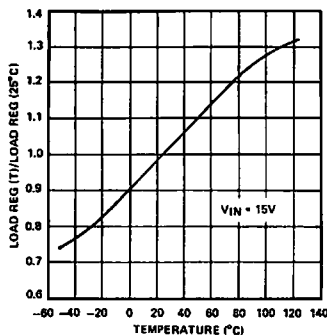
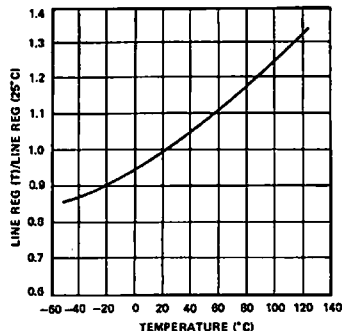
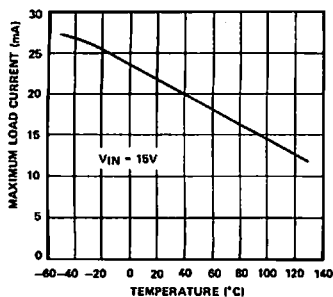
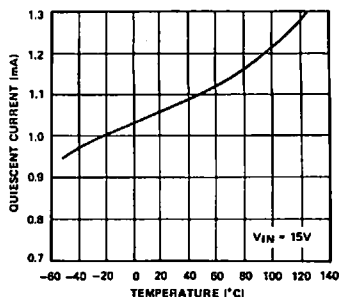
TYPICAL ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-01NT TYPICAL	REF-01N TYPICAL	REF-01GT TYPICAL	REF-01G TYPICAL	UNITS
Load Regulation		$I_L = 0$ to 10mA $I_L = 0$ to 8mA, NT, GT @ +125°C	0.007	0.005	0.009	0.006	%/mA
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	20	20	20	20	μV_{p-p}
Turn-On Settling Time	t_{ON}	To ±0.1% of Final Value NT, GT @ +125°C	7.5	5.0	7.5	5.0	μs
Quiescent Current	I_{SY}	No Load, NT, GT @ +125°C	1.4	1.0	1.4	1.0	mA
Load Current	I_L		21	21	21	21	mA
Sink Current	I_S		-0.5	-0.5	-0.5	-0.5	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	30	30	30	30	mA
Output Voltage Temperature Coefficient	TCV_O		10	10	10	10	ppm/°C

NOTE:

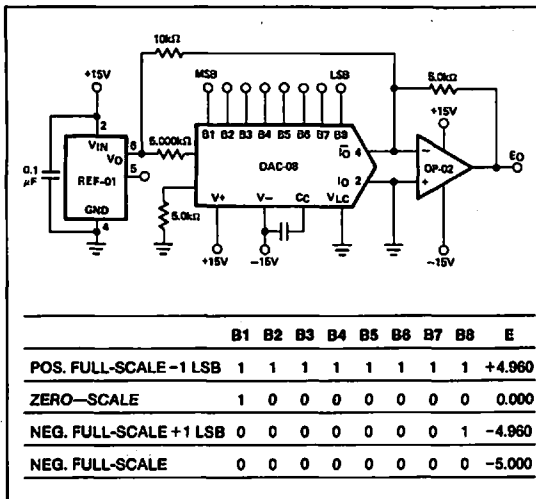
1. For +25°C specifications of REF-01NT and REF-01GT, see REF-01N and REF-01G respectively.

TYPICAL PERFORMANCE CHARACTERISTICS

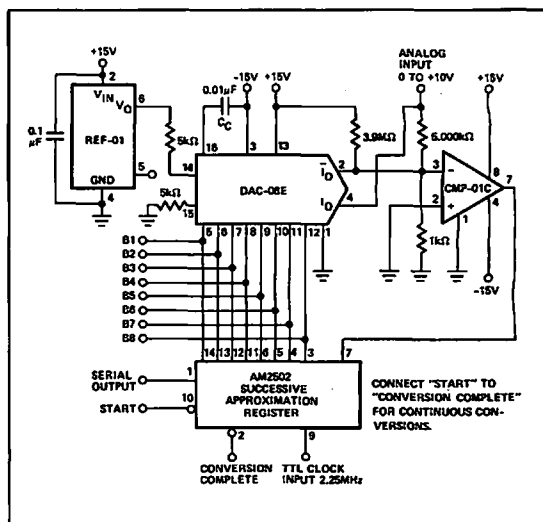
LINE REGULATION
vs FREQUENCY

OUTPUT WIDEBAND
NOISE vs BANDWIDTH (0.1Hz
TO FREQUENCY INDICATED)

OUTPUT CHANGE DUE TO
THERMAL SHOCK

MAXIMUM LOAD CURRENT
vs INPUT VOLTAGE

NORMALIZED LOAD
REGULATION ($\Delta I_L = 10mA$)
vs TEMPERATURE

NORMALIZED
LINE REGULATION
vs TEMPERATURE

MAXIMUM LOAD CURRENT
vs TEMPERATURE

QUIESCENT CURRENT
vs TEMPERATURE


TYPICAL APPLICATIONS

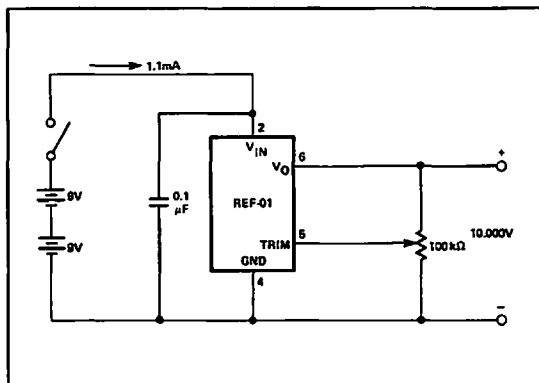
D/A CONVERTER REFERENCE



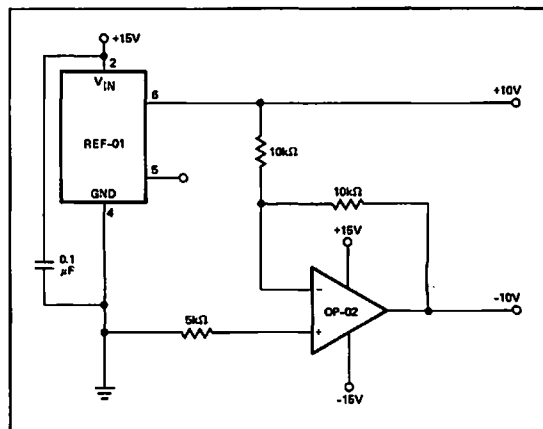
A/D CONVERTER REFERENCE



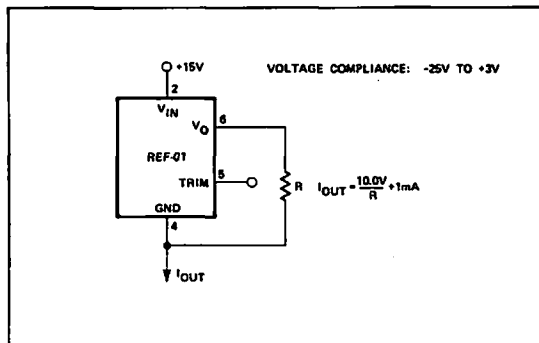
PRECISION CALIBRATION STANDARD



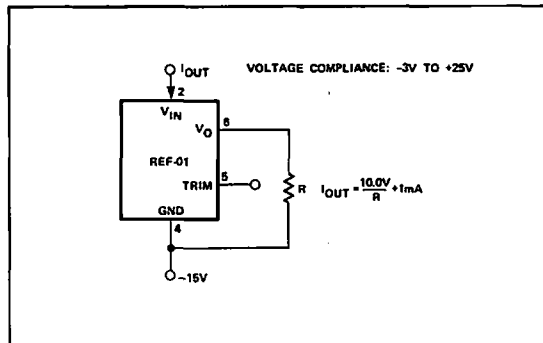
±10V REFERENCE



CURRENT SOURCE



CURRENT SINK





REF-02

+5V PRECISION VOLTAGE
REFERENCE/TEMPERATURE TRANSDUCER

Precision Monolithics Inc.

FEATURES

- 5 Volt Output $\pm 0.3\%$ Max
- Temperature Voltage Output $2.1\text{mV}/^\circ\text{C}$
- Adjustment Range $\pm 3\%$ Min
- Excellent Temperature Stability $8.5\text{ppm}/^\circ\text{C}$ Max
- Low Noise $15\mu\text{V}_{\text{p-p}}$ Max
- Low Supply Current 1.4mA Max
- Wide Input Voltage Range 7V to 40V
- High Load-Driving Capability 20mA
- No External Components
- Short-Circuit Proof
- MIL-STD-883 Screening Available

ORDERING INFORMATION†

$T_A = 25^\circ\text{C}$ ΔV_O MAX (mV)	PACKAGE				OPERATING TEMPERATURE RANGE
	TO-99	CERDIP	PLASTIC	LCC	
± 15	REF02AJ*	REF02AZ*	—	—	MIL
± 15	REF02EJ	REF02EZ	—	—	COM
± 25	REF02J*	REF02Z*	—	REF02RC/883	MIL
± 25	REF02HJ	REF02HZ	REF02HP	—	COM
± 50	REF02CJ	REF02CZ	REF02CP	—	COM
± 50	—	—	REF02CS††	—	COM
± 100	REF02DJ	REF02DZ	REF02DP	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1888 Data Book, Section 2.

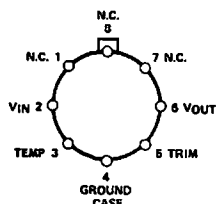
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

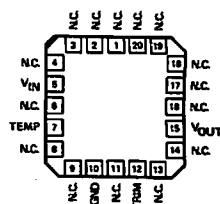
The REF-02 precision voltage reference provides a stable +5V output which can be adjusted over a $\pm 6\%$ range with

minimal effect on temperature stability. Single-supply operation over an input voltage range of 7V to 40V , low current drain of 1mA , and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-02 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-02 is enhanced by its use as a monolithic temperature transducer. For +10V references, see the REF-01 and REF-10 data sheets.

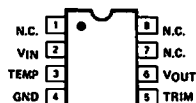
PIN CONNECTIONS



TO-99 (J-Suffix)

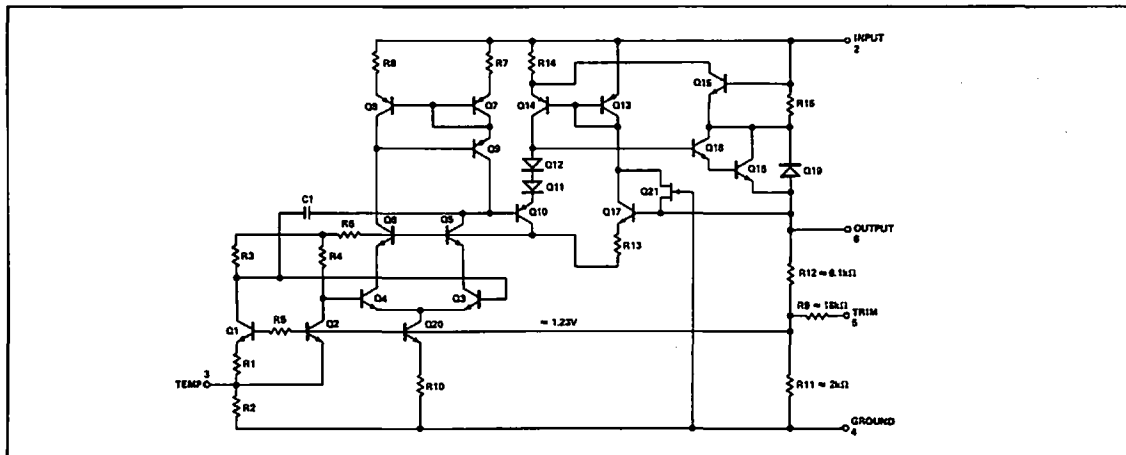


REF-02RC/883
LCC (RC-Suffix)



8-PIN HERMETIC DIP
(Z-Suffix)
EPOXY MINI-DIP
(P-Suffix)
8-PIN SO
(S-Suffix)

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

Input Voltage	
REF-02 A, E, H, RC, All DICE	40V
REF-02 C, D	30V
Power Dissipation (Note 1)	500mW
Output Short-Circuit Duration (to Ground or V_{IN})	Indefinite
Storage Temperature Range	
J, RC, and Z Packages	-65°C to +150°C
P Package	-65°C to +125°C
Operating Temperature Range	
REF-02A, REF-02, REF-02RC	-55°C to +125°C
REF-02E, REF-02H	0°C to +70°C
REF-02C, REF-02D	0°C to +70°C

Lead Temperature (Soldering, 60 sec) 300°C
 DICE Junction Temperature (T_J) -65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Hermetic DIP (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	38°C	5.6mW/°C
LCC (RC)	72°C	7.8mW/°C

2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02A/E			REF-02/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0$	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	$R_p = 10k\Omega$	± 3	± 6	—	± 3	± 6	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 7)	—	10	15	—	10	15	μV_{p-p}
Line Regulation (Note 2)		$V_{IN} = 8V$ to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 2)		$I_L = 0$ to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To $\pm 0.1\%$ of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S	(Note 8)	-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for REF-02A and REF-02, $0^\circ C \leq T_A \leq +70^\circ C$ for REF-02E and REF-02H, $I_L = 0mA$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02A/E			REF-02/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 4, 5)	ΔV_{OT}	$0^\circ C \leq T_A \leq +70^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	0.02	0.06	—	0.07	0.17	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_p = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 8$ to 33V) (Note 2)		$0^\circ C \leq T_A \leq +70^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	0.007	0.012	—	0.007	0.012	%/V
Load Regulation ($I_L = 0$ to 8mA) (Note 2)		$0^\circ C \leq T_A \leq +70^\circ C$ $-55^\circ C \leq T_A \leq +125^\circ C$	—	0.006	0.010	—	0.007	0.012	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/°C

NOTES:

- Guaranteed by design.
- Line and Load Regulation specifications include the effect of self heating.
- Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
- ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

- ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
- TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70^\circ C}$$

- Sample Tested.
- During sink current test the driver meets the output voltage specified.

**ELECTRICAL CHARACTERISTICS** at $V_{IN} = +15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02C			REF-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0mA$	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	$R_P = 10k\Omega$	± 2.7	± 6.0	—	± 2.0	± 6.0	—	%
Output Voltage Noise	e_{n-p-p}	0.1Hz to 10Hz (Note 7)	—	12	18	—	12	—	μV_{p-p}
Line Regulation (Note 2)		$V_{IN} = 8V$ to $30V$	—	0.009	0.015	—	0.010	0.04	%/V
Load Regulation (Note 2)		$I_L = 0$ to $8mA$	—	0.008	0.015	—	—	—	%mA
		$I_L = 0$ to $4mA$	—	—	—	—	0.015	0.04	
Turn-on Settling Time	t_{ON}	To $\pm 0.1\%$ of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	—	1.0	2.0	mA
Load Current	I_L		8	21	—	8	21	—	mA
Sink Current	I_S	(Note 8)	-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $0^\circ C \leq T_A \leq +70^\circ C$ and $I_L = 0mA$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02C			REF-02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 4 and 5)	—	0.14	0.45	—	0.49	1.7	%
Output Voltage Temperature Coefficient	TCV_O	(Note 8)	—	20	65	—	70	250	ppm/ $^\circ C$
Change in V_O Temperature Coefficient With Output Adjustment		$R_P = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 2)		$V_{IN} = 8V$ to $30V$	—	0.011	0.018	—	0.012	0.05	%/V
Load Regulation (Note 2)		$I_L = 0$ to $5mA$	—	0.008	0.018	—	0.016	0.05	%mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/ $^\circ C$

NOTES:

1. Guaranteed by design.
2. Line and Load Regulation specifications include the effect of self heating.
3. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
4. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

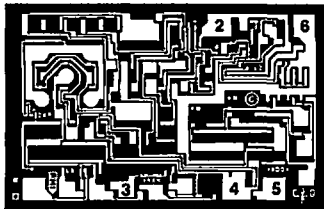
5. ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
6. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O = \frac{\Delta V_{OT}}{70^\circ C}$$

7. Sample Tested.
8. During sink current test the device meets the output voltage specified.



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.074 × 0.048 inch, 3552 sq. mils
(1.88 × 1.22 mm, 2.29 sq. mm)

2. INPUT VOLTAGE (V_{IN})
3. TEMPERATURE TRANSDUCER
OUTPUT VOLTAGE (TEMP)
4. GROUND
5. TRIM
6. OUTPUT VOLTAGE (V_{OUT})

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{IN} = +15V$, $T_A = 25^\circ C$ for REF-02N and REF-02G devices; $T_A = 125^\circ C$ for REF-02NT and REF-02GT devices, unless otherwise noted. (Note 3)

PARAMETER	SYMBOL	CONDITIONS	REF-02NT LIMIT	REF-02N LIMIT	REF-02GT LIMIT	REF-02G LIMIT	UNITS
Output Voltage	V_O	$I_L = 0$	4.975	4.985	4.950	4.975	V MIN
			5.025	5.015	5.050	5.025	V MAX
Output Adjustment Range	V_{trim}	$R_P = 10k\Omega$	—	±3	—	±3	% MIN
Line Regulation		$V_{IN} = 8V$ to 33V	0.015	0.01	0.015	0.01	%/V MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-02NT TYPICAL	REF-02N TYPICAL	REF-02GT TYPICAL	REF-02G TYPICAL	UNITS
Temp. Voltage Output	V_T	(Notes 1, 2)	630	630	630	630	mV
Temp. Voltage Output Temp. Coefficient	TCV_T	(Notes 1, 2)	2.1	2.1	2.1	2.1	mV/°C
Output Voltage Temp. Coefficient	TCV_O		10	10	10	10	ppm/°C
Load Regulation		$I_L = 0$ to 10mA	0.007	0.005	0.009	0.006	%mA
		$I_L = 0$ to 8mA, NT, GT @ +125°C					
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	10	10	10	10	μV_{p-p}
Turn-On Settling Time	t_{ON}	To ±0.1% of final value, NT, GT @ +125°C	7.5	5.0	7.5	5.0	μs
Quiescent Supply Current	I_{SY}	No Load, NT, GT @ +125°C	1.4	1.0	1.4	1.0	mA
Load Current	I_L		21	21	21	21	mA
Sink Current	I_S		-0.5	-0.5	-0.5	-0.5	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	30	30	30	30	mA

NOTES:

1. See AN-18 for detailed REF-02 thermometer applications information.
2. Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
3. For +25°C specifications of REF-02NT and REF-02GT, see REF-02N and REF-02G respectively.

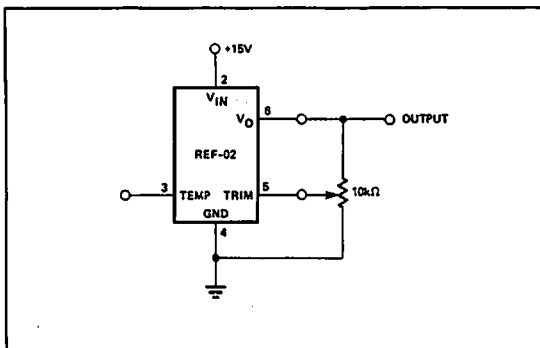


OUTPUT ADJUSTMENT

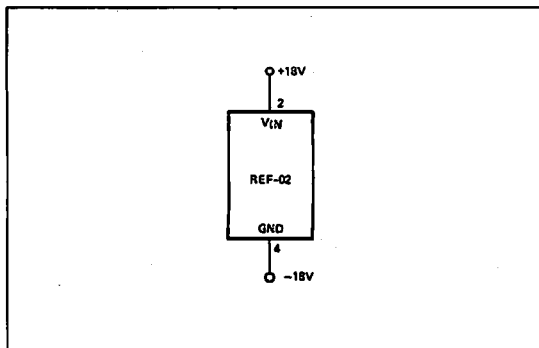
The REF-02 trim terminal can be used to adjust the output voltage over a $5V \pm 300mV$ range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5.000V or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically, the temperature coefficient change is $0.7ppm/^{\circ}C$ for 100mV of output adjustment.

OUTPUT ADJUSTMENT CIRCUIT

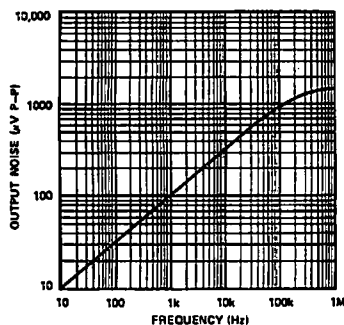


BURN-IN CIRCUIT

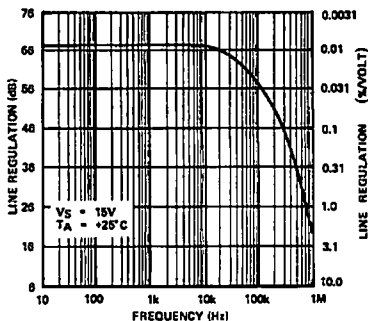


TYPICAL PERFORMANCE CHARACTERISTICS

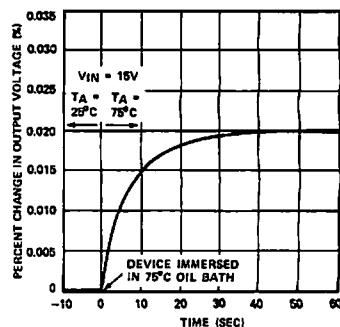
**OUTPUT WIDEBAND NOISE
vs BANDWIDTH (0.1Hz
TO FREQUENCY INDICATED)**



**LINE REGULATION
vs FREQUENCY**

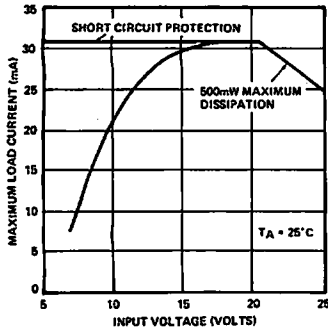


**OUTPUT CHANGE DUE TO
THERMAL SHOCK**

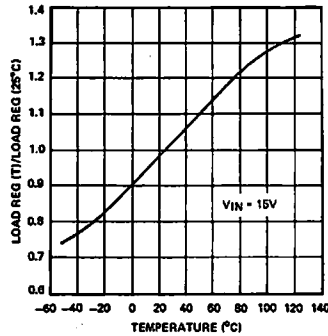


TYPICAL PERFORMANCE CHARACTERISTICS

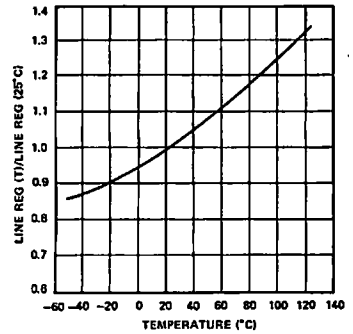
**MAXIMUM LOAD CURRENT
vs INPUT VOLTAGE**



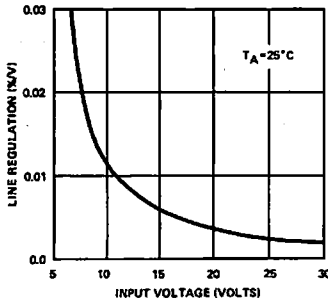
**NORMALIZED LOAD
REGULATION ($\Delta I_L = 10\text{mA}$)
vs TEMPERATURE**



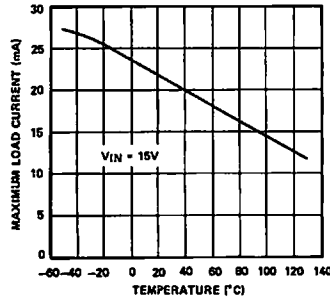
**NORMALIZED
LINE REGULATION
vs TEMPERATURE**



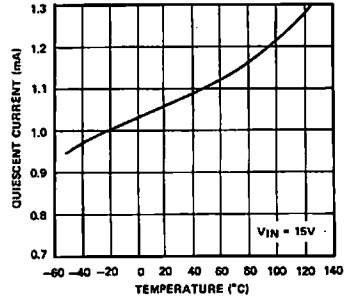
**LINE REGULATION
vs SUPPLY VOLTAGE**



**MAXIMUM LOAD CURRENT
vs TEMPERATURE**



**QUIESCENT CURRENT
vs TEMPERATURE**

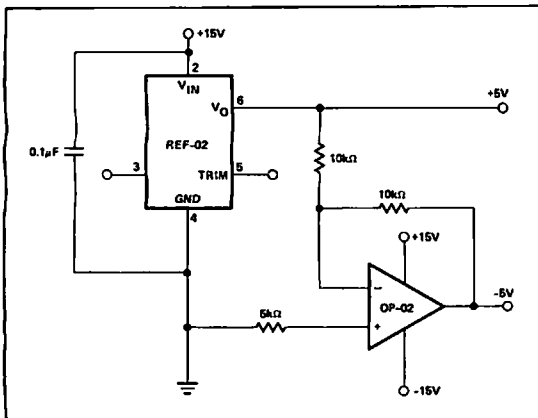


VOLTAGE REFERENCES

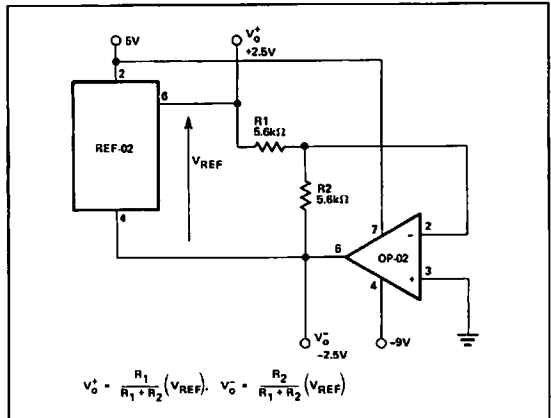
10

TYPICAL APPLICATIONS

±5V REFERENCE

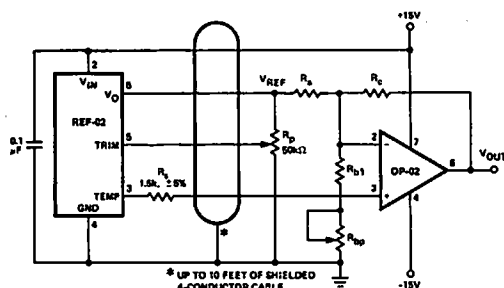


±2.5V REFERENCE





PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR

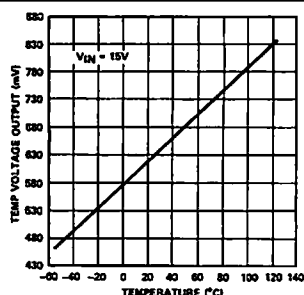


RESISTOR VALUES

TCV _{OUT} SLOPE (S)	10mV/°C	100mV/°C	10mV/°F
TEMPERATURE RANGE	-55°C to +125°C	-55°C to +125°C	-67°F to +257°F
OUTPUT VOLTAGE RANGE	-0.55V to +1.25V	-5.5V to +12.5V*	-0.87V to +2.57V
ZERO-SCALE	0V @ 0°C	0V @ 0°C	0V @ 0°F
R _B (± 1% resistor)	9.09kΩ	15kΩ	7.5kΩ
R _{b1} (± 1% resistor)	1.5kΩ	1.82kΩ	1.21kΩ
R _{b2} (Potentiometer)	200Ω	500Ω	200Ω
R _L (± 1% resistor)	5.11kΩ	84.5kΩ	8.25kΩ

*For 125°C operation, the op amp output must be able to swing to +12.5V. Increase V_{IN} to +18V from +15V if this is a problem.

TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF-02A)

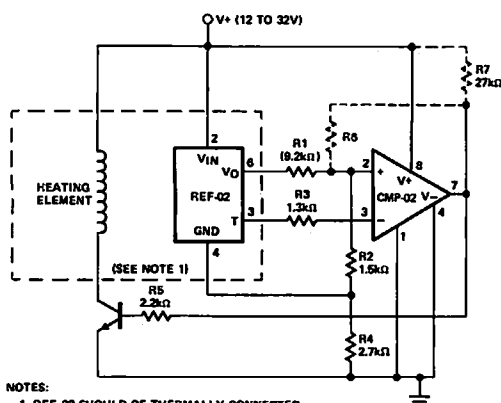


REFERENCE STACK WITH EXCELLENT LINE REGULATION

Two REF-01's and one REF-02 can be stacked to yield 5.000V, 15.000V and 25.000V outputs. An additional advantage of this circuit is near-perfect line regulation of the 5.0V and 15.0V outputs. A 27V to 55V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 15.000V regulator.

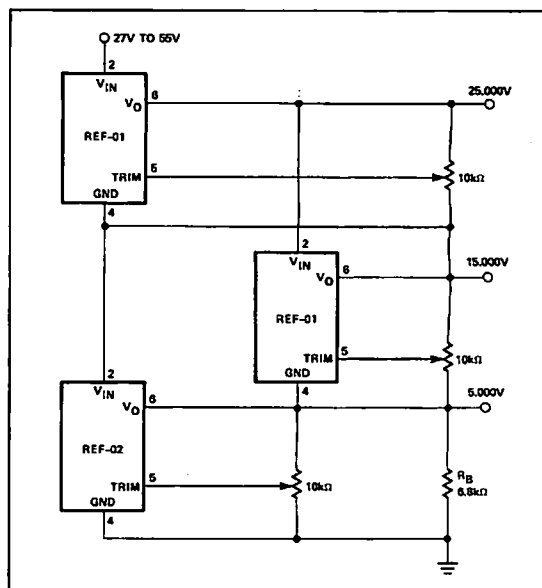
In general, any number of REF-01's and REF-02's can be stacked this way. For example, ten devices will yield ten outputs in 5V or 10V steps. The line voltage can range from 100V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).

TEMPERATURE CONTROLLER



NOTES:

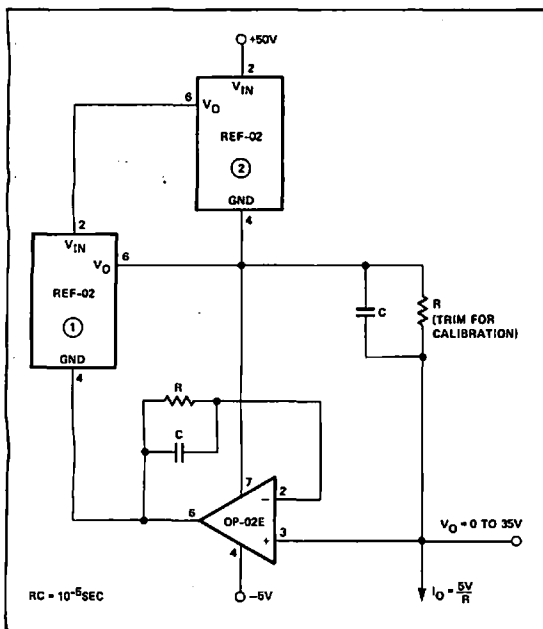
1. REF-02 SHOULD BE THERMALLY CONNECTED TO SUBSTANCE BEING HEATED.
2. NUMBERS IN PARENTHESES ARE FOR A SETPOINT TEMPERATURE OF 60°C.
3. R₅ = R1/R2/R3



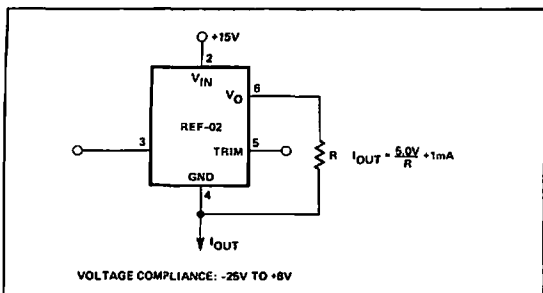
PRECISION CURRENT SOURCE

A current source with 35V output compliance and excellent output impedance can be obtained using this circuit. REF-02 (2) keeps the line voltage and power dissipation constant in device (1); the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical $3\mu\text{V/V}$ PSRR of the OP-02E will create a 20ppm change ($3\mu\text{V/V} \times 35\text{V}/5\text{V}$) in output current over a 35V range. For example, a 5mA current source can be built ($R = 1\text{k}\Omega$) with 350M Ω output impedance.

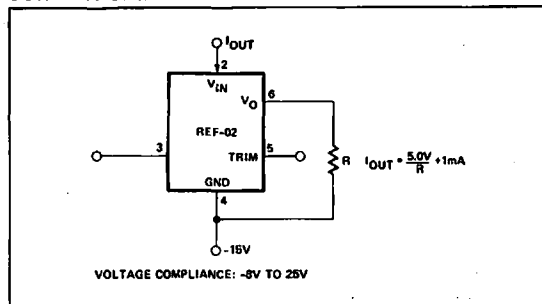
$$R_O = \frac{35\text{V}}{20 \times 10^{-6} \times 5\text{mA}}$$



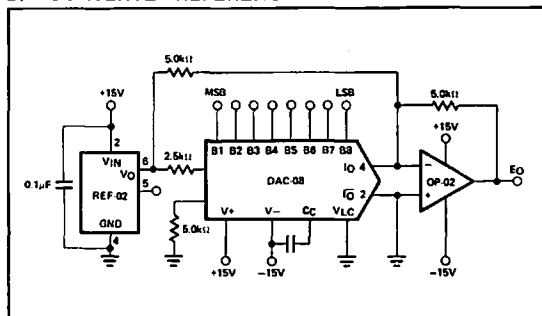
CURRENT SOURCE



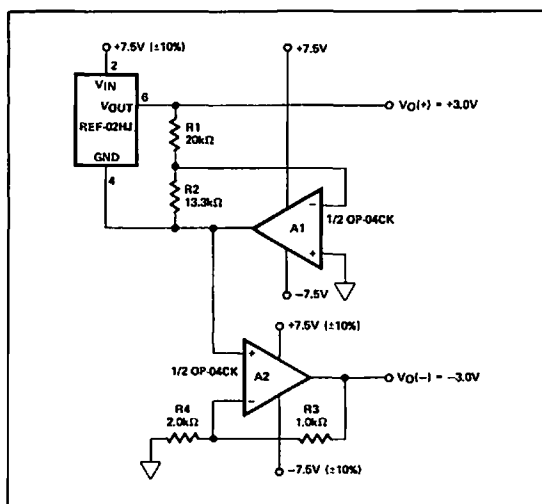
CURRENT SINK



D/A CONVERTER REFERENCE



±3V REFERENCE



SUPPLY BYPASSING

For best results, it is recommended that the power supply pin is bypassed with a 0.1 μF disc ceramic capacitor.



REF-03

+2.5V LOW-COST PRECISION
VOLTAGE REFERENCE

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- +2.5 Volt Output $\pm 0.5\%$ Max
- Wide Input Voltage Range 4.5V to 33V
- Supply Current 1.4mA Max
- Low Cost

ORDERING INFORMATION†

PLASTIC PACKAGE	OPERATING TEMPERATURE RANGE
REF03GP	COM
REF03GS††	COM

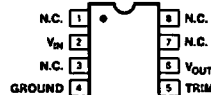
† Burn-in is available on commercial and industrial temperature range parts in cardip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

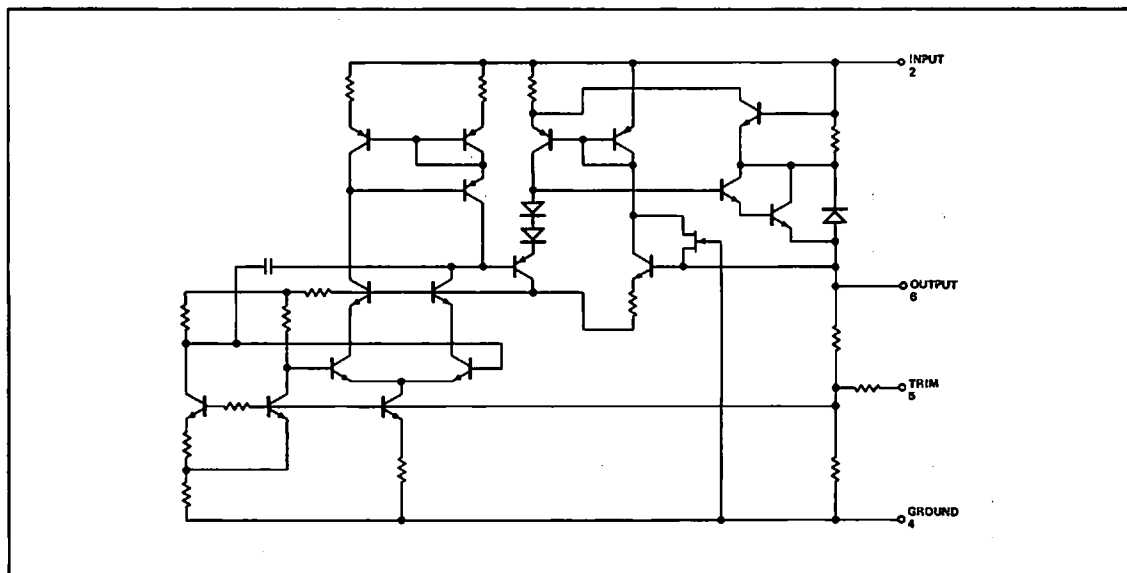
The REF-03 precision voltage reference provides a stable +2.5V output, with minimal change for variations in supply voltage, ambient temperature or loading conditions. Single-supply operation over an input voltage range of +4.5V to +33V with a current drain of 1mA and good temperature stability is achieved using an improved bandgap design. Primarily targeted at price-sensitive applications, the REF-03 is available in plastic mini-dips and surface-mountable small outline plastic packages. For improved performance, see REF-43.

PIN CONNECTIONS



8-PIN PLASTIC DIP
(P-Suffix)
8-PIN SO
(S-Suffix)

SIMPLIFIED SCHEMATIC



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Supply Voltage	40V
Internal Power Dissipation (Note 2)	500mW
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
REF-03G (P, S)	0°C to +70°C
Storage Temperature Range	-65°C to +175°C
Junction Temperature Range	-65°C to +175°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. See table for maximum ambient temperature and rating.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

ELECTRICAL CHARACTERISTICS at $V_{IN} = +5V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	REF-03G	MAX	UNITS
				TYP		
Output Voltage	V_O	No Load	2.485	2.500	2.515	V
Output Adjustment Range	ΔV_{TRIM}	$R_{POT} \approx 10k\Omega$	± 3.0	± 3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz	—	5	7.5	μV_{p-p}
Line Regulation		$V_{IN} = +4.5V$ to $+33V$	—	0.006	0.010	%/V
Load Regulation		$I_L = 0mA$ to $10mA$	—	0.006	0.010	%/mA
Turn-On Settling Time	t_{ON}	To $\pm 0.1\%$ of Final Value	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	mA
Load Current (Sourcing)	I_L		10	21	—	mA
Load Current (Sinking)	I_S		-0.3	-0.5	—	mA
Short-Circuit Output Current	I_{SC}	Output Shorted to Ground	—	30	—	mA
Output Voltage Tempco	TCV_O	$0^\circ C \leq T_A \leq 70^\circ C$	—	20	65	ppm/°C



REF-05

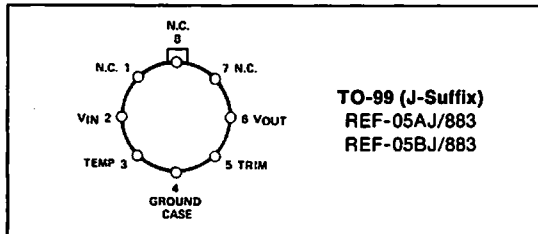
+5V PRECISION VOLTAGE REFERENCE
(GUARANTEED LONG-TERM STABILITY)

Precision Monolithics Inc.

FEATURES

- 5 Volt Output
- Guaranteed Long-Term Stability
 - 100ppm/1000 Hrs Max
- Excellent Temperature Stability 8.5ppm/°C Max
- Low Noise $15\mu V_{p-p}$ Max
- Low Supply Current 1.4mA Max
- Wide Input Voltage Range 7V to 40V
- High Load-Driving Capability 20mA
- Short-Circuit Proof
- Processed Per MIL-STD-883

PIN CONNECTIONS & ORDERING INFORMATION

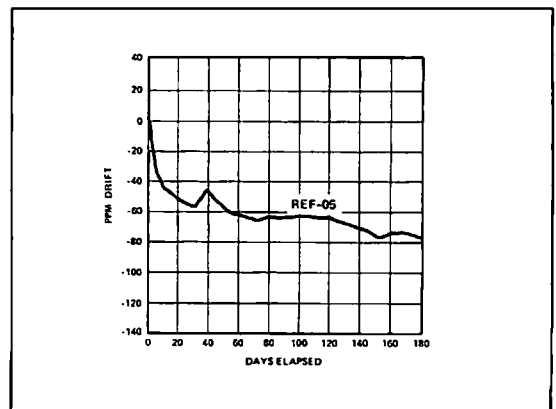


GENERAL DESCRIPTION

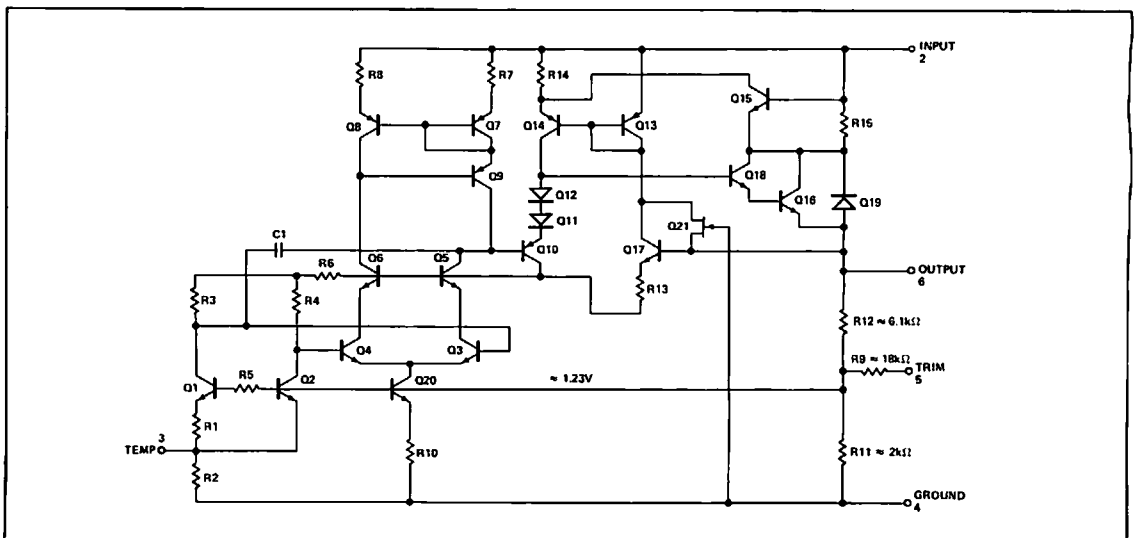
The REF-05 precision voltage reference provides a stable +5V output which can be adjusted over a $\pm 6\%$ range with minimal effect on temperature stability. Long-term drift is guaranteed

at 100ppm/1000 hrs. maximum. Single-supply operation over an input voltage range of 7V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-05 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. The versatility of the REF-05 is enhanced by its use as a monolithic temperature transducer. For +10V Precision Voltage References see the REF-10 data sheet.

LONG-TERM DRIFT PLOT (Average of 20 Devices)



SIMPLIFIED SCHEMATIC





ABSOLUTE MAXIMUM RATINGS

Input Voltage
 REF-05A, B 40V
 Power Dissipation (see note) 500mW
 Output Short-Circuit Duration
 (to Ground or V_{IN}) Indefinite

Storage Temperature Range -65°C to $+150^{\circ}\text{C}$
 Lead Temperature (Soldering, 60 sec) 300°C
 Operating Temperature Range
 REF-05A, REF-05B -55°C to $+125^{\circ}\text{C}$

NOTE: Derate at $7.1\text{mW}/^{\circ}\text{C}$ above 80°C ambient temperature for TO-99 (J) package.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-05A			REF-05B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0$	4.985	5.0	5.015	4.975	5.0	5.025	V
Output Adjustment Range	ΔV_{trim}	$R_P = 10\text{k}\Omega$	± 3	± 6	—	± 3	± 6	—	%
Output Voltage Noise	e_{n-p}	0.1Hz to 10Hz (Note 1)	—	10	15	—	10	15	μV_{p-p}
Long-Term Stability		(Note 1)	—	65	100	—	65	100	ppm/1kHrs
Line Regulation (Note 2)		$V_{IN} = 8\text{V}$ to 33V	—	0.008	0.010	—	0.008	0.010	%/V
Load Regulation (Note 2)		$I_L = 0$ to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-On Settling Time	t_{on}	To $\pm 0.1\%$ of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1	1.4	—	1	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S	(Note 7)	-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	15	30	60	15	30	60	mA
Temperature Voltage Output	V_T	(Note 3)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15\text{V}$, $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ and $I_L = 0\text{mA}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-05A			REF-05B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 4 & 5)	ΔV_{OT}	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	0.06	0.15	—	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 6)	—	3	8.5	—	10	25	ppm/ $^{\circ}\text{C}$
Change in V_O Temperature Coefficient with Output Adjustment		$R_P = 10\text{k}\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 8\text{V}$ to 33V) (Note 2)		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	0.009	0.015	—	0.009	0.015	%/V
Load Regulation ($I_L = 0$ to 8mA) (Note 2)		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	—	0.007	0.012	—	0.009	0.015	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 3)	—	2.1	—	—	2.1	—	mV/ $^{\circ}\text{C}$
Quiescent Supply Current	I_{SY}	No Load	—	1.6	2.0	—	1.6	2.0	mA

NOTES:

- Sample tested. Long-term stability is tested with power applied continuously.
- Line and Load Regulation specifications include the effect of self heating.
- Limit current in or out of pin 3 to 50mA and capacitance on pin 3 to 30pF.
- ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V.

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

- ΔV_{OT} specification applied trimmed to +5V or untrimmed.
- TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$\text{TCV}_O = \frac{\Delta V_{OT}}{180^{\circ}\text{C}}$$

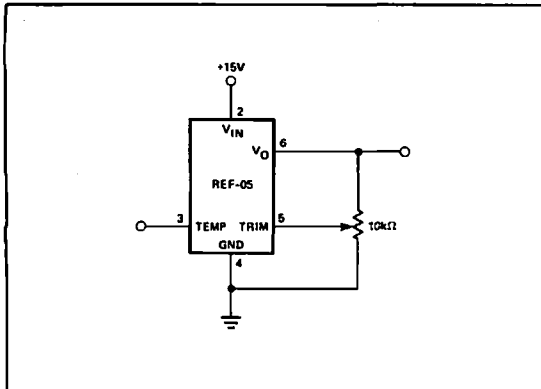
- During sink current test the device meets the output voltage specified.

OUTPUT ADJUSTMENT

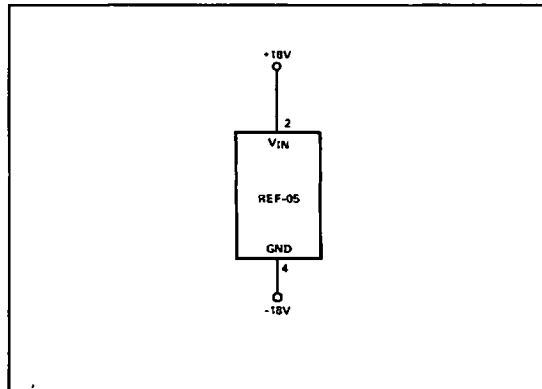
The REF-05 trim terminal can be used to adjust the output voltage over a $5V \pm 300mV$ range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V. Of course, the output can also be set to exactly 5V or to 5.12V for binary applications.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically the temperature coefficient change is $0.7ppm/^{\circ}C$ for 100mV of output adjustment.

OUTPUT ADJUSTMENT CIRCUIT

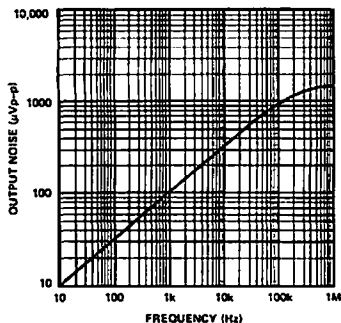


BURN-IN CIRCUIT

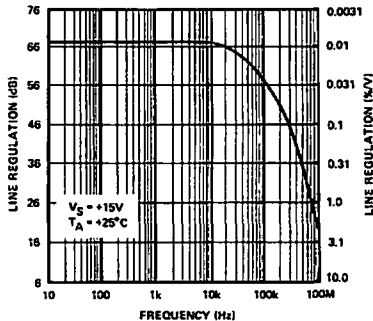


TYPICAL PERFORMANCE CHARACTERISTICS

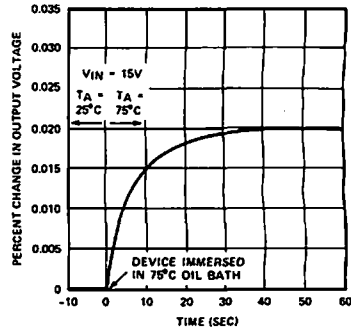
**OUTPUT WIDEBAND NOISE
vs BANDWIDTH (0.1Hz
TO FREQUENCY INDICATED)**



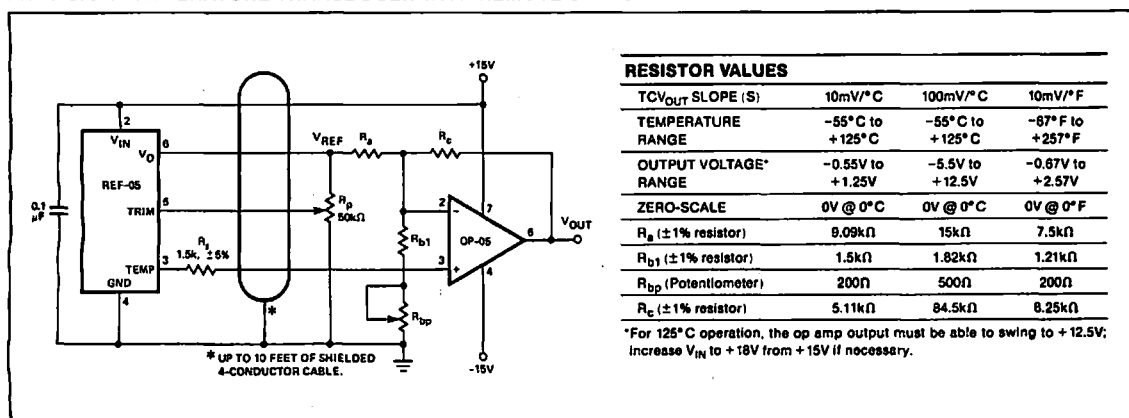
**LINE REGULATION
vs FREQUENCY**



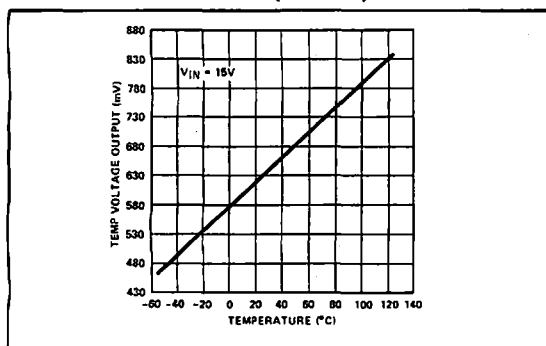
**OUTPUT CHANGE DUE TO
THERMAL SHOCK**



PRECISION TEMPERATURE TRANSDUCER WITH REMOTE SENSOR



TYPICAL TEMPERATURE VOLTAGE OUTPUT vs TEMPERATURE (REF-05A)

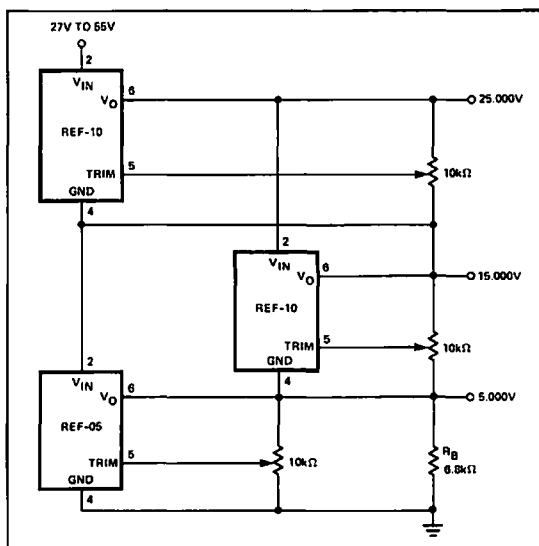
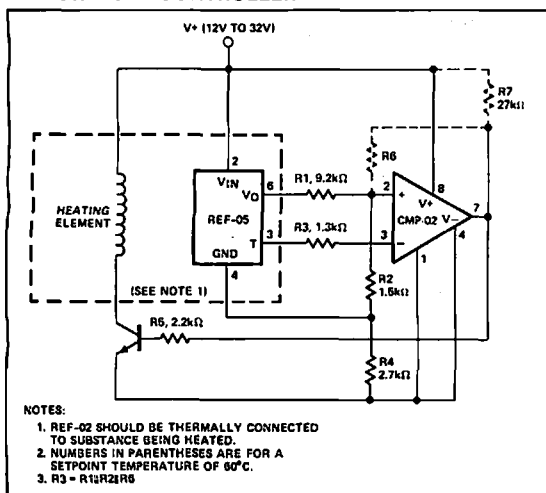


REFERENCE STACK WITH EXCELLENT LINE REGULATION

Two REF-10's and one REF-05 can be stacked to yield 5V, 15V and 25V outputs. An additional advantage is near-perfect line regulation of the 5V and 15V outputs. A 27V to 55V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R₀) provides a path for the supply current (I_{SV}) of the 15V regulator.

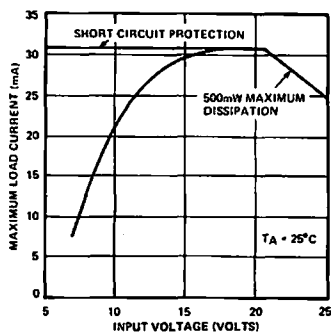
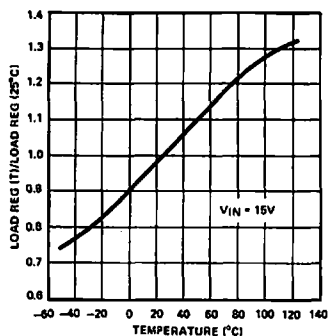
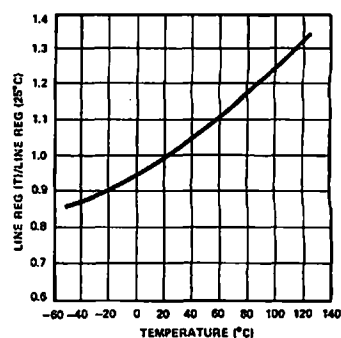
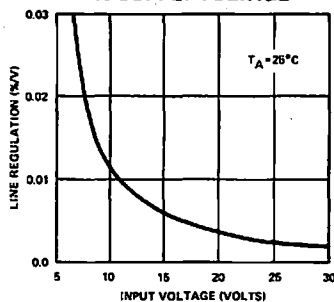
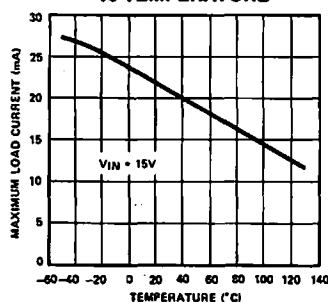
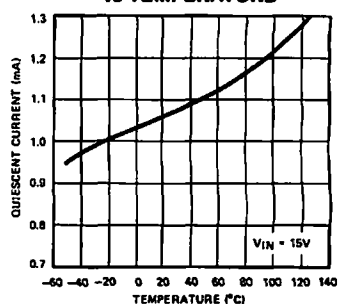
In general, any number of REF-10's and REF-05's can be stacked this way. For example, ten devices will yield ten outputs in 5V or 10V steps. The line voltage can range from 100V to 130V, however, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).

TEMPERATURE CONTROLLER

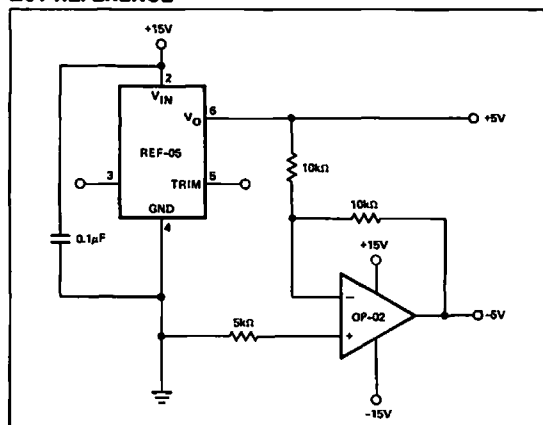
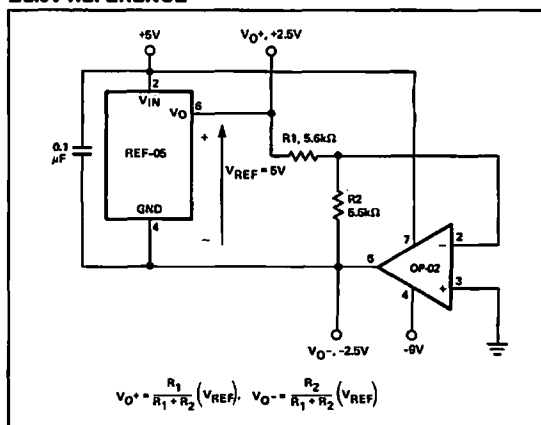




TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM LOAD CURRENT
vs INPUT VOLTAGENORMALIZED LOAD
REGULATION ($\Delta I_L = 10\text{mA}$)
vs TEMPERATURENORMALIZED
LINE REGULATION
vs TEMPERATURELINE REGULATION
vs SUPPLY VOLTAGEMAXIMUM LOAD CURRENT
vs TEMPERATUREQUIESCENT CURRENT
vs TEMPERATURE

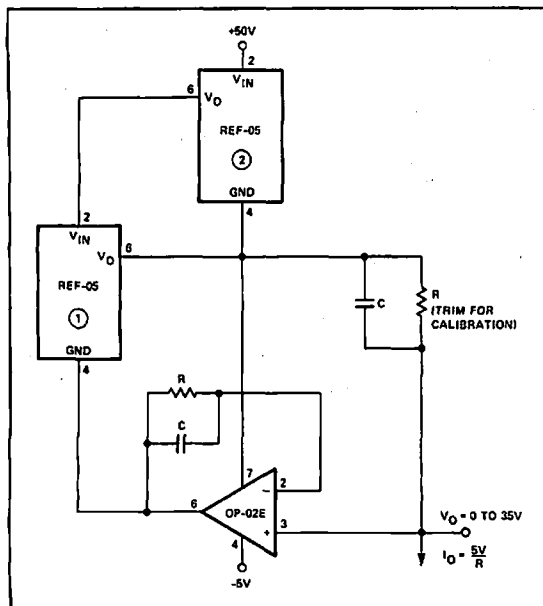
TYPICAL APPLICATIONS

 $\pm 5\text{V}$ REFERENCE $\pm 2.5\text{V}$ REFERENCE

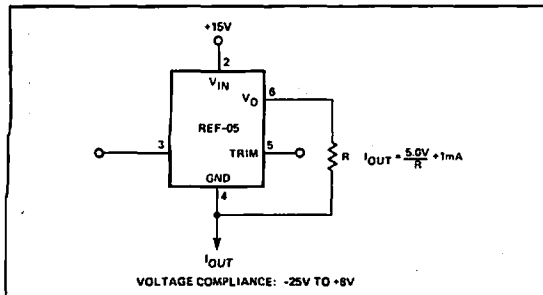
PRECISION CURRENT SOURCE

A current source with 35V output compliance and excellent output impedance can be obtained using this circuit. REF-05 ② keeps the line voltage and power dissipation constant in device ①; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical $3\mu\text{V/V}$ PSRR of the OP-02E will create a 20ppm change ($3\mu\text{V/V} \times 35\text{V}/5\text{V}$) in output current over a 35V range. For example, a 5mA current source can be built ($R = 1\text{k}\Omega$) with $350\text{M}\Omega$ output impedance.

$$R_0 = \frac{35\text{V}}{20 \times 10^{-6} \times 5\text{mA}}$$



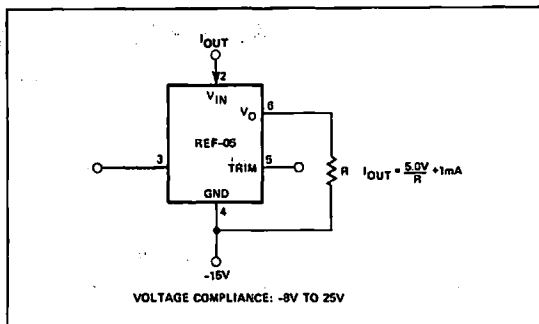
CURRENT SOURCE



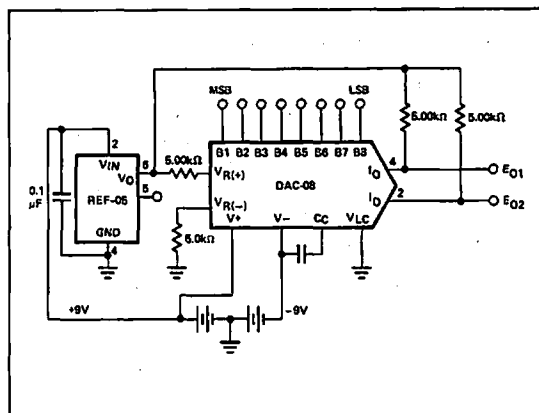
SUPPLY BYPASSING

For best results, it is recommended that the power supply pin is bypassed with a $0.1\mu\text{F}$ disc ceramic capacitor.

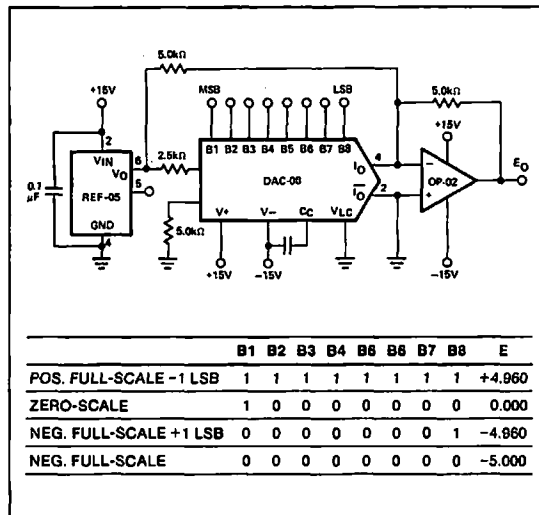
CURRENT SINK



BATTERY-OPERATED D/A CONVERTER REFERENCE



D/A CONVERTER REFERENCE



	B1	B2	B3	B4	B5	B6	B7	B8	E
POS. FULL-SCALE -1 LSB	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG. FULL-SCALE +1 LSB	0	0	0	0	0	0	0	1	-4.960
NEG. FULL-SCALE	0	0	0	0	0	0	0	0	-5.000



REF-08

NEGATIVE 10V/10.24V
VOLTAGE REFERENCE

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Pin Selectable -10V or -10.24V Output
- No Trim Required for Most 8-Bit and 10-Bit Applications
- Suitable for 12-Bit Systems
- Low Initial Tempco 10ppm/°C Max
- Low Adjustment Tempco 0.04ppm/°C/mV of Adjustment Typ
- Wide Input Voltage Range -11.4V to -36V
- Initial Accuracy ±20mV Max
- 10mA Min Output Current
- Wide 3% Output Adjustment Range

GENERAL DESCRIPTION

The REF-08 is a series regulation, negative voltage reference with pin selectable output voltage. Its low temperature coefficient, low noise, and selectable output make it an ideal reference for A/D converters such as the ADC-908 or the PM-7574. At 8 bits of resolution, the REF-08 is accurate, untrimmed, to within ±1/2 LSB Max. At 10 bits, the error is only 2 LSB Max. The REF-08 is also well suited for CMOS DAC applications where a positive output voltage is desired.

Applications with 8-bit and 10-bit accuracy will typically be able to use the REF-08 without trimming its output voltage. This is particularly true of CMOS DACs with low gain errors such as the DAC-8408 and PM-7528.

Higher accuracy, 12-bit applications may require trimming, but here the very low temperature coefficients of the REF-08 will

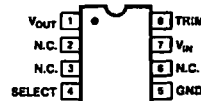
allow excellent accuracy to be maintained over a broad range of temperatures.

Leaving the SELECT pin open will result in a -10V output. Grounding SELECT will produce a -10.24V output (i.e. -10mV per 10-bit LSB) that is ideal for binary applications.

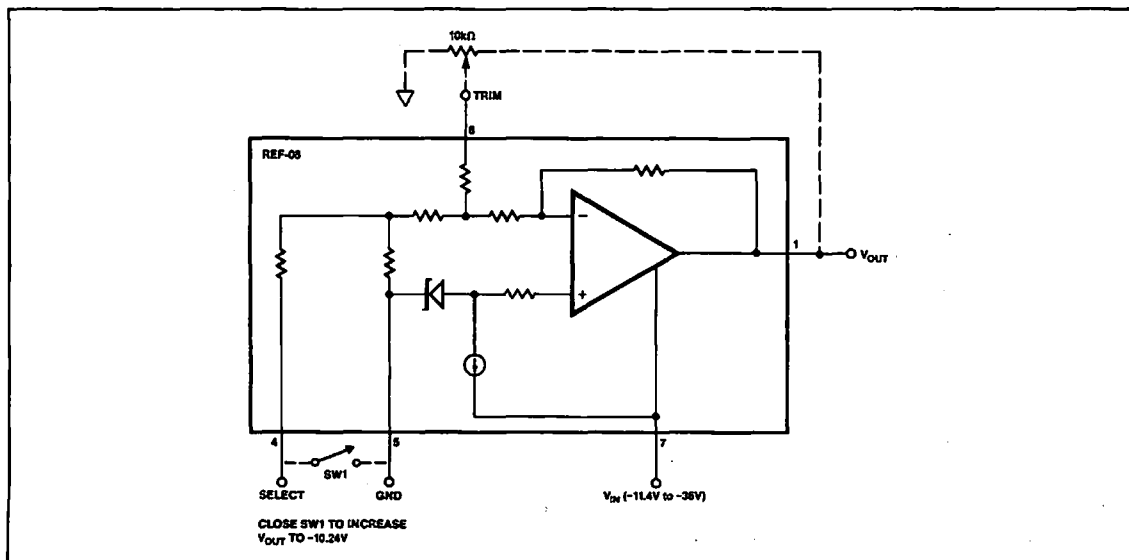
A 3% adjustment range is available with the REF-08 which exhibits a tight 0.04ppm/°C/mV of adjustment temperature coefficient. In many applications, the combined tempcos of an adjusted REF-08 will be superior to more expensive precision references with tighter initial tempcos but greater changes with adjustment.

The REF-08 has been designed to operate from a "worst case" -12V power supply (-11.4V). This low dropout voltage makes the best of the poor supply regulation in some digital systems. Its 10mA output current capability and unloaded supply current of only 2mA provide better power/performance than most traditional op amp inverter circuits.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ABSOLUTE MAXIMUM RATINGS**

Input Voltage +0.3V to -36V
 Output Voltage +0.3V to $V_{IN} - 0.3V$
 Power Dissipation 500mW
 Output Short-Circuit Duration
 (to Ground or V_{IN}) 30 seconds
 Operating Temperature Ranges -55°C to +125°C,
 -40°C to +85°C,
 0°C to +70°C

Storage Temperature Range

Z Package -65°C to +150°C
 S, P Packages -65°C to +125°C
 Lead Temperature (Soldering, 60 sec) 300°C

ELECTRICAL CHARACTERISTICS at $V_{IN} = -15V$, $R_L = 2k\Omega$ to ground, $T_A = +25^\circ C$, SELECT and TRIM inputs unconnected, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-08A/G	UNITS
Output Voltage	V_O	No Load, SELECT Floating	-10.020 -9.980	V MIN V MAX
Output Voltage	V_O	No Load, SELECT = GND	-10.270 -10.210	V MIN V MAX
Line Regulation		$V_{IN} = -11.4V$ to $-16.5V$ $T_{MIN} \leq T_A \leq T_{MAX}$	± 10	ppm/V MAX
Load Regulation		Load Current = 0mA to 10mA $T_{MIN} \leq T_A \leq T_{MAX}$	± 10	ppm/mA MAX
Output Voltage Temperature Coefficient	TCV_O	Average Over Temperature	± 10	ppm/°C MAX
Output Noise	$e_{N RMS}$	10Hz to 1kHz (sampled)	20	μV_{RMS} MAX
Output Current (Sink)	I_{OUT}	$V_{IN} = -11.4$ to $-16.5V$ $T_{MIN} \leq T_A \leq T_{MAX}$	-20	mA MIN
Output Current (Source)	I_{OUT}	$V_{IN} = -11.4$ to $-16.5V$ $T_{MIN} \leq T_A \leq T_{MAX}$	0.2	mA MIN
Quiescent Supply Current	I_{SY}	No Load	2.0	mA MAX
Output Adjustment Voltage Range	V_{TRIM}	$R_{TRIM} = 10k\Omega$	± 3	% TYP
TCV_O Change with Adjustment		$R_{TRIM} = 10k\Omega$	± 0.04	ppm/°C/mV of Adjustment TYP

TYPICAL APPLICATIONS

FIGURE 1: -10V Reference for 8-Bit CMOS Analog-to-Digital Converter

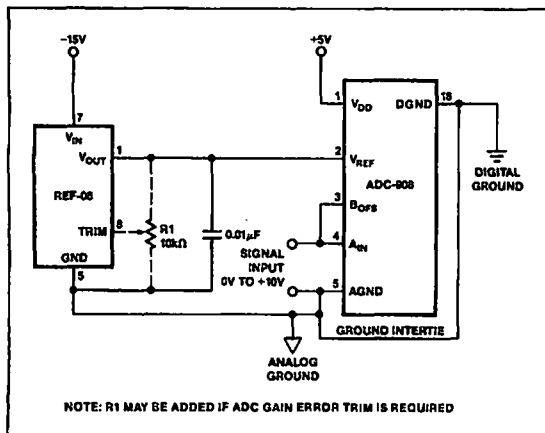


FIGURE 2: ±10V Reference

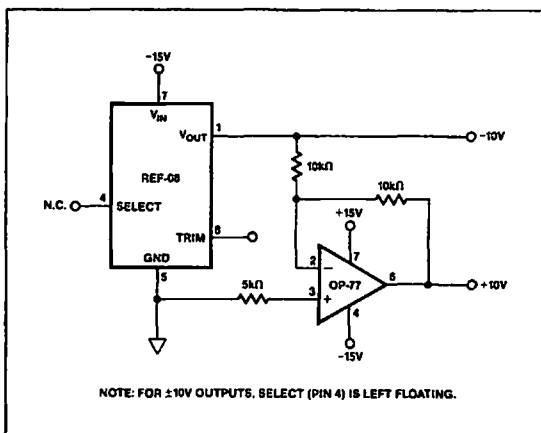


FIGURE 3: 8-Bit Resolution, Dual Output "No-Trim" DAC with 0V to +10V and 0V to -10V Outputs

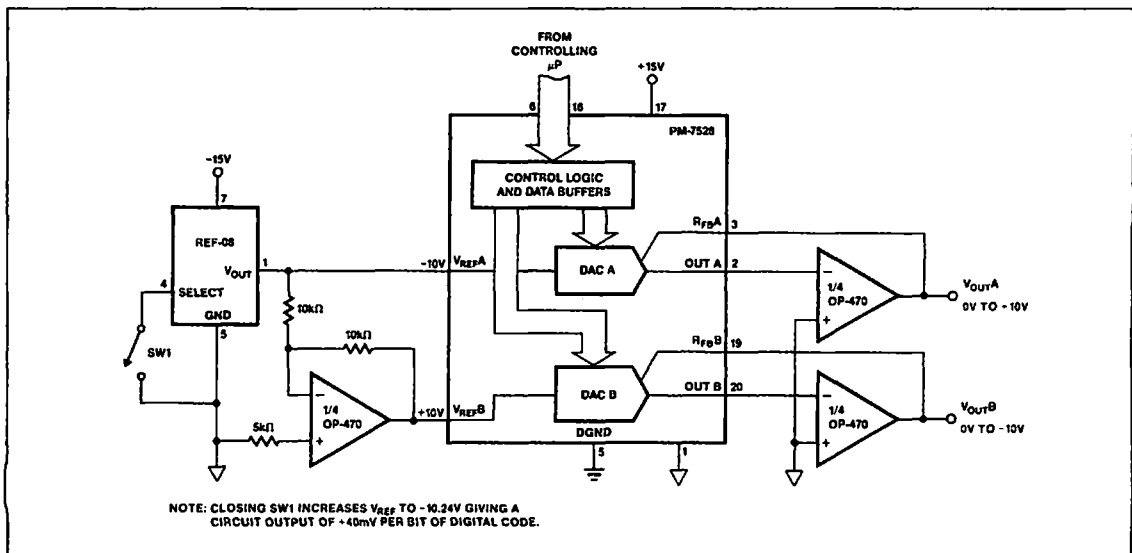
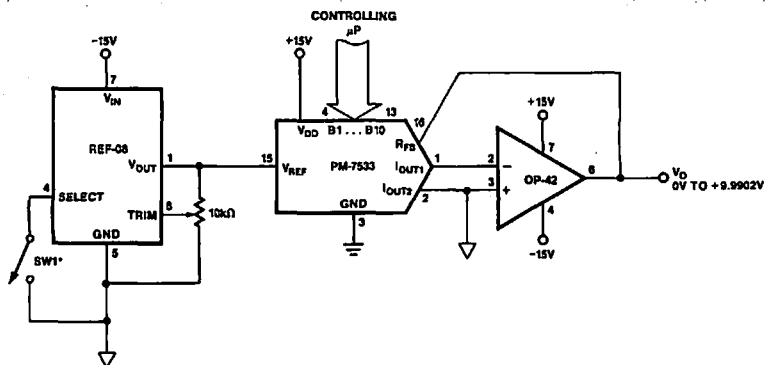
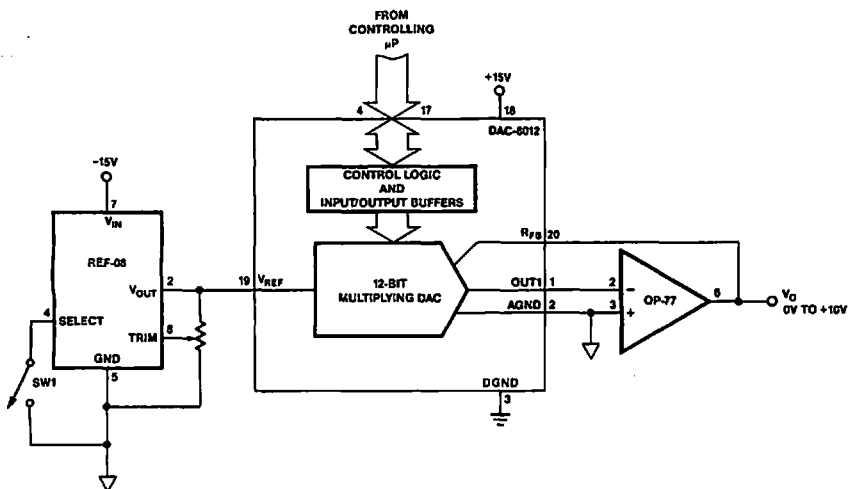


FIGURE 4: 10-Bit CMOS DAC with 0V to +10V Output



NOTE: IF SW1 IS CLOSED, $V_{REF} = 10.24V$ AND $V_O = +10mV$ PER BIT OF DIGITAL CODE.

FIGURE 5: 12-Bit CMOS DAC with 0V to 10V Output





REF-10

+10V PRECISION VOLTAGE REFERENCE
(GUARANTEED LONG-TERM STABILITY)

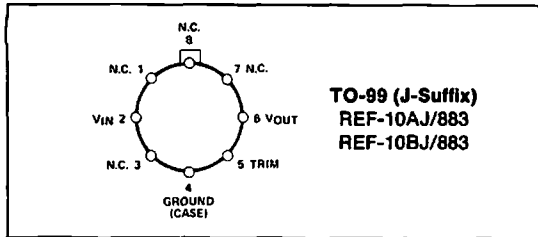
Precision Monolithics Inc.

FEATURES

- 10 Volt Output
- Guaranteed Long-Term Stability 50ppm/1000 Hrs Max
- Excellent Temperature Stability 8.5ppm/°C Max
- Low Noise $30\mu V_{p-p}$ Max
- Low Supply Current 1.4mA Max
- Wide Input Voltage Range 12V to 40V
- High Load-Driving Capability 20mA
- Short-Circuit Proof
- Processed Per MIL-STD-883

guaranteed at 50ppm/1000 hrs. maximum. Single-supply operation over an input voltage range of 12V to 40V, low current drain of 1mA, and excellent temperature stability are achieved with an improved bandgap design. Low cost, low noise, and low power make the REF-10 an excellent choice whenever a stable voltage reference is required. Applications include D/A and A/D converters, portable instrumentation, and digital voltmeters. For +5V precision voltage references, see the REF-05 data sheet.

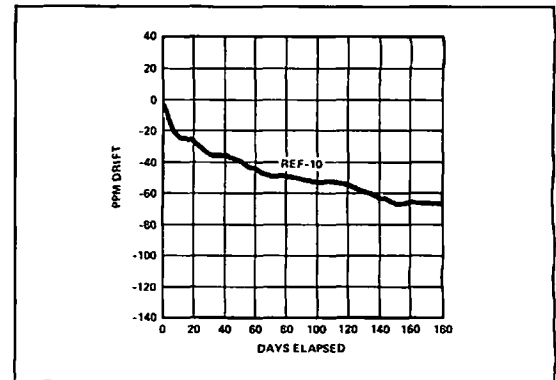
PIN CONNECTIONS & ORDERING INFORMATION



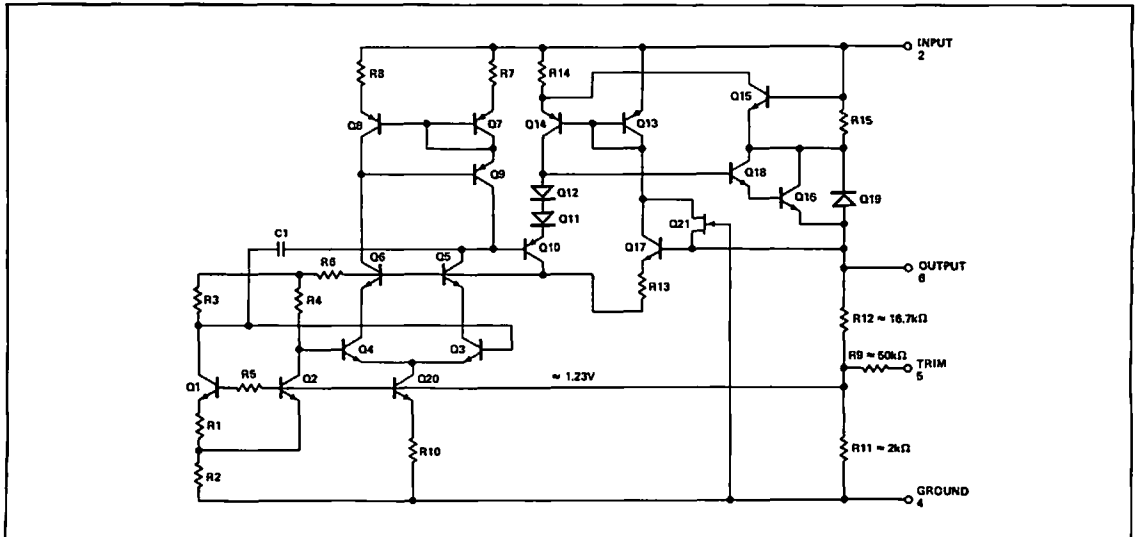
GENERAL DESCRIPTION

The REF-10 precision voltage reference provides a stable +10V output that can be adjusted over a $\pm 3\%$ range with minimal effect on temperature stability. Long-term drift is

LONG-TERM DRIFT PLOT (Average of 20 Devices)



SIMPLIFIED SCHEMATIC





ABSOLUTE MAXIMUM RATINGS

Input Voltage	
REF-10A, B	40V
Power Dissipation (see note)	500mW
Output Short-Circuit Duration (to Ground or V_{IN})	Indefinite

Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	
REF-10A, REF-10B	-55°C to +125°C

NOTE: Derate at 7.1mW/°C above 80°C ambient temperature for TO-99 (J) package.

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $T_A = 25^\circ C$, unless otherwise noted:

PARAMETER	SYMBOL	CONDITIONS	REF-10A			REF-10B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	$I_L = 0$	9.97	10	10.03	9.95	10	10.05	V
Output Adjustment Range	ΔV_{trim}	$R_P = 10k\Omega$	+3	± 3.3	—	± 3	± 3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	20	30	—	20	30	μV_{p-p}
Long-Term Stability		(Note 5)	—	—	50	—	—	50	ppm/1000 Hrs
Line Regulation (Note 4)		$V_{IN} = 13V$ to $33V$	—	0.008	0.010	—	0.008	0.010	%/V
Load Regulation (Note 4)		$I_L = 0$ to $10mA$	—	0.005	0.08	—	0.008	0.010	%/mA
Turn-On Settling Time	t_{on}	To $\pm 0.1\%$ of final value	—	5	—	—	5	—	$\mu sec.$
Quiescent Supply Current	I_{SV}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S	(Note 6)	-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	$V_O = 0$	15	30	60	15	30	60	mA

ELECTRICAL CHARACTERISTICS at $V_{IN} = +15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ and $I_L = 0$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-10A			REF-10B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 1 & 2)	ΔV_{OT}	$-55^\circ C \leq T_A \leq +125^\circ C$	—	0.06	0.15	—	0.18	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		$R_P = 10k\Omega$	—	0.7	—	—	0.7	—	ppm/%
Line Regulation ($V_{IN} = 13V$ to $33V$) (Note 4)		$-55^\circ C \leq T_A \leq +125^\circ C$	—	0.009	0.015	—	0.009	0.015	%/V
Load Regulation ($I_L = 0$ to $8mA$) (Note 4)		$-55^\circ C \leq T_A \leq +125^\circ C$	—	0.007	0.012	—	0.009	0.015	%/mA
Quiescent Supply Current	I_{SV}	No Load	—	1.6	2.0	—	1.6	2.0	mA

NOTES:

1. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V.

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

2. ΔV_{OT} specification applied trimmed to +10.000V or untrimmed.

3. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.,

$$TCV_O (-55^\circ C \text{ to } +125^\circ C) = \frac{\Delta V_{OT} (-55^\circ C \text{ to } +125^\circ C)}{180^\circ C}$$

4. Line and Load Regulation specifications include the effect of self heating.
5. Sample tested. Long-term stability is tested with power applied continuously.
6. During sink current test the device meets the output voltage specified.

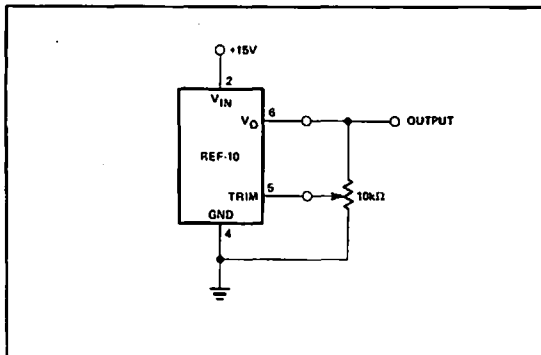


OUTPUT ADJUSTMENT

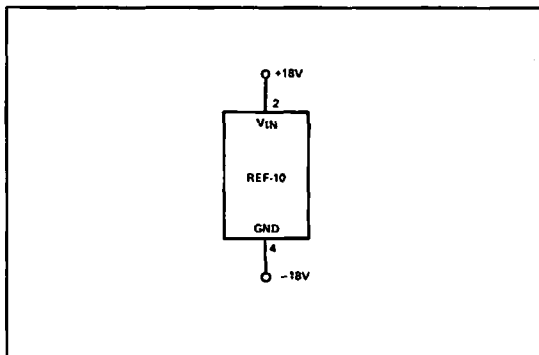
The REF-10 trim terminal can be used to adjust the output voltage over a $10V \pm 300mV$ range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V. Of course, the output can also be set to exactly 10.000V.

Adjustment of the output does not significantly affect the temperature performance of the device. Typically, the temperature coefficient change is 0.7ppm/°C per 100mV of output adjustment.

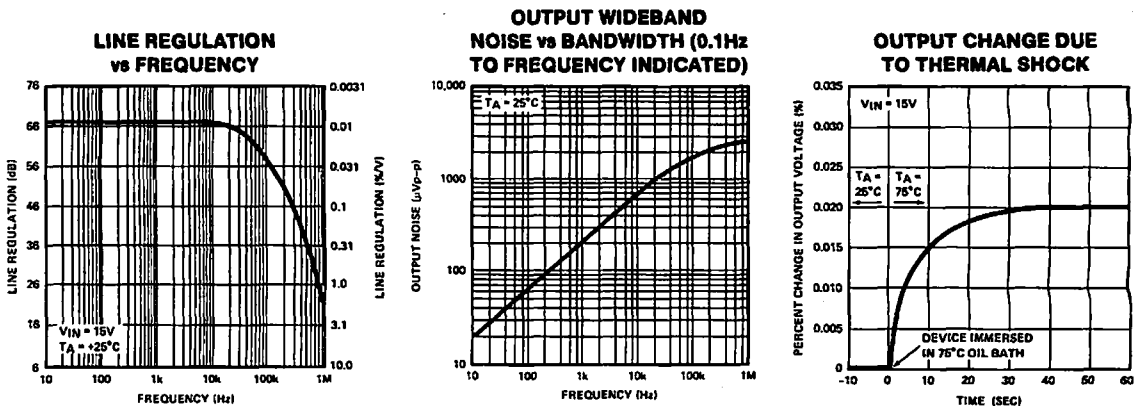
OUTPUT ADJUSTMENT CIRCUIT



BURN-IN CIRCUIT

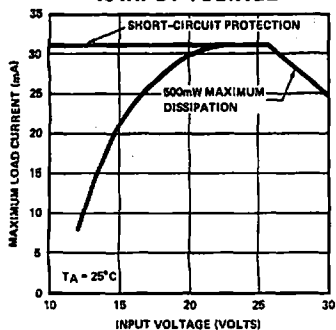


TYPICAL PERFORMANCE CHARACTERISTICS

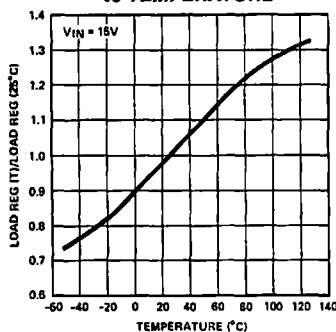


TYPICAL PERFORMANCE CHARACTERISTICS

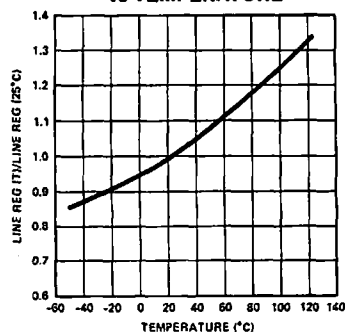
**MAXIMUM LOAD CURRENT
vs INPUT VOLTAGE**



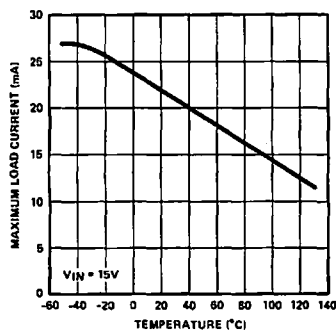
**NORMALIZED LOAD
REGULATION ($\Delta I_L = 10\text{mA}$)
vs TEMPERATURE**



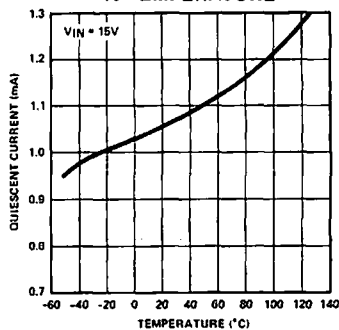
**NORMALIZED
LINE REGULATION
vs TEMPERATURE**



**MAXIMUM LOAD CURRENT
vs TEMPERATURE**

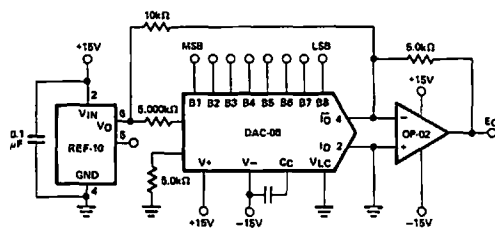


**QUIESCENT CURRENT
vs TEMPERATURE**

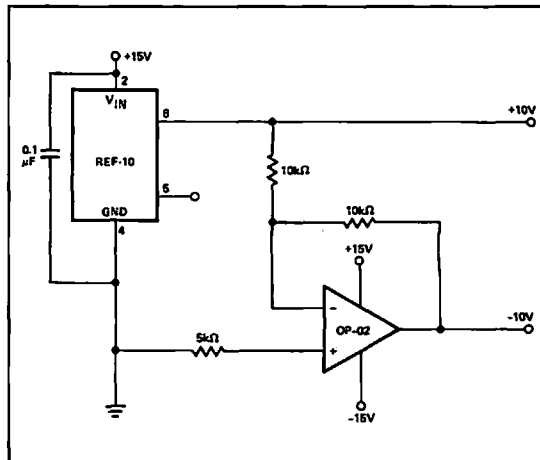


TYPICAL APPLICATIONS

D/A CONVERTER REFERENCE



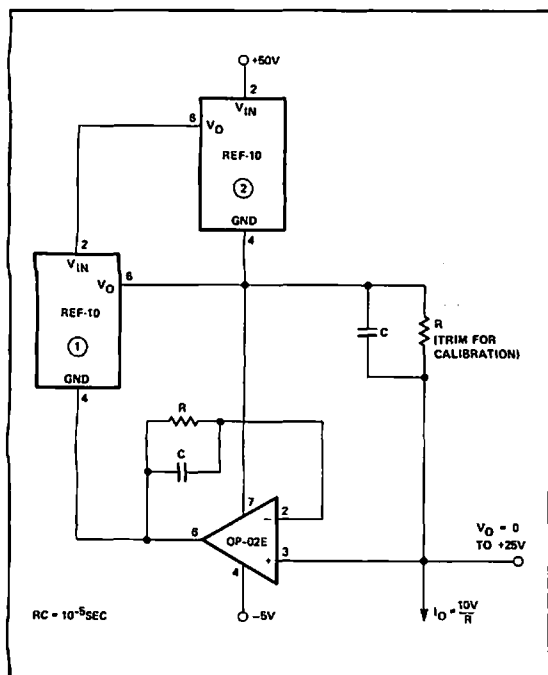
	B1	B2	B3	B4	B5	B6	B7	B8	E
POS FULL-SCALE -1LSB	1	1	1	1	1	1	1	1	+4.960
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEG FULL-SCALE +1LSB	0	0	0	0	0	0	0	1	-4.960
NEG FULL-SCALE	0	0	0	0	0	0	0	0	-5.000



PRECISION CURRENT SOURCE

A current source with 25V output compliance and excellent output impedance can be obtained using this circuit. REF-10② keeps the line voltage and power dissipation constant in device①; the only important error consideration at room temperature is the negative supply rejection of the op amp. The typical $3\mu\text{V/V}$ PSRR of the OP-02E will create an 8ppm change ($3\mu\text{V/V} \times 25\text{V}/10\text{V}$) in output current over a 25V range. For example, a 10mA current source can be built ($R = 1\text{k}\Omega$) with 300 M Ω output impedance.

$$R_O = \frac{25\text{V}}{8 \times 10^{-6} \times 10\text{mA}}$$



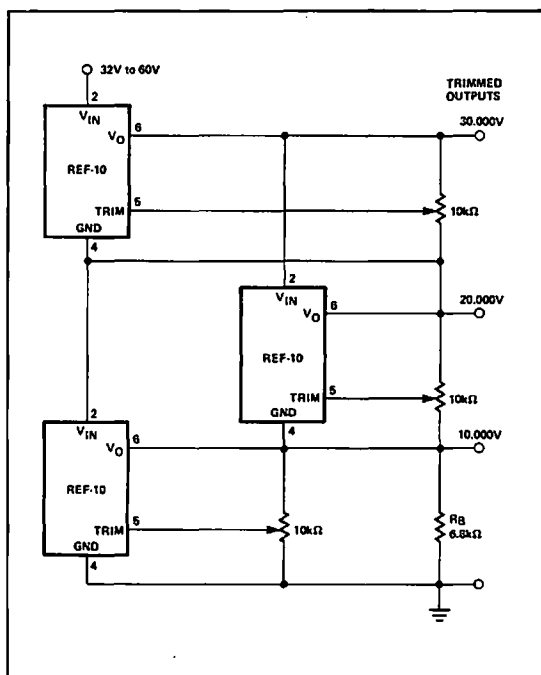
SUPPLY BYPASSING

For best results, it is recommended that the power supply pin is bypassed with a 0.1 μF disc ceramic capacitor.

REFERENCE STACK WITH EXCELLENT LINE REGULATION

Three REF-10's can be stacked to yield 10,000, 20,000 and 30,000V outputs. An additional advantage is near-perfect line regulation of the 10,000 and 20,000V output. A 32V to 60V input change produces an output change which is less than the noise voltage of the devices. A load bypass resistor (R_B) provides a path for the supply current (I_{SY}) of the 20,000V regulator.

In general, any number of REF-10's can be stacked this way. For example, ten devices will yield outputs of 10, 20, 30 ... 100V. The line voltage can range from 105V to 130V. However, care must be taken to ensure that the total load currents do not exceed the maximum usable current (typically 21mA).





REF-43

+2.5V LOW-POWER PRECISION
VOLTAGE REFERENCE

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- +2.5 Volt Output $\pm 0.05\%$ Max
- Low Temperature Coefficient 10ppm/ $^{\circ}\text{C}$ Max
- Excellent Regulation
 - Load Regulation 20ppm/mA Max
 - Line Regulation 2ppm/V Max
- Supply Current 350 μA Max
- Operating Voltage Range +4.5V to +40V
- Extended Industrial Temp Range -40°C to $+85^{\circ}\text{C}$

ORDERING INFORMATION†

TCV _o	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99	CERDIP	PLASTIC	
10	REF43BJ*	REF43BZ*	—	MIL
10	REF43FJ	REF43FZ	—	XIND
20	REF43GJ	REF43GZ	REF43GP	XIND

REF43ARC/833 will be available in hermetic LCC package.

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

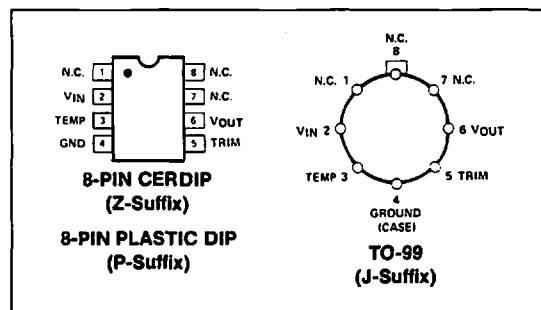
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

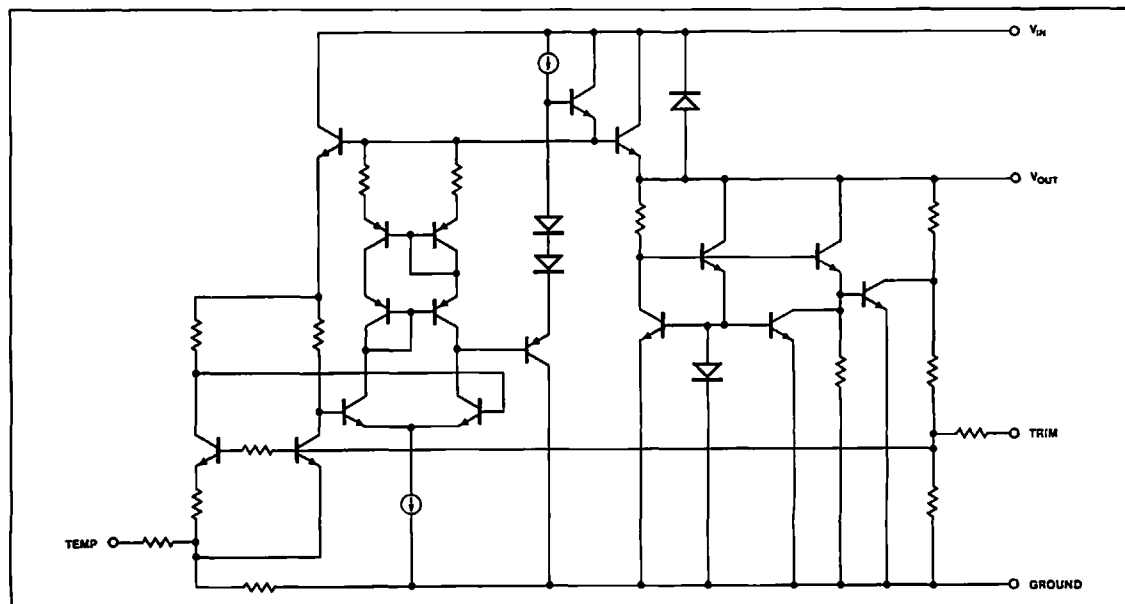
The REF-43 is a low-power precision reference providing a stable +2.5V output independent of variations in supply voltage, load conditions or ambient temperature. It is suitable as a reference level for 8, 10 and 12-bit data acquisition systems, or wherever a stable, known voltage is required.

Tight output tolerances and low thermal drift are assured by zener-zap trimming of both output voltage and its temperature coefficient. A unique curvature correction circuit reduces the thermal curvature characteristic of many previous bandgap references.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



The REF-43 may be operated with supply voltages from +4.5V to +40V. The output voltage changes by less than $355\mu\text{V}$ from one extreme of supply voltage to the other. With only $350\mu\text{A}$ maximum quiescent current, the REF-43 is ideally suited to applications where power dissipation must be minimized, as in precision battery-powered equipment. The low supply current minimizes drift due to self-heating after power-up.

A temperature output provides a means of determining system ambient temperature. Applications of the REF-43 include A/D and D/A conversion, 4-20mA transmitter/receiver operation and log amplifiers.

For a low-cost 2.5V reference available in small-outline packages consult the REF-03 data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	40V
Internal Power Dissipation (Note 2)	500mW
Output Short-Circuit Duration	Indefinite

Operating Temperature Range

REF-43B (J, Z)	-55°C to +125°C
REF-43F, (J, Z)	-40°C to +85°C
REF-43G, (J, Z, P)	-40°C to +85°C
Storage Temperature Range	-65°C to +175°C
Junction Temperature Range	-65°C to +175°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. See table for maximum ambient temperature and rating.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Cerdip (Z)	75°C	6.7mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

ELECTRICAL CHARACTERISTICS at $V_{\text{IN}} = +5\text{V}$, $I_{\text{L}} = 0\text{mA}$, $T_{\text{A}} = 25^{\circ}\text{C}$ unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	REF-43B			REF-43F			REF-43G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Tolerance		No Load	—	0.03	0.1	—	0.02	0.05	—	0.05	0.2	%
Output Voltage	V_{O}	No Load	2.4975	2.500	2.5025	2.4988	2.500	2.5012	2.495	2.500	2.505	V
Output Voltage Noise	e_{nRMS}	0.1Hz to 1kHz	—	5	8	—	5	8	—	5	8	μVRMS
Line Regulation		$V_{\text{IN}} = +4.5\text{V}$ to +40V	—	1	5	—	0.6	2	—	1	5	ppm/V
Load Regulation		$I_{\text{L}} = 0\text{mA}$ to 10mA	—	12	20	—	12	20	—	15	30	ppm/mA
Quiescent Supply Current	I_{SV}	No Load	—	200	350	—	200	350	—	200	350	μA
Load Current (Sourcing)	I_{L}		10	20	—	10	20	—	10	20	—	mA
Load Current (Sinking)	I_{S}		—	-3	—	—	-3	—	—	-3	—	mA
Short-Circuit Output Current	I_{SC}	Output Shorted to Ground	—	30	—	—	30	—	—	30	—	mA
Output Voltage Temperature Coefficient	TCV_{O}	$-55^{\circ}\text{C} \leq T_{\text{A}} \leq +125^{\circ}\text{C}$	—	5	10	—	—	—	—	—	—	ppm/°C
		$-40^{\circ}\text{C} \leq T_{\text{A}} \leq +85^{\circ}\text{C}$	—	—	—	—	4	10	—	5	20	
Temperature Voltage Output Tempco	TCV_{TEMP}		—	2.1	—	—	2.1	—	—	2.1	—	mV/°C

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*Indicates new product or product whose data sheet has been finalized since the 1986 data book.

DAC-87
COMDAC® Company
D/A Converter



Precision Monolithics Inc.

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DIGITAL-TO-ANALOG CONVERTERS

11

INTRODUCTION

A D/A converter accepts a digital input and produces an analog output. The basic DAC consists of a voltage or current reference, binary-weighted precision resistors, a set of electronic switches, and a means of summing the weighted currents.

Three important criteria for selecting a good DAC are resolution, accuracy, and speed. Other essential requirements to be considered are temperature stability, input coding, output format, reference requirements, and power consumption.

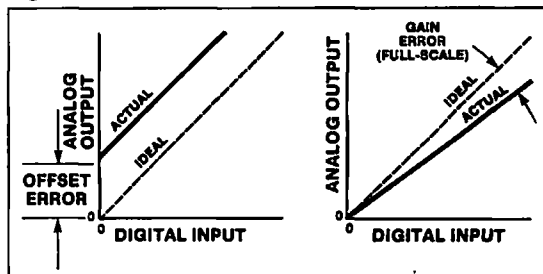
Since introducing the first monolithic D/A converter in 1970, PMI has continually improved and updated its DAC product line. Using both bipolar and CMOS technologies, PMI offers complete selections of parametric trade-offs available from these technologies. Very high speed, internal references and amplifiers are key features of the bipolar technology DACs. The CMOS technology DACs offer a much higher degree of logic interface function, while maintaining absolute minimums in power dissipation. A wide offering of microprocessor-interfaceable DACs simplify connection to 4, 8, and 16-bit microprocessor systems. The DAC with "memory" is another first offered by PMI to simplify system self-diagnosis of data path integrity.

The selection guides following the definitions will aid you in quickly locating the appropriate DAC for your application.

DEFINITIONS — LINEAR DIGITAL-TO-ANALOG CONVERTERS

Absolute Accuracy — The absolute accuracy of a DAC is the difference between the actual unadjusted analog output and the ideal output that is expected when a given digital code is applied. Sources of error include full-scale error (gain error), zero-scale error (offset error), nonlinearity errors, and the drift of all of these. Therefore, absolute accuracy includes all deviations from the ideal. (See Figure 11.1)

Figure 11.1 Gain and Offset Error Defined



A.C. Feedthrough — The ratio of the amplitude of signal at the DAC output to the reference input with all DAC switches off. This parameter is expressed in dBs.

BCD — The abbreviation BCD stands for binary-coded decimal. It is a binary code used to represent decimal numbers in which the digits 0 through 9 are coded, using the 4-bit binary 8-4-2-1 code.

Binary — A positive-weighted code in which a number is represented by:

$$N = a_0 2^0 + a_1 2^1 + a_2 2^2 + \dots + a_n 2^n$$

where each coefficient "a_i" has a value of zero or one. Data converters use this code in its fractional form where:

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \dots + a_n 2^{-n}$$

and N has a fractional value between zero and one.

Bit — The unit of binary information. It can have the value of zero or one.

Bipolar Output — When the analog signal range includes both positive and negative values, the output is said to be bipolar. The transfer characteristic of an ideal 2-quadrant bipolar-output DAC is shown in Figure 11.2.

Differential Nonlinearity (DNL) — Differential nonlinearity is the worst case deviation of any adjacent analog outputs from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called differential nonlinearity error or DNL. DACs with DNL greater than ± 1 LSB may be nonmonotonic. Maximum DNL error is less than or equal to twice the maximum INL. (See Figure 11.3)

Figure 11.2 Bipolar Output Converter

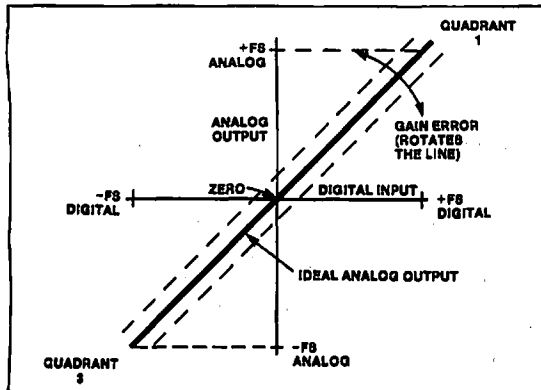
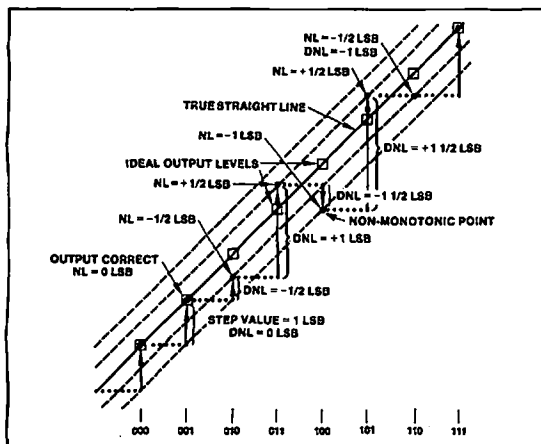


Figure 11.3 Nonlinearity (NL) and Differential Nonlinearity (DNL)



Digital Crosstalk (Q) — Digital crosstalk is a parameter that is used with multiple converters in a single package. It is the glitch impulse that is transferred from one converter that is being addressed to another converter that is not being addressed. It is specified in nV-secs and is measured with $V_{REF} = 0V$.

Digital Feedthrough (FT) — Digital feedthrough is the glitch-energy impulse transferred from the DAC's digital input to the analog output. It is specified in nV-secs and is measured with $V_{REF} = 0V$.

Dynamic Range (DR) — The dynamic range of a DAC is the ratio of the largest output to the smallest output (excluding zero) expressed in decibels (dB). For linear DACs, this ratio is 2^n , where n = number of bits of resolution:

DR (in dB) = $20 \text{ Log}_{10} 2^n \approx 6n$ for linear DACs;
(COMDACs® are 66 or 72dB.)

Endpoint Linearity — See Integral Nonlinearity.

Functional Compliance — The functional compliance of a DAC is the voltage range over which the current output can be driven and for which the DAC output current will maintain the same relative accuracy (the output can change absolutely).

Full Scale (FS) — The full-scale output of a DAC is its maximum voltage or current. For a binary DAC, the full-scale output occurs when the digital inputs are all ones. The full-scale value is one LSB less than the reference value.

Full-Scale Gain Error (G_{FSE}) — See Gain Error.

Full-Scale Range (FSR) — The difference between the maximum analog output and the minimum analog output of a DAC.

Gain Drift (TCG_{FS}) — The variation of the full-scale value (voltage or current) measured over the operating temperature range is called gain drift. This parameter has units of %FS, ppmFS, or LSB. It may also be expressed % of FS/°C, ppmFS/°C, etc.

Gain Error (G_{FSE}) — The difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value (see Figure 11.1). It is the deviation in slope of the DAC transfer characteristic from ideal.

Glitch — A glitch is a switching transient appearing in the output during a code transition. Its value is expressed as a product of voltage ($V \times ns$) or current ($mA \times ns$) and time duration or charge transferred (in Picocoulombs).

Integral Nonlinearity (INL) or Nonlinearity (NL)

- This is the single most important DAC specification. PMI measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the

end points, expressed as a percent of full-scale range or in terms of LSBs. (See Figure 11.5)

For DACs, a specification of $\pm 1/2$ LSB INL guarantees monotonicity and ± 1 LSB maximum differential nonlinearity.

Least Significant Bit (LSB) — The analog value of the LSB is the smallest change that can occur in the output of a DAC. It corresponds to a one-bit change in the binary input. The analog value will be either a voltage or current.

$$\text{LSB (Analog Value)} = \frac{\text{FSR}}{2^n}$$

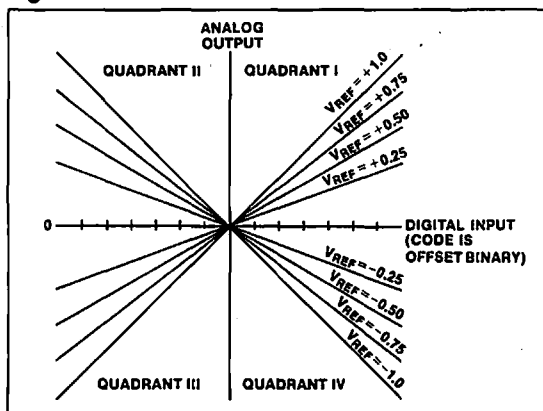
where FSR = Full-Scale Range
n = number of bits

Most Significant Bit (MSB) — The analog value of the MSB is the largest incremental output change obtainable by switching a single input bit. The analog value will be either a voltage or current.

$$\text{MSB (Analog Value)} = \frac{\text{FSR}}{2}$$

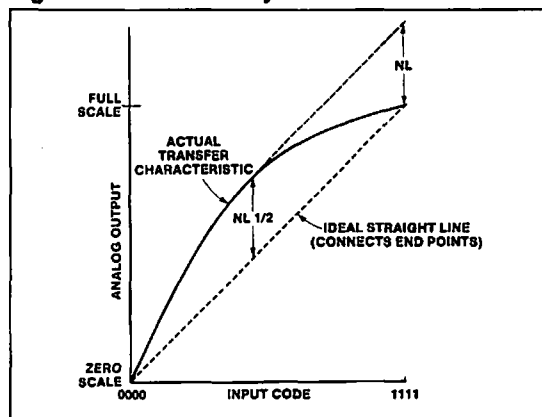
Monotonicity — A DAC is monotonic if the analog output either increases or remains the same for an increasing digital input code. If the DNL is less than or equal to ± 1 LSB, monotonicity is guaranteed. (See Figure 11.3)

Figure 11.4 DAC Transfer Curves



Multiplying DACs — The DAC multiplies an analog reference by a digital word. Some DACs can multiply only positive digital words by a positive reference. This is known as single quadrant operation (Quadrant I, see Figure 11.4). Two quadrant operation (Quadrants I and III) can be performed by a DAC that usually operates in Quadrant I by configuring the output for bipolar output operation. This is accomplished by offsetting the output by a negative MSB ($1/2$ of FSR), so that the MSB becomes the sign bit. CMOS DACs provide four quadrant operation by allowing the use of both positive and negative references. (Quadrants I, II, III, IV).

Figure 11.5 Nonlinearity



Nonlinearity (NL) — See Integral Nonlinearity.

Offset Drift (TCV_{OS}, TC_IOS) — The variation of the offset (voltage or current) measured over the operating temperature range. The offset drift is divided by the temperature range over which it is measured, and expressed in ppm per degree centigrade or percent of full-scale range. This parameter applies to DACs operating in the bipolar output mode. See zero-scale drift for DACs operating in the unipolar output mode.

Offset Error (V_{OS}, I_{OS}) — The offset error is the error at analog zero for a data converter operating in the bipolar mode.

Output Resistance (R_O) — Output resistance is the equivalent internal resistance for a current output D/A converter as seen at its output. It is measured as the change in output current ΔI with the change in output voltage ΔV . It is a direct measure of the true compliance.

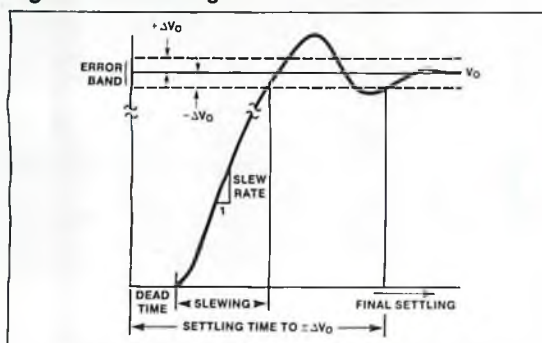
Power Supply Sensitivity (P_{SS}) — The change in the output of the converter due to a change in the power supply value. This may be expressed as a percent of full-scale range per one percent change in the power supply, or as a percent of full scale per volt of power supply change. Normally P_{SS} is specified at DC; it is sometimes specified over a given frequency range.

Relative Accuracy — See Integral Nonlinearity.

Resolution (n) — The resolution of a DAC is the number of states (2^n) that the FSR is divided (or resolved) into, where n is equal to the number of bits.

Settling Time — Settling time is the elapsed time for the analog output to reach its final value within a specified error band after a digital input code change. It is usually specified for a full-scale change and measured from the 50% point of the logic input change to the time the output reaches its final value within the specified error band. (See Figure 11.6)

Figure 11.6 Settling Time Measurement



Three-State Outputs — A digital output circuit that can be programmed to output a logic low, logic high, or a high output impedance state. These devices are generally connected to digital buses.

Total Unadjusted Error (TUE) — The total unadjusted error is a comprehensive specification which includes full scale error, relative accuracy, and zero code error. It is noted that the maximum ideal output voltage is $V_{REF} - 1\text{LSB}$, where $1\text{LSB} = V_{REF}/2^n$, and n is the DAC resolution. This clearly indicates that the LSB voltage size is dependent on V_{REF} , and the zero code error will increase as V_{REF} decreases (in terms of LSB). The total unadjusted error then, will vary over the V_{REF} voltage range.

True Compliance — The true compliance of a DAC is the voltage range over which the current output can vary while the DAC maintains an absolute accuracy of $\pm 1/2$ LSB. The higher the DAC output impedance, the better the voltage compliance will be.

Unipolar Output — A DAC operates in the unipolar output mode when the analog output starts at zero, stopping at a full-scale positive or negative value, while the digital inputs are changed from zero to all-ones code. The analog output occurs in one quadrant.

Zero-Scale Error (V_{ZSE} , I_{ZSE}) — The zero-scale error is the error at analog zero for a data converter operating in the unipolar mode.

Zero-Scale Drift (TCV_{ZS} , TCI_{ZS}) — The variation of zero scale measured over the operating temperature. It is expressed in ppmFS/ $^{\circ}\text{C}$, or %FS/ $^{\circ}\text{C}$, etc.

Zero-Scale Symmetry Error (V_{ZSS}) — This definition applies only to sign-magnitude DACs. It is the change in the analog output produced by switching the sign bit with a zero-code input to the magnitude bits. It is expressed in units of voltage, current, or in fractions of an LSB.

DEFINITIONS — COMPANDING DACs

The companding (COMDAC®) DACs that PMI manufactures are the DAC-86, DAC-88, and the DAC-89. They are constructed such that the more significant bits of the digital input have a larger than binary relationship to the less significant bits. This decreases the resolution of the more significant bits, which increases the analog signal range. The effect of this is to compress more data into the more significant bits.

Chord — The mathematical formula, describing the DAC transfer function, is implemented by performing a piecewise linear approximation of the function. The straight line segments used in the approximation are called chords.

Chord Endpoints — The digital code corresponding to the maximum analog output for a given chord is called the chord endpoint.

Dynamic Range (DR) — The dynamic range of a DAC is the ratio of the largest output to the smallest output (excluding zero) expressed in decibels (dB). For the COMDACs® this would be output (11_{7,15}) divided by output (1_{0,1}). This is then converted to dB using the formula:

$$DR = 20 \log_{10} \left(\frac{I_{7,15}}{I_{0,1}} \right) \text{ (dB)}$$

Encode Current — The encode current is the difference between $I_{OE(+)}$ and $I_{OD(+)}$ or the difference between $I_{OE(-)}$ and $I_{OD(-)}$ at any code.

Full-Scale Symmetry Error — The full-scale symmetry error of a DAC is the difference between the maximum and the minimum analog output values. For the COMDACs® this is the difference between $I_{OD(-)}$ and $I_{OD(+)}$ or $I_{OE(+)}$ and $I_{OE(-)}$.

Output-Level Notation — Each output current level may be designated by the digital input code as $I_{c,s}$; where c = chord number and s = step number. For example, $I_{0,0}$ = zero scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of the first chord (C_0); and $I_{7,15}$ = full-scale current.

Steps — Each chord is divided into equal increments called steps.

Step Nonlinearity — This is the deviation of the actual step size from the ideal step size within a chord. In a linear DAC, it corresponds to differential nonlinearity.



D/A CONVERTERS

Precision Monolithics Inc.

DIGITAL-TO-ANALOG CONVERTER SELECTION GUIDE

PMI offers a complete line of digital-to-analog converters (DACs), all of which are guaranteed to be monotonic over their operating temperature ranges, and some which have become industry standards. The D/A converters have been

arranged in the selector guide by resolution. Eight-bit through 12-bit devices are sorted by settling time and number of D/A converters per package. At 8-bit resolution PMI offers single, dual and quad products. At 12-bit resolution a choice of single and dual products are available.

8-Bit Resolution, Single Digital-to-Analog Converters

Product	Type	Settling Time to 1/2LSB (μ s)	Linearity INL	Output Range	Ref. Input	Power Dissipation (mW)	Digital Input Coding	Digital Interface Architecture
DAC08	Bipolar	0.135	0.1%FS	2mA	2mA	136	Binary	Parallel
DAC20	Bipolar	0.150	$\pm 1/2$ LSB	2mA	2mA	194	2 Digit BCD	Parallel
PM7524	CMOS	0.300	$\pm 1/8$ LSB	1mA	10V	5	Binary	Latch
DAC888	Bipolar	0.400	0.1%FS	2mA	2mA	190	Binary	Latch
DAC208	Bipolar	0.750†	0.1%FS	+5 or ± 10 V	Int Ref	315	Sign-Magnitude	Parallel
PM7224	CMOS	5.0	$\pm 1/2$ LSB	10V	10V	60	Binary	Double-Latch

8-Bit Resolution, Dual Digital-to-Analog Converters

Product	Type	Settling Time to 1/2LSB (μ s)	Linearity INL	Output Range	Ref. Input	Power Dissipation (mW)	Digital Input Coding	Digital Interface Architecture
PM7528	CMOS	0.350	$\pm 1/2$ LSB	1mA	10V	5	Binary	Latch

8-Bit Resolution, Quad Digital-to-Analog Converters

Product	Type	Settling Time to 1/2LSB (μ s)	Linearity INL	Output Range	Ref. Input	Power Dissipation (mW)	Digital Input Coding	Digital Interface Architecture
DAC8408	CMOS	0.250	$\pm 1/4$ LSB	1mA	10V	5	Binary	Readback-Latch
PM7226	CMOS	5.0	$\pm 1/2$ LSB	10V	10V	250	Binary	Latch

8-Bit Resolution, Companding Digital-to-Analog Converters

Product	Type	Settling Time to 1/2LSB (μ s)	Linearity INL	Output Range	Ref. Input	Power Dissipation (mW)	Digital Input Coding	Digital Interface Architecture
DAC88	Bipolar, μ -law	0.5†	$\pm 1/2$ STEP	2mA	0.5mA	263	Sign-Chord Step	Parallel
DAC89	Bipolar, A-law	0.5†	$\pm 1/2$ STEP	2mA	0.5mA	263	Sign-Chord Step	Parallel

† Typical value



D/A CONVERTERS

Precision Monolithics Inc.

10-Bit Resolution Single Digital-to-Analog Converters

Product	Type	Settling Time to 1/2LSB (μ s)	Linearity INL	Output Range	Ref. Input	Power Dissipation (mW)	Digital Input Coding	Digital Interface Architecture
DAC10	Bipolar	0.150	$\pm 1/2$ LSB	4mA	2mA	285	Binary	Parallel
DAC100	Bipolar	0.300	0.05%FS	2mA	Int Ref	250	Complementary	Parallel
PM7533	CMOS	0.600†	0.05%FS	1mA	10V	30	Binary	Parallel
DAC06	Bipolar	1.5	0.1%FS	± 5 V	Int Ref	300	1's Complement	Parallel
DAC210	Bipolar	1.5	0.05%FS	± 10 V	Int Ref	315	Sign-Magnitude	Parallel
DAC03	Bipolar	2.0	0.1%FS	+5 or +10V	Int Ref	350	Sign-Magnitude	Parallel

12-Bit Resolution, Single Digital-to-Analog Converters

Product	Type	Settling Time to 1/2LSB (μ s)	Linearity INL	Output Range	Ref. Input	Power Dissipation (mW)	Digital Input Coding	Digital Interface Architecture
DAC312	Bipolar	0.5	0.05%FS	4mA	1mA	305	Binary	Parallel
DAC8012	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Readback- Latch
DAC8043	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Serial
PM7541	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Parallel
PM7541A	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Parallel
PM7542	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Nibble
PM7543	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Serial
PM7545	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Latch
PM7548	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Byte-Latch
PM7645	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Latch
PM562	Bipolar	1.5†	$\pm 1/4$ LSB	2mA	10V	465	Binary	Parallel

12-Bit Resolution, Dual Digital-to-Analog Converters

Product	Type	Settling Time to 1/2LSB (μ s)	Linearity INL	Output Range	Ref. Input	Power Dissipation (mW)	Digital Input Coding	Digital Interface Architecture
DAC8212	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Latch
DAC8221	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Latch
DAC8222	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Double-Latch
DAC8248	CMOS	1.0	$\pm 1/2$ LSB	1mA	10V	10	Binary	Byte-Latch

DIGITAL-TO-ANALOG CONVERTERS

11

† Typical value



DAC-01

6-BIT VOLTAGE-OUTPUT D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- Fast $3\mu\text{s}$ Settling Time Max
- Complete Includes Reference, Ladder, Op Amp
- Low Power Consumption 250mW Max
- 6-Bit Resolution 7-Bit Accuracy
- 3 Output Options $+10\text{V}, \pm 5\text{V}, \pm 10\text{V}$
- Standard Power Supplies $\pm 12\text{V}$ to $\pm 18\text{V}$
- TTL — Compatible Logic Levels
- MIL-STD-883 Class B Processing Available From Stock

ORDERING INFORMATION†

FULL TEMP. N.L. LSB	14-PIN HERMETIC DIP	
	MILITARY TEMP.	COMMERCIAL TEMP.
$\pm 1/8$	DAC01Y*	—
$\pm 1/4$	DAC01BY*	DAC01CY
	DAC01FY**	DAC01HY**
$\pm 1/2$	—	DAC01DY

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

** Unipolar only — all others unipolar or bipolar.

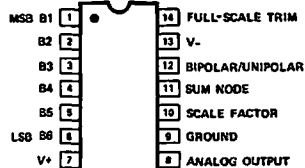
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The DAC-01 is a complete monolithic 6-bit digital-to-analog converter. The device contains current steering logic, current sources, a diffused resistor ladder network, precision

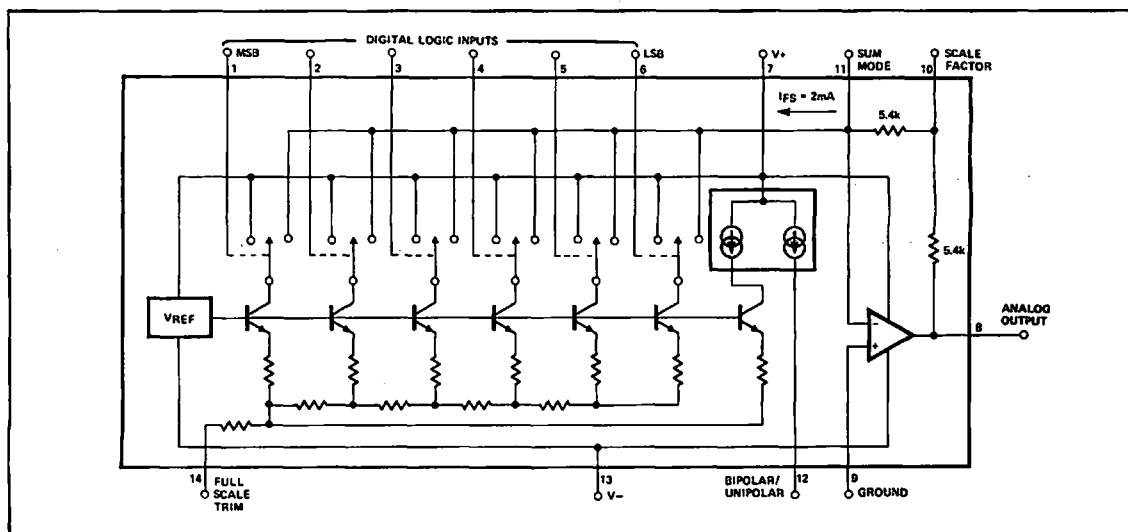
voltage reference and fast summing op amp on one chip. Monolithic construction provides low power consumption and high reliability. Wide power supply range, three output voltage options, and three input code options assure flexibility for a wide variety of applications. A seventh bit may also be added for greater resolution. Introduced in 1970, the DAC-01 is still the fastest, lowest power, most accurate 6-bit complete monolithic DAC available. The DAC-01 is ideal for CRT deflection circuits, servo positioning controls, digitally programmed power supplies and pulse generators, modem and telephone system digitizing and demodulation circuits, digital filters, and 6-bit A/D converters.

PIN CONNECTIONS



14-PIN HERMETIC DIP
(Y-Suffix)

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (See Note 3)

Operating Temperature	
DAC-01, DAC-01B, DAC-01F	-55°C to +125°C
DAC-01C, DAC-01H, DAC-01D	0°C to +70°C
DICE Junction Temperature (T_j)	-65°C to +150°C
V+ Supply Voltage to Ground	0 to +18V
V- Supply Voltage to Ground	0 to -18V
Logic Input to Ground	-0.7 to +6V
Internal Power Dissipation (Note 1)	500mW

Storage Temperature	-85°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (Note 2)	Indefinite

NOTES:

1. Rating applies to ambient temperatures of 100°C. For temperatures above 100°C, derate linearly at 10mW/°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
3. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and over the rated operating temperature range, unless otherwise noted.

PARAMETER	SYMBOL	DAC-01*	DAC-01B*	DAC-01F	DAC-01C	DAC-01H	DAC-01D	UNITS
Output Options		Unipolar Bipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	Unipolar	Unipolar Bipolar	
Temperature Range	T_A	-55/+125	-55/+125	-55/+125	0/+70	0/+70	0/+70	°C
Nonlinearity 25°C/Maximum	NL	±0.40	±0.40	±0.40	±0.40	±0.40	±0.78	%FS
Nonlinearity Over Temperature — Maximum	NL	±0.45	±0.45	±0.45	±0.45	±0.45	±0.78	%FS
Full-Scale Tempco — Maximum	T_C	±80	±120	±60	±180	±160	±160	ppm/°C
Unipolar Zero-Scale Output Voltage — Maximum (Notes 1, 2)	V_{ZS}	25	25	40	25	40	50	mV

* Processed to MIL-STD-883 only.

ELECTRICAL CHARACTERISTICS for all DAC-01 grades, $V_S = \pm 15V$ and over the rated operating temperature range unless otherwise noted.

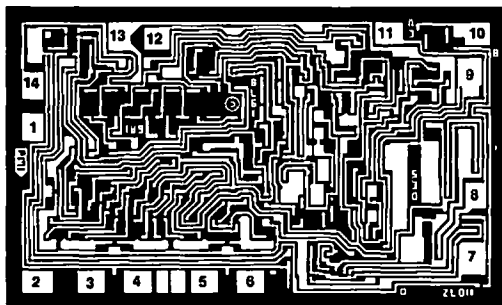
PARAMETER	SYMBOL	CONDITIONS	MIN	DAC-01 TYP	MAX	UNITS
Unipolar Full Range Output Voltage (Note 3)	V_{FR}	2k Ω load, logic $\leq 0.8V$, short pin 13 to pin 14. Short pin 12 to Ground and pin 10 to pin 11.	+10.0	—	+11.75	V
Bipolar Output Voltage (Note 3)		2k Ω load, short pin 11 to pin 12. Short pin 13 to pin 14, short pin 10 to pin 11.				
±5 Volt Range	V_{FR+} V_{FR-}	Logic Inputs $\leq 0.8V$ Logic Inputs $\geq 2.0V$ Open pin 10	+4.93 -5.94	—	+5.94 -4.93	V
±10 Volt Range	V_{FR+} V_{FR-}	Logic Inputs $\leq 0.8V$ Logic Inputs $\geq 2.0V$	+9.86 -11.89	—	+11.89 -9.86	V
Bipolar Offset Voltage (Note 1)		±5 Volt Range	—	±40	±70	mV
±1/2 ($ V_{FR+} - V_{FR-} $)		±10 Volt Range	—	±80	±140	mV
Resolution			6	—	—	Bits
Logic Input "0"	V_{INL}		—	—	0.8	V
Logic Input "1"	V_{INH}		2	—	—	V
Logic Input Current, Each Input	I_{IN}		—	±2	±8	μA
Power Supply Sensitivity	P_{SS}	±12V $\leq V_S \leq \pm 18V$ $V_{FS} \sim 10.0V$	—	±0.01	±0.15	% V_{FS}/V
Power Consumption	P_D	No Load	—	200	250	mW
Supply Current	I+ I-	V+ = +15V V- = -15V Logic Inputs $\leq 0.8V$	— —	— —	7.3 9.3	mA
Setting Time to ±1/2 LSB (Note 4)	t_s	2.0V $\leq$ Logic Level $\leq 0.8V$ $T_A = 25^\circ C$	—	1.5	3	μs

NOTES:

1. Zero-scale or bipolar offset voltage can be trimmed to zero volts or to the exact one's or two's complement condition with an external resistor network to pin 11.
2. Logic input voltage $\geq 2.0V$.
3. Full-scale is adjustable to precisely 10V for unipolar operation and 10V or 20V peak-to-peak bipolar operation with an external 500 Ω potentiometer from pin 14 to V-.
4. Guaranteed by design.



DICE CHARACTERISTICS



1. B1 (MSB)
2. B2
3. B3
4. B4
5. B5
6. B6 (LSB)
7. V+
8. ANALOG OUTPUT
9. GROUND
10. SCALE FACTOR
11. SUM NODE
12. BIPOLAR/UNIPOLAR
13. V-
14. FULL-SCALE TRIM

DIE SIZE 0.093 × 0.055 inch, 5115 sq. mils (2.36 × 1.40 mm, 3.30 sq. mm)

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-01N BIPOLAR AND UNIPOLAR LIMIT	DAC-01G BIPOLAR AND UNIPOLAR LIMIT	UNITS
Nonlinearity	NL	$V_S = \pm 15\text{V}$	1/4	1/2	L.S.B. MAX
Zero-Scale Voltage	V_{ZS}	$V_S = \pm 15\text{V}$	25	35	mV MAX

WAFER TEST LIMITS at $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

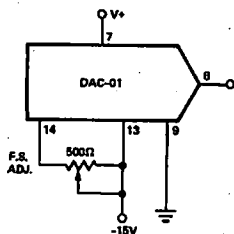
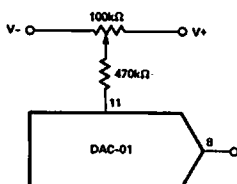
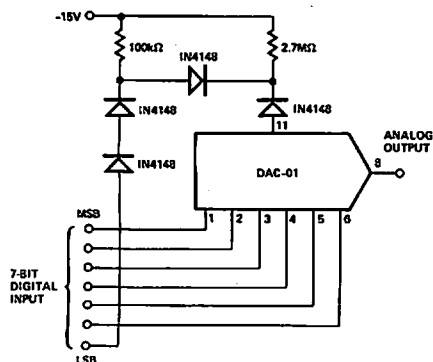
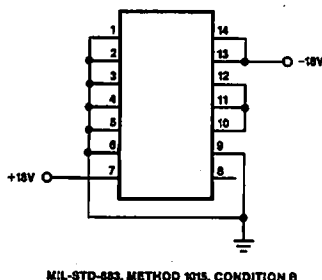
PARAMETER	SYMBOL	CONDITIONS	DAC-01 LIMIT	UNITS
Unipolar Full-Scale Output Voltage (All Models)	V_{FR}	2k Ω Load, Logic $\leq 0.8\text{V}$, Short V- to Full-Scale Trim, Unipolar/Bipolar to Ground, and Scale Factor to Sum Node	10.00 11.75	V MIN V MAX
Bipolar Output Voltage	V_{FR+}	2k Ω Load, Short Sum Node to Unipolar/Bipolar. Short V- to Full-Scale Trim and Scale Factor to Sum Node.	+4.93	V MIN
±5 Volt Range	V_{FR-}	Logic Inputs $\leq 0.8\text{V}$	-5.94	V MAX
±10 Volt Range	V_{FR+}	Open-Scale Factor	+9.78	V MIN
	V_{FR-}	Logic Inputs $\leq 0.8\text{V}$	-11.89	V MAX
Bipolar Offset Voltage		±5 Volt Range	±1/2	LSB MAX
±1/2 ($IV_{FR+} - IV_{FR-}$)		±10 Volt Range		
Resolution			6	Bits MAX
Logic Input "0"	V_{INH}		0.8	V MAX
Logic Input "1"	V_{INH}		2	V MIN
Logic Input Current, Each Input	I_{OVI}		±8	μA MAX
Power Supply Rejection	PSR	$\pm 12\text{V} \leq V_S \leq \pm 18\text{V}$, $V_S = 10.0\text{V}$	0.15	%FS/V MAX
Power Consumption	P_d	No Load	250	mW MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at 25°C .

PARAMETER	SYMBOL	CONDITIONS	DAC-01N TYPICAL	DAC-01G TYPICAL	UNITS
Settling Time	t_s	To $\pm 1/2$ LSB	1.5	1.5	μs
Full-Scale Tempco	TCV_{FS}	$V_S = \pm 15\text{V}$	60	90	ppm/°C

**BASIC CIRCUIT CONNECTIONS****FULL-SCALE ADJUSTMENT TECHNIQUE****OPTIONAL ZERO-SCALE OR BIPOLAR OFFSET ADJUSTMENT****ADDITION OF 7th BIT****BURN-IN CIRCUIT****APPLICATIONS INFORMATION****INPUT CODES**

The DAC-01 uses standard complementary binary coding for unipolar operation (all inputs logic high produces zero output voltage). One's complement coding may be implemented by shorting pin 11 to pin 12 and inverting the MSB (all other bits are not inverted). Complementary offset binary coding may be implemented by shorting pin 11 to pin 12, and injecting approximately $5\mu\text{A}$ into pin 11 (which is at ground potential) by using the "optional Zero-Scale or bipolar offset adjustment" circuit. Two's complement code is achieved when the MSB for complementary offset binary is inverted.

FULL-SCALE ADJUST

A 500Ω pot from pin 14 to V^- can be used to adjust the Full-Scale output voltage to exactly 10 volts in unipolar mode or 10 to 20 volts peak-to-peak in bipolar mode. If no pot is used, connect pin 14 to V^- .

SCALE FACTOR

For +10 volts or ± 5 volt outputs, short pin 10 to pin 11 (adjusts the feedback resistor around the output amplifier). For ± 10 volt output, leave pin 10 open. Intermediate output voltages may be obtained by placing a pot between pin 10 and pin 11. This will, however, seriously degrade the Full-Scale temperature coefficient due to the mismatch between the $+1150\text{ppm}/^\circ\text{C}$ tempco of the diffused resistors and the pot tempco.

CAPACITIVE LOADS

When driving capacitive loads greater than 50pF in Unipolar mode or 30pF in Bipolar mode a 100pF capacitor may be placed from pin 11 to ground for added stability.

LOWER RESOLUTION APPLICATIONS

When less than 6 bits of resolution is required, connect unused bits to a voltage level greater than $+2.0$ volts. The $+5$ volt logic supply is adequate.



DAC-02/DAC-03/DAC-05

10-BIT-PLUS-SIGN VOLTAGE-OUTPUT
D/A CONVERTERS

Precision Monolithics Inc.

FEATURES

- Complete Includes Reference and Op Amp
- Compact Single 18-Pin DIP Package
- Bipolar Output ($\pm 10V$) Sign-Magnitude Coding
- DAC-03 — Unipolar Only; +5V or +10V
- Monotonicity Guaranteed
- Nonlinearity ± 1 LSB
- Fast 2.0 μ s Settling Time
- Stable Full-Scale Tempco 60ppm/ $^{\circ}$ C
- Low Power Consumption 300mW Max
- TTL, CMOS Compatible Inputs
- MIL-STD-883 Class B Processing Available on DAC-05

ORDERING INFORMATION †

MONO- TONOCITY BITS	PACKAGE: 18-PIN HERMETIC DIP			
	MILITARY TEMP*	COMMERCIAL TEMP		
10	DAC05AX	DAC02ACX	DAC03ADX	DAC05EX
8	—	DAC02CCX	DAC03CDX	—
7	—	DAC02DDX	—	—

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

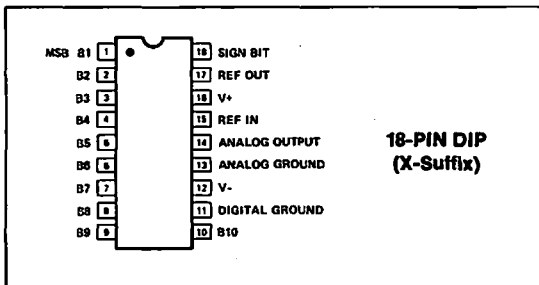
GENERAL DESCRIPTION

The DAC-02 and DAC-05 are complete 10-bit plus sign D/A converters on a single monolithic chip. All elements of a complete sign-magnitude DAC are included; precision vol-

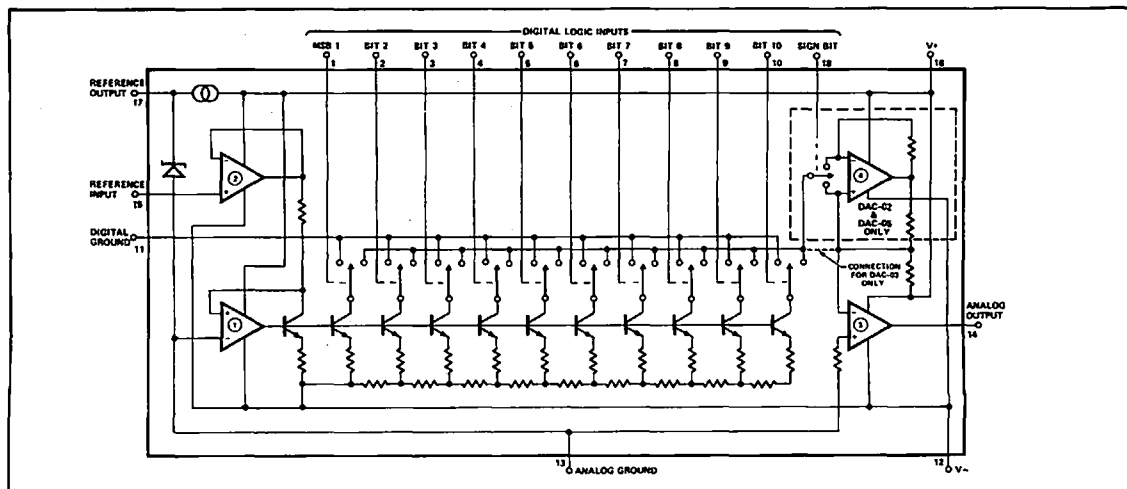
tage reference, current steering logic, current sources, R-2R resistor network, logic-controlled polarity switch, and high speed internally-compensated output op amp. Monotonicity guaranteed over the entire temperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The wide power supply range, low power consumption, wide logic input compatibility and sign-magnitude coding assures utility in a wide range of applications including CRT displays, data acquisition systems, A/D converters, servo positioning controls, and audio digitizing/reconstruction systems.

The DAC-03 is similar in construction to the DAC-02/DAC-05 except for a unipolar only output. This device is intended for low cost, limited temperature range applications, with the same general specifications as its premium counterparts.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note)

Operating Temperature Range

DAC-05A -55°C to +125°C

DAC-02 and DAC-03, All

DAC-05E 0°C to +70°C

Storage Temperature Range -65°C to +150°C

V+ Supply to Analog Ground 0 to +18V

V- Supply to Analog Ground 0 to -18V

Analog Ground to Digital Ground 0 to ±0.5V

Logic Inputs to Digital Ground -5V to (V+ - 0.7V)

Internal Reference Output Current 300µA

Reference Input Voltage 0 to +10V

Internal Power Dissipation 500mW

Lead Temperature (Soldering, 60 sec) 300°C

Output Short-Circuit Duration Indefinite

(Short circuit may be to ground or either supply.)

NOTE: For ambient temperatures above 100°C derate 100mW/°C.

OUTPUT VOLTAGE RANGE SELECTION TABLE

PRODUCT	OUTPUT VOLTAGE RANGE	ADD AS SUFFIX TO PART NO.
DAC02	±10V	1
DAC03	0 to +10V	1
DAC03	0 to +5V	2
DAC05	±10V	1

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0 \leq T_A \leq +70^\circ C$ for DAC-02 and DAC-05E, $T_A = 25^\circ C$ for DAC-03 and $-55 \leq T_A \leq +125^\circ C$ for DAC-05A, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-02	DAC-03	DAC-05	MIN	TYP	MAX	UNITS
Monotonicity			AC	AD	A/E	10	—	—	Bits
			CC	CD		8	—	—	
			DD			7	—	—	
Nonlinearity	NL		AC	AD	A/E	—	—	±0.1	% FS
			CC	CD		—	—	±0.2	
			DD			—	—	±0.4	
Full-Scale Tempco	T_C	INT REF	AC/CC	ALL	A	—	—	±80	ppm/°C
					E	—	±60	—	
		EXT REF	DD			—	±45	±100	ppm/°C
						—	±40	±150	
Settling Time	t_s	To 1/2 LSB, 10V Step (Note 4)	ALL	ALL	ALL	—	2	—	µs
Full Range Output Voltage (Note 1)	V_{FR}	V_{FR+} (SB High)	ALL		ALL	+10	—	+11.5	Volts
		V_{FR-} (SB Low)	ALL		ALL	-11.5	—	-10	
		DAC-03 +10V +5V		ALL ALL		+10 +5.0	—	+11.5 +5.75	
Zero-Scale Offset	V_{ZS}	SB High. All other logic inputs low. $T_A = 25^\circ C$			ALL	—	±1	±5	mV
			ALL	ALL		—	±1	±10	
		$T_A = \text{Min or Max}$	ALL		ALL	—	±2	±10	
Zero-Scale Symmetry	V_{ZSS}	(Note 2)	AC/CC	N/A		—	±1	±5	mV
			DD			—	±1	±10	
Full Range Bipolar Symmetry	V_{FRS}	$V_{FR+} - V_{FR-} $ (Note 3)	AC/CC	N/A		—	±30	±60	mV
			DD			—	±30	±80	
		$T_A = \text{Min or Max}$ $T_A = 25^\circ C$			ALL	—	±20	±70	mV
					ALL	—	±10	±50	
Reference Input Bias Current	I_B		ALL	ALL	ALL	—	100	—	nA
Reference Input Impedance	Z_{IN}		ALL	ALL	ALL	—	200	—	MΩ
Reference Input Slew Rate	SR		ALL	ALL	E	—	1.5	—	V/µs
					A	—	2	—	
Reference Output Voltage	V_{REF}		ALL	ALL	ALL	—	6.7	—	Volts
Logic Input Current	I_{IN}	Each Input -5V to (V+ - 0.7)V	ALL	ALL	ALL	—	±1	±10	µA
Logic Input 0	V_{INL}		ALL	ALL	ALL	—	—	0.8	Volts
Logic Input 1	V_{INH}		ALL	ALL	ALL	2	—	—	

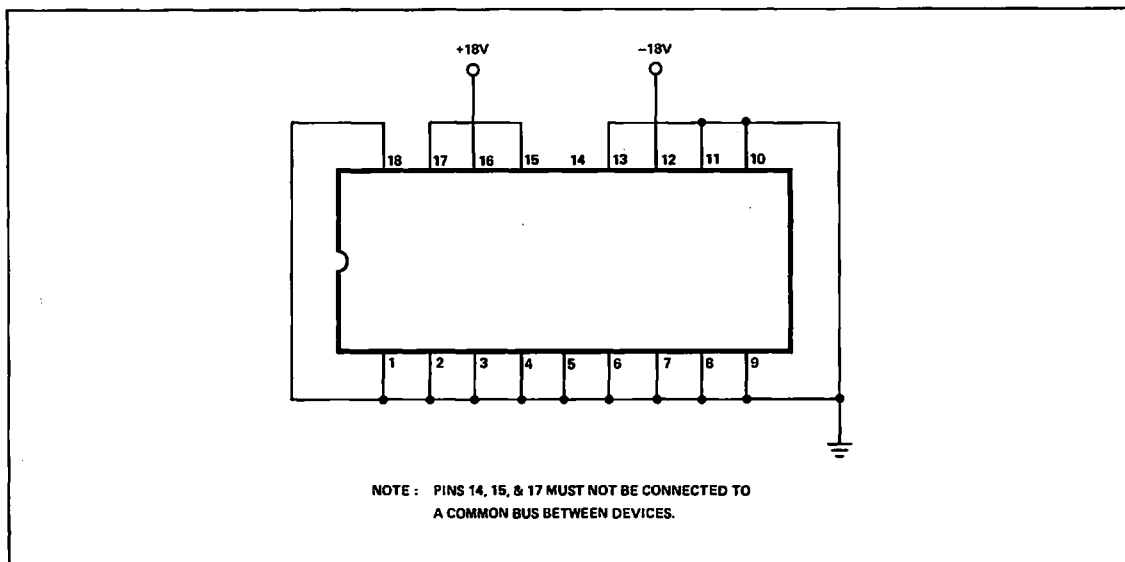


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0 \leq T_A \leq +70^\circ C$ for DAC-02 and DAC-05E, $T_A = 25^\circ C$ for DAC-03 and $-55 \leq T_A \leq +125^\circ C$ for DAC-05A, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-02	DAC-03	DAC-05	MIN	TYP	MAX	UNITS
Positive Supply Current	I^+	SB High. All other logic inputs low.	AC/CC DD	ALL	ALL	—	+7	+10	mA
						—	+7	+11.6	
Negative Supply Current	I^-	SB High. All other logic inputs low.	AC/CC DD	ALL	ALL	—	-9	-10	mA
						—	-9	-11.6	
				ALL		—	-10	-11.6	
Power Supply Sensitivity	P_{SS}	$V_S = \pm 12$ to $\pm 18V$ $T_A = \text{Min to Max}$ $T_A = 25^\circ C$	AC/CC DD	ALL	ALL	—	± 0.015	± 0.05	% V_{FS}/V
						—	± 0.015	± 0.1	
					ALL	—	± 0.05	± 0.1	
					ALL	—	± 0.02	± 0.05	
Power Dissipation	P_d	$I_{OUT} = 0$ $T_A = 25^\circ C$ $T_A = \text{Min to Max}$	AC/CC DD	ALL	ALL	—	225	300	mW
						—	225	350	
					ALL	—	200	300	
					ALL	—	250	350	
Output Drive Current	I_O	Guaranteed by V_{FR} test	ALL	ALL	ALL	—	—	5	mA

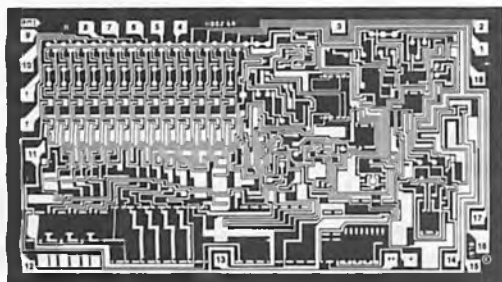
NOTES:

1. Reference output terminal connected directly to reference input terminal, $R_L = 2k\Omega$ for 10V devices, $R_L = 1k\Omega$ for 5V devices, all logic inputs $\geq 2.0V$.
2. Zero-scale symmetry is the change in the output voltage produced by switching the sign-bit with all logic bits low ($V_{ZS+} - V_{ZS-}$).
3. Full-scale bipolar symmetry is the magnitude of the difference between V_{FR+} and $|V_{FR-}|$.
4. Guaranteed by design.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.162 × 0.090 inch; 14,580 sq. mils
(4.114 × 2.286 mm, 9.405 sq. mm)

- | | |
|--------------|--------------------|
| 1. BIT 1-MSB | 10. BIT 10 |
| 2. BIT 2 | 11. DIGITAL GROUND |
| 3. BIT 3 | 12. V- |
| 4. BIT 4 | 13. ANALOG GROUND |
| 5. BIT 5 | 14. ANALOG OUTPUT |
| 6. BIT 6 | 15. REF IN |
| 7. BIT 7 | 16. V+ |
| 8. BIT 8 | 17. REF OUT |
| 9. BIT 9 | 18. SIGN BIT |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

NOTE:

Voltage output range programmable by connecting V_{REF} to analog output for 10 volt range. Jumps from V_{REF} (5V) to analog output for 5 volt range. † Bits 11 & 12 (not normally used)

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$ and +10V full-scale output, unless otherwise noted.

PARAMETER	CONDITIONS	DAC-02-N LIMIT	DAC-02-G LIMIT	UNITS
Resolution (Bits 11 and 12 Not Normally Used)	Bipolar Output	13	13	Bits MAX
	Unipolar Output	12	12	
Monotonicity		9	8	Bits MIN
Nonlinearity		±0.1	±0.2	% FS MAX
Zero-Scale Offset	Sign Bit High, All Other Inputs Low	±10	±10	mV MAX
Zero-Scale Symmetry	±10V Full-Scale	±5	±5	mV MAX
Full-Scale Bipolar Symmetry	±10V Full-Scale	±60	±60	mV MAX
Power Supply Rejection	$V_S = \pm 12V$ to $\pm 18V$	0.05	0.05	% V_{FS}/V MAX
Power Dissipation	$I_{OUT} = 0$	300	300	mW MAX
Logic Input "0"		0.8	0.8	V MAX
Logic Input "1"		2	2	V MIN
Full Range Output Voltage	Sign-Bit	±11.5	±11.5	V MAX
	High or Low	±10	±10	V MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and +10V full-scale output, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-02-N TYPICAL	DAC-02-G TYPICAL	UNITS
Full-Scale Tempco	TCV_{FS}	Internal Reference	60	60	ppm/ $^\circ C$
Settling Time ($T_A = 25^\circ C$)	t_s	To $\pm 1/2$ LSB 10 Volt Step	2	2	μs
Logic Input Current	I_{IN}	$T_A = 25^\circ C$	1	1	μA

NOTE:

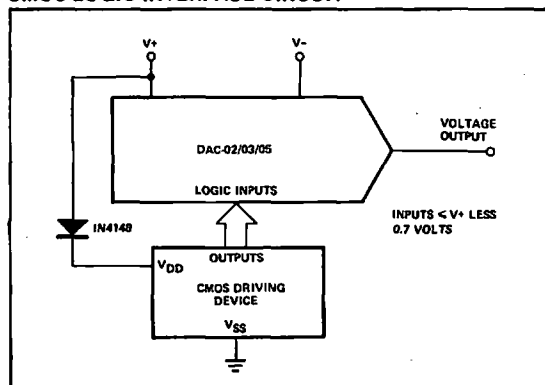
When ordering DICE in this series, use DAC-02 numbers and grades above.

TYPICAL APPLICATIONS

The DAC-02's, DAC-03's and DAC-05's logic input stages require about $1\mu\text{A}$ and are capable of operation with inputs between -5 volts and $V+$ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where the CMOS logic and D/A converter must use the same positive power supply.

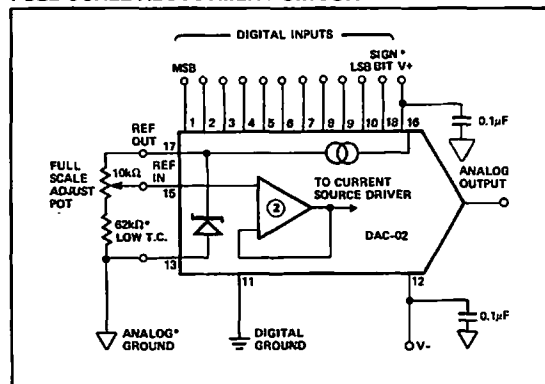
In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 1. The diode limits V_D to $V+$ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-02, DAC-03 and DAC-05 require either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

CMOS LOGIC INTERFACE CIRCUIT



CONNECTION INFORMATION

FULL-SCALE ADJUSTMENT CIRCUIT



FULL-SCALE ADJUSTMENT

Full-scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results

will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of $\leq 72\text{k}\Omega$ may be used.

REFERENCE INPUT BYPASS

Lowest noise and fastest settling operation will be obtained by bypassing the reference input to analog ground with a $0.01\mu\text{F}$ disk capacitor.

GROUNDING

For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably near the DAC-02, DAC-03 and DAC-05 package, so that the large digital currents do not flow through the analog ground path.

APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATIONS

For applications not requiring full 10-bit resolution, unused logic inputs should be tied to ground.

UNIPOLAR OPERATION

Operation as a 10-bit straight binary converter may be implemented by permanently tying the sign-bit to $+5\text{V}$ (for positive full-scale output) or to ground (for negative full-scale output). In the DAC-03 only, Pin 18 unipolar enable is tied to Pin 17.

POWER SUPPLIES

The DAC-02, DAC-03 and DAC-05 will operate within specifications for power supplies ranging from $\pm 12\text{V}$ to $\pm 18\text{V}$. Power supplies should be bypassed near the package with a $0.1\mu\text{F}$ disk capacitor.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF .

REFERENCE OUTPUT

For best results, reference output current should not exceed $100\mu\text{A}$.

USE WITH EXTERNAL REFERENCES

Positive-polarity external reference voltages referred to analog ground may be applied to the reference input terminal to improve full-scale tempco, to provide tracking to other system elements, or to slave a number of DAC-02's, DAC-03's and DAC-05's to the reference output of any one of them. This reference voltage should be between $+5\text{V}$ to $+7\text{V}$ for optimum performance.

SIGN PLUS MAGNITUDE CODING TABLE (DAC-02, DAC-03 and DAC-05)

	SIGN-BIT	MSB										LSB
+ FULL SCALE	1	1	1	1	1	1	1	1	1	1	1	1
+ HALF-SCALE	1	1	0	0	0	0	0	0	0	0	0	0
ZERO-SCALE (+)	1	0	0	0	0	0	0	0	0	0	0	0
ZERO-SCALE (-)	0	0	0	0	0	0	0	0	0	0	0	0
- HALF-SCALE	0	1	0	0	0	0	0	0	0	0	0	0
- FULL-SCALE	0	1	1	1	1	1	1	1	1	1	1	1

FEATURES

- Complete Includes Reference and Op Amp
- Compact..... Single 18-Pin DIP Package
- Bipolar Output Two's Complement Coding
- Monotonicity Guaranteed
- Nonlinearity..... ± 1 LSB
- Fast $1.5\mu s$ Settling Time
- Low Power Consumption 300mW Max
- TTL, CMOS Compatible Inputs

ORDERING INFORMATION†

MONO- TONICITY BITS	PACKAGE 18-PIN HERMETIC DIP	
	MILITARY TEMP	COMMERCIAL TEMP
10		DAC-06EX
9	DAC-06BX*	DAC-06FX

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

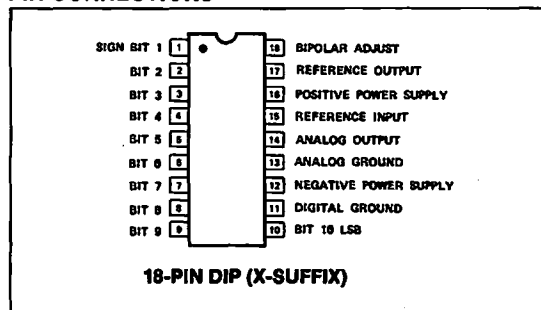
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

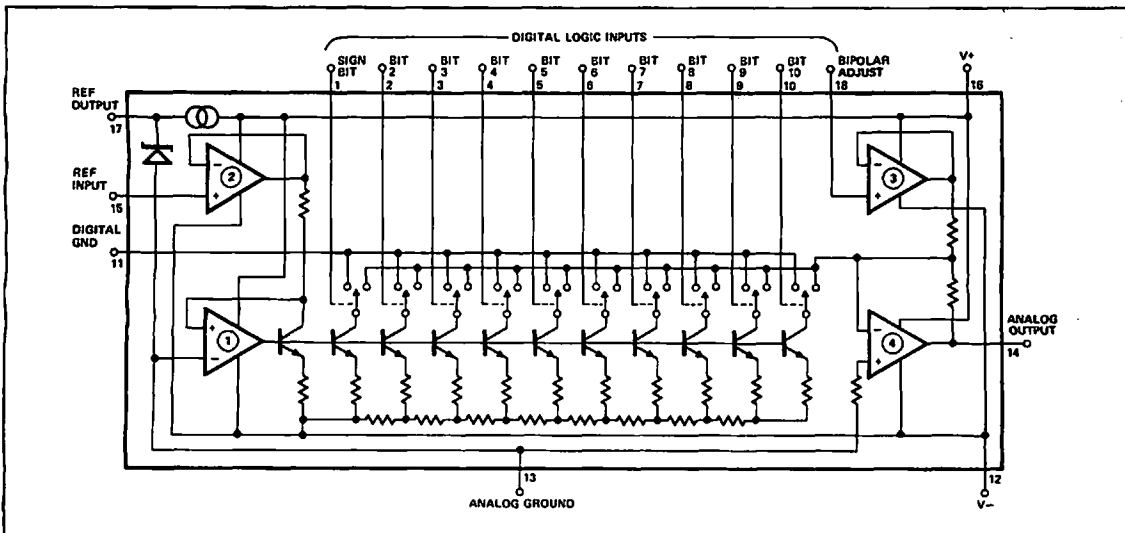
The DAC-06 is a complete 10-bit two's complement D/A converter on a single 90 x 163 mil monolithic chip. All elements of a complete bipolar output two's complement DAC

are included — precision voltage reference, current steering logic, current sources, R-2R resistor network, bipolar offset circuit and high speed internally compensated output op amp. Monotonicity guaranteed over the entire operating temperature range is achieved using an untrimmed diffused R-2R resistor network. The buffered reference input is capable of tracking over a wide range of voltages, increasing application flexibility. The user may also easily implement one's complement, straight offset binary, or unipolar operation. The $\pm 12V$ to $\pm 18V$ power supply range, low power consumption, TTL and CMOS compatibility, wide logic input compatibility and adaptable logic coding capability assure utility in a wide range of applications.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature Range

DAC-06B -55°C to +125°C

DAC-06E, F 0°C to +70°C

DICE Junction Temperature (T_j) -65°C to +150°C

Storage Temperature Range -65°C to +150°C

V+ Supply to Analog Ground 0 to +18V

V- Supply to Analog Ground 0 to -18V

Analog Ground to Digital Ground 0 to $\pm 0.5V$

Logic Inputs to Digital Ground -5V to (V+ - 0.7)V

Internal Reference Output Current 300 μ A

Reference Input Voltage 0 to +10V

Bipolar Offset Input Voltage 0 to +10V

Internal Power Dissipation 500mW

Lead Temperature (Soldering, 60 sec) 300°C

Output Short-Circuit Duration Indefinite

(Short circuit may be to ground or either supply)

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; -55°C $\leq T_A \leq +125^\circ C$ for DAC-06B; and 0°C $\leq T_A \leq +70^\circ C$ for DAC-06E & F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-06	MIN	TYP	MAX	UNITS
Resolution			All	10	—	—	Bits
Monotonicity			E	10	—	—	Bits
			B/F	9	—	—	
Nonlinearity	NL	$T_A = 25^\circ C$	E	—	—	± 0.1	% FS
			B/F	—	—	± 0.2	
		$T_A = \text{Full Temp.}$	E	—	—	± 0.2	% FS
			B/F	—	—	± 0.3	
Full-Scale Tempco	TCV_{FS}	Total Internal Ref Connected	B	—	± 45	± 90	ppm/ $^\circ C$
			E/F	—	± 45	± 100	
		Zero Drift Ext Ref Applied	All	—	± 30	—	ppm/ $^\circ C$
Settling Time	t_S	To $\pm 1/2$ LSB, 10V Step	All	—	1.5	—	μs
Unipolar Zero-Scale Output	V_{ZS}	Short Pin 18 to $T_A = 25^\circ C$	All	—	± 1	± 5	mV
		Ground (Note 1) $T_A = \text{Full Temp.}$	All	—	± 2	± 10	
Bipolar Offset Voltage	BP Off	Connect Pins 15, 17 & 18 (Note 3)	All	-5	—	+2.5	% Range
Full Range Output Voltage	V_{FR}	Connect Pin 15 to 17 (Note 2) $R_L = 2k\Omega$	All	10	—	11.5	V
Reference Input Bias Current	I_B		All	—	100	—	nA
Reference Input Impedance	Z_{IN}		All	—	200	—	M Ω
Reference Input Slew Rate	SR		All	—	1.5	—	V/ μs
Reference Output Voltage	V_{REF}		All	—	6.7	—	V
Logic Input Current	I_{IN}	Each Input -5V to (V+ - 0.7)V	All	—	1	10	μA
Logic Input "0"	V_{INL}		All	—	—	0.8	V
Logic Input "1"	V_{INH}		All	2	—	—	V
Power Supply Sensitivity	P_{SS}	$V_S = \pm 12V$ to $\pm 18V$ $T_A = 25^\circ C$	All	—	± 0.02	± 0.05	% FS/V
		$T_A = \text{Full Temp.}$	All	—	± 0.02	± 0.1	
Supply Current	I^+ I^-	$T_A = 25^\circ C$	All	—	7	10	mA
			All	—	-9	-10	
Power Dissipation	P_D	$T_A = 25^\circ C$	All	—	250	300	mW
		$T_A = \text{Full Temp.}$	All	—	—	350	

NOTES:

- May be operated in the 0 to +10V unipolar mode by shorting Pin 18 to Ground.
- $V_{FR} = |V_{FR}^+| + |V_{FR}^-|$ and is trimmable to exactly 10V range with the circuit shown in typical applications.
- Bipolar offset voltage is trimmable to exact two's or one's complement condition with the circuit shown in typical applications.



TYPICAL APPLICATIONS

ADJUSTING FOR TWO'S COMPLEMENT CODING

1. Connect Full-Scale Adjust and Bipolar Adjust Circuitry as shown in figure.
2. Turn all bits OFF ($V_{FS-} - 1\text{LSB}$) = 1000000000
3. Adjust Bipolar Pot for V_{FS-} at output -5.000V
4. Turn all bits ON (V_{FR+}) = 0111111111
5. Adjust Full-Scale Pot for desired V_{FR+} value +4.990V
6. Check Zero-Scale Reading (V_{ZS}) = 0000000000
If this reading is outside desired V_{ZS} range, readjust Bipolar Pot until the output reads 0.0000V.

TWO'S COMPLEMENT CODING TABLE

	INPUT										IDEAL OUTPUT
	MSB					LSB					
$V_{FS+} - 1\text{LSB}$	0	1	1	1	1	1	1	1	1	1	+4.990V
$V_{FS+} - 2\text{LSB}$	0	1	1	1	1	1	1	1	1	0	+4.980V
+1LSB	0	0	0	0	0	0	0	0	0	1	+0.010V
Zero	0	0	0	0	0	0	0	0	0	0	0.000V
-1LSB	1	1	1	1	1	1	1	1	1	1	-0.010V
$V_{FS-} + 1\text{LSB}$	1	0	0	0	0	0	0	0	0	1	-4.990V
V_{FS-}	1	0	0	0	0	0	0	0	0	0	-5.000V

ADJUSTING FOR ONE'S COMPLEMENT CODING

1. Connect Full-Scale Adjust and Bipolar Adjust Circuitry as shown in above figure.
2. Turn all bits OFF (V_{FR-}) = 1000000000
3. Adjust Bipolar Pot for V_{FR-} at output -5.0000V
4. Turn all bits ON (V_{FR+}) = 0111111111
5. Adjust Full-Scale Pot for desired V_{FR+} value +5.0000V

ONE'S COMPLEMENT CODING TABLE

	INPUT										IDEAL OUTPUT
	MSB					LSB					
$V_{FS+} - 1\text{LSB}$	0	1	1	1	1	1	1	1	1	1	+5.000V
$V_{FS+} - 2\text{LSB}$	0	1	1	1	1	1	1	1	1	0	+4.990V
+0	0	0	0	0	0	0	0	0	0	0	+0.005V
-0	1	1	1	1	1	1	1	1	1	1	-0.005V
$V_{FS-} + 2\text{LSB}$	1	0	0	0	0	0	0	0	0	1	-4.990V
$V_{FS-} + 1\text{LSB}$	1	0	0	0	0	0	0	0	0	0	-5.000V

Note that two zero states will straddle ($\pm 1/2 \text{ LSB}$) the true zero. Therefore the DAC will give symmetrical outputs for both positive and negative full-scale.

REFERENCE OUTPUT

For best results, reference output current should not exceed $100\mu\text{A}$.

POWER SUPPLIES

The DAC-06 will operate within specifications for power supplies ranging from $\pm 12\text{V}$ to $\pm 18\text{V}$. Power supplies should be bypassed near the package with a $0.1\mu\text{F}$ disk capacitor. Chip users should connect the substrate to V_{-} .

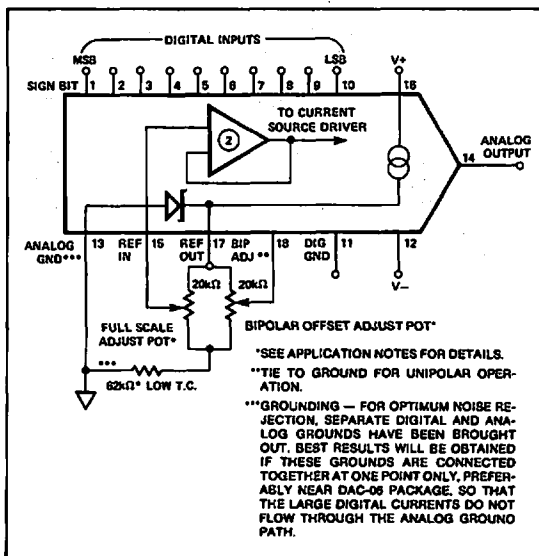
GROUNDING

For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the DAC-06 package, so that large digital currents do not flow through the analog ground path.

CAPACITIVE LOADING

The output operational amplifier provides stable operation with capacitive loads up to 100pF .

FULL-SCALE OUTPUT RANGE AND BIPOLAR OFFSET ADJUSTMENT CIRCUIT



EXTERNAL ADJUSTMENT NETWORK

Full-scale output range and bipolar offset may be adjusted by using the circuit shown in the figure above. Best results will be obtained when low tempco pots and resistors are used, or if pot and resistor tempcos match.

CODE CONVERSION TO OFFSET BINARY

Offset binary coding is exactly the same as two's complement coding except that the most significant bit occurs in true, rather than inverted form and the output states are relabeled. To convert the DAC-06 to offset binary code operation, simply place a logic inverter in series with the MSB input (Pin 1) and invert the MSB value shown in steps 2, 4 and 6 of the two's complement adjustment procedure shown above.

OFFSET BINARY CODING TABLE

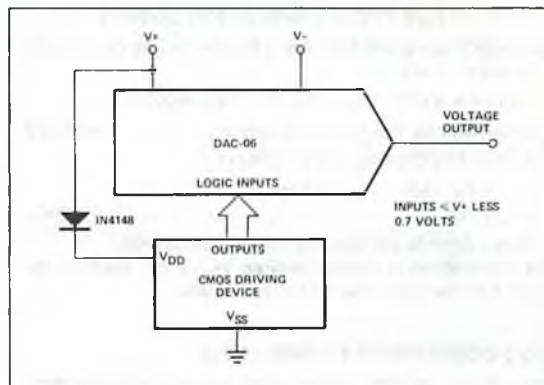
	INPUT										IDEAL OUTPUT
	MSB					LSB					
$V_{FS+} - 1LSB$	1	1	1	1	1	1	1	1	1	1	+4.990V
$V_{FS+} - 2LSB$	1	1	1	1	1	1	1	1	1	0	+4.980V
ZERO	1	0	0	0	0	0	0	0	0	0	0.00
-1LSB	0	1	1	1	1	1	1	1	1	1	-0.005V
$V_{FS-} + 1LSB$	0	0	0	0	0	0	0	0	0	1	-4.990V
V_{FS-}	0	0	0	0	0	0	0	0	0	0	-5.000V

INTERFACING WITH CMOS LOGIC

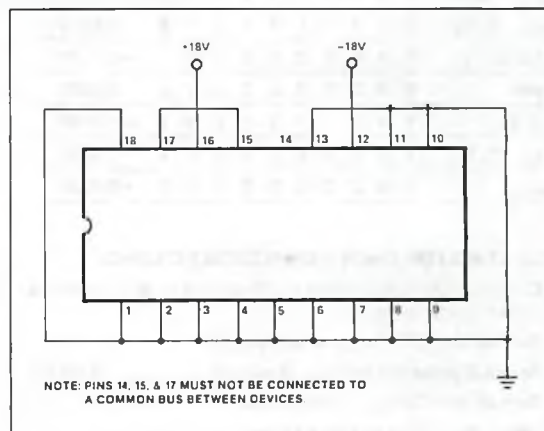
The DAC-06 logic input stages require about $1\mu\text{A}$ and are capable of operation with inputs between -5 volts and $V+ \text{ less } 0.7$ volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where the CMOS logic and D/A converter must use the same positive power supply.

In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 1. The diode limits V_D to $V+ \text{ less } 0.7$ volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-06 requires either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

CMOS LOGIC INTERFACE CIRCUIT



BURN-IN CIRCUIT





DAC-08

8-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER (UNIVERSAL DIGITAL LOGIC INTERFACE)

Precision Monolithics Inc.

FEATURES

- Fast Settling Output Current 85ns
- Full-Scale Current Prematched to ± 1 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to 0.1% Maximum Over Temperature Range
- High Output Impedance and Compliance -10V to +18V
- Complementary Current Outputs
- Wide Range Multiplying Capability ... 1MHz Bandwidth
- Low FS Current Drift $\pm 10\text{ppm}/^\circ\text{C}$
- Wide Power Supply Range $\pm 4.5\text{V}$ to $\pm 18\text{V}$
- Low Power Consumption 33mW @ $\pm 5\text{V}$
- Low Cost

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic digital-to-analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full-scale trimming in most applications. Direct

interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic input.

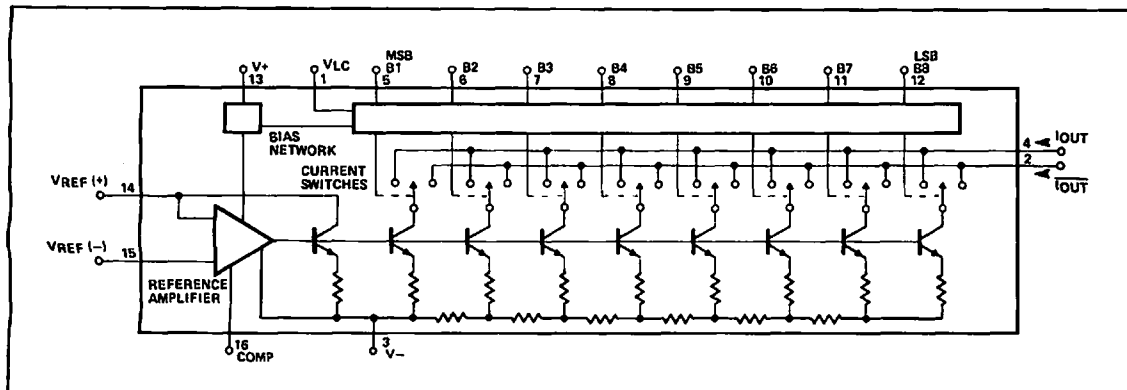
High voltage compliance complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as $\pm 0.1\%$ over the entire operating temperature range are available. Device performance is essentially unchanged over the ± 4.5 to $\pm 18\text{V}$ power supply range, with 33mW power consumption attainable at $\pm 5\text{V}$ supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications; devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, $1\mu\text{s}$ A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



DIGITAL-TO-ANALOG CONVERTERS

11



ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
DAC-08AQ, Q	-55°C to +125°C
DAC-08HQ, EQ, CQ, HP, EP, CP, CS	0°C to +70°C
DICE Junction Temperature (T _J)	-65°C to +150°C
Storage Temperature Q Package	-65°C to +150°C
Storage Temperature P Package	-65°C to +125°C
Power Dissipation	500mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C
V+ Supply to V- Supply	36V

Logic Inputs	V- to V- plus 36V
V _{LC}	V- to V+
Analog Current Outputs (at V _S = 15V)	4.25mA
Reference Input (V ₁₄ to V ₁₅)	V- to V+
Reference Input Differential Voltage (V ₁₄ to V ₁₅)	±18V
Reference Input Current (I ₁₄)	5.0mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, I_{REF} = 2.0mA, -55°C ≤ T_A ≤ +125°C for DAC-08/08A, 0°C ≤ T_A ≤ +70°C for DAC-08C, E & H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-08A/H			DAC-08E			DAC-08C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			8	—	—	8	—	—	8	—	—	Bits
Monotonicity			8	—	—	8	—	—	8	—	—	Bits
Nonlinearity	NL		—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time	t _S	To ±1/2 LSB, all bits switched ON or OFF, T _A = 25°C, (Note)	—	85	135	—	85	150	—	85	150	ns
Propagation Delay												
Each bit	t _{PLH}	T _A = 25°C	—	35	60	—	35	60	—	35	60	ns
All bits switched	t _{PHL}	(Note)	—	35	60	—	35	60	—	35	60	ns
Full-Scale Tempco (Note)	TC _{IFS}	DAC-08E	—	±10	±50	—	±10	±80	—	±10	±80	ppm/°C
Output Voltage Compliance (True Compliance)	V _{OC}	Full-Scale current change < 1/2 LSB, R _{OUT} > 20MΩ typical	-10	—	+18	-10	—	+18	-10	—	+18	V
Full Range Current	I _{FR4}	V _{REF} = 10.000V R ₁₄ , R ₁₅ = 5.000kΩ T _A = +25°C	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I _{FRS}	I _{FR4} - I _{FR2}	—	±0.5	±4	—	±1	±8	—	±2	±16	μA
Zero-Scale Current	I _{ZS}		—	0.1	1	—	0.2	2	—	0.2	4	μA
Output Current Range	I _{OR1} I _{OR2}	R ₁₄ , R ₁₅ = 5.000kΩ V _{REF} = +15.0V, V- = -10V V _{REF} = +25.0V, V- = -12V	2.1	—	—	2.1	—	—	2.1	—	—	mA
Output Current Noise		I _{REF} = 2mA	—	25	—	—	25	—	—	25	—	nA
Logic Input Levels												
Logic "0"	V _{IL}	V _{LC} = 0V	—	—	0.8	—	—	0.8	—	—	0.8	V
Logic Input "1"	V _{IH}		2	—	—	2	—	—	2	—	—	V
Logic Input Current												
Logic "0"	I _{IL}	V _{LC} = 0V V _{IN} = -10V to +0.8V	—	-2	-10	—	-2	-10	—	-2	-10	μA
Logic Input "1"	I _{IH}	V _{IN} = 2.0V to 18V	—	0.002	10	—	0.002	10	—	0.002	10	μA
Logic Input Swing	V _{IS}	V- = -15V	-10	—	+18	-10	—	+18	-10	—	+18	V
Logic Threshold Range	V _{THR}	V _S = ±15V, (Note)	-10	—	+13.5	-10	—	+13.5	-10	—	+13.5	V
Reference Bias Current	I ₁₅		—	-1	-3	—	-1	-3	—	-1	-3	μA
Reference Input Slew Rate	dI/dt	R _{EO} = 200Ω See fast pulsed R _L = 100Ω ref. info. C _C = 0pF following, (Note)	4	8	—	4	8	—	4	8	—	mA/μs
Power Supply Sensitivity	PSSI _{FS+} PSSI _{FS-}	V+ = 4.5V to 18V V- = -4.5V to -18V I _{REF} = 1.0mA	—	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	%ΔV _O /%ΔV ₊ %ΔV _O /%ΔV ₋

NOTE: Guaranteed by design.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $-55^\circ C \leq T_A \leq +125^\circ C$ for DAC-08/08A, $0^\circ C \leq T_A \leq +70^\circ C$ for DAC-08C, E & H, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\bar{I}_{OUT}$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-08A/H			DAC-08E			DAC-08C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Power Supply Current	I+	$V_S = \pm 5V$, $I_{REF} = 1.0mA$	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	mA
	I-		—	-4.3	-5.8	—	-4.3	-5.8	—	-4.3	-5.8	
	I+	$V_S = +5V$, $-15V$, $I_{REF} = 2.0mA$	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
	I-		—	-8.4	-7.8	—	-8.4	-7.8	—	-8.4	-7.8	
	I+	$V_S = \pm 15V$, $I_{REF} = 2.0mA$	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
	I-		—	-8.5	-7.8	—	-8.5	-7.8	—	-8.5	-7.8	
Power Dissipation	P_d	$\pm 5V$, $I_{REF} = 1.0mA$	—	33	48	—	33	48	—	33	48	mW
		$+5V$, $-15V$, $I_{REF} = 2.0mA$	—	108	138	—	103	138	—	108	138	
		$\pm 15V$, $I_{REF} = 2.0mA$	—	135	174	—	135	174	—	135	174	

NOTE: Guaranteed by design.

ORDERING INFORMATION†

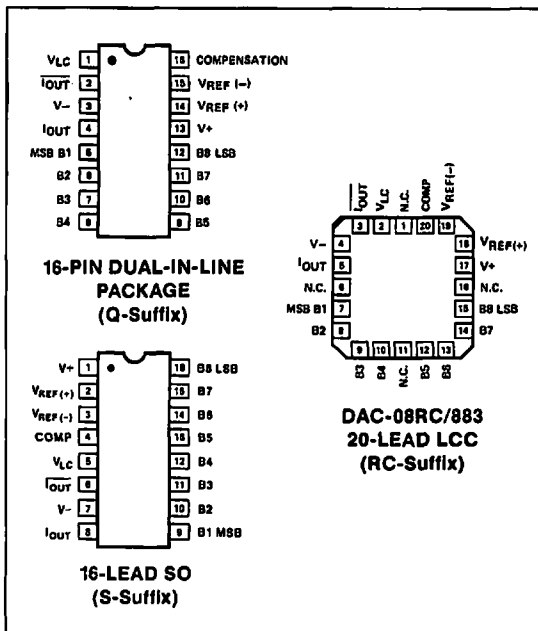
NL	18-PIN DUAL-IN-LINE PACKAGE			OPERATING TEMPERATURE RANGE
	HERMETIC	PLASTIC	LCC	
0.1%	DAC08AQ*	—	—	MIL
	DAC08HQ	DAC08HP	—	COM
0.18%	DAC08Q*	—	DAC08RC/883	MIL
	DAC08EQ	DAC08EP	—	COM
0.38%	DAC08CQ	DAC08CP	—	—
	—	DAC08CS††	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

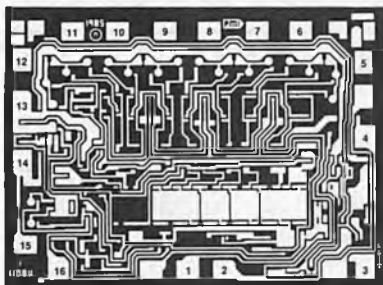
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS





DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.087 × 0.063 inch, 5,270 sq. mils
(2.209 × 1.601 mm, 3.54 sq. mm)

- | | |
|----------------|-------------------|
| 1. V_{LC} | 9. BIT 5 |
| 2. I_{OUT} | 10. BIT 6 |
| 3. V^- | 11. BIT 7 |
| 4. I_{OUT} | 12. BIT 8 (LSB) |
| 5. BIT 1 (MSB) | 13. V^+ |
| 6. BIT 2 | 14. $V_{REF} (+)$ |
| 7. BIT 3 | 15. $V_{REF} (-)$ |
| 8. BIT 4 | 16. COMP |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

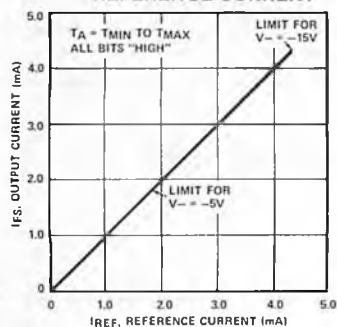
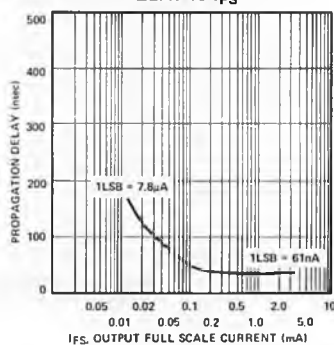
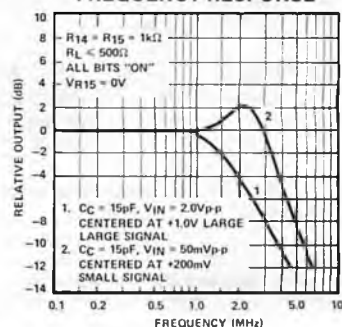
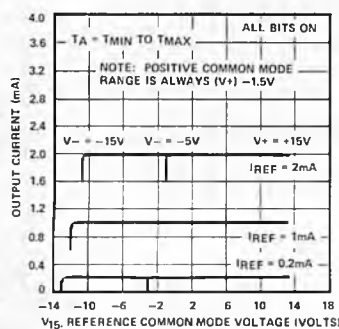
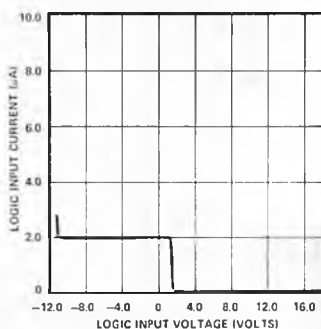
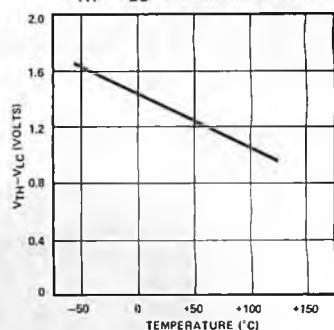
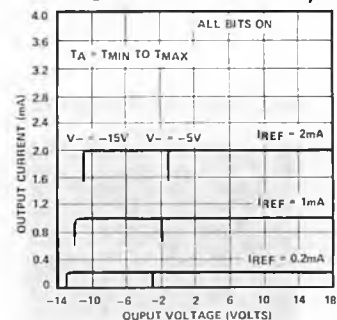
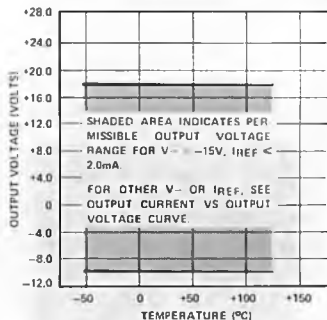
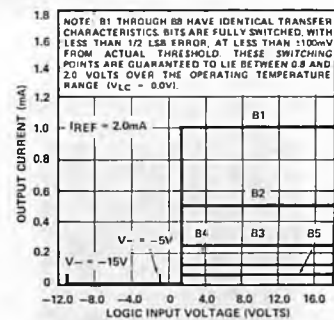
WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 125^\circ C$ for DAC-08NT, DAC-08GT devices; $T_A = 25^\circ C$ for DAC-08N, DAC-08G and DAC-08GR devices, unless otherwise noted. Output characteristics apply to both I_{OUT} and I_{OUT} .

PARAMETER	SYMBOL	CONDITIONS	DAC-08NT LIMIT	DAC-08N LIMIT	DAC-08GT LIMIT	DAC-08G LIMIT	DAC-08GR LIMIT	UNITS
Resolution			8	8	8	8	8	Bits MIN
Monotonicity			8	8	8	8	8	Bits MIN
Nonlinearity	NL		± 0.1	± 0.1	± 0.19	± 0.19	± 0.39	%FS MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change < 1/2 LSB	∓ 18 -10	$+18$ -10	$+18$ -10	$+18$ -10	$+18$ -10	V MAX V MIN
Full-Scale Current	I_{FS4} or I_{FS2}	$V_{REF} = 10.000V$ $R_{14}, R_{15} = 5.000k\Omega$	2.04 1.94	2.04 1.94	2.04 1.94	2.04 1.94	2.04 1.94	mA MAX mA MIN
Full-Scale Symmetry	I_{FS5}		± 8	± 8	± 8	± 8	± 16	μA MAX
Zero-Scale Current	I_{ZS}		2	2	4	4	4	μA MAX
Output Current Range	I_{FS1} or	$V^- = -10V$, $V_{REF} = +15V$	2.1	2.1	2.1	2.1	2.1	mA MIN
	I_{FS2}	$V^- = -12V$, $V_{REF} = +25V$ $R_{14}, R_{15} = 5.000k\Omega$	4.2	4.2	4.2	4.2	4.2	mA MIN
Logic Input "0"	V_{IL}		0.8	0.8	0.8	0.8	0.8	V MAX
Logic Input "1"	V_{IH}		2	2	2	2	2	V MIN
Logic Input Current		$V_{LC} = 0V$						
Logic "0"	I_{IL}	$V_{IN} = -10V$ to $+0.8V$	± 10	± 10	± 10	± 10	± 10	μA MAX
Logic "1"	I_{IH}	$V_{IN} = 2.0V$ to $18V$	± 10	± 10	± 10	± 10	± 10	μA MAX
Logic Input Swing	V_{IS}	$V^- = -15V$	$+18$ -10	$+18$ -10	$+18$ -10	$+18$ -10	$+18$ -10	V MAX V MIN
Reference Bias Current	I_{15}		-3	-3	-3	-3	-3	μA MAX
Power Supply Sensitivity	$PSSI_{FS+}$, $PSSI_{FS-}$	$V^+ = 4.5V$ to $18V$ $V^- = -4.5V$ to $-18V$ $I_{REF} = 1.0mA$	0.01	0.01	0.01	0.01	0.01	%FS/%V MAX
Power Supply Current	I^+	$V_S = \pm 15V$ $I_{REF} \leq 2.0mA$	3.8 -7.8	3.8 -7.8	3.8 -7.8	3.8 -7.8	3.8 -7.8	mA MAX
Power Dissipation	P_d	$V_S = \pm 15V$ $I_{REF} \leq 2.0mA$	174	174	174	174	174	mW MAX

NOTE:

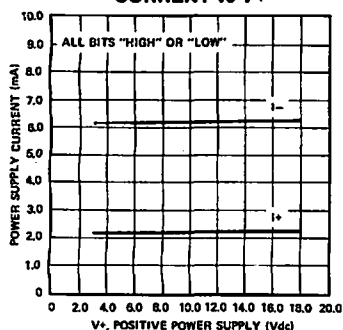
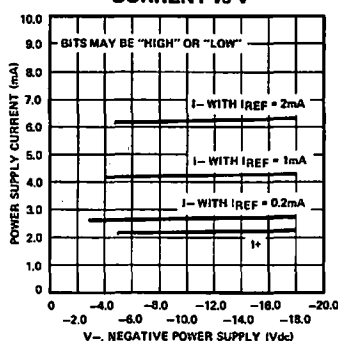
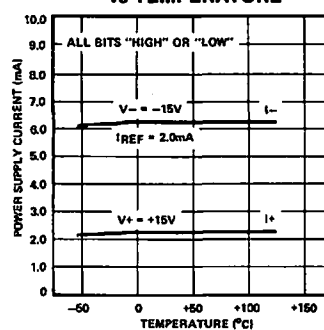
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

FULL-SCALE CURRENT vs
REFERENCE CURRENTLSB PROPAGATION
DELAY vs I_{FS} REFERENCE INPUT
FREQUENCY RESPONSEREFERENCE AMP
COMMON-MODE RANGELOGIC INPUT CURRENT vs
INPUT VOLTAGE $V_{TH} - V_{LC}$ vs TEMPERATUREOUTPUT CURRENT vs
OUTPUT VOLTAGE (OUTPUT
VOLTAGE COMPLIANCE)OUTPUT VOLTAGE COMPLIANCE
vs TEMPERATUREBIT TRANSFER
CHARACTERISTICS

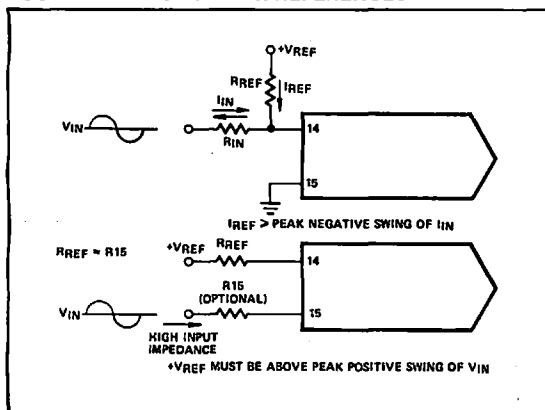


TYPICAL PERFORMANCE CHARACTERISTICS

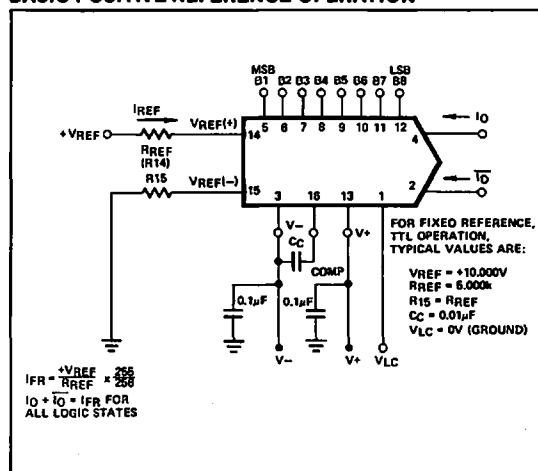
POWER SUPPLY
CURRENT vs V_+ POWER SUPPLY
CURRENT vs V_- POWER SUPPLY CURRENT
vs TEMPERATURE

BASIC CONNECTIONS

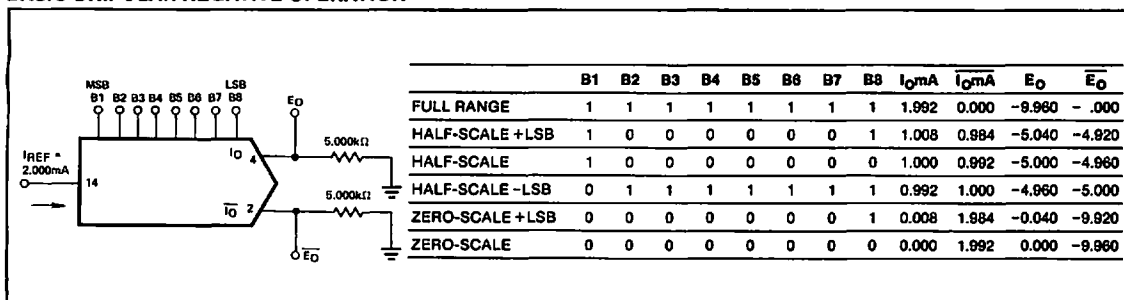
ACCOMODATING BIPOLAR REFERENCES



BASIC POSITIVE REFERENCE OPERATION

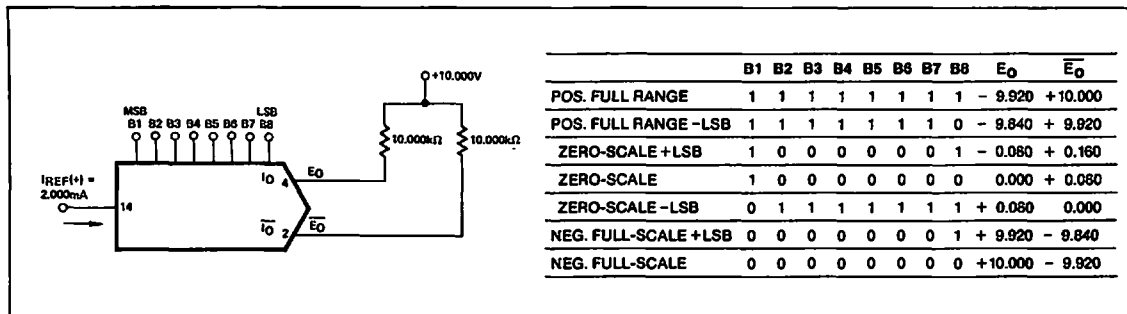


BASIC UNIPOLAR NEGATIVE OPERATION

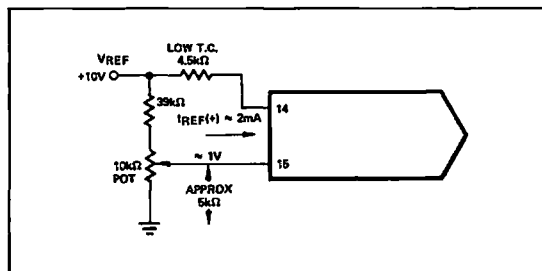


BASIC CONNECTIONS

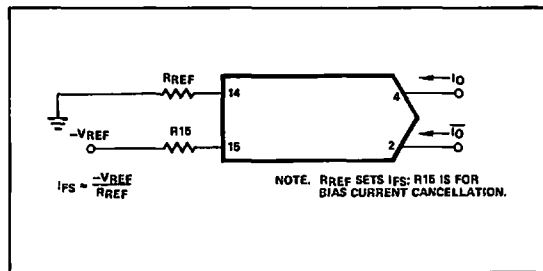
BASIC BIPOLAR OUTPUT OPERATION



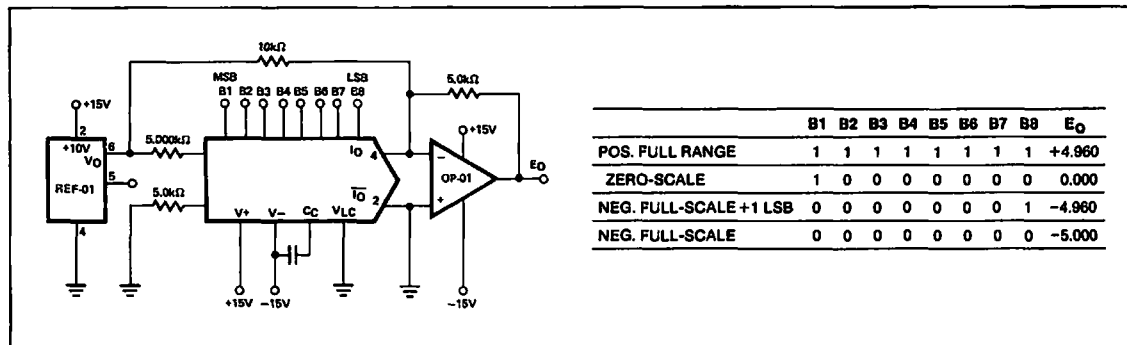
RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



BASIC NEGATIVE REFERENCE OPERATION

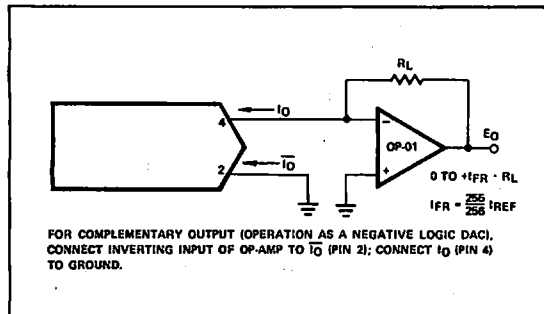


OFFSET BINARY OPERATION

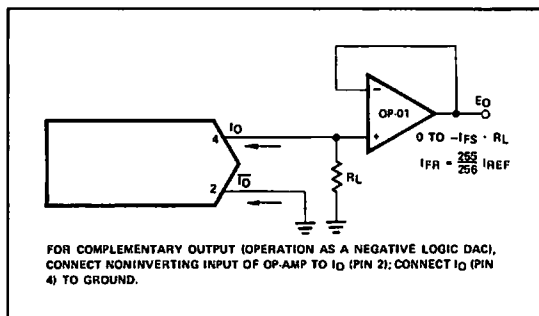


BASIC CONNECTIONS

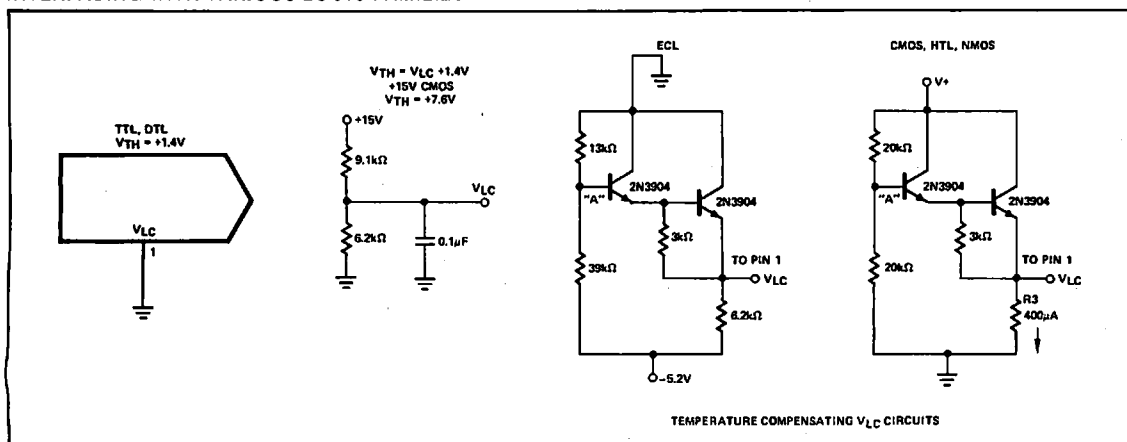
POSITIVE LOW IMPEDANCE OUTPUT OPERATION



NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



INTERFACING WITH VARIOUS LOGIC FAMILIES



APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SET-UP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF}, \text{ where } I_{REF} = I_{14}.$$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15; reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin

15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V_-$ plus $(I_{REF} \times 1k\Omega)$ plus 2.5V. The positive common-mode range is V_+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF} . If required, full-scale trimming may be accomplished by adjusting the value of R_{14} , or by using a potentiometer for R_{14} . An improved

method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full-scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V-. The value of this capacitor depends on the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0k Ω , minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin, such that the ratio of C_C (pF) to R_{14} (k Ω) = 15.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For $R_{14} = 1\text{k}\Omega$ and $C_C = 15\text{pF}$, the reference amplifier slews at 4mA/ μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2\text{mA}$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 14 is 200 Ω and $C_C = 0$. This yields a reference slew rate of 16mA/ μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2 μA logic input current and completely adjustable logic threshold voltage. For $V_- = -15\text{V}$, the logic inputs may swing between -10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V_- plus ($I_{REF} \times 1\text{k}\Omega$) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC} . For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an $I_{REF} = 1\text{mA}$ is recommended. For interfacing other logic families, see preceding page. For general set-up of the logic control circuit, it should be noted that pin 1 will source 100 μA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1k Ω divider, for example, it should be bypassed to ground by a 0.01 μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \bar{I}_O = I_{FS}$. Current appears at the "true" (I_O) output when a "1" (logic high) is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\bar{I}_O$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must be connected to ground or to a point capable of sourcing I_{FS} ; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V_- and is independent of the positive supply. Negative compliance is given by V_- plus ($I_{REF} \times 1\text{k}\Omega$) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of $\pm 5\text{V}$ or less, $I_{REF} \leq 1\text{mA}$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -4.5V with $I_{REF} = 2\text{mA}$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

$P_d = (I_+) (V_+) + (I_-) (V_-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is low, typically $\pm 10\text{ppm}/^\circ\text{C}$, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for min-

imum overall full-scale drift. Settling times of the DAC-08 decrease approximately 10% at -55°C ; at $+125^{\circ}\text{C}$ an increase of about 15% is typical.

The reference amplifier must be compensated by using a capacitor from pin 16 to V_{-} . For fixed reference operation, a $0.01\mu\text{F}$ capacitor is recommended. For variable reference applications, see previous section entitled "Reference Amplifier Compensation for Multiplying Applications".

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to $4\mu\text{A}$. Monotonic operation is maintained over a typical range of I_{REF} from $100\mu\text{A}$ to 4.0mA .

SETTLING TIME

The DAC-08 is capable of extremely fast settling times, typically 85ns at $I_{\text{REF}} = 2.0\text{mA}$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within $1/2$ LSB of the LSB is therefore 35ns , with each progressively larger bit taking successively longer. The MSB settles in 85ns , thus determining the overall settling time of 85ns . Settling to 6-bit accuracy requires about 65 to 70ns . The output capacitance of the DAC-08 including the package is approximately 15pF , therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive

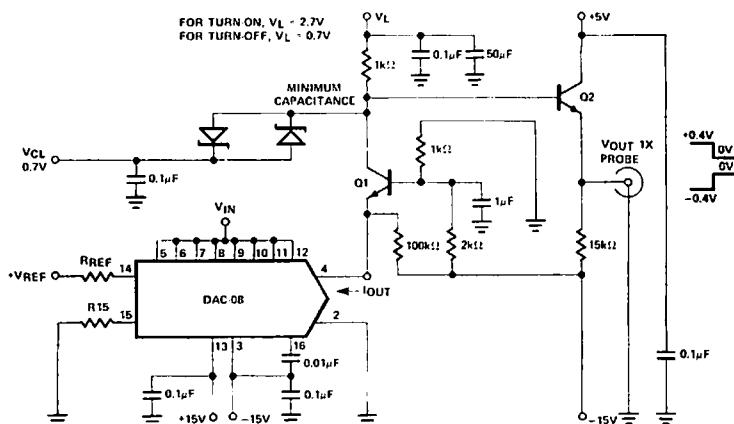
to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve $\pm 4\mu\text{A}$, therefore a $1\text{k}\Omega$ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture shown in schematic labelled "Settling Time Measurement" uses a cascode design to permit driving a $1\text{k}\Omega$ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1.0mA , excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within $\pm 0.2\%$ of the final value, and thus settling times may be observed at lower values of I_{REF} .

DAC-08 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; $0.1\mu\text{F}$ capacitors at the supply pins provide full transient protection.

SETTLING TIME MEASUREMENT





DAC-10

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER (UNIVERSAL DIGITAL LOGIC INTERFACE)

Precision Monolithics Inc.

FEATURES

- Fast Settling 85ns
- Low Full-Scale Drift 10ppm/°C
- Nonlinearity to 0.05% Max Over Temp Range
- Complementary Current Outputs 0 to 4mA
- Wide Range Multiplying Capability ... 1MHz Bandwidth
- Wide Power Supply Range .. +5, -7.5 Min to ±18V Max
- Direct Interface to TTL, CMOS, ECL, PMOS, NMOS

ORDERING INFORMATION†

NL LSB	18-PIN HERMETIC DUAL-IN-LINE PACKAGE	
	MILITARY TEMP.	COMMERCIAL TEMP.
±1/2	DAC10B*	DAC10FX
±1	DAC10CX	DAC10GX

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The DAC-10 series of 10-bit monolithic multiplying digital-to-analog converters provide high-speed performance and full-scale accuracy.

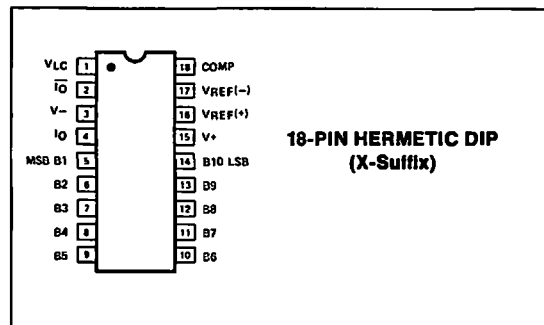
Advanced circuit design achieves 85ns settling times with very low 'glitch' energy and low power consumption. Direct interface to all-popular logic families with full noise immunity is provided by the high-swing, adjustable-threshold logic inputs.

All DAC-10 series models guarantee full 10-bit monotonicity, and nonlinearities as tight as $\pm 0.05\%$ over the entire operating temperature range are available. Device performance is essentially unchanged over the $\pm 18V$ power supply range, with 85mW power consumption attainable at lower supplies.

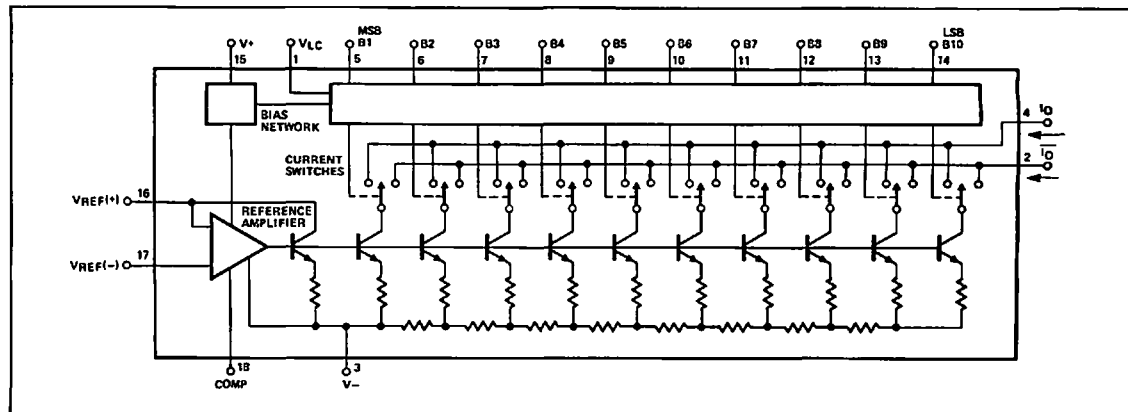
A highly stable, unique trim method is used, which selectively shorts zener diodes, to provide 1/2 LSB full-scale accuracy without the need for laser trimming.

Single-chip reliability coupled with low cost and outstanding flexibility make the DAC-10 device an ideal building block for A/D converters, Data Acquisition systems, CRT display, programmable test equipment, and other applications where low power consumption, input/output versatility, and long-term stability are required.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC





ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
DAC-10BX, CX	-55°C to +125°C
DAC-10FX, GX	0°C to +70°C
DICE Junction Temperature (T_J)	-65°C to +150°C
Storage Temperature	-65°C to +150°C
Power Dissipation	500mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C
V+ Supply to V- Supply	36V

Logic Inputs	V- to V- plus 36V
V_{LC}	V- to V+
Analog Current Outputs	+18V to -18V
Reference Inputs (V_{16} to V_{17})	V- to V+
Reference Input Differential Voltage (V_{16} to V_{17})	±18V
Reference Input Current (I_{16})	2.5mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $I_{REF} = 2mA$; $-55^\circ C \leq T_A \leq 125^\circ C$ for DAC-10B and DAC-10C, $0^\circ C \leq T_A \leq 70^\circ C$ for DAC-10F and G, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-10B/F			DAC-10C/G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Monotonicity			10	—	—	10	—	—	Bits
Nonlinearity	NL		—	0.3	0.5	—	0.6	1	LSB
Differential Nonlinearity	DNL		—	0.3	1	—	0.7	—	LSB
Settling Time	t_s	All Bits Switched ON or OFF Settle to 0.05% of FS (See Note)	—	85	135	—	85	150	ns
Output Capacitance	C_O		—	18	—	—	18	—	pF
Propagation Delay	t_{PLH} t_{PHL}	All Bits Switched $R_L = 5k\Omega$ $R_L = 0$	—	50	—	—	50	—	ns
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1 LSB	—	-5.5	—	—	-5.5	—	V
Gain Tempco	TCI_{FS}	(See Note)	—	±10	±25	—	±10	±50	ppm/°C
Full-Scale Symmetry	I_{FSS}	$I_{FR} - \overline{I_{FR}}$	—	0.1	4	—	0.1	4	μA
Zero-Scale Current	I_{ZS}		—	0.01	0.5	—	0.01	0.5	μA
Full-Scale Current	I_{FR}	(See Note)	3.960	3.996	4.032	3.920	3.996	4.072	mA
Reference Input Slew Rate	DI/dt		—	6	—	—	6	—	mA/μs
Reference Bias Current	I_B		—	-1	-3	—	-1	-3	μA
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	$4.5V \leq V+ \leq 18V$ $-18V \leq V- \leq -10V$	—	0.001	0.01	—	0.001	0.01	% ΔI_{FS} /% ΔV
Power Supply Current	$I+$	$V_S = \pm 15V$; $I_{REF} = 2mA$	—	2.3	4	—	2.3	4	mA
	$I-$		—	-9	-15	—	-9	-15	
	$I+$	$V_S = +5V, -7.5V$; $I_{REF} = 1mA$	—	1.8	4	—	1.8	4	
	$I-$		—	-5.9	-9	—	-5.9	-9	
Power Dissipation	P_d	$V_S = \pm 15V$; $I_{REF} = 2mA$	—	231	285	—	231	285	mW
		$V_S = +5V, -7.5V$; $I_{REF} = 1mA$	—	85	88	—	85	88	
Logic Input Levels	V_{IL} V_{IH}	$V_{LC} = 0$	—	—	0.8	—	—	0.8	V
			2	—	—	2	—	—	
Logic Input Currents	I_{IL} I_{IH}	$V_{LC} = 0$; $V_{IN} = 0.8V$	-10	-5	—	-10	-5	—	μA
		$V_{IN} = 2.0V$	—	0.001	10	—	0.001	10	

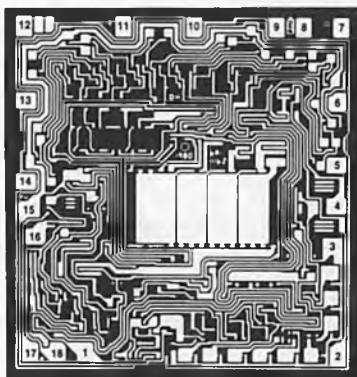
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$; $I_{REF} = 2mA$; $T_A = 25^\circ C$, unless otherwise noted. Output characteristics apply to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-10B/C/F			DAC-10G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Monotonicity			10	—	—	10	—	—	Bits
Nonlinearity	NL		—	0.3	0.5	—	0.6	1	LSB
Differential Nonlinearity	DNL		—	0.3	1	—	0.7	—	LSB
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1 LSB	-5	-6/+18	+10	-5	-6/+15	+10	V
Full-Scale Current	I_{FS}	$V_{REF} = 10.000V$, $R_{14} = R_{15} = 5.000k\Omega$	3.978	3.996	4.014	3.956	3.996	4.036	mA
Full-Scale Symmetry	I_{FSS}	$I_{FR} - \overline{I_{FR}}$	—	0.1	4	—	0.1	4	μA
Zero-Scale Current	I_{ZS}		—	0.01	0.5	—	0.01	0.5	μA

NOTE: Guaranteed by design.



DICE CHARACTERISTICS



DIE SIZE 0.091 × 0.087 inch, 7917 sq. mils
(2.311 × 2.210 mm, 5.107 sq. mm)

- | | |
|---------------------|-------------------|
| 1. V_{LC} (LOGIC) | 10. B6 |
| THRESHOLD CONTROL | 11. B7 |
| 2. I_O | 12. B8 |
| 3. V_- | 13. B9 |
| 4. I_O | 14. B10 (LSB) |
| 5. B1 (MSB) | 15. V_+ |
| 6. B2 | 16. $V_{REF} (+)$ |
| 7. B3 | 17. $V_{REF} (-)$ |
| 8. B4 | 18. COMPENSATION |
| 9. B5 | |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2mA$, $T_A = 25^\circ C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT} .

PARAMETER	SYMBOL	CONDITIONS	DAC-10N LIMIT	DAC-10G LIMIT	UNITS
Resolution			10	10	Bits MIN
Monotonicity			10	10	Bits MIN
Nonlinearity	NL		± 0.5	± 1	LSB MAX
Output Voltage Compliance	V_{OC}	True 1 LSB	+10 -5	+10 -5	V MAX V MIN
Output Current Range		$I_{FS} \pm 3.996 mA$	± 18	± 40	μA MAX
Zero-Scale Current	I_{ZS}	All Bits OFF	0.5	0.5	μA MAX
Logic Input "1"	V_{IH}	$I_{IN} = 100nA$	2	2	V MIN
Logic Input "0"	V_{IL}	V_{LC} @ Ground $I_{IN} = -100\mu A$	0.8	0.8	V MAX
Positive Supply Current	I_+	$V_+ = 15V$	4	4	mA MAX
Negative Supply Current	I_-	$V_- = -15V$	-15	-15	mA MAX

NOTE:

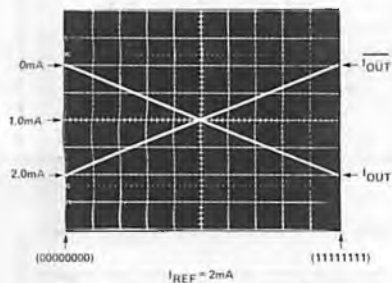
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $I_{REF} = 2mA$, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT} .

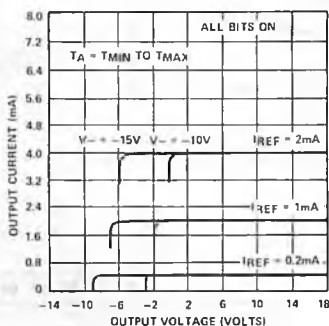
PARAMETER	SYMBOL	CONDITIONS	DAC-10N TYPICAL	DAC-10G TYPICAL	UNITS
Settling Time	t_s	To $\pm 1/2$ LSB When Output is Switched from 0 to FS	85	85	ns
Gain Temperature Coefficient (TC)		V_{REF} Tempco Excluded	± 10	± 10	ppm FS/ $^\circ C$
Output Capacitance			18	18	pF
Output Resistance			10	10	M Ω

TYPICAL PERFORMANCE CHARACTERISTICS

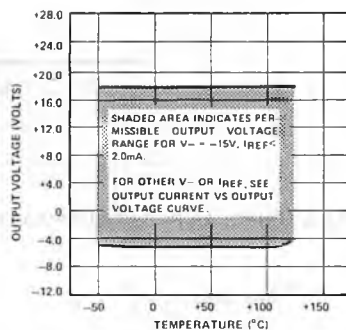
TRUE AND COMPLEMENTARY OUTPUT OPERATIONS



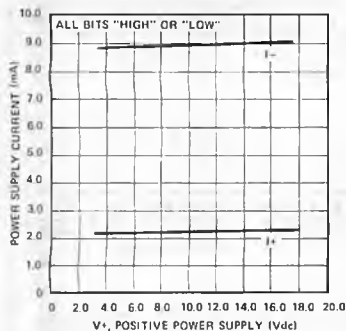
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



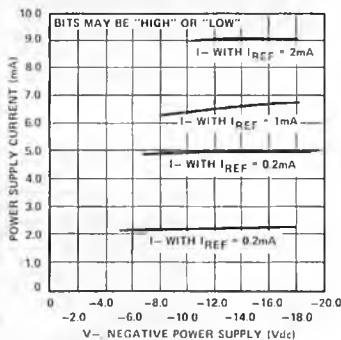
OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



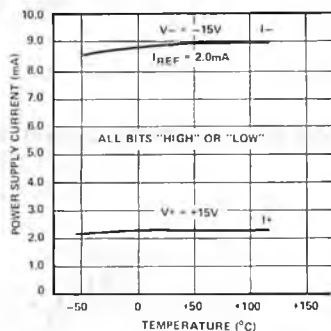
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V-

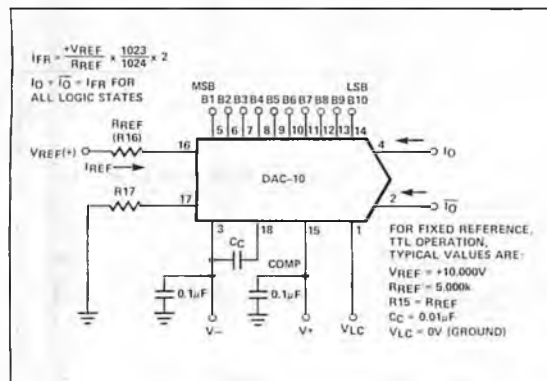


POWER SUPPLY CURRENT vs TEMPERATURE

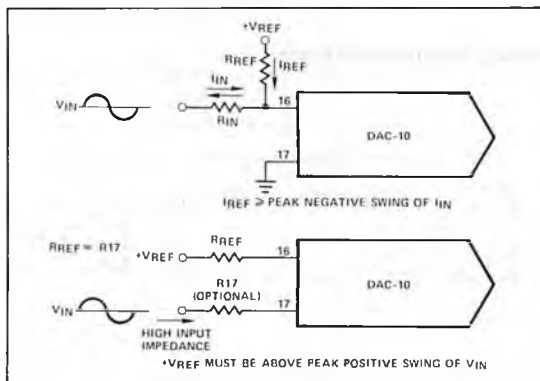


BASIC CONNECTIONS

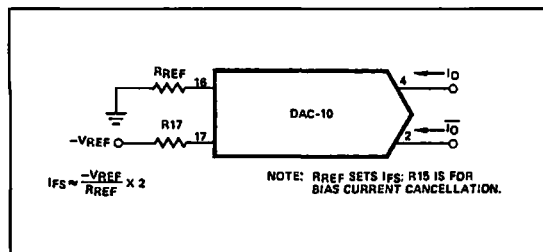
BASIC POSITIVE REFERENCE OPERATION



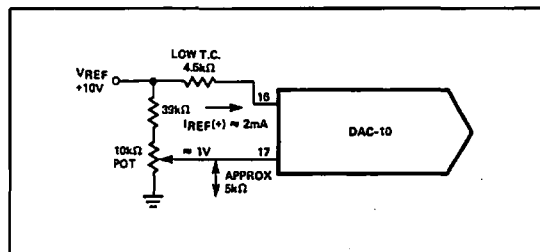
ACCOMMODATING BIPOLAR REFERENCES



BASIC NEGATIVE REFERENCE OPERATION



RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



BASIC UNIPOLAR NEGATIVE OPERATION

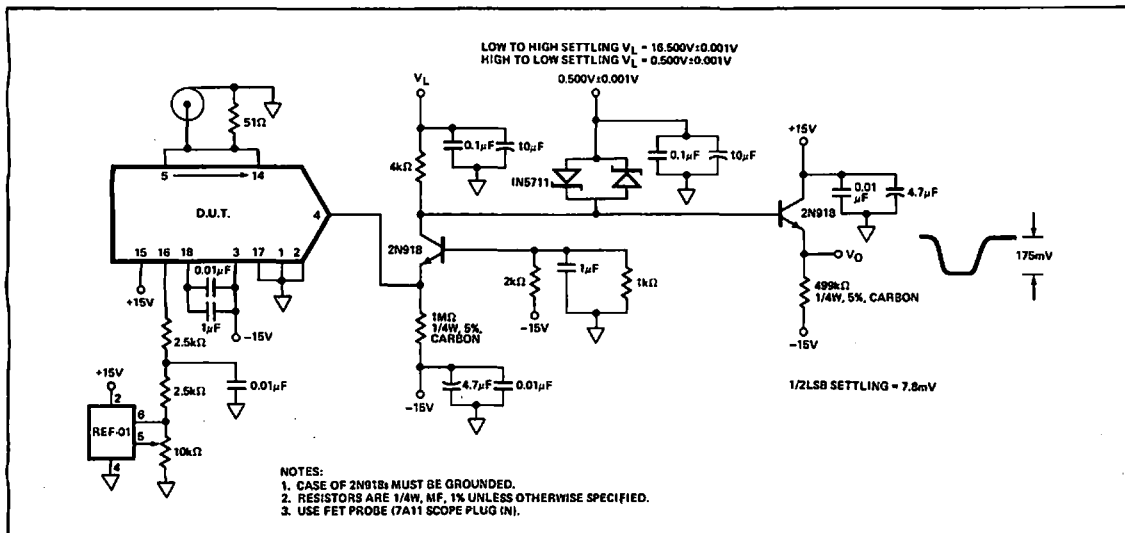
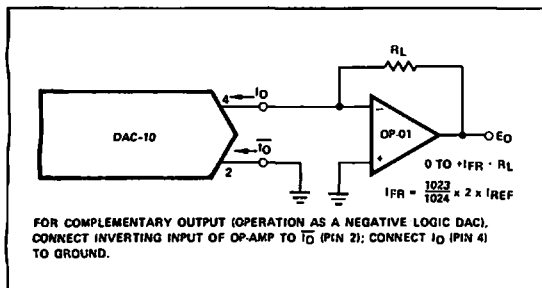
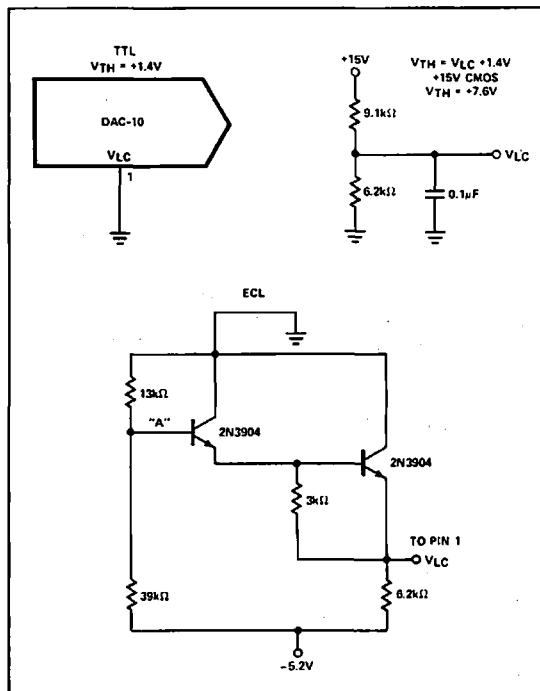
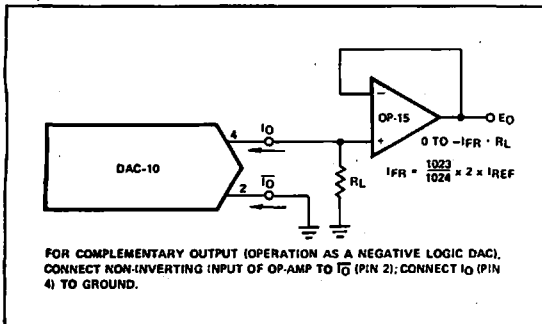
	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	$I_{O}mA$	$\bar{I}_{O}mA$	E_O	$\bar{E}_O$
FULL RANGE	1	1	1	1	1	1	1	1	1	1	3.996	0.000	-4.995	-0.000
HALF-SCALE +LSB	1	0	0	0	0	0	0	0	0	1	2.004	1.992	-2.505	-2.490
HALF-SCALE	1	0	0	0	0	0	0	0	0	0	2.000	1.996	-2.500	-2.495
HALF-SCALE -LSB	0	1	1	1	1	1	1	1	1	1	1.996	2.000	-2.495	2.500
ZERO-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	0.004	3.992	-0.005	-4.990
ZERO-SCALE	0	0	0	0	0	0	0	0	0	0	0.000	3.996	-0.000	-4.995

BASIC BIPOLAR OUTPUT OPERATION

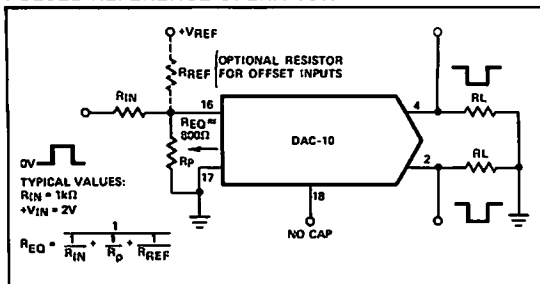
	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	E_O	$\bar{E}_O$
POS FULL RANGE	1	1	1	1	1	1	1	1	1	1	-4.990	+5.000
POS FULL RANGE -LSB	1	1	1	1	1	1	1	1	1	0	-4.980	+4.990
ZERO-SCALE +LSB	1	0	0	0	0	0	0	0	0	1	-0.010	+0.020
ZERO-SCALE	1	0	0	0	0	0	0	0	0	0	0.000	+0.010
ZERO-SCALE -LSB	1	1	1	1	1	1	1	1	1	1	+0.010	0.000
NEG FULL-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	+4.990	-4.980
NEG FULL-SCALE	0	0	0	0	0	0	0	0	0	0	+5.000	-4.990

OFFSET BINARY OPERATION

	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	E_O
POS FULL RANGE	1	1	1	1	1	1	1	1	1	1	+4.990
ZERO-SCALE	1	0	0	0	0	0	0	0	0	0	0.00
NEG FULL-SCALE +LSB	0	0	0	0	0	0	0	0	0	1	-4.990
NEG FULL-SCALE	0	0	0	0	0	0	0	0	0	0	-5.000

SETTLING TIME MEASUREMENT

POSITIVE LOW IMPEDANCE OUTPUT OPERATION

INTERFACING WITH VARIOUS LOGIC FAMILIES

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


PULSED REFERENCE OPERATION



APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-10 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to 2mA. The full-scale output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{1023}{1024} \times 2 \times (I_{REF}) \text{ where } I_{REF} = I_{16}$$

In positive reference applications, an external positive reference voltage forces current through R16 into the $V_{REF(+)}$ terminal (pin 16) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 17; reference current flows from ground through R16 into $V_{(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 17. The voltage at pin 18 is equal to and tracks the voltage at pin 17 due to the high gain of the internal reference amplifier. R17 (nominally equal to R16) is used to cancel bias current errors; R17 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 17. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V_- \text{ plus } (I_{REF} \times 2k\Omega) \text{ plus } 2V$. The positive common-mode range is V_+ less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R16 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF} . If required, full-scale trimming may be accomplished by adjusting the value of R16, or by using a potentiometer for R16. An improved method effects is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 18 to V_- . For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-10 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 2mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 18 to V_- . The value of this capacitor depends on the impedance presented to pin 16 for R16 values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R16 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R16 enabling small C_C values should be used. If pin 16 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R16 = 1kΩ and C_C = 15pF, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 16 is 200Ω and $C_C = 0$. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{1N} and V_{IN} values.

LOGIC INPUTS

The DAC-10 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For $V_- = -15V$, the logic inputs may swing between -5 and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-10 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: $V_- \text{ plus } (I_{REF} \times 2k\Omega) \text{ plus } 3V$. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4V above V_{LC} . For TTL interface, simply ground pin 1. When interfacing ECL, an $I_{REF} = 1mA$ is recommended. For interfacing other logic families, see previous page. For general setup of the logic control circuit, it should be noted that pin 1 will sink 1.1mA typical; external circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I}_O = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases $\overline{I}_O$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS} ; DO NOT LEAVE AN UNUSED OUTPUT PIN OPEN.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V_- and is independent of the positive supply. Negative compliance is +10V above V_- .

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-10 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating with V_- supplies of -10V or less, $I_{REF} \leq 1\text{mA}$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -9V with $I_{REF} = 2\text{mA}$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-10 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain within acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-10 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically $\pm 10\text{ppm}/^\circ\text{C}$, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-10 decrease approximately 10% at -55°C ; at $+125^\circ\text{C}$ an increase of about 15% is typical.

SETTLING TIME

The DAC-10 is capable of extremely fast settling times; typically 85ns at $I_{REF} = 2\text{mA}$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 10 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 85ns, thus determining the overall settling time of 130ns. Settling to 8-bit accuracy requires about 60 to 78ns. The output capacitance of the DAC-10 including the package is approximately 18pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve $\pm 2\mu\text{A}$, therefore a $4\text{k}\Omega$ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of schematic titled "Settling Time Measurement" uses a cascode design to permit driving a $4\text{k}\Omega$ load with less than 5pF of parasitic capacitance at the measurement node. At I_{REF} values of less than 1mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111 to 100000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within $\pm 0.2\%$ of the final value, and thus settling times may be observed at lower values of I_{REF} .

DAC-10 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; $0.1\mu\text{F}$ capacitors at the supply pins provide full transient protection.



DAC-20

2-DIGIT BCD HIGH-SPEED MULTIPLYING D/A CONVERTER (UNIVERSAL DIGITAL LOGIC INTERFACE)

Precision Monolithics Inc.

FEATURES

- Fast Settling Output Current 85ns
- Full-Scale Current Prematched to ± 0.3 LSB
- Direct Interface to TTL, CMOS, ECL, PMOS, NMOS
- Nonlinearity to $\pm 1/2$ LSB Maximum Over Temp.
- High Output Impedance and Compliance $-10V$ to $+18V$
- Complementary Current Outputs
- Wide Range Multiplying Capability ... 1MHz Bandwidth
- Low FS Current Drift $\pm 10\text{ppm}/\Delta C$
- Wide Power Supply Range $\pm 4.5V$ to $\pm 18V$
- Low Power Consumption 37mW @ $\pm 5V$
- Low Cost

ORDERING INFORMATION†

NL LSB	16-PIN DUAL-IN-LINE PACKAGE COMMERCIAL TEMPERATURE RANGE	
	HERMETIC	PLASTIC
$\pm 1/2$	DAC20CQ	DAC20CP

†Burn-In is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The DAC-20 series of 2-digit BCD monolithic multiplying digital to analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB

between reference and full-scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

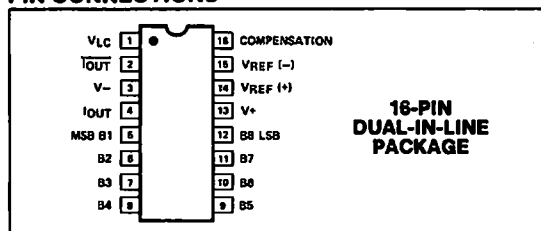
Complementary current outputs with $-10V$ to $+18V$ voltage compliance enable resistive termination, a voltage output without an external op amp.

Both DAC-20 models guarantee full 2-digit monotonicity, some have nonlinearity as tight as $\pm 1/2$ LSB over the entire operating temperature range. Nonlinearity is unchanged over the $\pm 4.5V$ to $\pm 18V$ power supply range, with 37mW power consumption attainable at $\pm 5V$ supplies.

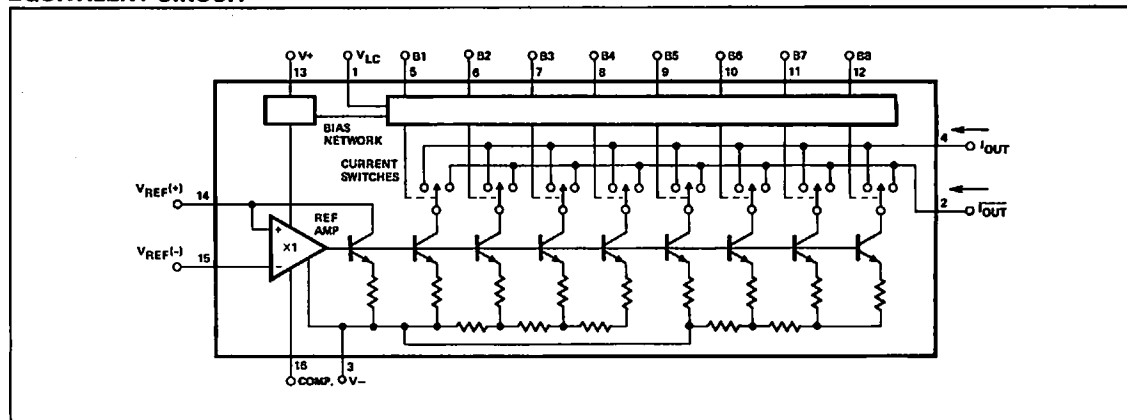
The compact size and low power consumption make the DAC-20 attractive for portable applications.

DAC-20 applications include A/D converters, audio attenuators, analog meter drivers, programmable power supplies, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

PIN CONNECTIONS



EQUIVALENT CIRCUIT



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639

**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Operating Temperature Range	
DAC-20 CQ, CP	0°C to $+70^\circ\text{C}$
DICE Junction Temperature (T_J)	-65°C to $+150^\circ\text{C}$
Storage Temperature Range	
Q Package	-65°C to $+150^\circ\text{C}$
P Package	-65°C to $+125^\circ\text{C}$
Power Dissipation	
Derate above 100°C	$10\text{mW}/^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C

V+ Supply to V- Supply	36V
Logic Inputs	V- to V- plus 36V
V _{LC}	V- to V+
Reference Inputs (V_{14} , V_{15})	V- to V+
Reference Input Differential Voltage (V_{14} to V_{15})	$\pm 18\text{V}$
Reference Input Current (I_{14})	5.0mA

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, $I_{\text{REF}} = 2.0\text{mA}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT} .

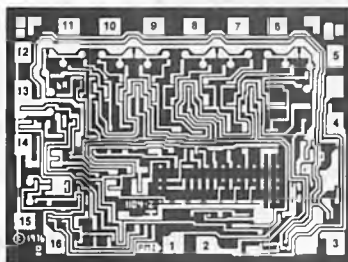
PARAMETER	SYMBOL	CONDITIONS	DAC-20C			UNITS
			MIN	TYP	MAX	
Resolution		BCD 0 to 99 steps	2	—	—	Digits
Monotonicity		BCD 99 steps	2	—	—	Digits
Nonlinearity	NL	0000 0000 to 1001 1001	—	—	$\pm 1/2$	LSB
Settling Time	t_s	To $\pm 1/2$ LSB ($\pm 0.5\%$ FS) all bits switched ON or OFF, $T_A = 25^\circ\text{C}$ (Note 1)	—	85	150	ns
Propagation Delay						
Each Bit	t_{PLH}	$T_A = 25^\circ\text{C}$ (Note 1)	—	35	60	ns
All bits switched	t_{PHL}					
Full Tempco	TCI_{FS}	(Note 1)	—	± 10	± 60	ppm/ $^\circ\text{C}$
Output Voltage Compliance (True Compliance)	V_{OC}	Full-scale current change < $1/2$ LSB ($< 0.5\%$ FS) $R_{\text{OUT}} > 20\text{M}\Omega$ typical $I_{\text{REF}} = 1\text{mA}$	-10	—	+18	V
Full Range Output (Digital Input 1001 1001)	I_{FR4}	$T_A = 25^\circ\text{C}$, $I_{\text{REF}} = 2\text{mA}$	1.92	1.88	2.04	mA
Zero-Scale Current	I_{ZS}		—	0.2	5	μA
Output Current Range	I_{OR}	$V = -10\text{V}$ $V = -12\text{V}$ to -18V	2.2 4.2	2 2	— —	mA
Logic Input Levels						
Logic "0"	V_{IL}	$V_{\text{LC}} = 0\text{V}$	—	—	0.8	V
Logic "1"	V_{IH}					
Logic Input Current						
Logic "0"	I_{IL}	$V_{\text{LC}} = 0\text{V}$ $V_{\text{IN}} = -10\text{V}$ to $+0.8\text{V}$	—	-2	± 10	μA
Logic "1"	I_{IH}	$V_{\text{IN}} = 2\text{V}$ to 18V	—	0.002	± 10	
Logic Input Swing	V_{IS}	$V = -15\text{V}$	-10	—	+18	V
Logic Threshold Range	V_{THR}	$V_S = \pm 15\text{V}$ (Note 1)	-10	—	+13.5	V
Reference Bias Current	I_{15}		—	-1	-3	μA
Reference Input Slew Rate	dI/dt	(Note 1)	4	8	—	mA/ μs
Power Supply Sensitivity	$\text{PSSI}_{\text{FS}+}$ $\text{PSSI}_{\text{FS}-}$	$V+ = 4.5\text{V}$ to 18V $V- = -4.5\text{V}$ to -18V $I_{\text{REF}} = 1\text{mA}$	— ± 0.0003	± 0.03		$\% \Delta I_{\text{FS}}$
			— ± 0.002	± 0.03		$\% \Delta V$
Power Supply Current	$I+$ $I-$ $I+$ $I-$	$V_S = \pm 5\text{V}$, $I_{\text{REF}} = 1\text{mA}$ $V_S = \pm 15\text{V}$, $I_{\text{REF}} = 2\text{mA}$	— — — —	2.3 -5.0 2.5 -7.8	3.8 -6.5 3.8 -9.1	mA
Power Dissipation	P_d	$V_S = \pm 5\text{V}$, $I_{\text{REF}} = 1\text{mA}$ $V_S = \pm 15\text{V}$, $I_{\text{REF}} = 2\text{mA}$	— —	37 152	52 194	mW

NOTE:

1. Guaranteed by design.



DICE CHARACTERISTICS

DIE SIZE 0.086 × 0.064 inch, 5,504 sq. mils
(2.184 × 1.625 mm, 3.55 sq. mm)

- | | |
|----------------|-------------------|
| 1. V_{LC} | 9. BIT 5 |
| 2. I_{OUT} | 10. BIT 6 |
| 3. V^- | 11. BIT 7 |
| 4. I_{OUT} | 12. BIT 8 (LSB) |
| 5. BIT 1 (MSB) | 13. V^+ |
| 6. BIT 2 | 14. $V_{REF} (+)$ |
| 7. BIT 3 | 15. $V_{REF} (-)$ |
| 8. BIT 4 | 16. COMP |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 25^\circ C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT-} .

PARAMETER	SYMBOL	CONDITIONS	DAC-20G LIMIT	UNITS
Resolution		BCD 0 to 99 steps	2	Digits MIN
Monotonicity		BCD 99 steps	2	Digits MIN
Nonlinearity	NL	FS = 1001 1001	$\pm 1/2$	LSB MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change $< 1/2$ LSB	+18 -10	V MAX V MIN
Full-Scale Current	I_{FS4}	$V_{REF} = 10V$ $R_{14}, R_{15} = 5k\Omega$	2.04 1.92	mA MAX mA MIN
Zero-Scale Current	I_{ZS}		5	μA MAX
Output Current Range	I_{OR}	$V^- = -10V$ $V^- = -12V$ to $-18V$	2.1 4.2	mA MIN
Logic "0" Input Level	V_{IL}		0.8	V MAX
Logic "1" Input Level	V_{IH}		2	V MIN
Logic Input Current				
Logic "0"	I_{IL}	$V_{IN} = -10V$ to $+0.8V$	± 10	μA MAX
Logic "1"	I_{IH}	$V_{IN} = 2V$ to $18V$	± 10	
Logic Input Swing	V_{IS}	$V^- = -15V$	+18 -10	V MAX V MIN
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	$V^- = -4.5V$ to $-18V$ $V^- = -4.5V$ to $-18V$ $I_{REF} = 1mA$	± 0.03 ± 0.03	$\% \Delta I_{FS}$ MAX $\% \Delta V$ MAX
Power Supply Current	I^+ I^-	$V_S = \pm 18V$ $I_{REF} \leq 2mA$	3.8 -7.8	mA MAX
Power Dissipation	P_d	$V_S = \pm 18V$ $I_{REF} \leq 2mA$	194	mW MAX

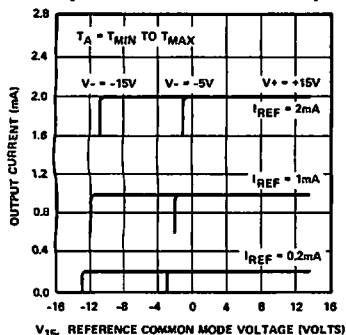
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

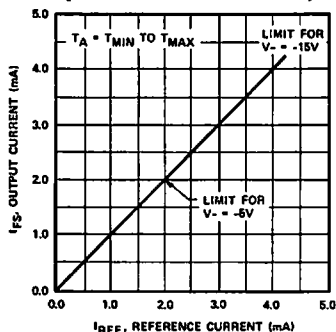
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, unless otherwise noted specified. Output characteristics refer to both I_{OUT} and I_{OUT-} .

PARAMETER	SYMBOL	CONDITIONS	DAC-20G TYPICAL	UNITS
Reference Input Slew Rate	dl/dt		8	mA/ μs
Propagation Delay	t_{PLH}, t_{PHL}	$T_A = 25^\circ C$, Any Bit	35	ns
Settling Time	t_s	To $\pm 1/2$ LSB, All Bits Switched ON or OFF, $T_A = 25^\circ C$	85	ns

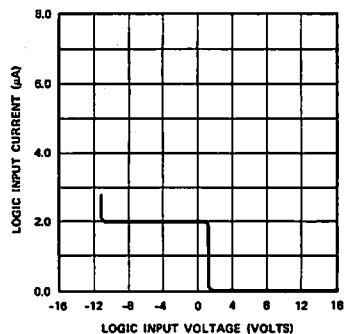
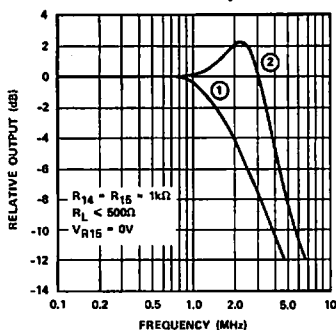
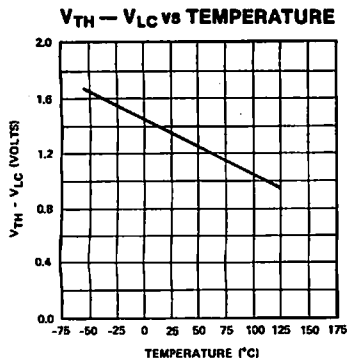
TYPICAL REFERENCE PERFORMANCE CHARACTERISTICS

 REFERENCE AMP
COMMON-MODE RANGE
(DIGITAL INPUT 1001 1001)


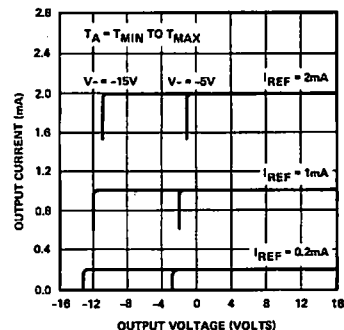
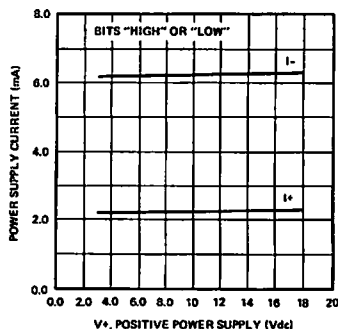
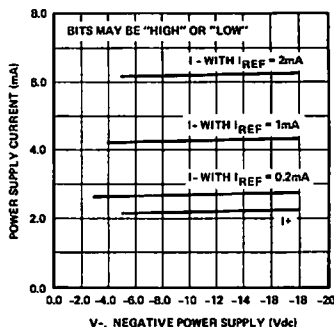
NOTE: POSITIVE COMMON MODE IS ALWAYS $(V+) - 1.5V$;
NEGATIVE COMMON MODE RANGE IS $V-$ PLUS
 $(I_{REF} \times 800\Omega)$ PLUS 2.5V.

 FULL-SCALE CURRENT vs
REFERENCE CURRENT
(DIGITAL INPUT 1001 1001)


NOTE: THE RECOMMENDED RANGE FOR OPERATION WITH
WITH A DC REFERENCE CURRENT IS $+0.2mA$
TO $+4.0mA$.

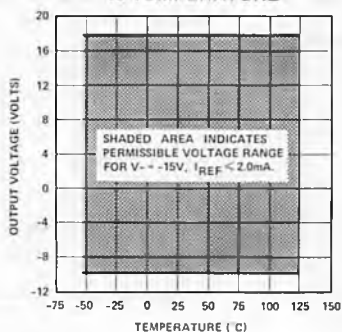
 LOGIC INPUT CURRENT
vs INPUT VOLTAGE

 REFERENCE INPUT FREQUENCY
RESPONSE (DIGITAL INPUT
1001 1001)


CURVE 1: $C_C = 15pF$, $V_{IN} = 2.0V_{p-p}$ CENTERED AT
 $+1.0V$, LARGE SIGNAL.
CURVE 2: $C_C = 15pF$, $V_{IN} = 50mV_{p-p}$ CENTERED AT
 $+200mV$, SMALL SIGNAL.

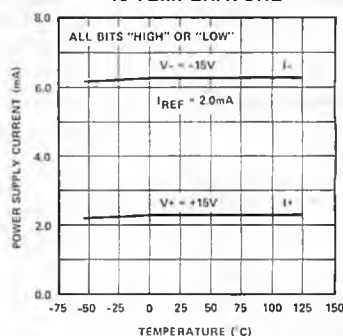
 OUTPUT CURRENT
vs OUTPUT VOLTAGE
(OUTPUT VOLTAGE COMPLIANCE)
(DIGITAL INPUT 1001 1001)

 POWER SUPPLY
CURRENT vs $V+$

 POWER SUPPLY
CURRENT vs $V-$


TYPICAL REFERENCE PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE COMPLIANCE
vs TEMPERATURE



POWER SUPPLY CURRENT
vs TEMPERATURE



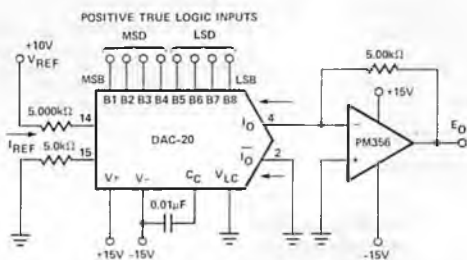
BASIC OUTPUT CONNECTIONS

With complementary current outputs, the DAC-20 may be used with either positive true or negative true (complementary) logic. Current appears at the "true" output (I_O) when a "1" is applied to a logic input. As the BCD-coded input increases, the sink current at Pin 4 increases proportionately, in the fashion of a "positive logic" D/A converter. When a "0" is applied to a logic input, that current is turned OFF at Pin 4 and ON at Pin 2 ($\bar{I}_O$) which is used for negative true or "negative logic" D/A converters.

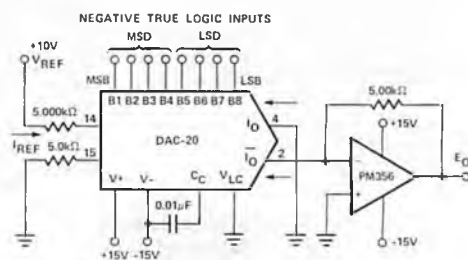
The unused output must be connected to ground or some voltage source capable of sourcing 1.65 times I_{REF} . A detailed discussion of reference input operation begins on the next page.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V_- and is independent of the positive supply. Negative compliance is given by V_- plus $(I_{REF} \times 800\Omega)$ plus 2.5V.

POSITIVE VOLTAGE OUTPUT

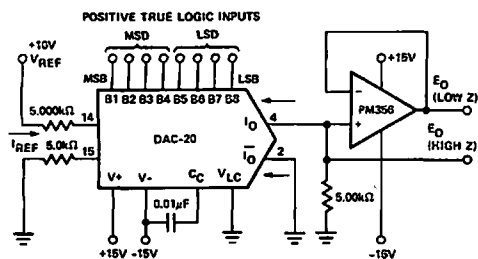


DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	I_O	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	+1.0V
20	0010	0000	0.40mA	+2.0V
30	0011	0000	0.60mA	+3.0V
40	0100	0000	0.80mA	+4.0V
80	1000	0000	1.60mA	+8.0V
99	1001	1001	1.98mA	+9.9V

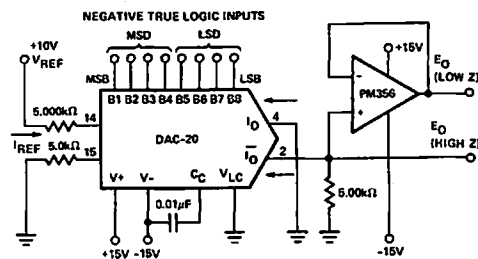


DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	$\bar{I}_O$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	+1.0V
20	1101	1111	0.40mA	+2.0V
30	1100	1111	0.60mA	+3.0V
40	1011	1111	0.80mA	+4.0V
80	0111	1111	1.60mA	+8.0V
99	0110	0110	1.98mA	+9.9V

NEGATIVE VOLTAGE OUTPUT



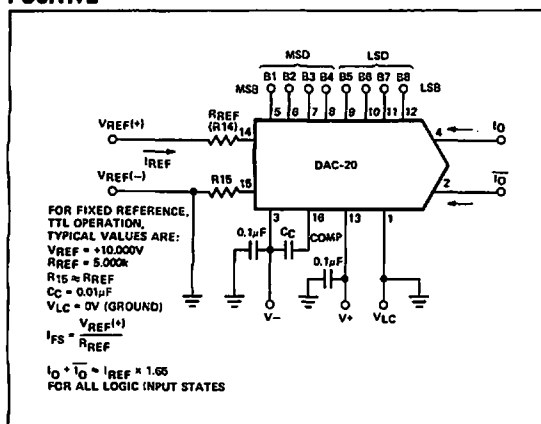
DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	I_o	E_o
0	0000	0000	0	0
10	0001	0000	0.20mA	-1.0V
20	0010	0000	0.40mA	-2.0V
30	0011	0000	0.60mA	-3.0V
40	0100	0000	0.80mA	-4.0V
80	1000	0000	1.60mA	-8.0V
99	1001	1001	1.98mA	-9.9V



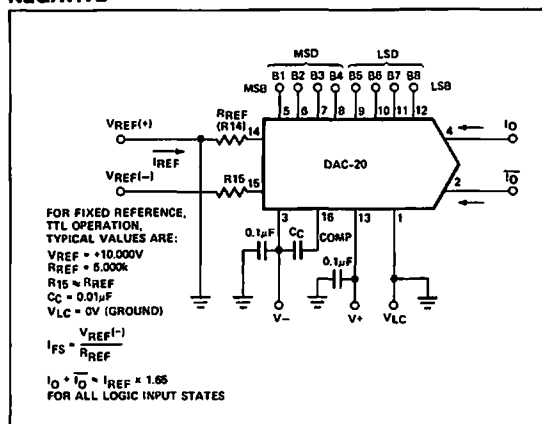
DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	$\bar{I}_o$	E_o
0	1111	1111	0	0
10	1110	1111	0.20mA	-1.0V
20	1101	1111	0.40mA	-2.0V
30	1100	1111	0.60mA	-3.0V
40	1011	1111	0.80mA	-4.0V
80	0111	1111	1.60mA	-8.0V
99	0110	0110	1.98mA	-9.9V

REFERENCE OPERATION

POSITIVE



NEGATIVE



REFERENCE AMPLIFIER SETUP

The DAC-20 is a multiplying converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = 99/100 \times I_{REF}, \text{ where } I_{REF} = I_{14}.$$

In positive reference applications an external positive reference voltage forces current through R_{14} into the $V_{REF}(+)$ terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF}(-)$ at Pin 15; reference current flows from ground through R_{14} into $V_{REF}(+)$, as in the positive reference case. This negative reference con-

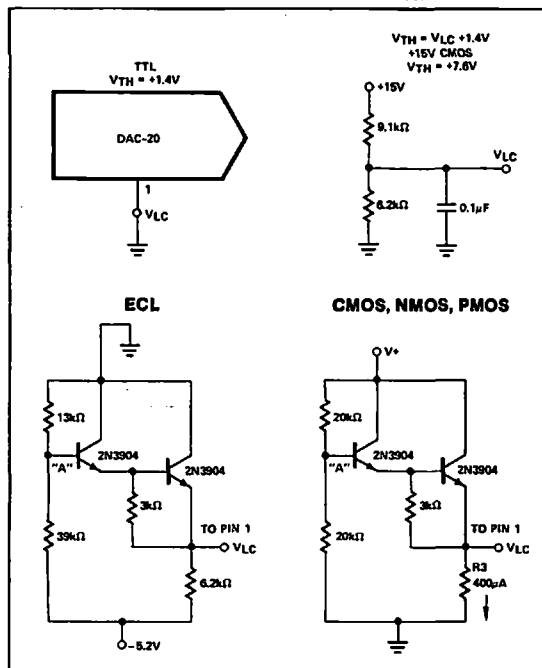
section has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

When a DC reference is used, a reference bypass capacitor is recommended. A 5V TTL logic supply is not recommended as reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a $0.1\mu\text{F}$ capacitor.

For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF} . If required, full-scale trimming may be accomplished by adjusting the value of R_{14} .

The reference amplifier must be compensated by using a capacitor from Pin 16 to V^- . For fixed reference operation, a $0.01\mu\text{F}$ capacitor is recommended. For variable reference applications, see section entitled "Multiplying Operation."

LOGIC INPUT OPERATION AND INTERFACING



LOGIC THRESHOLD CONTROL

The DAC-20 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, $2\mu\text{A}$ logic input current and completely adjustable logic threshold voltage.

For $V^- = -15\text{V}$, the logic inputs may swing between -10V and $+18\text{V}$. This enables direct interface with a $+15\text{V}$ CMOS logic, even when the DAC-20 is powered from a $+5\text{V}$ supply. Minimum logic threshold voltage are given by: V^- plus $(I_{REF} \times 800\Omega)$ plus 2.5V . The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (Pin 1, V_{LC}).

The logic input threshold is 1.4V above V_{LC} . For TTL and DTL interface, simply ground Pin 1. When interfacing ECL, an $I_{REF} = 1\text{mA}$ is recommended. For interfacing other logic families, see the figure. Pin 1 will source $100\mu\text{A}$ typically, so the external circuitry must be designed to accommodate this current. Note that the threshold voltage has the temperature dependence of two forward biased diodes. The two V_{LC} setting circuits shown, include temperature compensation.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a $1\text{k}\Omega$ divider, for example, it should be bypassed to ground by a $0.01\mu\text{F}$ capacitor.

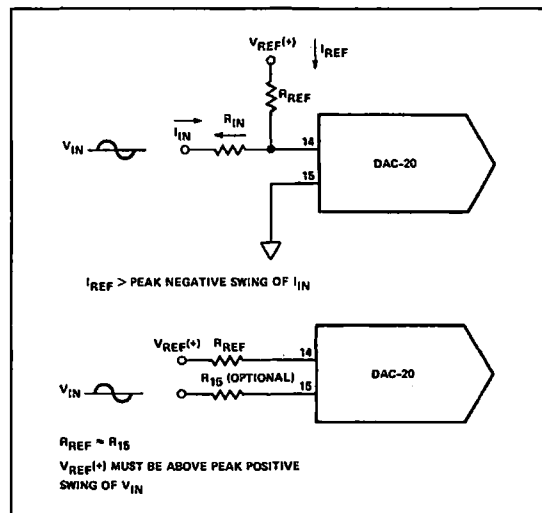
MULTIPLYING OPERATION

The DAC-20 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 2mA to $4\mu\text{A}$. Monotonic operation is maintained over a typical range of I_{REF} from $100\mu\text{A}$ to 2mA .

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM} = V^-$ plus $(I_{REF} \times 800\Omega)$ plus 2.5V . The positive common mode range is V^+ less 1.5V .

AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V^- . The value of this capacitor depends on the impedance presented to Pin 14: for R_{14} values of 1.0 , 2.5 and $5.0\text{k}\Omega$, minimum value of C_C are 15 , 37 , and 75pF . Larger values of R_{14} require

ACCOMMODATING BIPOLAR REFERENCES

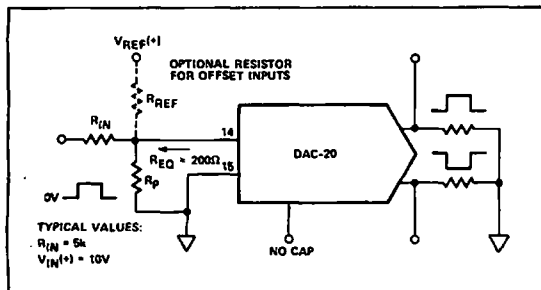


proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For $R_{14} = 1\text{k}\Omega$ and $C_C = 15\text{pF}$, the reference amplifier slews at $4\text{mA}/\mu\text{s}$ enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2\text{mA}$ in 500ns .

Operation with pulse inputs to the reference amplifier may be accommodated by the alternate compensation scheme shown above. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier for a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at Pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of $16\text{mV}/\mu\text{s}$, which is relatively independent of R_{IN} and V_{IN} values.

PULSED REFERENCE OPERATION



POWER SUPPLY CONSIDERATIONS

The DAC-20 operates over a wide range of power supply voltages from a total supply of 9V to 36V . When operating at supplies of $\pm 5\text{V}$ or less, $I_{REF} \leq 1\text{mA}$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -4.5V with $I_{REF} = 2\text{mA}$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V total must be applied to insure turn-on of the internal bias network.

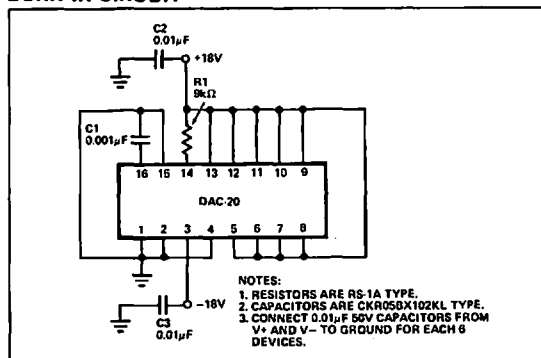
Symmetrical supplies are not required, as the DAC-20 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required:

however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power Consumption may be calculated as follows:

$P_d = (I_+) \times (V_+) + (I_-) \times (V_-)$. A useful feature of the DAC-20 design is that supply current is constant and independent of input logic states; this reduces the size of the power supply bypass capacitors.

BURN-IN CIRCUIT



TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specification of the DAC-20 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically $\pm 10\text{ppm}/^\circ\text{C}$, with zero-scale output current and drift essentially negligible compared to $1/2$ LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full-scale drift.

SETTLING TIME OPTIMIZATION

The DAC-20 is capable of extremely fast settling times, typically 85ns at $I_{REF} = 2.0\text{mA}$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The output capacitance of the DAC-20, including the package, is approximately 15pF ; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; $0.1\mu\text{F}$ capacitors at the supply pins provide full transient protection.



DAC-86

COMDAC® COMPANDING
D/A CONVERTER (μ -255 LAW)

Precision Monolithics Inc.

FEATURES

- Conforms With Bell System μ -255 Companding Law
- Meets D3 Compander Tracking Specifications
- Both Encode and Decode Capability
- Tight Full-Scale Tolerance Eliminates Calibration
- Low Full-Scale Drift Over Temperature
- Extremely Low Noise Contribution
- Multiplying Reference Inputs
- Simplifies PCM System Design
- High Reliability
- Low Power Consumption and Low Cost
- Two Grades Available

GENERAL DESCRIPTION

The DAC-86 monolithic COMDAC® D/A Converter provides a 15 segment linear approximation to the Bell System μ -255 companding law. The law is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. A sign bit determines signal polarity, and an encode/decode input determines the mode of operation.

Accuracy is assured by specifying chord end point values, step nonlinearity, and monotonicity over the full operating temperature range. Typical applications include PCM carrier systems, digital PBX's intercom systems, and PCM recording. For CCITT "A" Law models, refer to the DAC-89 data sheet.

PIN CONNECTIONS & ORDERING INFORMATION

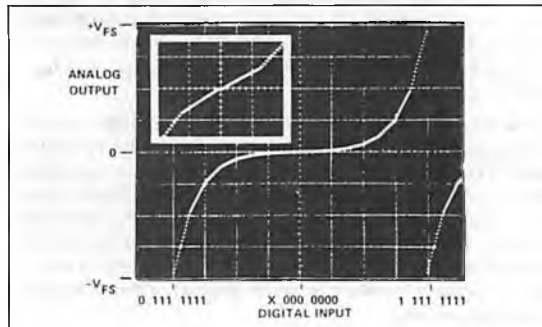
ENCODE/DECODE SELECT: 1 - ENCODE	1	E/D	V+	18	POSITIVE POWER SUPPLY
SIGN BIT INPUT: 1 - POSITIVE	2	S8	IOE(-)	17	DECODE OUT: E/D SB = 00
MOST SIGNIFICANT CHORD BIT INPUT	3	B1	IOE(+)	16	DECODE OUT: E/D SB = 01
SECOND CHORD BIT INPUT	4	B2	IOE(-)	15	ENCODE OUT: E/D SB = 10
LEAST SIGNIFICANT CHORD BIT INPUT	5	B3	IOE(+)	14	ENCODE OUT: E/D SB = 11
MOST SIGNIFICANT STEP BIT INPUT	6	I14	V-	13	NEGATIVE POWER SUPPLY
SECOND STEP BIT INPUT	7	B5	VR(-)	12	NEGATIVE REFERENCE INPUT
THIRD STEP BIT INPUT	8	B6	VR(+)	11	POSITIVE REFERENCE INPUT
LEAST SIGNIFICANT STEP BIT INPUT	9	B7	VLC	10	LOGIC THRESHOLD CONTROL

18-PIN HERMETIC DUAL-IN-LINE (X-Suffix)

GRADE	TEMP. RANGE	ACCURACY
DAC-86EX†	-25°C/+85°C	±1/2 Step
DAC-86CX†	-25°C/+85°C	±1 Step

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

COMDAC® TRANSFER CHARACTERISTIC



BELL μ -255 LAW TRANSFER CHARACTERISTIC

The DAC-86 transfer characteristic is a piecewise linear approximation to the Bell System μ -255 law expressed by:

$$Y(x) = \text{sgn}(x) \frac{\ln(1 + \mu|x|)}{\ln(1 + \mu)} \quad -1 \leq x \leq 1$$

for a normalized coding range of ± 1

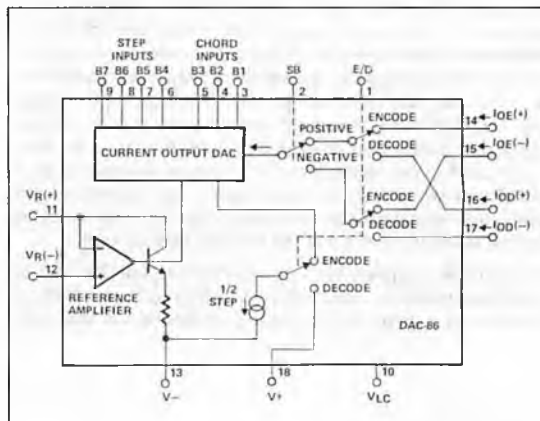
where: x = input signal level

Y = output compressed signal level

$\mu = 255$

This law is implemented with a eight chord (or segment) piecewise linear approximation with 16 linear steps in each chord. Dynamic range of 72dB in both polarities is achieved with eight-bit coding.

EQUIVALENT CIRCUIT





ABSOLUTE MAXIMUM RATINGS

V+ Supply to V- Supply	36V
V _{LC} Swing	V- plus 8V to V+
Analog Current Outputs	V- plus 8V to V- plus 36V
Reference Inputs	V- to V+
Reference Input Differential Voltage	±18V
Reference Input Current	1.25mA

Logic Inputs	V- plus 8V to V- plus 36V
Operating Temperature	-25°C to +85°C
Storage Temperature	-65°C to +150°C
Power Dissipation	500mW
Derate Above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25^\circ C \leq T_A \leq +85^\circ C$, for all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-86E			DAC-86C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	dB
Monotonicity		Sign-Bit + or -	128	—	—	128	—	—	Steps
Chord End-Point Accuracy All Chords		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	Step
Encode Decision Level Current		Additional output encode/decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
Settling Time (Note 1)	t_s	To within ±1/2 step	—	1	—	—	1	—	μsec
Full-Scale Drift (C_7) (Note 2)	ΔI_{FS}	Full temperature range	—	±1/16	±1/10	—	±1/10	±1/4	Step
Output Voltage Compliance	V_{OC}	Full-scale current change ≤ 1/2 step	-5	—	+18	-5	—	+18	Volts
Full-Scale Symmetry Error	$I_{O(+)} - I_{O(-)}$	Decode or encode pair Input Code 111 1111	—	±1/40	±1/8	—	±1/40	±1/4	Step
Zero-Scale Current (C_0)	I_{ZS}	Measured at selected output with 000 0000 input	—	±1/40	±1/8	—	±1/40	±1/4	Step
Disable Current (All bits high)	I_{DIS}	Leakage of output disabled by E/D and SB	—	5	75	—	5	75	nA
Step Accuracy All Chords		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	Step
Output Current Range	I_{FSR}		—	2.0	4.2	—	2.0	4.2	mA
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2	—	—	2	—	—	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to +18V	—	—	120	—	—	120	μA
Logic Input Swing	V_{IS}	$V- = -15V$	-5	—	+18	-5	—	+18	Volts
Reference Bias Current	I_{12}		—	-3	-12	—	-3	-12	μA
Reference Input Slew Rate	di/dt		—	0.25	—	—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$	$V+ = 4.5V$ to 18V, $V- = -15V$	—	±1/20	±1/2	—	±1/20	±1/2	Step
	$PSSI_{FS-}$	$V- = -10.6V$ to -18V, $V+ = 15V$	—	±1/10	±1/2	—	±1/10	±1/2	
Power Supply Current	I+	$V_S = +5V$, -15V, $I_{FS} = 2.0mA$	—	2.7	4.5	—	2.7	4.5	mA
	I-	$V_S = +5V$, -15V, $I_{FS} = 2.0mA$	—	-6.7	-9.3	—	-6.7	-9.3	
	I+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	2.7	4.5	—	2.7	4.5	
	I-	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	-6.7	-9.3	—	-6.7	-9.3	
Power Dissipation	P_d	$V_S = +5V$, -15V, $I_{FS} = 2.0mA$	—	114	167	—	114	167	mW
		$V_S = \pm 15V$, $I_{FS} = 2.0mA$	—	141	207	—	141	207	

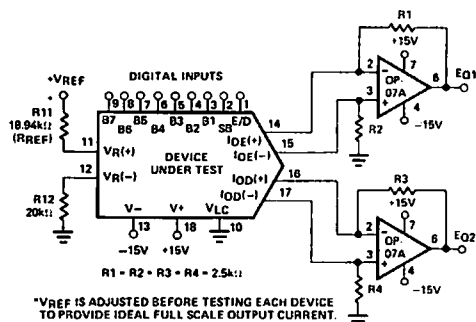
NOTE:

1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is $0.5\mu A$, while in the last chord near full-scale (C_7) step size is $64\mu A$. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading. In decode operation, the DAC-88

and OP-18 combination will decode eight channels. In the encode mode, the DAC-88 and CMP-01 combination will encode eight channels. Both encode and decode statements assume a 5.2μsec channel time.

2. Guaranteed by design.

OUTPUT CURRENT DC TEST CIRCUIT



LINE SELECTION TABLE

TEST GROUP	ENCODE/DECODE	SIGN BIT	OUTPUT MEASUREMENT
1	1	1	$I_{OE}(+)$ ($E_{01}/R1$)
2	1	0	$I_{OE}(-)$ ($E_{01}/R2$)
3	0	1	$I_{OD}(+)$ ($E_{02}/R3$)
4	0	0	$I_{OD}(-)$ ($E_{02}/R4$)

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonicity is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES ($I_{REF} = 528\mu A$)

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD	0	1	2	3	4	5	6	7
STEP	000	001	010	011	100	101	110	111
0	0000	0.0	8.25	24.75	57.75	123.75	255.75	519.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	2007.75
STEP SIZE		0.5	1	2	4	8	16	32

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD	0	1	2	3	4	5	6	7
STEP	000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75
15	1111	7.75	23.25	55.75	119.75	247.75	503.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32

NOTE:

These tables may be extended to include all of the encode/decode currents (ideal with $S I_{REF} = 528\mu A$) by multiplying any of the numbers in the normalized tables by $0.5\mu A$.

PARAMETER DEFINITIONS

FULL-SCALE DRIFT

The change in output current over the full operating temperature with $V_{REF} = 10.000V$, $R11 = 18.94k\Omega$, and $R12 = 20k\Omega$.

FULL-SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full-scale output.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes $< 1/2$ step change in output current.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord; used to specify accuracy.

STEPS

Increments in each chord which divides the chord into 16 equal levels.

OUTPUT LEVEL NOTATION

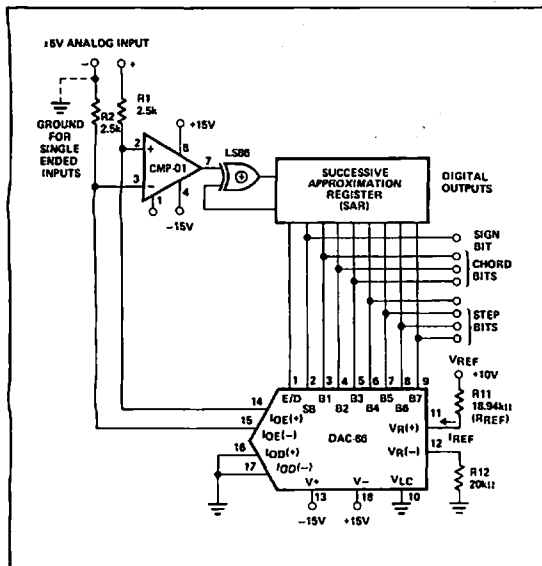
Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero-scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full-scale current.

DYNAMIC RANGE

Ratio of full-scale current to step size in chord zero, expressed in dB. This can be measured peak or peak-to-peak with the same result.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

BASIC ENCODE CONNECTIONS



ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-86 requires a comparator, an EXCLUSIVE-OR gate, and a successive approximation register — the usual elements in any sign-

magnitude A/D converter. However, a compressing A/D has one significant difference. In a conventional (linear converter), the step size is a constant percentage of full-scale. In a compressing A/D converter, the step size increases as the output changes from zero-scale to full-scale.

When the DAC is used in the feedback loop of a successive approximation analog to digital converter (ADC) the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode the outputs correspond to the center of the quantizing bands. The encode mode output exceeds the decode mode output by one-half step. See AN-39 for detailed explanation.

ENCODING SEQUENCE

An encoding sequence begins with the sign-bit decision. During this time the comparator functions as a polarity detector. The encode/decode (E/D) input is held at a logic "0". In this mode, current flows into the decode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input toggles to a logic "1" allowing current to flow into $IOE(+)$ or $IOE(-)$.

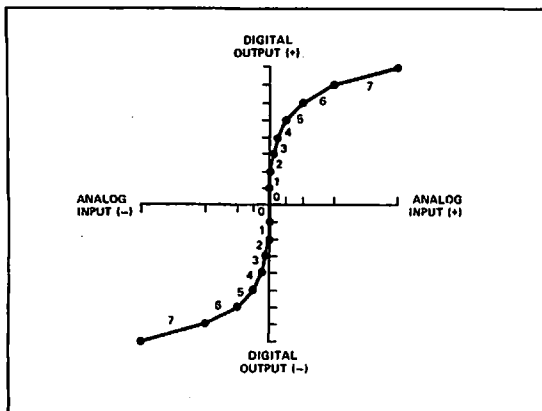
For positive inputs, current flows into $IOE(+)$ through R1, and the comparator's output is entered as the answer for each successive decision. For negative inputs, current flows into $IOE(-)$ through R2 developing a negative voltage which is compared with the analog input. An EXCLUSIVE-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full-scale and all zeros for zero-scale.

The bits are converted with a successive removal technique, starting with a decision at the code 011 111 and turning off bits sequentially until all decisions have been made.

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) ($I_{C,S} = 2[2^C(S + 17) - 16.5]$)

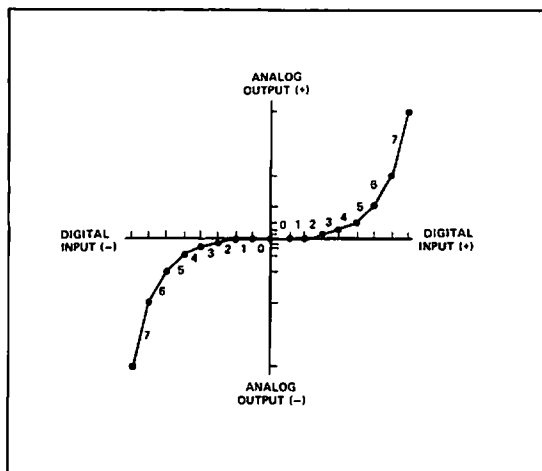
C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

**ENCODE TRANSFER CHARACTERISTICS
(A/D CONVERSION)**

**BASIC DECODE OPERATION
(EXPANDING D/A CONVERSION)**

D/A conversion with the DAC-88 is implemented by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the encode/decode input. This enables the $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the sign-bit input. When the sign-bit input is high, a logic "1", all of the output current flows into

$I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the sign-bit input is low, logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. The sign-bit steers current into $I_{OD}(+)$ or $I_{OD}(-)$, therefore the output will always be symmetrical, limited only by the matching of R1 and R2.

**DECODE TRANSFER CHARACTERISTIC
(D/A CONVERSION)**

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) ($I_{C,S} = 2[2^C(S + 16.5) - 16.5]$)

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2483	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

NORMALIZED TABLES

The encode and decode tables are used to calculate the ideal output current at any point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. $343/8031 \times I_{FS} = 85.75\mu A$ ($I_{FS} = 2007.75\mu A$). Alternatively, use the condensed current tables and add up the number of steps.

BASIC REFERENCE CONSIDERATIONS

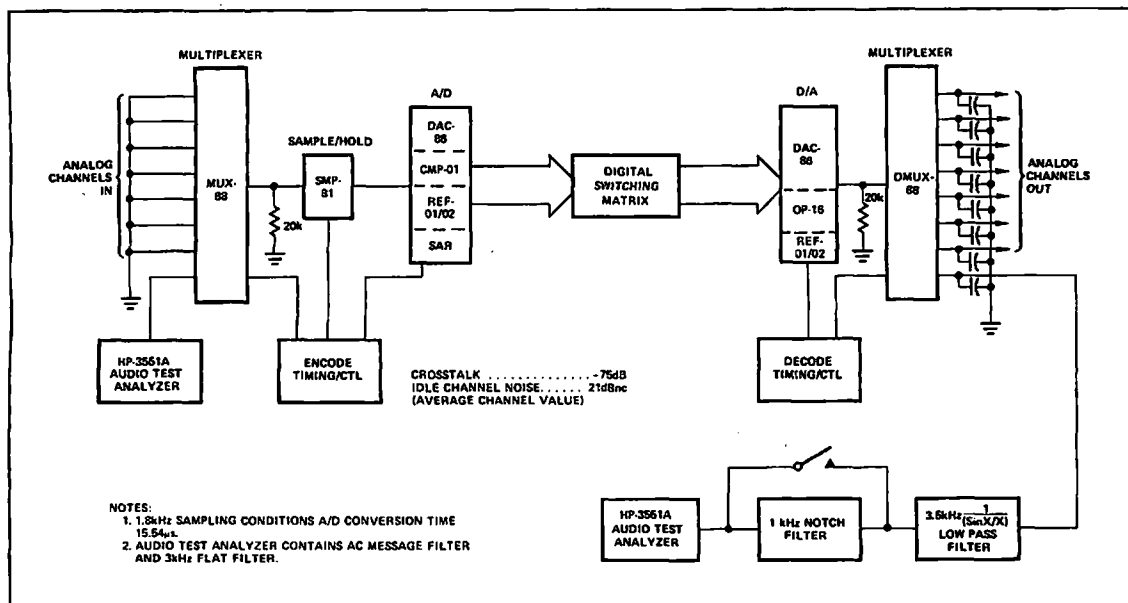
Full-scale output current is ideally $2007.75\mu A$ when the reference current is $528\mu A$ in the decode mode. In the encode mode $I_{FS} = 2039.75\mu A$ due to the additional 1/2 step ($32\mu A$). A percentage change in I_{REF} will produce the same percentage change in output current.

The large step size at full-scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with $V+ = 15V$, $R_{REF} = 15V/528\mu A$ or $28.4k\Omega$. When using a power supply as a reference, R11 becomes two resistors, R11A and R11B, and the junction bypassed to ground with a $0.1\mu F$ monolithic capacitor.

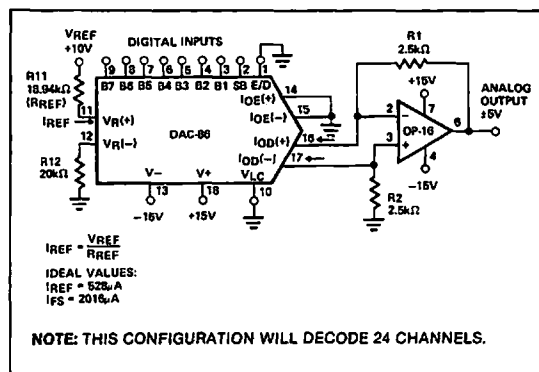
DECODE OUTPUT VOLTAGE

	E/D	S0	B1	B2	B3	B4	B5	B6	B7	VOLT
POS FULL-SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO-SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012
(+) ZERO-SCALE	0	1	0	0	0	0	0	0	0	0V
(-) ZERO-SCALE	0	0	0	0	0	0	0	0	0	0V
(-) ZERO-SCALE +1 STEP	0	0	0	0	0	0	0	0	1	-0.0012
NEG FULL-SCALE	0	0	1	1	1	1	1	1	1	-5.019V

SYSTEM TEST CIRCUIT



BASIC DECODE CONNECTIONS



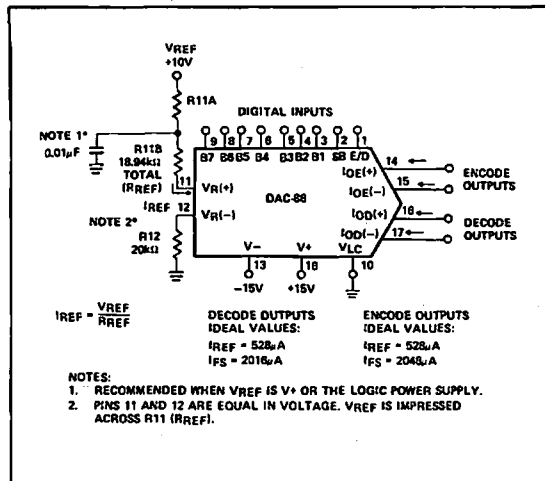
REFERENCE AMPLIFIER SETUP

The DAC-88 is a multiplying D/A converter. The output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full-scale output current is a linear function of the reference current.

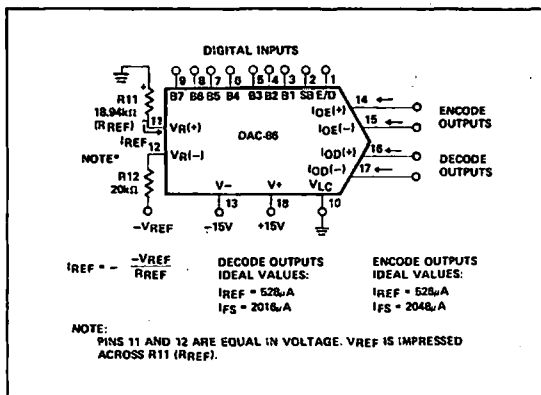
In external reference applications a positive reference voltage forces current through R11 in the $V_R(+)$ terminal (pin 11) of the reference amplifier. Alternatively, a negative reference may be applied to $V_R(-)$ at pin 12; reference current flows from ground through R11 into $V_R(+)$. This negative reference connection has the advantage of presenting a very high impedance at pin 12. The voltage at pin 11 is equal to and tracks the voltage at pin 12 due to the high gain of the internal

reference amplifier. R12 (nominally equal to R11) is used to cancel bias current errors and may be eliminated with a minor increase in error.

POSITIVE REFERENCE OPERATION



NEGATIVE REFERENCE OPERATION



REFERENCE AMPLIFIER OPERATION

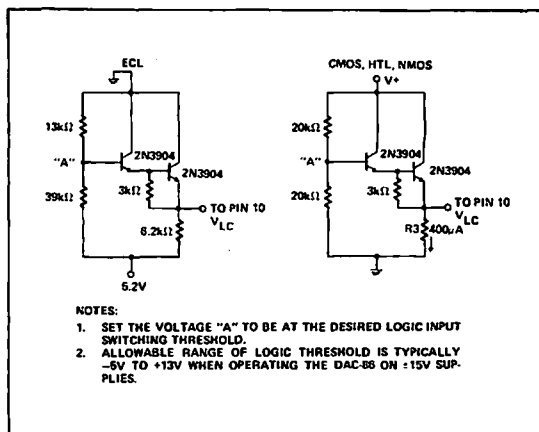
For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full-scale temperature performance. (This also minimizes the contributions of reference amplifier V_{OS} and TCV_{OS}). For most applications the tight relationship between I_{REF} and I_{FS} eliminates the need for trimming I_{REF} ; but if desired full-scale trimming is

accomplished by selecting R11 or by using a potentiometer for R11.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. While the recommended operating range of DC reference current is 0.1mA to 1.0mA, monotonic operation is maintained over an even wider range.

LOGIC INPUT AND POWER SUPPLY CONSIDERATIONS

INTERFACING CIRCUIT FOR ECL, CMOS, HTL, AND NMOS LOGIC INPUTS



LOGIC INPUTS

The DAC-86 interfaces with various logic families by referencing V_{LC} (pin 10) at a potential which is 1.4V below the desired logic input switching threshold. However, this voltage source must be capable of sourcing and sinking a changing current at pin 10.

The negative voltage at the logic inputs must be limited to +10V with respect to V₋ (pin 13).

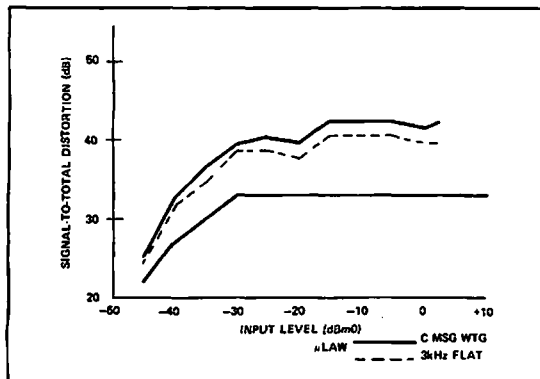
POWER SUPPLIES

Power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

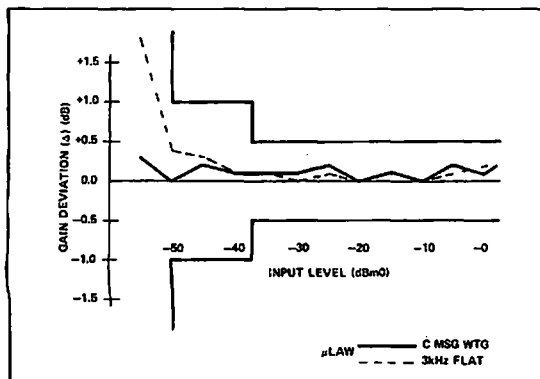
When operating with V_- between $-15V$ and $-11V$, output negative voltage compliance, $V_{OC(-)}$, reference input amplifier common-mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between $-15V$ and the V_- supply in use. Operation with V_+ between $+5V$ and $+15V$ affects V_{LC} and the reference amplifier common-mode positive voltage range in the same manner.

SYSTEM PERFORMANCE CHARACTERISTICS

SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL



GAIN TRACKING



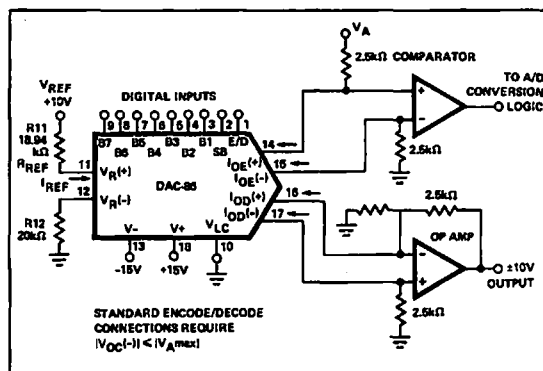
OUTPUT VOLTAGE COMPLIANCE

The DAC-88 has true current outputs with wide voltage compliance that enables single ended and balanced load drive capability. Positive voltage compliance is +18V and negative voltage compliance is -5.0V with $I_{REF} = 528\mu A$ and $V_- = -15V$. Negative voltage compliance $V_{OC(-)}$ for other values of I_{REF} and V_- may be obtained from the table, or calculated as follows:

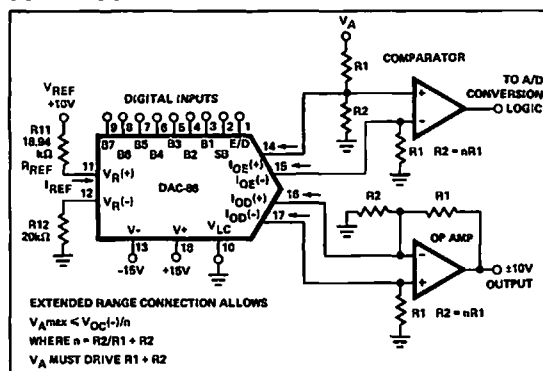
$$V_{OC(-)} \min = (V_-) + (2 I_{REF} \times 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the connections shown above.

STANDARD OUTPUT CONNECTIONS



OUTPUT COMPLIANCE EXTENSION CONNECTIONS



NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC(-)}$

V-	I_{FS}		
	1.0mA	2.0mA	4.0mA
-12V	-2.8V	-2.0V	-0.4V
-15V	-5.8V	-5.0V	-3.4V
-18V	-8.8V	-8.0V	-6.4V

MINIMUM NEGATIVE COMPLIANCE

$$V_{OC(-)} \min = (V_-) + (2 I_{REF} 1.6k\Omega) + 8.4V$$

DICE

For applicable DICE Information, see DAC-88 Data Sheet.



Precision Monolithics Inc.

DAC-88

COMDAC® COMPANDING
D/A CONVERTER [μ -255 LAW]

FEATURES

- **IMPROVED ACCURACY** over DAC-86
- **IMPROVED SPEED** over DAC-86
- **Conforms With Bell System μ -255 Companding Law**
- **Meets D3 Compander Tracking Specifications**
- **Both Encode and Decode Capability**
- **Tight Full-Scale Tolerance Eliminates Calibration**
- **Low Full-Scale Drift Over Temperature**
- **Extremely Low Noise Contribution**
- **Multiplying Reference Inputs**
- **Simplifies PCM System Design**
- **High Reliability**
- **Low Power Consumption and Low Cost**
- **Fully Specified Dice Available**

GENERAL DESCRIPTION

The DAC-88 monolithic COMDAC® D/A Converter provides a 15 segment linear approximation to the Bell System μ -255 companding law. The law is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. A sign bit determines signal polarity, and an encode/decode input determines the mode of operation.

Accuracy is assured by specifying chord end point values, step nonlinearity, and monotonicity over the full operating temperature range. Typical applications include PCM carrier systems, digital PBX's, intercom systems, and PCM recording. For CCITT "A" Law models, refer to the DAC-89 data sheet.

PIN CONNECTIONS & ORDERING INFORMATION

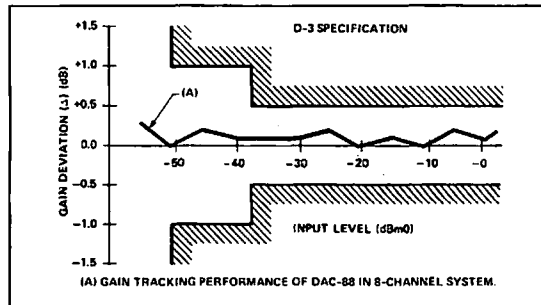
ENCODE/DECODE SELECT: 1 = ENCODE	1	E/D	V+	18	POSITIVE POWER SUPPLY
SIGN BIT INPUT: 1 = POSITIVE	2	S8	IOd(-)	17	DECODE OUT: E/D S8 = 00
MOST SIGNIFICANT CHORD BIT INPUT	3	B1	IOd(+)	16	DECODE OUT: E/D S8 = 01
SECOND CHORD BIT INPUT	4	B2	IOe(-)	15	ENCODE OUT: E/D S8 = 10
LEAST SIGNIFICANT CHORD BIT INPUT	5	B3	IOe(+)	14	ENCODE OUT: E/D S8 = 11
MOST SIGNIFICANT STEP BIT INPUT	6	B4	V-	13	NEGATIVE POWER SUPPLY
SECOND STEP BIT INPUT	7	B5	VR(-)	12	NEGATIVE REFERENCE INPUT
THIRD STEP BIT INPUT	8	B6	VR(+)	11	POSITIVE REFERENCE INPUT
LEAST SIGNIFICANT STEP BIT INPUT	9	B7	VLC	10	LOGIC THRESHOLD CONTROL

18-PIN HERMETIC DUAL-IN-LINE (X-Suffix)

Grade	Temp. Range	Accuracy
DAC-88EX†	-25°C/+85°C	± 1/4 Step

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GAIN TRACKING



BELL μ -255 LAW TRANSFER CHARACTERISTIC

The DAC-88 transfer characteristic is a piecewise linear approximation to the Bell System μ 255 law expressed by:

$$Y(x) = \text{sgn}(x) \frac{\ln(1 + \mu |x|)}{\ln(1 + \mu)} \quad -1 \leq x \leq 1$$

for a normalized coding range of ± 1

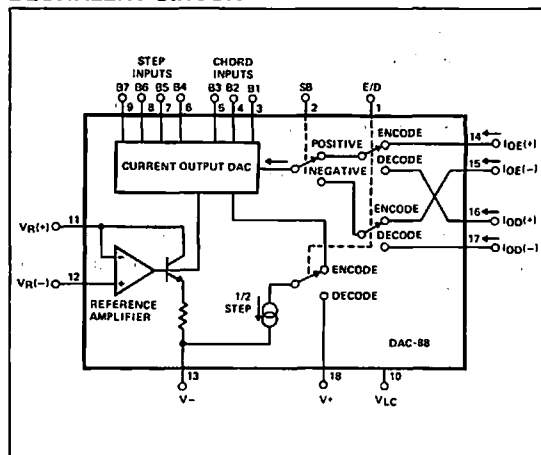
where: x = input signal level

Y = output compressed signal level

$\mu = 255$

This law is implemented with an eight chord (or segment) piecewise linear approximation with 16 linear steps in each chord. Dynamic range of 72dB in both polarities is achieved with eight-bit coding.

EQUIVALENT CIRCUIT





ABSOLUTE MAXIMUM RATINGS

V+ Supply to V- Supply	36V
V _{LC} Swing	V- plus 8V to V+
Analog Current Outputs	V- plus 8V to V- plus 36V
Reference Inputs	V- to V+
Reference Input Differential Voltage	±18V
Reference Input Current	1.25mA
Logic Inputs	V- plus 8V to V- plus 36V

Operating Temperature	-25°C to +85°C
Storage Temperature	-65°C to +150°C
Power Dissipation	500mW
Derate Above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, I_{REF} = 528μA, -25°C ≤ T_A ≤ +85°C, all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-88E			UNITS
			MIN	TYP	MAX	
Resolution		8 chords with 16 steps each	±128	±128	±128	Steps
Dynamic Range		20 log (I _{7,15} /I _{0,1})	72	72	72	dB
Monotonicity		Sign-Bit + or -	128	—	—	Steps
Chord End-Point Accuracy Chord Zero		Error relative to ideal values at I _{FS} = 2007.75μA	—	—	±1/4	Step
Chord End-Point Accuracy All Chords Other Than Zero		Error relative to ideal values at I _{FS} = 2007.75μA	—	—	±1/2	Step
Encode Decision Level Current		Additional output encode/decode = 1	3/8	1/2	5/8	Step
Settling Time (Note 1)	t _S	To within ±1/2 step	—	500	—	ns
Settling Time in Chord Zero	T _{SCO}	To within ±1/2 step	—	500	—	ns
Full-scale Drift (C ₇) (Note 3)	ΔI _{FS}	Full temperature range	—	±1/16	±1/10	Step
Output Voltage Compliance	V _{OC}	Full-Scale current change ≤ 1/2 step	-5	—	+18	Volts
Full-Scale Symmetry Error (Note 2)	I _{O(+)} - I _{O(-)}	Decode or encode pair Input Code 111 1111	—	±1/40	±1/8	Step
Zero-Scale Current (C ₀) (Note 2)	I _{ZS}	Measured at selected output with 000 0000 input	—	±1/40	±1/8	Step
Disable Current (All bits high) (Note 2)	I _{DIS}	Leakage of output disabled by E/D and SB	—	5	100	nA
Step Accuracy Chord Zero		Error relative to ideal values at I _{FS} = 2007.75μA	—	—	±1/4	Step
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at I _{FS} = 2016μA	—	—	±1/2	Step
Output Current Range	I _{FSR}		—	2.0	4.2	mA
Logic Input Levels, Logic "0"	V _{IL}	V _{LC} = 0V	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V _{IH}	V _{LC} = 0V	2	—	—	Volts
Logic Input Current	I _{IN}	V _{IN} = -5V to +18V	—	—	120	μA
Logic Input Swing	V _{IS}	V- = -15V	-5	—	+18	Volts
Reference Bias Current	I ₁₂		—	-3	-12	μA
Reference Input Slow Rate	dI/dt		—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	PSSI _{FS+}	V+ = 4.5V to 18V, V- = -15V	—	±1/20	±1/2	Step
	PSSI _{FS-}	V- = -10.8V to -18V, V+ = 15V	—	±1/10	±1/2	

NOTES:

- In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C₀) step size is 0.5μA, while in the last chord near full-scale (C₇) step size is 84μA. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading. In decode operation, the DAC-88 and OP-16 combination will decode 24 channels. In the encode mode, the

DAC-88 and CMP-01 combination will encode eight channels. Both encode and decode statements assume a 5.2μs channel time.

- Current specifications relate to differential currents between (+) and (-) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
- Guaranteed by design.

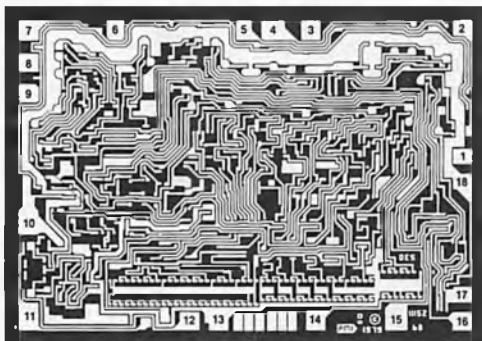


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25^\circ C \leq T_A \leq +85^\circ C$, all 4 outputs, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-88E			UNITS
			MIN	TYP	MAX	
Power Supply Current	I+	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	2.7	5.5	mA
	I-	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	-6.7	-12	
	I+	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	2.7	5.5	
	I-	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	-6.7	-12	
Power Dissipation	P_d	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	114	207	mW
		$V_S = \pm 15V, I_{FS} = 2.0mA$	—	141	262	
Full-Scale Current Deviation From Ideal Deviation (See Tables) (Note 2)	$I_{FS}(D)$	$V_{REF} = 10.000V, T_A = 25^\circ C$	—	—	$\pm 1/2$	Step
	$I_{FS}(E)$	$R_{11} = 19.53k\Omega, R_{12} = 20k\Omega$	—	—	$\pm 1/2$	
Idle Current (Note 2)	I_I		—	10	—	μA

NOTE:

2. Current specifications relate to differential currents between (+) and (-) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.

DICE CHARACTERISTICS

DIE SIZE 0.124×0.086 inch, 10,664 sq. mils
(3.150×2.184 mm, 6,880 sq. mm)

- | | |
|----------------|------------------|
| 1. E/D | 10. V_{LC} |
| 2. SIGN-BIT | 11. $V_R (+)$ |
| 3. BIT 1 (MSB) | 12. $V_R (-)$ |
| 4. BIT 2 | 13. V_- |
| 5. BIT 3 | 14. $I_{OE} (+)$ |
| 6. BIT 4 | 15. $I_{OE} (-)$ |
| 7. BIT 5 | 16. $I_{OD} (+)$ |
| 8. BIT 6 | 17. $I_{OD} (-)$ |
| 9. BIT 7 (LSB) | 18. V_+ |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25^\circ C$, all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-88N (NOTE 3) LIMIT	UNITS
Resolution		8 chords with 16 steps each	± 128	Steps MIN
Dynamic Range		$20 \log (I_{7,15}/I_{0,1})$	72	dB MIN
Monotonicity		Sign-Bit + or -	128	Steps MIN
Chord End-Point Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/4$	Step MAX
Chord End-Point Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/2$	Step MAX
Encode Decision Level Current		Additional output encode/decode = 1	3/8	Step MIN
			5/8	Step MAX
Output Voltage Compliance	V_{OC}	Full-scale current change $\leq 1/2$ step	-5	Volts MIN
			+18	Volts MAX



WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $T_A = 25^\circ C$, all 4 outputs, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-88N (NOTE 3) LIMIT	UNITS
Full-Scale Symmetry Error (Note 2)	$I_{O+} - I_{O-}$	Decode or encode pair Input Code 111 1111	$\pm 1/8$	Step MAX
Zero-Scale Current (Note 2)	I_{ZS}	Measured at selected output 000 0000 input	1/8	Step Max
Disable Current (All bits high) (Note 2)	I_{DIS}	Leakage of output disabled by E/D and SB	100	nA MAX
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/4$	Step MAX
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	$\pm 1/2$	Step MAX
Output Current Range	I_{FSR}		4.2	mA MIN
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	0.8	Volts MAX
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2	Volts MIN
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to $+18V$	120	μA MAX
Logic Input Swing	V_{IS}	$V_- = -15V$	-5 +18	Volts MIN Volts MAX
Reference Bias Current	I_{I2}		-12	μA MAX
Power Supply Sensitivity Over Supply Range	$PSS_{I_{FS-}}$ $PSS_{I_{FS+}}$	$V_+ = 4.5V$ to $18V$ $V_- = -10.8V$ to $-18V$	$\pm 1/2$ $\pm 1/2$	Step MAX Step MAX
Power Supply Current	I_+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.75	mA MAX
	I_-		-12.0	
	I_+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.75	mA MAX
	I_-		-12.0	
Full-Scale Current Deviation From Ideal Deviation	$I_{FS D}$	$V_{REF} 10.000V$, $T_A = 25^\circ C$	$\pm 1/2$	Step MAX
(See Tables) (Note 2)	$I_{FS E}$	$R_{11} = 19.53k\Omega$ $R_{12} = 20k\Omega$	$\pm 1/2$	Step MAX

NOTE:

Electrical tests performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

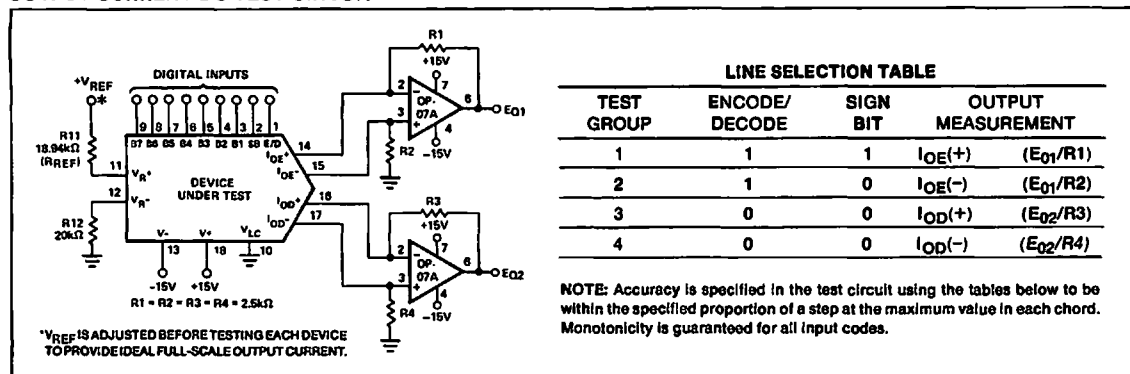
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-88N TYPICAL	UNITS
Settling Time (Note 1)	t_S	To within $\pm 1/2$ step	500	ns
Settling Time in Chord Zero	T_{SCO}	To within $\pm 1/2$ step	500	ns
Full-Scale Drift (C_7)	ΔI_{FS}	Full temperature range	$\pm 1/16$	Step
Reference Input Slew Rate	dI/dt		0.25	mA/ μs
Power Dissipation	P_D	$V_S +5V$, $-15V$	114	mW
	P_D	$V_S = \pm 15V$	141	mW
Idle Current (Note 2)	I_I		10	μA

NOTES:

- In a companding DAC, the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is $0.5\mu A$. While in the last chord near full-scale (C_7) step size is $64\mu A$. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading.
- Current specifications relate to differential currents between (+) and (-) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
- See DAC-88E for typical values.

OUTPUT CURRENT DC TEST CIRCUIT



CONDENSED CURRENT OUTPUT TABLES ($I_{REF} = 528\mu A$)

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.50	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.75	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

NOTE: These tables may be extended to include all of the encode/ decode currents (ideal with $I_{REF} = 528\mu A$) by multiplying any of the numbers in the normalized tables by $0.25\mu A$.

PARAMETER DEFINITIONS

FULL-SCALE DRIFT

The change in output current over the full operating temperature with $V_{REF} = 10.000V$, $R11 = 18.94k\Omega$, and $R12 = 20k\Omega$.

ENCODE CURRENT

The difference between $I_{OE}(+)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OD}(-)$ at any code.

FULL-SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full-scale output.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes $< 1/2$ step change in output current.

IDEAL OUTPUT CURRENT

The difference between the (+) and (-) currents (encode or decode) at any code.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord; used to specify accuracy.

STEPS

Increments in each chord which divides the chord into 16 equal levels.

OUTPUT LEVEL NOTATION

Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero-scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full-scale current.

DYNAMIC RANGE

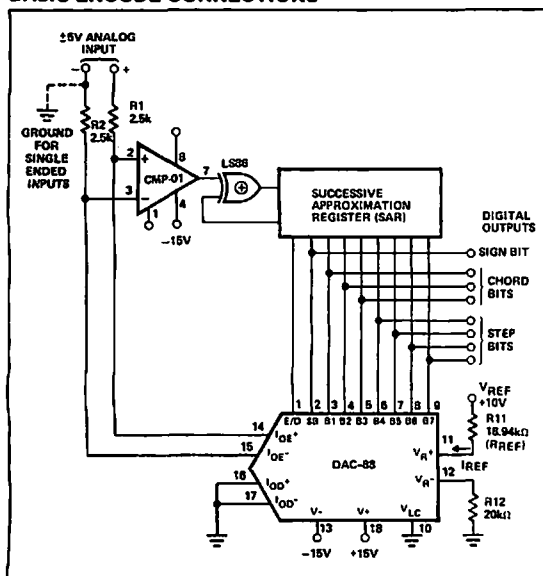
Ratio of full scale current to step size in chord zero, expressed in dB.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

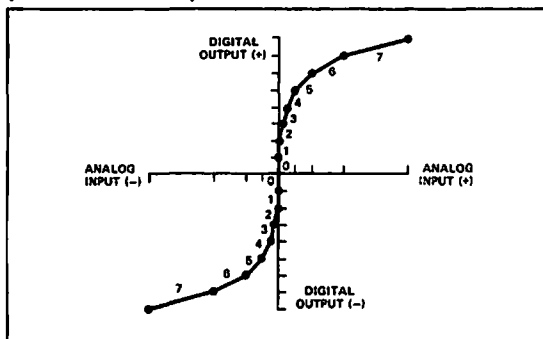
ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-88 requires a comparator, an EXCLUSIVE-OR gate, and a successive approximation register — the usual elements in any sign magnitude A/D converter. However, a compressing A/D has one significant difference. In a conventional (linear converter), the step size is a constant percentage of full-scale. In a compressing A/D converter, the step size increases as the output changes from zero-scale to full-scale.

BASIC ENCODE CONNECTIONS



ENCODE TRANSFER CHARACTERISTICS (A/D CONVERSION)



When the DAC is used in the feedback loop of a successive approximation analog to digital converter (ADC) the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode the outputs correspond to the center of the quantizing bands. The encode mode output exceeds the decode mode output by one-half step. See AN 39 for detailed explanation.

ENCODING SEQUENCE

An encoding sequence begins with the sign-bit decision. During this time the comparator functions as polarity detector only. The Encode/Decode (E/D) input is held at a logic "0". In this mode current flows into the decode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input toggles to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$.

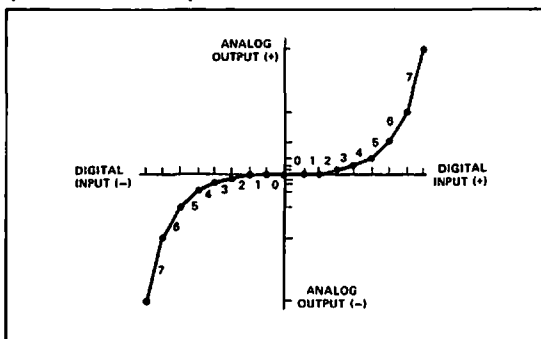
For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output is entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An EXCLUSIVE-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full-scale and all zeros for zero-scale.

The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made.

BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

D/A conversion with the DAC-88 is implemented by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This mode enables the $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the sign-bit input. When the sign-bit input is high, a logic "1", all of the output current flows into

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)





$I_{OP}(+)$ forcing a positive voltage at the operational amplifier's output. When the sign-bit input is low, logic "0", all of the output current flows into $I_{OP}(-)$ through R2 forcing a negative voltage output. The sign-bit steers current into $I_{OP}(+)$ or $I_{OP}(-)$, the output will therefore always be symmetrical, limited only by the matching of R1 and R2.

NORMALIZED TABLES

The encode and decode tables are used to calculate ideal output current at any point. For example, in decode mode at $I_{3.7}$ (011 011) find 343. 343/8031 $\times I_{FS} = 85.75\mu A$ ($I_{FS} = 2007.75\mu A$). Alternatively, use the condensed current tables and add up the number of steps.

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) ($I_{C,S} = 2[2^C(S + 17) - 16.5]$)

C = chord no. (0 through 7)
S = step no. (0 through 15)

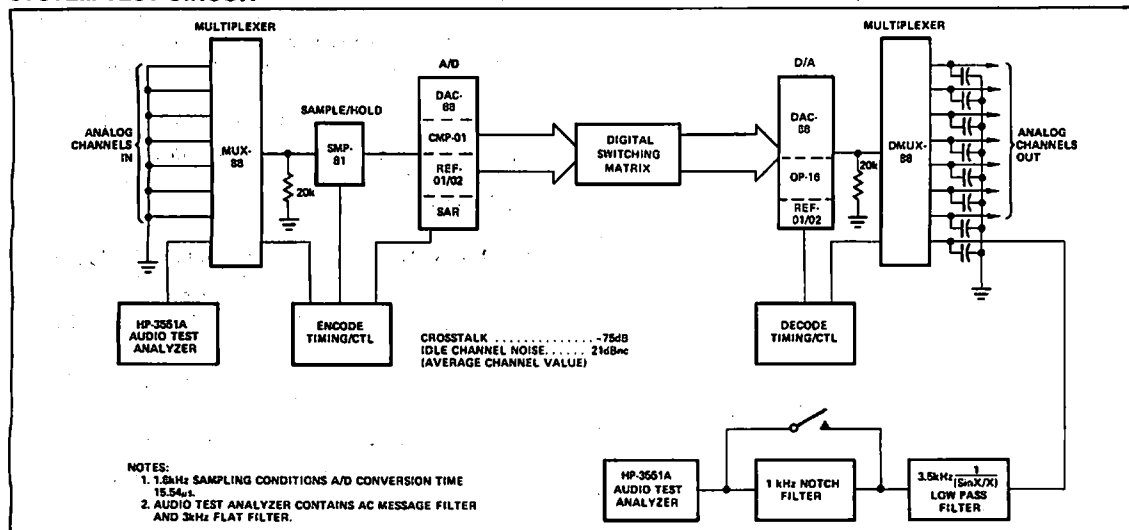
STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) ($I_{C,S} = 2[2^C(S + 16.5) - 16.5]$)

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4291
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	212	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

SYSTEM TEST CIRCUIT



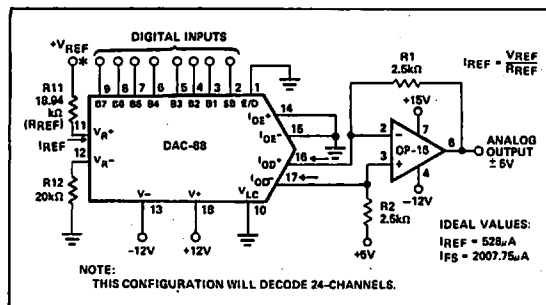
BASIC REFERENCE CONSIDERATIONS

Full-scale output current is ideally 2007.75μA when the reference current is 528μA in the decode mode. In the encode mode $I_{FS} = 2039.75\mu A$ due to the additional 1/2 step (32μA). A percentage change in I_{REF} will produce the same percentage change in output current.

DECODE OUTPUT VOLTAGE

	E/D	S8	B1	B2	B3	B4	B5	B6	B7	E ₀
POS FULL-SCALE	0	1	1	1	1	1	1	1	1	5.018V
(+) ZERO-SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO-SCALE	0	1	0	0	0	0	0	0	0	0V
(-) ZERO-SCALE	0	0	0	0	0	0	0	0	0	0V
(-) ZERO-SCALE +1 STEP	0	0	0	0	0	0	0	0	1	-0.0012V
NEG FULL-SCALE	0	0	1	1	1	1	1	1	1	-5.018V

BASIC DECODE CONNECTIONS



The large step size at full-scale allows the use of inexpensive references in many applications. In some applications V_{REF} may even be the positive power supply. For example, with $V+ = 15V$, $R_{REF} = 15V/528\mu A$ or 28.4kΩ. When using a power supply as a reference, R11 becomes two resistors, R11A and R11B, and the junction bypassed to ground with a 0.1μF monolithic capacitor.

REFERENCE AMPLIFIER OPERATION

The DAC-88 is a multiplying D/A converter. The output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full-scale output current is a linear function of the reference current and is given for all four outputs in the figures above.

REFERENCE RECOMMENDATIONS

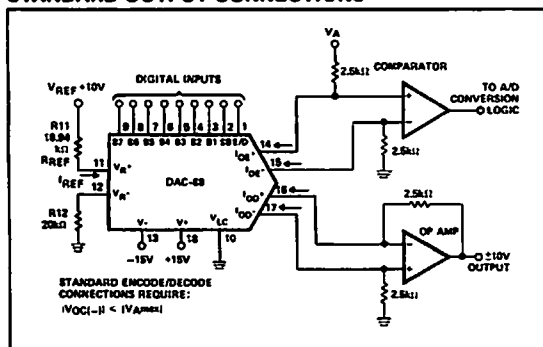
For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full-scale temperature performance.

POWER SUPPLIES

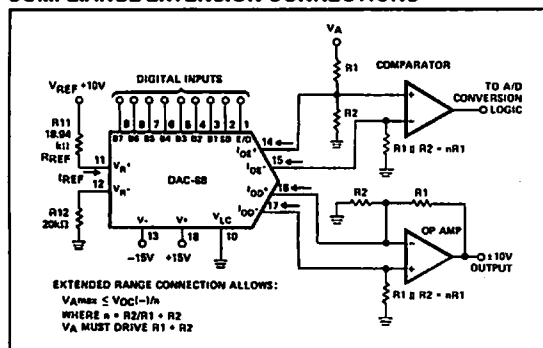
Power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

When operating with $V-$ between -15V and -11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common-mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between -15V and the $V-$ supply. Operation with $V+$ between +5V and +15V affects V_{LC} and the reference amplifier common-mode positive voltage range in the same manner.

STANDARD OUTPUT CONNECTIONS



COMPLIANCE EXTENSION CONNECTIONS

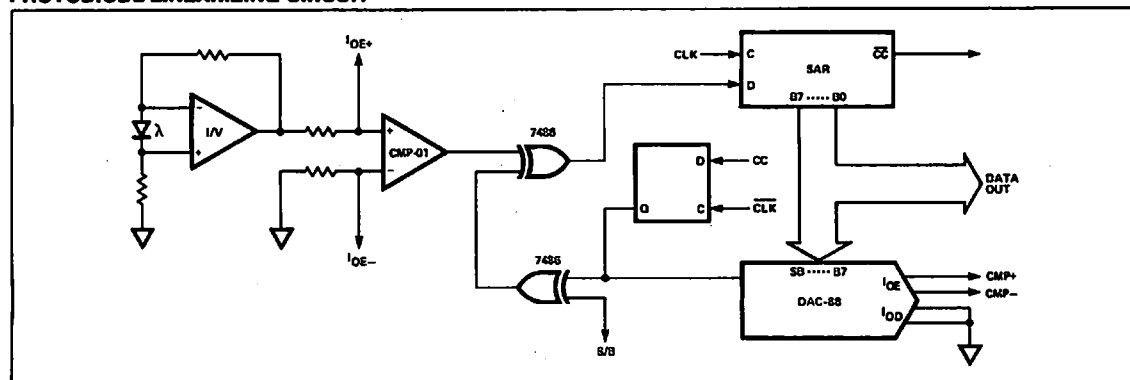


OUTPUT VOLTAGE COMPLIANCE

The DAC-88 has true current outputs with wide voltage compliance that enables single ended and balanced load driving

APPLICATIONS

PHOTODIODE LINEARIZING CIRCUIT



capability. Positive voltage compliance is +18V and negative voltage compliance is -5.0V with $I_{REF} = 528\mu A$ and $V = -15V$. Negative voltage compliance $V_{OC(-)}$ for other values of I_{REF} and V may be obtained from the table, or calculated as follows:

$$V_{OC(-)} \min = (V-) + (2 I_{REF} \times 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the connections shown in the compliance extension diagram.

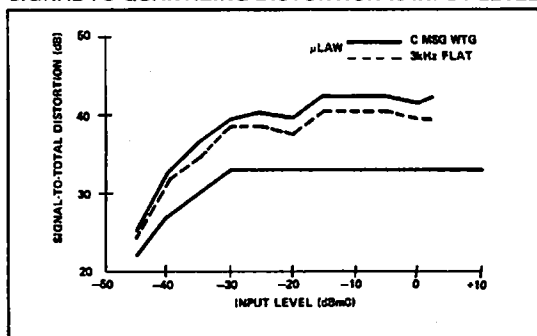
NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC(-)}$

$V-$	I_{FS} 1.0mA	I_{FS} 2.0mA	I_{FS} 4.0mA
-12V	-2.8V	-2.0V	-0.4V
-15V	-5.8V	-5.0V	-3.4V
-18V	-8.8V	-8.0V	-8.4V

MINIMUM NEGATIVE COMPLIANCE

$$V_{OC(-)} \min = (V-) + (2 I_{REF} 1.6k\Omega) + 8.4V$$

SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL





Precision Monolithics Inc.

DAC-89

COMDAC® COMPANDING
D/A CONVERTER ("A" LAW)

FEATURES

- 11-Bit Accuracy and Resolution Around Zero
- Sign Plus 66dB Dynamic Range
- True Current Outputs: -5V to +18V Compliance
- Tight Full-Scale Tolerance Eliminates Calibration
- Low Full-Scale Drift Over Temperature
- Low Power Consumption and Low Cost
- Ideal for PCM and 8-Bit μ P Applications
- Outputs Multiplexed for Time Shared Applications
- Fully Specified Dice Available

GENERAL DESCRIPTION

The DAC-89 monolithic COMDAC® converter provides the complete decode function for "A" Law PCM CODECs. The DAC-89 may be configured in an encoder, decoder, or time-shared between encoding and decoding.

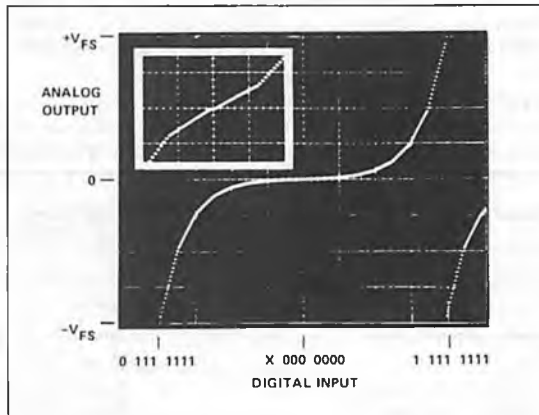
Specifying chord end-point values assures accuracy chord nonlinearity, and monotonicity over the full operating temperature range. For companding D/A converters with Bell μ -255 law conformance, refer to the DAC-88 data sheet. For industrial, process control, and audio applications, see the DAC-86 data sheet.

CCITT "A" LAW CHARACTERISTIC

The DAC-89 output is an approximation to the CCITT "A" law which can be expressed as:

$$Y = \frac{1 + \ln AX}{1 + \ln A} \quad 1/A \leq X \leq 1$$

COMDAC® TRANSFER CHARACTERISTIC



$$Y = \frac{AX}{1 + \ln A} \quad 0 \leq X \leq 1/A \text{ where:}$$

X = Normalized input signal level of the compressor (encoder), V_{IN}/V_{FS} .

Y = Output signal level of the compressor (encoder).

A = 87.6

The DAC-89 implements this law with an eight chord (or segment) piecewise linear approximation for each polarity with sixteen linear steps in each chord. The first two chords are co-linear and of equal step size, and may be considered as one chord of 32 steps. Step sizes of the remaining six chords are binarily related to the first chord.

PIN CONNECTIONS & ORDERING INFORMATION

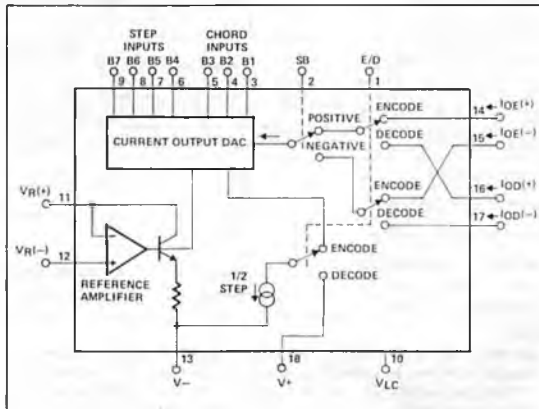
ENCODE/DECODE SELECT		1 = ENCODE		2 = DECODE	
SIGN BIT INPUT	1	SB	100(-)	17	DECODE OUT E/D SB - 00
MOST SIGNIFICANT CHORD BIT INPUT	2	B1	100(+)	16	DECODE OUT E/D SB - 01
SECOND CHORD BIT INPUT	3	B2	100(-)	15	ENCODE OUT E/D SB - 10
LEAST SIGNIFICANT CHORD BIT INPUT	4	B3	100(+)	14	ENCODE OUT E/D SB - 11
MOST SIGNIFICANT STEP BIT INPUT	5	B4	V-	13	NEGATIVE POWER SUPPLY
SECOND STEP BIT INPUT	6	B5	VR(-)	12	NEGATIVE REFERENCE INPUT
THIRD STEP BIT INPUT	7	B6	VR(+)	11	POSITIVE REFERENCE INPUT
LEAST SIGNIFICANT STEP BIT INPUT	8	B7	VLC	10	LOGIC THRESHOLD CONTROL

TOP VIEW
18-PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

GRADE	TEMP RANGE	ACCURACY
DAC-89EX†	-25°C/+85°C	± 1/4 step

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

EQUIVALENT CIRCUIT



DIGITAL-TO-ANALOG CONVERTERS

11

**ABSOLUTE MAXIMUM RATINGS**

V+ Supply to V- Supply 36V
 V_{LC} Swing V- plus 8V to V+
 Analog Current Outputs V- plus 8V to V- plus 36V
 Reference Inputs V- to V+
 Reference Input Differential Voltage $\pm 18V$
 Reference Input Current 1.25mA
 Logic Inputs V- plus 8V to V- plus 36V

Operating Temperature Range -25°C to +85°C
 Storage Temperature Range -65°C to +150°C
 Power Dissipation 500mW
 Derate Above 100°C 10mW/°C
 Lead Temperature (Soldering, 60 sec) 300°C

NOTE: Absolute ratings apply to both DICE and packaged parts unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_S = $\pm 15V$, I_{REF} = 512 μA , -25°C $\leq$ T_A $\leq$ +85°C, all 4 outputs, unless otherwise noted. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C₀) step size is 1.0 μA , while in the last chord near full-scale (C₇) step size is 64 μA .

PARAMETER	SYMBOL	CONDITIONS	DAC-89E			UNITS
			MIN	TYP	MAX	
Resolution		8 chords with 16 steps each	± 128	± 128	± 128	Steps
Dynamic Range		$20 \log (I_{7.5}/I_{0.0})$	66	—	66	dB
Monotonicity		Sign Bit + or -	128	—	—	Steps
Chord End-Point Accuracy Chord Zero		Error relative to ideal values at I _{FS} = 2016 μA	—	—	$\pm 1/4$	Step
Chord End-Point Accuracy All Chords Other Than Zero		Error relative to ideal values at I _{FS} = 2016 μA	—	—	$\pm 1/2$	Step
Step Accuracy Chord Zero		Error relative to ideal values at I _{FS} = 2016 μA	—	—	$\pm 1/4$	Step
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at I _{FS} = 2016 μA	—	—	$\pm 1/2$	Step
Encode Decision Level Current		Additional output Encode/Decode = 1	1/4	1/2	3/4	Step
Settling Time (Note 1)	t _s	To within $\pm 1/2$ step	—	500	—	ns
Full-Scale Drift (Note 3)	ΔI_{FS}	Full temperature range	—	$\pm 1/20$	$\pm 1/4$	Step
Output Voltage Compliance	V _{OC}	Full-scale current change $\leq 1/2$ step	-5	—	+18	Volts
Full-Scale Current Deviation from Ideal (See Tables) (Note 2)	I _{FS} (D)	V _{REF} 10.000V T _A = 25°C	—	—	$\pm 1/2$	Step
	I _{FS} (E)	R ₁₁ = 19.53k Ω , R ₁₂ = 20k Ω	—	—	$\pm 1/2$	Step
Full-Scale Symmetry Error (Note 2)	I _O (+) - I _O (-)	Decode or Encode pair	—	$\pm 1/40$	$\pm 1/8$	Step
Zero-Scale Current (Note 2)	I _{ZS}	Measured at selected output with 000 0000 input	1/4	1/2	3/4	Step
Disable Current (Note 2)	I _{OIS}	Disabled by E/D and SB	—	5.0	100	nA
Idle Current (Note 2)	I _I		—	10	—	μA
Output Current Range	I _{FSR}	V _{REF} = 25.000V T _A = 25°C	4.2	2.0	0	mA
Logic Input Levels, Logic "0"	V _{IL}	V _{LC} = 0V	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V _{IH}	V _{LC} = 0V	2.0	—	—	Volts
Logic Input Current	I _{IN}	V _{IN} = -5V to +18V	—	—	120	μA
Logic Input Swing	V _{IS}	V- = -15V	-5	—	+18	Volts
Reference Bias Current	I ₁₂		—	-3	-12	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	mA/ μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	PSSI _{FS+}	V+ = 4.5V to 18V, V- = -15V	—	$\pm 1/20$	$\pm 1/2$	Step
	PSSI _{FS-}	V- = -10.8V to -18V, V+ = 15V	—	$\pm 1/10$	$\pm 1/2$	

NOTES:

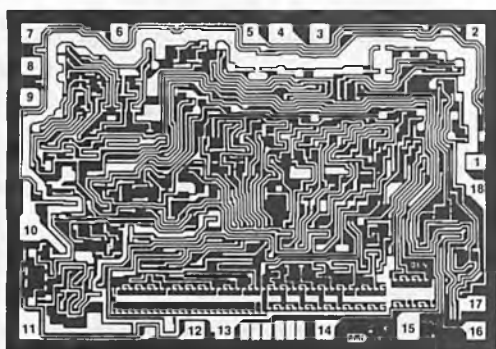
- Settling time varies for each of the chord bits and step bits and a maximum specification may be misleading. In decode operation, the DAC-89 and OP-16 combination will decode 8 channels. In the encode mode, the DAC-89 and CMP-01 combination will encode 8 channels. Both encode and decode statements assume a 3.9 μs channel time.
- Current specifications relate to differential currents between (+) and (-) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
- Guaranteed by design.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 512\mu A$, $-25^\circ C \leq T_A \leq +85^\circ C$, all 4 outputs, unless otherwise noted. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is $1.0\mu A$, while in the last chord near full-scale (C_7) step size is $64\mu A$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-89E			UNITS
			MIN	TYP	MAX	
Power Supply Current	I+	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	2.7	5.5	mA
	I-	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	-6.7	-12	
	I+	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	2.7	5.5	
	I-	$V_S = \pm 15V, I_{FS} = 2.0mA$	—	-6.7	-12	
Power Dissipation	P_d	$V_S = +5V, -15V, I_{FS} = 2.0mA$	—	114	207	mW
		$V_S = \pm 15V, I_{FS} = 2.0mA$	—	141	262	

DICE CHARACTERISTICS



DIE SIZE 0.123 × 0.085 inch, 10.455 sq. mils
(3.124 × 2.159 mm, 6.745 sq. mm)

- | | |
|----------------|------------------|
| 1. E/D | 10. V_{LC} |
| 2. SIGN-BIT | 11. $V_R (+)$ |
| 3. BIT 1 (MSB) | 12. $V_R (-)$ |
| 4. BIT 2 | 13. V^- |
| 5. BIT 3 | 14. $I_{OE} (+)$ |
| 6. BIT 4 | 15. $I_{OE} (-)$ |
| 7. BIT 5 | 16. $I_{OD} (+)$ |
| 8. BIT 6 | 17. $I_{OD} (-)$ |
| 9. BIT 7 (LSB) | 18. V^+ |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 512\mu A$, $T_A = 25^\circ C$, all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-89N (NOTE 3) LIMIT	UNITS
Resolution		8 chords with 16 steps each	± 128	Steps MIN
Dynamic Range		$20 \log (I_{7-15}/I_{0-1})$	66	dB MIN
Monotonicity		Sign-Bit + or -	128	Steps MIN
Chord End-point Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/4$	Step MAX
Chord End-point Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/2$	Step MAX
Encode Decision Level Current		Additional output encode/decode = 1	1/4 3/4	Step MIN Step MAX
Output Voltage Compliance	V_{OC}	Full-scale current change $\leq 1/2$ step	-5 +18	Volts MIN Volts MAX
Full-Scale Symmetry Error (Note 2)	$I_{O+} - I_{O-}$	Decode or encode pair Input Code 111 1111	$\pm 1/8$	Step MAX
Zero-Scale Current (Note 2)	I_{ZS}	Measured at selected output 000 0000 input	1/4	Step Max
Disable Current (All bits high) (Note 2)	I_{DIS}	Leakage of output disabled by E/D and SB	100	nA MAX



WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 512\mu A$, $T_A = 25^\circ C$, all 4 outputs, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-89N (NOTE 3) LIMIT	UNITS
Step Accuracy Chord Zero		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	$\pm 1/4$	Step MAX
Step Accuracy All Chords Other Than Zero		Error relative to ideal values at $I_{FS} = 2016\mu A$	$\pm 1/2$	Step MAX
Output Current Range	I_{FSR}	$V_{REF} = 25.000V$, $T_A = 25^\circ C$	4.2	mA MIN
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	0.8	Volts MAX
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2	Volts MIN
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to $+18V$	120	μA MAX
Logic Input Swing	V_{IS}	$V = -15V$	-5 +18	Volts MIN Volts MAX
Reference Bias Current	I_{12}		-12	μA MAX
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS-}$ $PSSI_{FS-}$	$V^+ = 4.5V$ to $18V$ $V^- = 10.8V$ to $-18V$	$\pm 1/2$ $\pm 1/2$	Step MAX Step MAX
Power Supply Current	I^+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.5	mA MAX
	I^-		-12.0	
	I^+	$V_S = \pm 15V$, $I_{FS} = 2.0mA$	5.75	mA MAX
	I^-		-12.0	
Full-Scale Current Deviation From Ideal Deviation	I_{FSD}	$V_{REF} = 10.000V$, $T_A = 25^\circ C$	$\pm 1/2$	Step MAX
(See Tables) (Note 2)	I_{FSE}	$R_{11} = 19.53k\Omega$ $R_{12} = 20k\Omega$	$\pm 1/2$	Step MAX

NOTE:

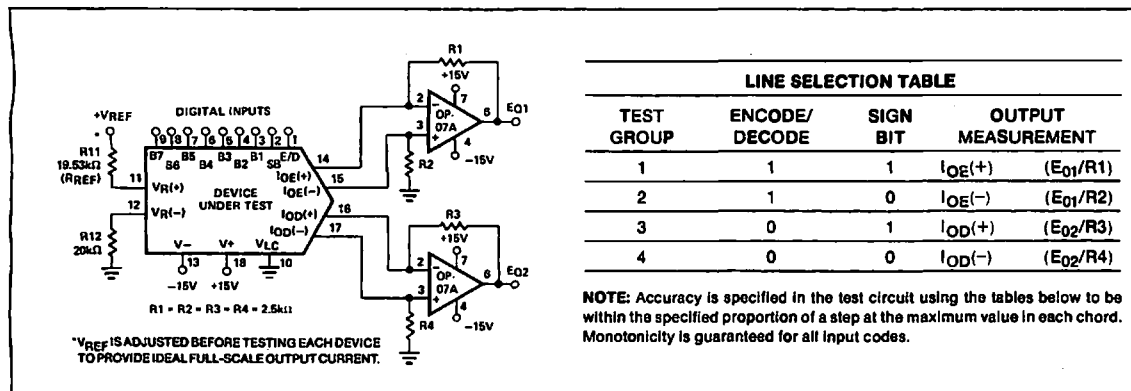
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-89N TYPICAL	UNITS
Settling Time (Note 1)	t_S	To within $\pm 1/2$ step	500	ns
Settling Time in Chord Zero	T_{SCO}	To within $\pm 1/2$ step	500	ns
Full-Scale Drift (C_7)	ΔI_{FS}	Full temperature range	$\pm 1/20$	Step
Reference Input Slew Rate	dI/dt		0.25	mA/ μs
Power Dissipation	P_D	$V_S + 5V$, $-15V$	114	mW
	P_D	$V_S = \pm 15V$	141	mW
Idle Current (Note 2)	I_I		10	μA

NOTES:

1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is $0.5\mu A$. While in the last chord near full-scale (C_7) step size is $64\mu A$. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading.
2. Current specifications relate to differential currents between (+) and (-) output leads. At the selected outputs, equal idle currents are present simultaneously on both current output leads.
3. See DAC-89E for typical values.

OUTPUT CURRENT DC TEST CIRCUIT

CONDENSED CURRENT OUTPUT TABLES
IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD \ STEP		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0.5	16.5	33	66	132	264	528	1056
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

CHORD \ STEP		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	17	34	68	136	272	544	1088
15	1111	16	32	64	128	256	512	1024	2048
STEP SIZE		1	1	2	4	8	16	32	64

NOTE:

These tables may be extended to include all of the encode/decode currents (ideal with $I_{REF} = 512\mu A$) by multiplying any of the numbers in the normalized tables by $0.5\mu A$.

PARAMETER DEFINITIONS
STEP NONLINEARITY

Step size deviation from ideal within a chord.

ENCODE CURRENT

The difference between $I_{OE}(+)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OD}(-)$ at any code.

FULL-SCALE DRIFT

The change in output current over the full operating temperature with $V_{REF} = 10.000V$, $R_{11} = 19.53k\Omega$, and $R_{12} = 20k\Omega$.

FULL-SCALE SYMMETRY ERROR

The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full-scale output.

IDEAL OUTPUT CURRENT

The difference between the (+) and (-) currents (encode or decode) at any code.

OUTPUT VOLTAGE COMPLIANCE

The maximum output voltage swing at any current level which causes $< 1/2$ step change in output current.

CHORDS

Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS

The maximum code in each chord; used to specify accuracy.

STEPS

Increments in each chord which divides the chord into 16 equal levels.

OUTPUT LEVEL NOTATION

Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero-scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full-scale current.

DYNAMIC RANGE

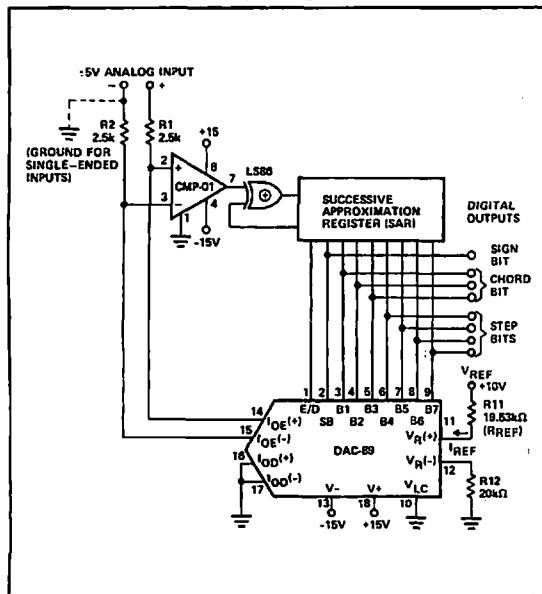
Ratio of full-scale current to step size in chord zero expressed in dB.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

ENCODING SEQUENCE

An encoding sequence begins with the sign-bit decision. During this time the comparator functions as a polarity detector only. The Encode/Decode (E/D) input is held at logic "0". In this mode current flows into the decode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input toggles "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$.

BASIC DECODE CONNECTIONS



For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output is entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An EXCLUSIVE-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full-scale and all zeros for zero-scale.

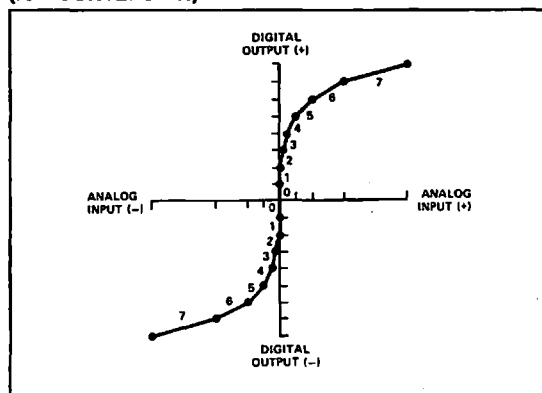
The bits are converted with a successive removal technique starting with a decision at the code 011 1111 and sequentially turning off bits until all decisions have been made.

ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-89 requires a comparator, an EXCLUSIVE-OR gate, and a successive approximation register — the usual elements in any sign-magnitude A/D converter. However, a compressing A/D has one significant difference. In a conventional (linear) converter, the step size is a constant percentage of full scale, but in a compressing A/D converter, the step size increases as the output changes from zero-scale to full-scale.

When the DAC is used in the feedback loop of a successive approximation analog to digital converter (ADC), the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode the outputs correspond to the center of the quantizing bands. The encode mode output exceeds the decode mode output by one-half step. See AN 39 for detailed explanation.

ENCODE TRANSFER CHARACTERISTIC (A/D CONVERSION)



NORMALIZED ENCODE DECISION LEVELS (SIGN-BIT EXCLUDED)

NORMALIZED ENCODE DECISION

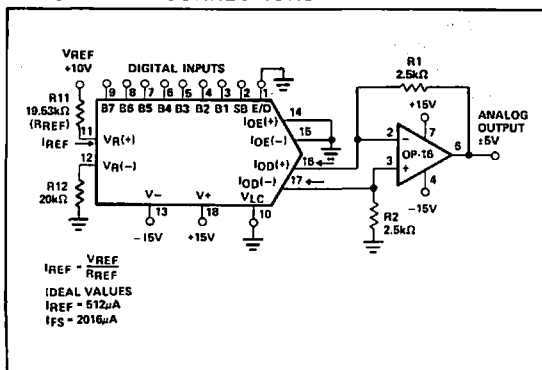
CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	2	34	68	136	272	544	1088	2176
1	0001	4	38	72	144	288	576	1152	2304
2	0010	6	38	76	152	304	608	1216	2432
3	0011	8	40	80	160	320	640	1280	2560
4	0100	10	42	84	168	336	672	1344	2688
5	0101	12	44	88	176	352	704	1408	2816
6	0110	14	46	92	184	368	736	1472	2944
7	0111	16	48	96	192	384	768	1536	3072
8	1000	18	50	100	200	400	800	1600	3200
9	1001	20	52	104	208	416	832	1664	3328
10	1010	22	54	108	216	432	864	1728	3456
11	1011	24	56	112	224	448	896	1792	3584
12	1100	26	58	116	232	464	928	1856	3712
13	1101	28	60	120	240	480	960	1920	3840
14	1110	30	62	124	248	496	992	1984	3968
15	1111	32	64	128	256	512	1024	2048	4096
STEP SIZE		2	2	4	8	16	32	64	128

*Virtual Decision Level

BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

D/A conversion with the DAC-89 is implemented by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the Encode/Decode input. This mode enables the I_{OD} outputs, disables the I_{OE} outputs, and allows $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the sign-bit input. When the sign-bit input is high, logic "1", the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the sign-bit input is low, logic "0", the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. The sign-bit steers current into $I_{OD}(+)$ or $I_{OD}(-)$, the output will therefore always be symmetrical, limited only by the matching of R1 and R2.

BASIC DECODE CONNECTIONS

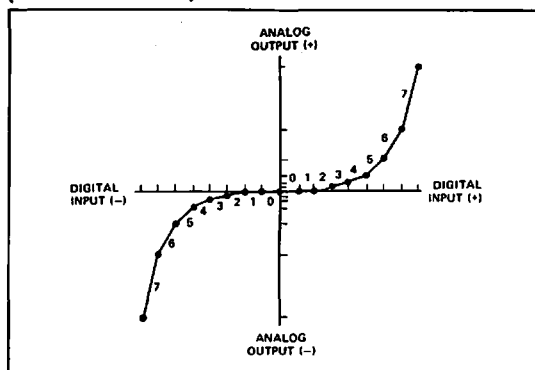


NORMALIZED TABLES

The encode and decode tables are used to calculate ideal output current at any code point. For example, in decode mode at $I_{3,7}$ (011 0111) find 188. 188/4032 times I_{FS} of $2016\mu A$ equals $94\mu A$.

	E/D	S8	B1	B2	B3	B4	B5	B6	B7	E_0
POS FULL-SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO-SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012V
(+) ZERO-SCALE	0	1	0	0	0	0	0	0	0	0.004V
(-) ZERO-SCALE	0	0	0	0	0	0	0	0	0	0.004V
(-) ZERO-SCALE +1 STEP	0	0	0	0	0	0	0	0	1	-0.0012V
NEG FULL-SCALE	0	0	1	1	1	1	1	1	1	-5.040V

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



**NORMALIZED DECODE OUTPUT (SIGN-BIT EXCLUDED)****NORMALIZED DECODE OUTPUT**

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	472	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	6	16	32	64	128

BASIC REFERENCE CONSIDERATIONS

Full-scale output current is ideally 2016 μ A when the reference current is 512 μ A in the decode mode. In the encode mode $I_{FS} = 2048\mu$ A due to the additional one-half step (32 μ A). A percentage change in I_{REF} caused by changes in V_{REF} or R_{REF} will produce the same percentage change in output current.

The large step size at full scale allows the use of inexpensive references in many applications. In some applications V_{REF} may even be the positive power supply. For example, with $V+ = 15V$, $R_{REF} = 15V/512\mu A$ or 29.3k Ω . When using a power supply as a reference, R11 should be two resistors, R11A and R11B, and the junction bypassed to ground to provide decoupling.

OUTPUT VOLTAGE COMPLIANCE

The DAC-89 has true current outputs with wide voltage compliance that enables single ended and balanced load driving capability. Positive voltage compliance is +18V and negative voltage compliance is -5.0V with $I_{REF} = 512\mu A$ and $V = -15V$. Negative voltage compliance $V_{OC(-)}$ for other values of I_{REF} and $V-$ may be obtained from the table, or calculated as follows:

$$V_{OC(-)} \text{ min} = (V-) + (2 I_{REF} \times 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the output compliance extension connections. (Figures 1 and 2).

NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC(-)}$

$V-$	1.0mA	I_{FS} 2.0mA	4.0mA
-12V	-2.8V	-2.0V	-0.4V
-15V	-5.8V	-5.0V	-3.4V
-18V	-8.8V	-8.0V	-6.4V

MINIMUM NEGATIVE COMPLIANCE

$$V_{OC(-)} \text{ MIN} = (V-) + (2 I_{REF} 1.6k\Omega) + 8.4V$$

IDLE OUTPUT CURRENT

In the selected output state (encode or decode), equivalent idle currents are present on the (+) and (-) output leads. The output will be symmetrical with the external resistor matching determining the overall system accuracy.



OUTPUT COMPLIANCE EXTENSION CONNECTIONS

STANDARD ENCODE/DECODE CONNECTIONS

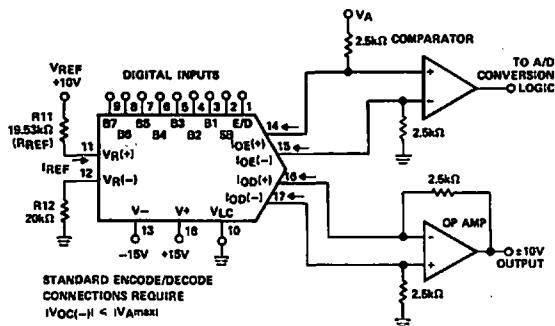


Figure 1

EXTENDED RANGE CONNECTIONS

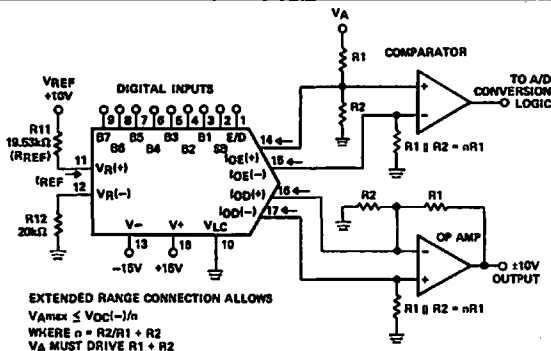


Figure 2

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS (SIGN-BIT EXCLUDED)

IDEAL DECODE OUTPUT

STEP	CHORD	0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0.5	18.5	33	88	132	264	528	1056
1	0001	1.5	17.5	35	70	140	280	560	1120
2	0010	2.5	18.5	37	74	148	296	592	1184
3	0011	3.5	19.5	39	78	156	312	624	1248
4	0100	4.5	20.5	41	82	164	328	656	1312
5	0101	5.5	21.5	43	86	172	344	688	1376
6	0110	6.5	22.5	45	90	180	360	720	1440
7	0111	7.5	23.5	47	94	188	376	752	1504
8	1000	8.5	24.5	49	98	196	392	784	1568
9	1001	9.5	25.5	51	102	204	408	816	1632
10	1010	10.5	26.5	53	106	212	424	848	1696
11	1011	11.5	27.5	55	100	220	440	880	1760
12	1100	12.5	28.5	57	114	228	456	912	1824
13	1101	13.5	29.5	59	118	236	472	944	1888
14	1110	14.5	30.5	61	122	244	488	976	1952
15	1111	15.5	31.5	63	126	252	504	1008	2016
STEP SIZE		1	1	2	4	8	16	32	64



DAC-100

10-BIT CURRENT-OUTPUT D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- Fast Settling 225nsec (8 Bits), 375nsec (10 Bits)
- Stable Tempcos to $\pm 15\text{ppm}/^\circ\text{C}$ Max
- Commercial, Industrial and Military Models Available
- TTL Compatible Logic Inputs
- Wide Supply Range $\pm 6\text{V}$ to $\pm 18\text{V}$

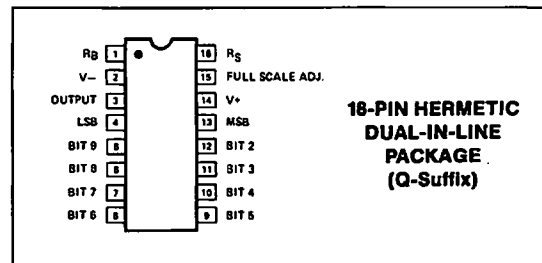
GENERAL DESCRIPTION

The DAC-100 is a complete 10-bit resolution digital-to-analog converter constructed on two monolithic chips in a single 16-pin DIP. Featuring excellent linearity vs. temperature performance, the DAC-100 includes a low tempco voltage reference, ten current source/switches and a high stability thin-film R-2R ladder network. Maximum application flexibility is provided by the fast current output, matched bipolar offset and feedback resistors. Resistors are included for use with an external op amp for voltage output applications.

Although all units have 10-bit resolution, a wide choice of linearity and temperature coefficient options are provided to allow price/performance optimization.

The small size, wide operating temperature range, and high reliability construction make the DAC-100 ideal for aerospace applications. Other applications include use in servo-positioning systems, X-Y plotters, CRT displays, programmable power supplies, analog meter movement drivers, waveform generators and high speed analog-to-digital converters.

PIN CONNECTIONS



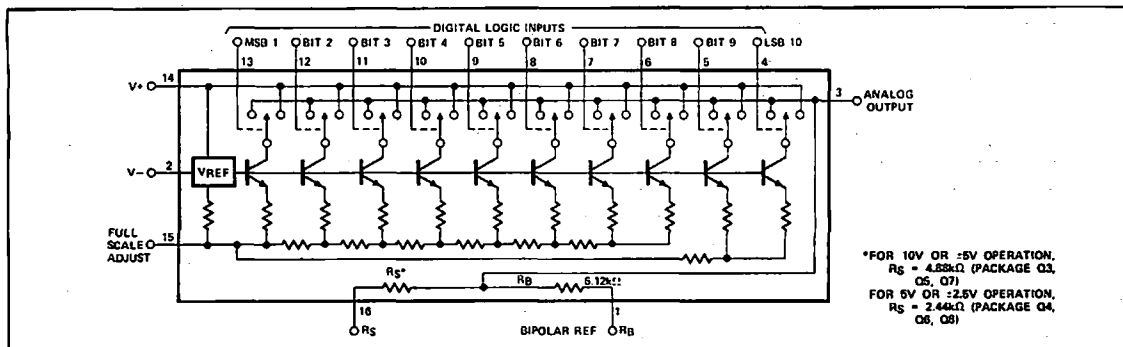
ORDERING INFORMATION†

N.L.* %FS MAX	TEMPCO* ppm/°C MAX	MILITARY TEMPERATURE		INDUSTRIAL TEMPERATURE		COMMERCIAL TEMPERATURE	
		$V_O = \pm 5\text{V}/10\text{V}$	$V_O = \pm 2.5\text{V}/5\text{V}$	$V_O = \pm 5\text{V}/10\text{V}$	$V_O = \pm 2.5\text{V}/5\text{V}$	$V_O = \pm 5\text{V}/10\text{V}$	$V_O = \pm 2.5\text{V}/5\text{V}$
± 0.05	± 15	—	—	DAC100AAQ7	DAC100AAQ8	—	—
± 0.05	± 30	—	—	DAC100ABQ7	DAC100ABQ8	—	—
± 0.05	± 60	DAC100ACQ5/883	DAC100ACQ6/883	DAC100ACQ7	DAC100ACQ8	DAC100ACQ3	DAC100ACQ4
± 0.10	± 30	DAC100BBQ5/883	—	DAC100BBQ7	DAC100BBQ8	—	—
± 0.10	± 60	DAC100BCQ5/883	—	DAC100BCQ7	—	DAC100BCQ3	DAC100BCQ4
± 0.10	± 120	—	—	—	—	—	—
± 0.20	± 60	DAC100CCQ5/883	DAC100CCQ6/883	DAC100CCQ7	—	DAC100CCQ3	DAC100CCQ4
± 0.20	± 120	—	—	—	—	—	—
± 0.30	± 120	—	—	DAC100DDQ7	—	DAC100DDQ3	—

*Part number construction: The 1st letter following DAC-100 (A-D) refers to the nonlinearity specification; the 2nd letter (A-D) refers to the full-scale tempco; the letter Q refers to the package; and the end numeral indicates the output voltage and temperature.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS** (Note 2)

V+ Supply to V- Supply	0 to +36V
V+ Supply to Output	0 to +18V
V- Supply to Output	0 to -18V
Logic Inputs to Output	-1V to +6V
Power Dissipation (Note 1)	500mW
Operating Temperature Range Q3, Q4	0°C to +70°C
Q5, Q6, Q7, Q8	-55°C to +125°C

DICE Junction Temperature	-25°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

NOTES:

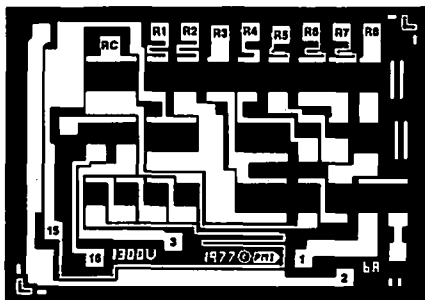
1. Rating applies to ambient temperature of 100°C. Above 100°C, derate at 10mW/°C.
2. Ratings apply to DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-25^\circ C \leq T_A \leq +85^\circ C$ for Q7 and Q8 devices; $0^\circ C \leq T_A \leq +70^\circ C$ for Q3 and Q4; $-55^\circ C \leq T_A \leq +125^\circ C$ for Q5 and Q6 devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-100	MIN	TYP	MAX	UNITS
Resolution				10	—	—	Bits
Nonlinearity (For nonlinearity/tempco combinations, see Ordering Information)	NL	($\pm 1/2$ LSB — 10 bits)	A—	—	—	± 0.05	%FS
		($\pm 1/2$ LSB — 9 bits)	B—	—	—	± 0.1	
		($\pm 1/2$ LSB — 8 bits)	C—	—	—	± 0.2	
		($\pm 3/4$ LSB — 8 bits)	D—	—	—	± 0.3	
Full-Scale Tempco (See Full-Scale Test Circuit)	T_C		—A	—	—	± 15	ppm/°C
			—B	—	—	± 30	
			—C	—	—	± 60	
			—D	—	—	± 120	
Settling Time $T_A = 25^\circ C$	t_S	to $\pm 0.05\%$ FS	ALL	—	—	375	ns
		to $\pm 0.1\%$ FS	ALL	—	—	300	
		to $\pm 0.2\%$ FS	ALL	—	—	225	
		to $\pm 0.4\%$ FS	ALL	—	—	150	
		to $\pm 0.8\%$ FS	ALL	—	—	100	
Full-Range Output Voltage (Limits guarantee adjustability to exact 10.0 (5.0)V with a 200 Ω Trimpot® between Adjust and V-)	V_{FR}	Connect FS Adjust to V- 10V Models (Q3, Q5, Q7) (See Full-Scale Test Circuit) 5V Models (Q4, Q6, Q8) $V_{IN} = 0.7V$ (See Basic Unipolar Voltage Output Circuit)		10	—	11.1	V
				5	—	5.55	
Zero-Scale Output Voltage	V_{ZS}	$V_{IN} = 2.1V$	ALL	—	—	0.013	%FS
Logic Inputs: High	V_{INH}	Measured with respect to output pin	ALL	2.1	—	—	V
Logic Inputs: Low	V_{INL}	Measured with respect to output pin	ALL	—	—	0.7	V
Logic Input Current, Each Input	I_{IN}	$V_{IN} = 0$ to +6V	ALL	—	—	5	μA
Logic Input Resistance	R_{IN}	$V_{IN} = 0$ to +8V	ALL	—	3	—	m Ω
Logic Input Capacitance	C_{IN}		ALL	—	2	—	pF
Output Resistance	R_O		ALL	—	500	—	k Ω
Output Capacitance	C_O		ALL	—	13	—	pF
Applied Power Supplies: V+			ALL	+6	—	+18	V
Applied Power Supplies: V-			ALL	-6	—	-18	V
Power Supply Sensitivity	P_{SS}	$V_S = \pm 6V$ to $\pm 18V$	ALL	—	—	± 0.10	% per Volt
Power Consumption	P_D	$V_S = \pm 15V$	Q3, Q4	—	200	300	mW
		$V_S = \pm 6V$	Q3, Q4	—	80	—	
		$V_S = \pm 15V$	Q5, Q6, Q7, Q8	—	200	250	
Positive Supply Current	I_+	$V_S = +15V$	Q3, Q4	—	—	10	mA
		$V_S = +15V$	Q5, Q6, Q7, Q8	—	—	8.33	
Negative Supply Current	I_-	$V_S = -15V$	Q3, Q4	—	—	-10	mA
		$V_S = -15V$	Q5, Q6, Q7, Q8	—	—	-8.33	

DICE CHARACTERISTICS

DAR-01



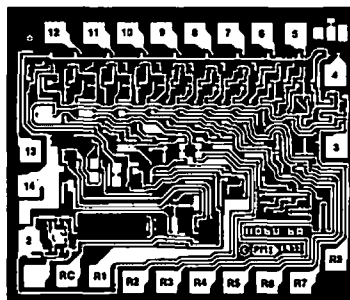
DIE SIZE .090 × .064 Inch, 5760 sq. mils
(2.286 × 1.701 mm, 3.888 sq. mm)

- 1. R_8
- 2. V^-
- 3. OUTPUT
- 15. FULL-SCALE ADJ
- 16. R_8

R — Pads are connected to similarly marked pads on DAI-01

Note: Pads 4 — 14, See DAI-01

DAI-01



DIE SIZE 0.111 × 0.064 Inch, 7104 sq. mils
(2.819 × 1.626 mm, 4.584 sq. mm)

- 2. V^-
- 3. OUTPUT
- 4. BIT 10 (LSB)
- 5. BIT 9
- 6. BIT 8
- 7. BIT 7
- 8. BIT 6
- 9. BIT 5
- 10. BIT 4
- 11. BIT 3
- 12. BIT 2
- 13. BIT 1 (MSB)
- 14. V^+

R — Pads are connected to similarly marked pads on DAR-01

Note: Pads 1, 2, 15, 16, See DAR-01

These die versions are available on special order; contact your PMI sales office.

WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$ for the R-2R Ladder Network comprised of R1—R8, R12, R23, R34, R45 and R56 when connected to an ideal DAI-01, unless otherwise noted.

PARAMETER	CONDITIONS	DAR-01-N			DAR-01-G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Nonlinearity	$VR1 = 3.2V$	—	—	±0.035	—	—	±0.05	%

WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$, $VR1 = 3.2V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAR-01			UNITS
		MIN	TYP	MAX	
Resistance R1	Absolute Measurement	2.56	—	3.84	k Ω
Ratio RC1 to R1	Ideal = 1.00503 to 1	-1	—	+1	%
Ratio R1 to RS1	Ideal = 1.29959 to 1	-1	—	+1	%
Ratio R1 to RS2	Ideal = 1.29959 to 1	-1	—	+1	%
Ratio RB to R1	Ideal = 1.92211 to 1	-1	—	+1	%

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

**TYPICAL ELECTRICAL CHARACTERISTICS** In common to all grades.

PARAMETER	CONDITIONS	DAR-01			UNITS
		MIN	TYP	MAX	
Absolute Temperature Coefficient	All Resistors	—	±180	—	ppm/°C
Tracking Temperature Coefficient	All Resistors with Respect to R1	—	3	—	ppm/°C

WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$ when connected to an ideal DAR-01, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAI-01-N			DAI-01-G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Nonlinearity	NL	$V_S = \pm 15\text{V}$	—	—	±0.05	—	—	±0.1	%
Internal Reference Voltage	V_{MCR}	$V_S = \pm 15\text{V}$	6.6	—	6.900	6.6	—	6.900	V

WAFER TEST LIMITS at $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ when connected to an ideal DAR-01, unless otherwise noted.

PARAMETER	CONDITIONS	DAI-01			UNITS
		MIN	TYP	MAX	
Resolution		10	—	10	Bits
Analog Output Current	All Bits Low, V_- Connected to FS Adjust	1840	—	2274	μA
Zero-Scale Output Current	All Bits High, V_- Connected to FS Adjust	—	—	±0.011	% I_{FS}
Logic Input "0"	Measured with Respect to Output	—	—	0.7	V
Logic Input "1"	Measured with Respect to Output	2.1	—	—	V
Supply Current	All Bits High, V_- Connected to FS Adjust	—	—	8.33	mA
Power Supply Rejection	$V_S = \pm 6\text{V}$ to $\pm 18\text{V}$	—	—	0.1	% I_{FS}/V

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, and when connected to an ideal DAR-01, unless otherwise noted.

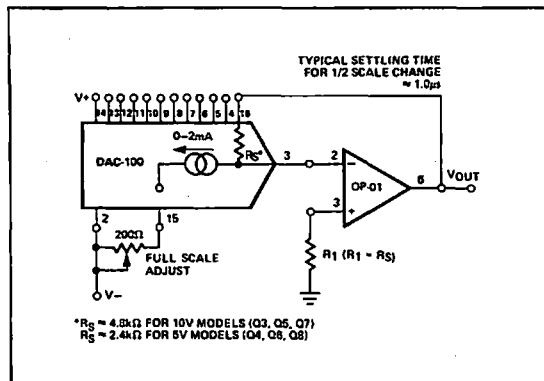
PARAMETER	CONDITIONS	DAI-01-N			DAI-01-G			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Full-Scale Temperature Coefficient (Note)		—	±60	—	—	±60	—	ppm/°C

NOTE:

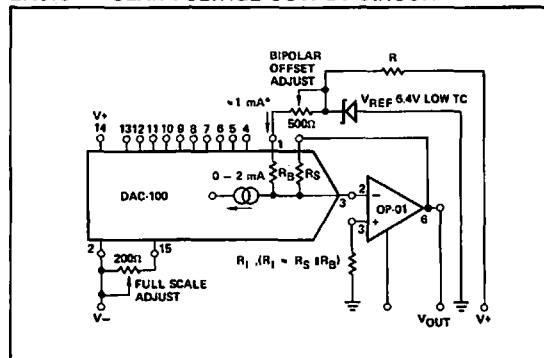
Full-Scale Temperature Coefficient is defined as the change in output voltage measured in the basic unipolar voltage output test circuit shown on the DAC-100 data sheet and is expressed in ppm between 25°C and either temperature extreme divided by the corresponding temperature change.

BASIC CONNECTIONS

BASIC UNIPOLAR VOLTAGE OUTPUT CIRCUIT



BASIC BIPOLAR VOLTAGE OUTPUT CIRCUIT

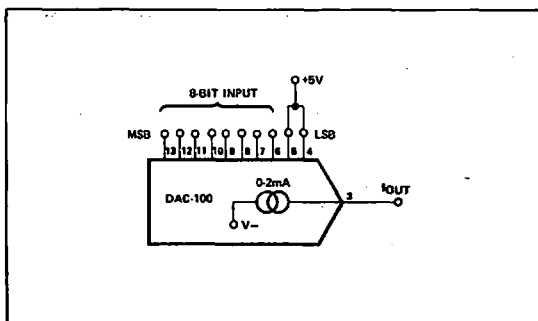


APPLICATIONS INFORMATION

FULL RANGE OUTPUT ADJUSTMENT — The output current of the DAC-100 may be reduced to produce an exact 10.000 (5.000) volt output by connecting a 200Ω adjustable resistance between the full-scale adjust pin and V_- . Adjustment should be made with an input of all "zeroes."

LOWER RESOLUTION APPLICATIONS — The DAC-100 may be used in applications requiring less than 10 bits of resolution. All unused logic inputs must be tied to logic high for proper operation. "Floating" logic inputs can cause improper operation.

REDUCED RESOLUTION APPLICATION



LOGIC CODING — The DAC-100 uses complementary or inverted binary logic coding, i.e., an all "zeroes" input produces a full range output, while an all "ones" input produces a zero-scale output. Each lesser significant bit's weight is one-half the previous more significant bit's value. High logic input turns the bit "OFF," low logic input level turns the bit "ON".

LOGIC COMPATIBILITY — The input logic levels are directly compatible with TTL logic and may also be used with CMOS logic powered from a single +5 volt supply.

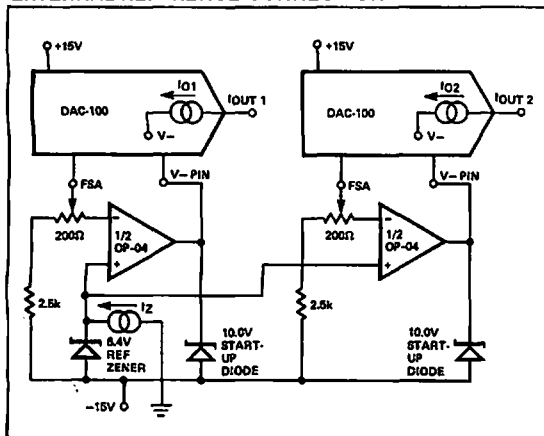
NONLINEARITY (NL) — The maximum deviation from an ideal straight line drawn between the end points, expressed as a percent of full-scale range (FSR) or given in terms of LSB value. The end points are zero-scale output to full-scale output for unipolar operation and minus full-scale to positive full-scale for bipolar operation.

BIPOLAR OPERATION — The DAC-100 may be converted to bipolar operation by injecting a half-scale current into the output; this is accomplished by connecting the internal bipolar resistor to a +6.4 volt reference. Trimming of the zero output may be facilitated by placing a 500Ω adjustable resistance in series with the +6.4 volts.

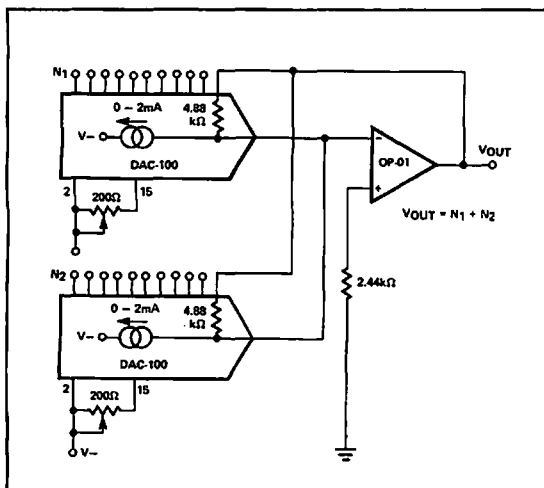
VOLTAGE AT OUTPUT PIN — The DAC-100 is designed to be operated with the voltage at the output pin held very close to zero volts. Input logic threshold levels are directly affected by output pin voltage changes; voltage swings at the output may cause loss of linearity due to improper switching of bits. Large voltage swings may cause permanent damage and should be avoided. Proper operation can be obtained with output voltages held within ± 0.7 volts; a pair of back-to-back silicon diodes tied from the output to ground is a convenient way of clamping the output to this limit.

TYPICAL APPLICATIONS

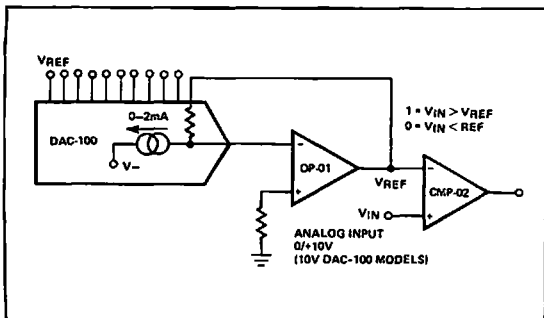
EXTERNAL REFERENCE CONNECTION



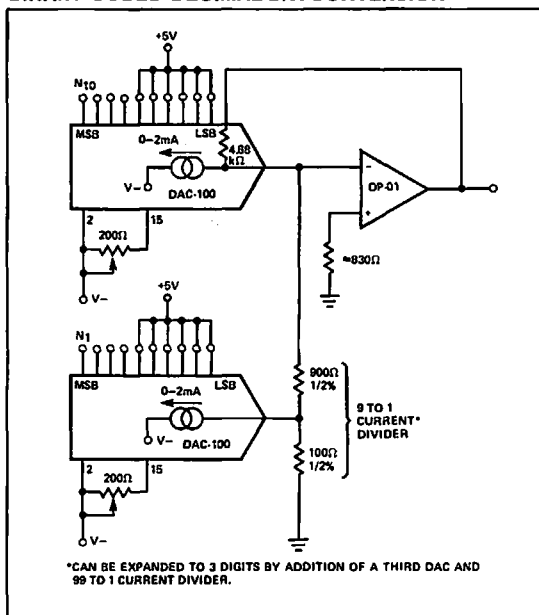
ANALOG SUM OF TWO DIGITAL NUMBERS



DIGITALLY PROGRAMMED LEVEL DETECTOR



BINARY-CODED-DECIMAL D/A CONVERSION



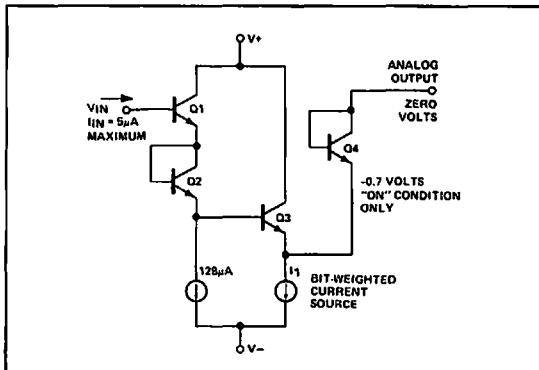
INTERFACING WITH CMOS LOGIC

The DAC-100 requires only about $1\mu\text{A}$ of input current into each logic stage. This enables use with CMOS inputs as long as one rule is observed; logic input voltages should not exceed 6.5 volts or $V+$, whichever is smaller. To provide an understanding of this rule, it is necessary to discuss the logic input stage design.

LOGIC INPUT STAGE DESIGN

For simplicity, only one of the ten identical input circuits is shown below. The DAC-100 uses a fast current-steering technique that switches a bit-weighted current between the positive supply ($V+$) and the analog output, which is usually constrained to be at zero volts (virtual ground) by an external summing amplifier.

DAC-100 — LOGIC INPUT STAGE



Switching is accomplished by forward biasing Q4, diode-connected transistor, for the bit "ON" condition and back biasing Q4 in the "OFF" condition. For the "ON" condition ($V_{IN} \leq 0.7$ volts), Q3 is "OFF" — all of the bit-weighted current, i_1 , flows from the analog output through Q4 and ultimately to V_- . In the "OFF" condition ($V_{IN} \geq 2.1$ volts), Q3 is "ON", Q4 is back biased, and the bit-weighted current is sourced from the positive power supply instead of the analog output.

If V_{IN} is too high, Q4's emitter-base junction will experience reverse breakdown and a fault condition will occur. Equation 1 describes this condition:

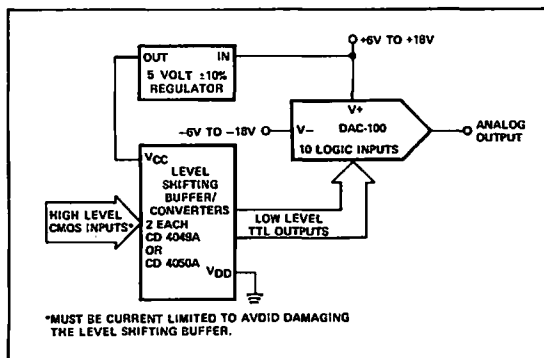
$$1) BV_{IH} = V_{BE1} + V_{BE2} + V_{BE3} + BV_{EB4} \approx 7.7 \text{ volts}$$

Using this relationship, it can be seen that a conservative input voltage limit would be around 6.5 volts. When the 6.5V input limit is observed, DAC-100 operation with CMOS inputs is easily achieved.

±6 VOLT POWER SUPPLY OPERATION

This is the most convenient method of interfacing the DAC-100 with CMOS logic. At ±6 volts the DAC-100 power dissipation is only 80mW, which is very small considering the inclusion of a complete internal reference. No interfacing components are required with ±5% power supplies, and the CMOS logic and DAC-100 can use the same +6 volt power supply. In this application the device is directly CMOS compatible.

BLOCK DIAGRAM — CMOS TO DAC-100 INTERFACE



HIGH LEVEL CMOS INTERFACING

The block diagram below illustrates a convenient method for interfacing CMOS input levels between 6.5 volts and 15 volts with the DAC-100. Inexpensive and readily available CMOS hex buffer/converters step down the high-level inputs to TTL levels that cannot exceed 5 volts — clearly satisfying the input stage voltage rule.

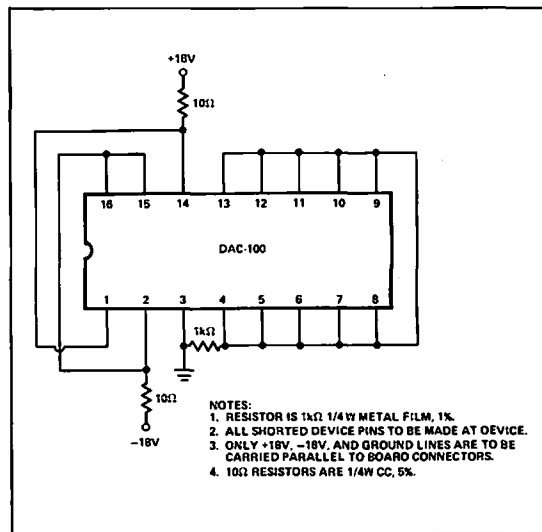
In addition to level shifting, buffer/converters provide input coding flexibility since they are available as inverting (CD4049A) or non-inverting (CD4050A) devices. This gives the user a choice between negative-true and positive-true binary coding and allows the same basic DAC-100 to CMOS interfacing method to be used in either type of application.

Since buffer/converter power consumption is very low, the required +5 volts can be provided by a simple regulator or even a resistive divider in some applications. In a multi-DAC system, one central, inexpensive three-terminal IC regulator can supply several level shifting devices.

NOTE:

For a more complete explanation and detailed circuit connections, refer to AN-14, "Interfacing PMI D/A's with CMOS Logic."

BURN-IN CIRCUIT



11





DAC-210

11-BIT VOLTAGE-OUTPUT D/A CONVERTER (10 BITS PLUS SIGN)

Precision Monolithics Inc.

FEATURES

- Complete Includes Reference and Op Amp
- Bipolar Output $\pm 10V$
- Sign-Magnitude Coding
- No Bipolar Offset Adjustment Required
- 10-Bit Linearity Maintained over Full Temperature
- Multiplying Operation
- Fast 1.5 μs Settling Time
- Monotonicity Guaranteed
- Reliable 100% Burned-In

ORDERING INFORMATION†

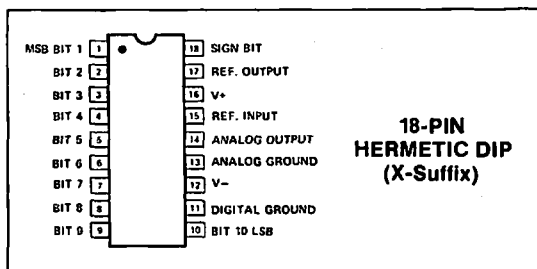
TEMPCO (ppm/°C)	NL %FS	COMMERCIAL TEMPERATURE
± 40	± 0.05	DAC210EX
± 60	± 0.05	DAC210FX
± 30 Typ	± 0.10	DAC210GX

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

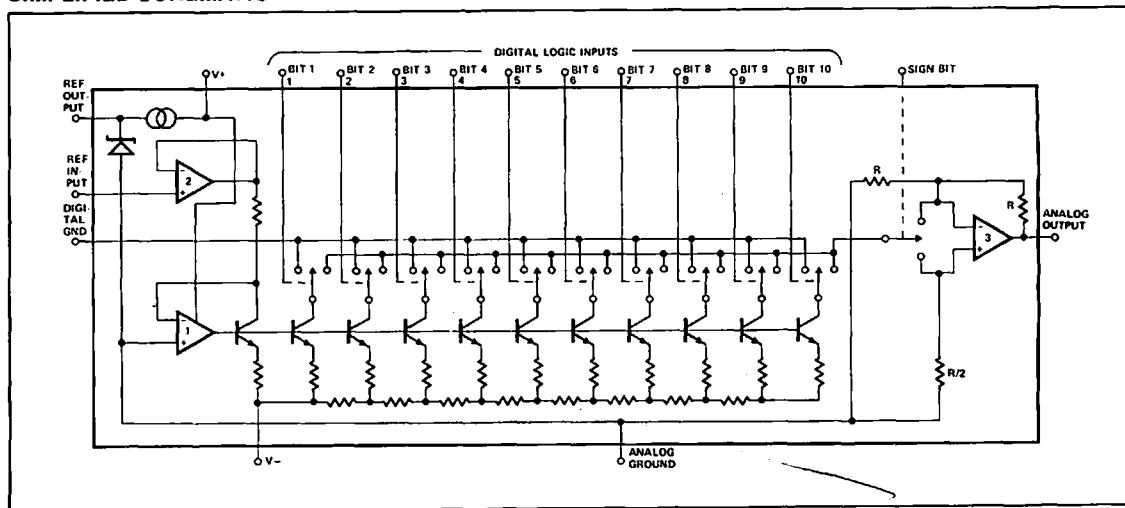
GENERAL DESCRIPTION

The DAC-210 is a complete, monolithic 10-bit plus sign DAC with a $\pm 10V$ output. A precision voltage reference, a logic controlled polarity switch and output amplifier are included. Linearity, monotonicity, and full-scale temperature coefficient are guaranteed over the full operating temperature range. Ease of application is achieved by the total D/A system specs given for nonlinearity and zero-scale offset. System specs eliminate the complex error budget analysis required by less "complete" DACs. Sign-magnitude coding minimizes the "major-carry" zero-code errors inherent in offset coding schemes.

PIN CONNECTION



SIMPLIFIED SCHEMATIC





1826-1155

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $0^\circ C \leq T_A \leq +70^\circ C$ for E, F and G grades, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-210E			DAC-210F			DAC-210G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution		Including Sign	11	—	—	11	—	—	11	—	—	Bits
Monotonicity			10	—	—	10	—	—	9	—	—	Bits
Nonlinearity	NL	$T_A = 25^\circ C$	—	—	± 0.05	—	—	± 0.05	—	—	± 0.10	%FS
		$T_A = \text{Full Range}$	—	—	± 0.05	—	—	± 0.10	—	—	—	
Zero-Scale Offset Voltage	V_{ZS}	$T_A = 25^\circ C$	—	—	± 0.05	—	—	± 0.1	—	—	—	%FS
		$T_A = \text{Full Range}$	—	—	± 0.06	—	—	± 0.1	—	—	—	
Bipolar Full Range Voltage Symmetry ($V_{FR+} - V_{FR-} $)	V_{FRS}	$T_A = 25^\circ C$	—	—	40	—	—	60	—	—	80	mV
		$T_A = \text{Full Range}$	—	—	50	—	—	70	—	50	—	
Zero-Scale Voltage Symmetry ($V_{ZS+} - V_{ZS-}$)	V_{ZSS}	$T_A = \text{Full Range}$	—	—	1	—	—	1	—	—	2	mV
Gain Tempco	T_C	Internal Reference	—	—	± 40	—	—	± 80	—	± 30	—	ppm/ $^\circ C$
		External Reference	—	± 15	—	—	± 30	—	—	± 30	—	
Output Voltage Range	V_{OR+} V_{OR-}	$R_L = 2k\Omega$	+10.0	—	+11.5	+10.0	—	+11.5	+10.0	—	+11.5	V
			-11.5	—	-10.0	-11.5	—	-10.0	-11.5	—	-10.0	
Differential Nonlinearity	DNL	$T_A = 25^\circ C$	—	—	± 1	—	—	± 1	—	± 1	—	LSB
Settling Time	T_S	(Note 4)	—	1.5	—	—	1.5	—	—	1.5	—	μs
Reference Input Slow Rate	SR_{REF}		—	1.5	—	—	1.5	—	—	1.5	—	V/ μs
Reference Input Impedance	Z_{IN}		—	200	—	—	200	—	—	200	—	M Ω
Reference Input Multiplying Range	IVR_m	For 0.1% Typical Nonlinearity (Note 1)	3	—	10	3	—	10	3	—	10	V
Reference Amplifier Bandwidth	BW		—	1	—	—	1	—	—	1	—	MHz
Reference Output Voltage	V_{REF}		—	7.6	—	—	7.6	—	—	7.6	—	V
DAC Output Current	I_O	(Note 3)	0	—	5	0	—	5	0	—	5	mA
Reference Output Current	I_{REF}		—	100	—	—	100	—	—	100	—	μA
Output Slew Rate	SR_O		—	10	—	—	10	—	—	10	—	V/ μs
Logic Input Current	I_{IN}	$-5V \leq V_i \leq V+$	—	± 2	± 10	—	± 2	± 10	—	± 2	± 10	μA
Logic "0" Input Voltage	V_{INL}		—	—	0.8	—	—	0.8	—	—	0.8	V
Logic "1" Input Voltage	V_{INH}		2.0	—	—	2.0	—	—	2.0	—	—	V
Power Supply Sensitivity (Note 2)	P_{SS}	$T_A = 25^\circ C$	—	0.015	0.05	—	0.015	0.05	—	0.015	0.1	% V_{FS}/V
		$T_A = \text{Full Range}$	—	0.015	0.1	—	0.015	0.1	—	0.015	0.1	
Positive Supply Current	$I+$		—	7	9	—	7	9	—	7	9	mA
Negative Supply Current	$I-$		—	-10	-12	—	-10	-12	—	-10	-12	mA

NOTES:

- Guaranteed by design.
- Power Supplies — The DAC-210 will operate within specifications for power supplies ranging from $\pm 12V$ to $\pm 18V$. Power supplies should be bypassed near the package with a $0.1\mu F$ disk capacitor.
- Guaranteed by V_{OR} test, $R_L = 2k\Omega$.
- To within $\pm 5mV$ of final settled value, (± 10 volt output step, $R_L = 2k\Omega$).

**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature Range

DAC-210E, F, G 0°C to +70°C

DICE Junction Temperature (T_J) -65°C to +150°C

Storage Temperature Range -65°C to +150°C

V+ Supply to Analog Ground 0 to +18V

Analog Ground to Digital Ground 0 to $\pm 0.5V$

Logic Inputs to Digital Ground -5V to (V+ - 0.7V)

V+ Supply to V- Supply 36V

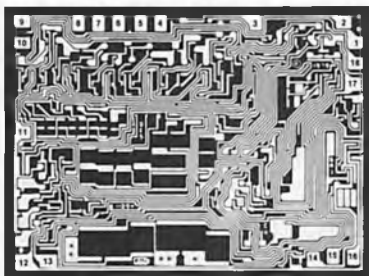
Internal Reference Output Current 300 μA

Reference Input Voltage 0 to +10V

Internal Power Dissipation 500mW

Derate Above 100°C 10mW/°C

Lead Temperature (Soldering, 60 sec) 300°C

Output Short-Circuit Duration Indefinite
(Short-circuit may be to ground or either supply.)**NOTE:** Absolute ratings apply to both DICE and packaged parts unless otherwise noted.**DICE CHARACTERISTICS**

- | | |
|-------------|----------------------|
| 1. B1 (MSB) | 10. B10 (LSB) |
| 2. B2 | 11. DIGITAL GROUND |
| 3. B3 | 12. V- |
| 4. B4 | 13. ANALOG GROUND |
| 5. B5 | 14. ANALOG OUTPUT |
| 6. B6 | 15. REFERENCE INPUT |
| 7. B7 | 16. V+ |
| 8. B8 | 17. REFERENCE OUTPUT |
| 9. B9 | 18. SIGN BIT |

NOTE: For 5 volt output option (+5V only) * is connected to analog output. ** is connected to analog ground.**DIE SIZE** 0.118 $\times$ 0.087 inch, 10,266 sq. mils
(2.997 $\times$ 2.210 mm, 6.623 sq. mm)

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, +10V full-scale output, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC-210N LIMIT	DAC-210G LIMIT	DAC-210GR LIMIT	UNITS
Resolution	Bipolar Output	11	11	11	Bits MAX
	Unipolar Output	10	10	10	
Monotonicity		10	9	8	Bits MIN
Nonlinearity		± 0.05	± 0.1	± 0.2	%FS MAX
Zero-Scale Offset	Sign-Bit High, All Other Inputs Low	± 5	± 10	± 10	mV MAX
Zero-Scale Symmetry	$V_{ZS+} - V_{ZS-}$	± 1	± 2	± 2	mV MAX
Full-Scale Bipolar Symmetry	$\pm 10V$ Full-Scale	± 40	± 80	± 80	mV MAX
Power Supply Rejection	$V_S = \pm 12V$ to $\pm 18V$	0.05	0.05	0.1	% V_{FS}/V MAX
Power Consumption	$I_{OUT} = 0$	300	300	300	mW MAX
Logic Input "0"		0.8	0.8	0.8	V MAX
Logic Input "1"		2	2	2	V MIN
Analog Output Voltage (All Bits High)	V+ (Sign-Bit High)	11.5 10	11.5 10	11.5 10	V MAX V MIN
	V- (Sign-Bit Low)	-10 -11.5	-10 -11.5	-10 -11.5	V MAX V MIN
		± 1	± 1	± 1	LSB MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

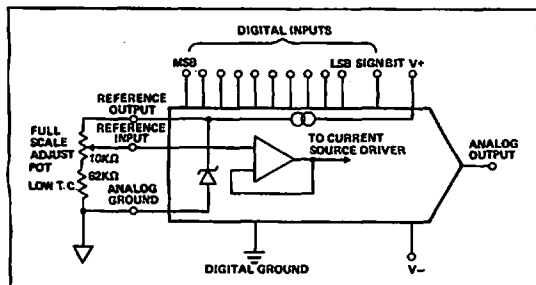
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and +10V full-scale output, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-210N TYPICAL	DAC-210G TYPICAL	DAC-210GR TYPICAL	UNITS
Full-Scale Tempco	TCV_{FS}	Internal Reference	15	30	30	ppm/°C
Settling Time ($T_A = 25^\circ C$)	I_S	To $\pm 1/2$ LSB 10 Volt Step	1.5	1.5	1.5	μs
Logic Input Current	I_{IN}	$T_A = 25^\circ C$	1	1	1	μA

CONNECTION INFORMATION

FULL-SCALE ADJUSTMENT — Full-scale output voltage may be trimmed by use of a potentiometer and series resistor as shown; however, best results will be obtained if a low tempco resistor is used or if pot and resistor tempcos match. Alternatively, a single pot of $\geq 75\text{k}\Omega$ may be used.

FULL SCALE ADJUSTMENT CIRCUIT



REFERENCE INPUT BYPASS — Lowest noise and fastest settling operation will be obtained by bypassing the reference input to analog ground with a $0.01\mu\text{F}$ disk capacitor.

VARIABLE REFERENCES — Operation as a two-quadrant multiplying DAC is achieved by applying an analog input varying between 0 and +10V to the reference input terminal. The DAC output is then the scaled product of this voltage and the digital input.

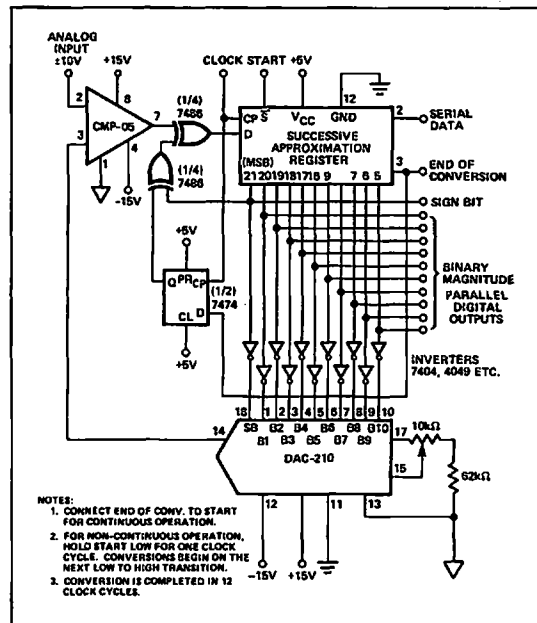
GROUNDING — For optimum noise rejection, separate digital and analog grounds have been brought out. Best results will be obtained if these grounds are connected together at one point only, preferably at the power supply, so that the large digital currents do not flow through the analog ground path.

SIGN — MAGNITUDE CODING TABLE

	SIGN-BIT	MSB	LSB
+FULL-SCALE -1 LSB	1	1 1 1 1 1 1 1 1 1 1	
+HALF-SCALE	1	1 0 0 0 0 0 0 0 0 0	
ZERO-SCALE (+)	1	0 0 0 0 0 0 0 0 0 0	
ZERO-SCALE (-)	0	0 0 0 0 0 0 0 0 0 0	
-HALF-SCALE	0	1 0 0 0 0 0 0 0 0 0	
-FULL-SCALE +1 LSB	0	1 1 1 1 1 1 1 1 1 1	

TYPICAL APPLICATIONS

10-BIT SIGN-MAGNITUDE ADC



APPLICATIONS INFORMATION

LOWER RESOLUTION APPLICATION — For applications not requiring full 10-bit resolution, unused logic inputs should be tied to ground.

CAPACITIVE LOADING — The output operational amplifier provides stable operation with capacitive loads up to 100pF.

REFERENCE OUTPUT — For best results, reference output current should not exceed 100 μ A.

INTERFACING WITH CMOS LOGIC — The DAC-210's logic input stages require about $1\mu\text{A}$ and are capable of operation with inputs between -5 volts and $V+$. This wide input voltage range allows direct CMOS Interface with no additional components.

USE WITH EXTERNAL REFERENCES — Positive polarity external reference voltages referred to analog ground may be applied to the reference input terminal to improve full-scale tempco, to provide tracking to other system elements, or to slave a number of DAC-210's to the reference output of any one of them.



DAC-312

12-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- Differential Nonlinearity $\pm 1/2$ LSB
- Nonlinearity 0.05%
- Fast Settling Time 250ns
- High Compliance -5V to +10V
- Differential Outputs 0 to 4mA
- Guaranteed Monotonicity 12 Bits
- Low Full-Scale Tempco 10ppm/ $^{\circ}$ C
- Circuit Interface to TTL, CMOS, ECL, PMOS/NMOS
- Low Power Consumption 225mW
- Industry Standard AM6012 Pinout

ORDERING INFORMATION†

DNL	20-PIN DIP		OPERATING TEMPERATURE RANGE
	HERMETIC	PLASTIC	
± 1 LSB	DAC312BR*	—	MIL
$\pm 1/2$ LSB	DAC312ER	—	COM
± 1 LSB	DAC312FR	—	COM
± 1 LSB	DAC312HR	—	COM
± 1 LSB	—	DAC312HP	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

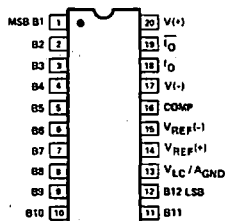
GENERAL DESCRIPTION

The DAC-312 series of 12-bit multiplying digital-to-analog converters provide high speed with guaranteed performance to 0.012% differential nonlinearity over the full commercial operating temperature range.

Based on the segmented design approach pioneered by PMI with the COMDAC® line of data converters, the DAC-312 combines a 9-bit master D/A converter with a 3-bit (MSB's) segment generator to form an accurate 12-bit D/A converter at low cost. This technique guarantees a very uniform step size (up to $\pm 1/2$ LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs. In order to provide the same performance with a 12-bit R-2R ladder design, an integral nonlinearity over temperature of $1/2$ LSB (0.012%) would be required.

The 250ns settling time with low glitch energy and low power consumption are achieved by careful attention to the circuit design and stringent process controls. Direct interface with all popular logic families is achieved through the logic threshold terminal.

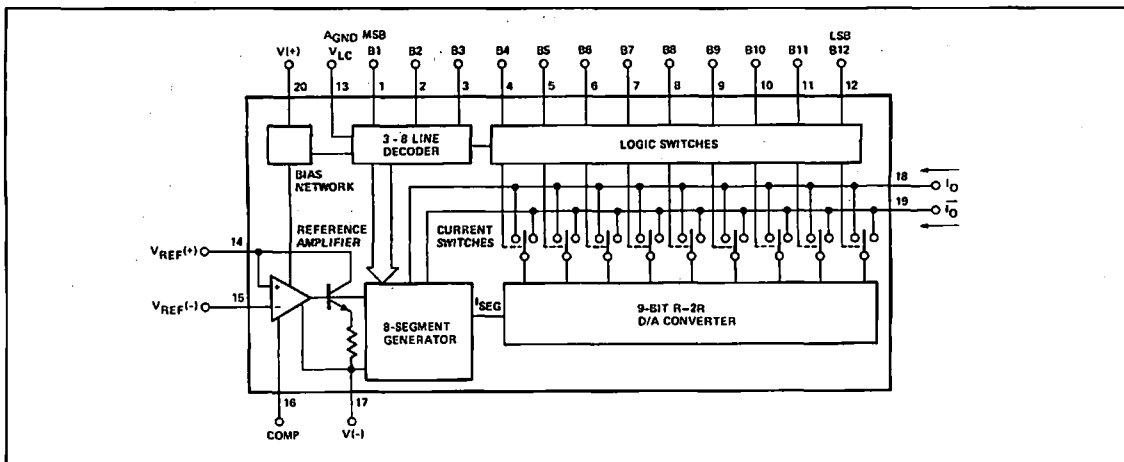
PIN CONNECTIONS



20-PIN HERMETIC DIP
(R-Suffix)

20-PIN PLASTIC DIP
(P-Suffix)

FUNCTIONAL DIAGRAM



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639



High compliance and low drift characteristics (as low as 10ppm/°C) are also features of the DAC-312 along with an excellent power supply rejection ratio of $\pm 0.001\%$ FS/% ΔV . Operating over a power supply range of $+5/-11V$ to $\pm 18V$ the device consumes 225mW at the lower supply voltages with an absolute maximum dissipation of 375mW at the higher supply levels.

With their guaranteed specifications, single chip reliability and low cost, the DAC-312 device makes excellent building blocks for A/D converters, data acquisition systems, video display drivers, programmable test equipment and other applications where low power consumption and complete input/output versatility are required.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature

DAC-312B	-55°C to +125°C
DAC-312E, DAC-312F, DAC-312H	0°C to +70°C
DICE Junction Temperature	-65°C to +150°C
Storage Temperature (T_J)	-65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
Power Supply Voltage	$\pm 18V$
Logic Inputs	-5V to +18V
Analog Current Outputs	-8V to +12V
Reference Inputs V_{14}, V_{15}	V- to V+
Reference Input Differential Voltage (V_{14} to V_{15})	$\pm 18V$
Reference Input Current (I_{14})	1.25mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 1.0mA$, $-55^\circ C \leq T_A \leq 125^\circ C$ for DAC-312B, $0^\circ C \leq T_A \leq 70^\circ C$ for DAC-312E, DAC-312F, DAC-312H, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT} .

PARAMETER	SYMBOL	CONDITIONS	DAC-312E			DAC-312B/F			DAC-312H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			12	—	—	12	—	—	12	—	—	Bits
Monotonicity			12	—	—	12	—	—	12	—	—	Bits
Differential Nonlinearity	DNL	Deviation from ideal step size (Note 2)	—	—	± 0.0125	—	—	± 0.0250	—	—	± 0.0250	%FS
Nonlinearity	INL	Deviation from ideal straight line (Note 2)	—	—	± 0.5	—	—	± 1	—	—	± 1	LSB
Full-Scale Current	I_{FS}	$V_{REF} = 10.000V$ $R_{14} = R_{15} = 10.000k\Omega$ (Note 2)	3.967	3.999	4.031	3.935	3.999	4.063	3.935	3.999	4.063	mA
Full-Scale Tempco	TCI_{FS}		—	± 10	± 30	—	± 10	± 40	—	± 60	—	ppm/°C
			—	± 0.001	± 0.003	—	± 0.001	± 0.004	—	± 0.008	—	%FS/°C
Output Voltage Compliance	V_{OC}	DNL Specification guaranteed over compliance range	-5	—	+10	-5	—	+10	-5	—	+10	V
Full-Scale Symmetry	I_{FSS}	$ I_{FS} - I_{FS} $	—	± 0.4	± 1	—	± 0.4	± 2	—	± 0.4	± 2	μA
Zero-Scale Current	I_{ZS}		—	—	0.10	—	—	0.10	—	—	0.10	μA
Settling Time	t_S	To $\pm 1/2$ LSB, all bits switched ON or OFF (Note 1)	—	250	500	—	250	500	—	250	500	ns
Propagation Delay — all bits	t_{PLH} t_{PHL}	All bits switched 50% point logic swing to 50% point output (Note 1)	—	25	50	—	25	50	—	25	50	ns
Output Resistance	R_O		—	>10	—	—	>10	—	—	>10	—	M Ω
Output Capacitance	C_{OUT}		—	20	—	—	20	—	—	20	—	pF
Logic Input Levels "0"	V_{IL}	$V_{LC} = GND$	—	—	0.8	—	—	0.8	—	—	0.8	V
Logic Input Levels "1"	V_{IH}	$V_{LC} = GND$	2	—	—	2	—	—	2	—	—	V
Logic Input Current	I_{IN}	$V_{IN} = -5$ to $+18V$	—	—	40	—	—	40	—	—	40	μA
Logic Input Swing	V_{IS}		-5	—	+18	-5	—	+18	-5	—	+18	V



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 1.0mA$, $-55^\circ C \leq T_A \leq 125^\circ C$ for DAC-312B, $0^\circ C \leq T_A \leq 70^\circ C$ for DAC-312E, DAC-312F, DAC-312H, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT-} . (Continued)

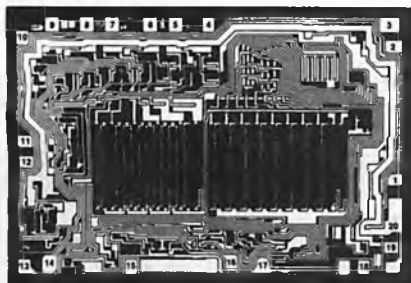
PARAMETER	SYMBOL	CONDITIONS	DAC-312E			DAC-312B/F			DAC-312H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Reference Bias Current	I_{15}		0	-0.5	-2	0	-0.5	-2	0	-0.5	-2	μA
Reference Input Slew Rate	dI/dt	$R_{14(eq)} = 800\Omega$ $C_C = 0pF$ (Note 1)	4	8	—	4	8	—	4	8	—	$mA/\mu s$
Power Supply Sensitivity	$PSSI_{FS+}$	$V+ = +13.5V$ to $+16.5V$, $V- = -15V$	—	± 0.0005	± 0.001	—	± 0.0005	± 0.001	—	± 0.0005	± 0.001	%FS/% ΔV
	$PSSI_{FS-}$	$V- = -13.5V$ to $-16.5V$, $V+ = +15V$	—	± 0.00025	± 0.001	—	± 0.00025	± 0.001	—	± 0.00025	± 0.001	
Power Supply Range	$V+$	$V_{OUT} = 0V$	4.5	—	18	4.5	—	18	4.5	—	18	V
	$V-$		-18	—	-10.8	-18	—	-10.8	-18	—	-10.8	
Power Supply Current	$I+$	$V+ = +5V$, $V- = -15V$	—	3.3	7	—	3.3	7	—	3.3	7	mA
	$I-$	$V+ = +5V$, $V- = -15V$	—	-13.9	-18	—	-13.9	-18	—	-13.9	-18	
	$I+$	$V+ = +15V$, $V- = -15V$	—	3.9	7	—	3.9	7	—	3.9	7	
	$I-$	$V+ = +15V$, $V- = -15V$	—	-13.9	-18	—	-13.9	-18	—	-13.9	-18	
Power Dissipation	P_d	$V+ = +5V$, $V- = -15V$	—	225	305	—	225	305	—	225	305	mW
		$V+ = +15V$, $V- = -15V$	—	267	375	—	267	375	—	267	375	

NOTES:

1. Guaranteed by design.
2. $T_A = 25^\circ C$ for DAC-312H grade only.



DICE CHARACTERISTICS



DIE SIZE 0.141 × 0.096 inch, 13,536 sq. mils (3.58 × 2.44 mm, 8.74 sq. mm)

- | | |
|-------------|---------------------------------------|
| 1. B1 (MSB) | 11. B11 |
| 2. B2 | 12. B12 (LSB) |
| 3. B3 | 13. V _{LC} /A _{GND} |
| 4. B4 | 14. V _{REF} (+) |
| 5. B5 | 15. V _{REF} (-) |
| 6. B6 | 16. COMP |
| 7. B7 | 17. V- |
| 8. B8 | 18. I _O |
| 9. B9 | 19. I _O |
| 10. B10 | 20. V+ |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 1.0mA$, $T_A = 25^\circ C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-312N LIMIT	DAC-312G LIMIT	UNITS
Resolution			12	12	Bits MIN
Monotonicity			12	12	Bits MIN
Nonlinearity			±0.05	±0.05	%FS MAX
Output Voltage Compliance	V _{OC}	Full-Scale Current Change < 1/2 LSB	+10 -5	+10 -5	V MAX V MIN
Full-Scale Current		V _{REF} = 10.000V R ₁₄ , R ₁₅ = 10.000kΩ	4.031 3.967	4.063 3.935	mA MAX mA MIN
Full-Scale Symmetry	I _{FS}		±1	±2	μA MAX
Zero-Scale Current	I _{ZS}		0.1	0.1	μA MAX
Differential Nonlinearity	DNL	Deviation from ideal step size	±0.012 ±1/2	±0.025 ±1	%FS MAX Bits (LSB) MAX
Logic Input Levels "0"	V _{IL}	V _{LC} = GND	0.8	0.8	V MAX
Logic Input Levels "1"	V _{IH}	V _{LC} = GND	2	2	V MIN
Logic Input Swing	V _{IS}		+18 -5	+18 -5	V MAX V MIN
Reference Bias Current	I ₁₅		-2	-2	μA MAX
Power Supply Sensitivity	PSSI _{FS+} PSSI _{FS-}	V+ = +13.5V to +16.5V, V- = -15V V- = -13.5V to -16.5V, V+ = +15V	±0.001 ±0.001	±0.001 ±0.001	%/% MAX
Power Supply Current	I+ I-	V _S = ±15V I _{REF} ≤ 1.0mA	7 -18	7 -18	mA MAX
Power Dissipation	P _D	V _S = ±15V I _{REF} ≤ 1.0mA	375	375	mW MAX

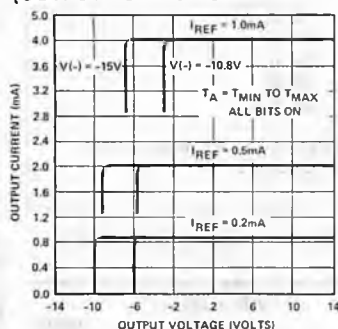
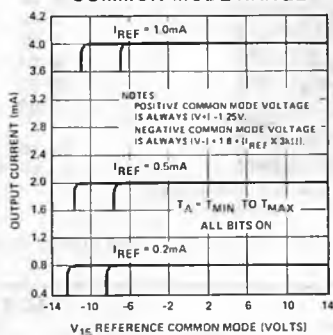
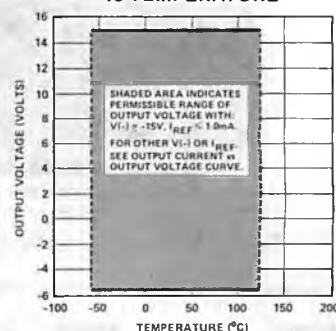
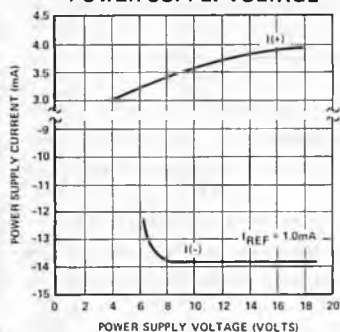
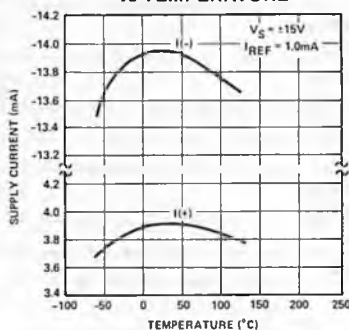
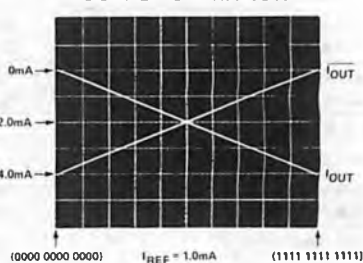
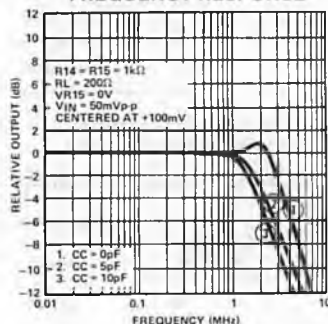
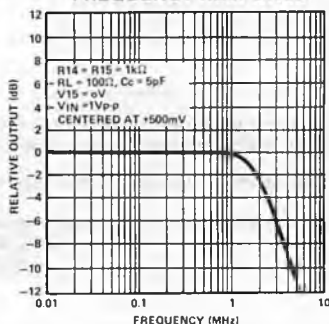
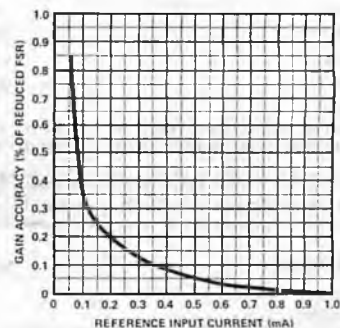
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at 25°C; $V_S = \pm 15V$, and $I_{REF} = 1.0mA$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

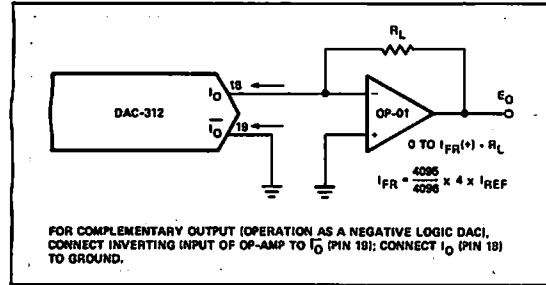
PARAMETER	SYMBOL	CONDITIONS	DAC-312N TYPICAL	DAC-312G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8	8	mA/μs
Propagation Delay	t _{PLH} , t _{PHL}	Any Bit	25	25	ns
Settling Time	t _S	To ±1/2 LSB, All Bits Switched ON or OFF.	250	250	ns
Full-Scale	TC _{IFS}		±10	±10	ppm/°C

TYPICAL PERFORMANCE CHARACTERISTICS

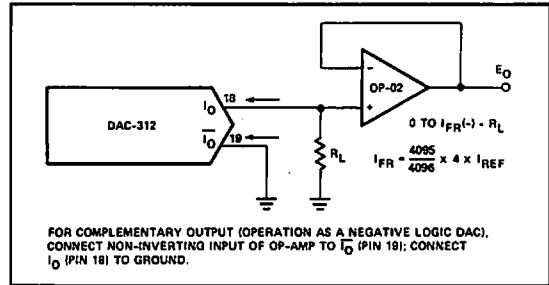
 OUTPUT CURRENT vs
OUTPUT VOLTAGE
(OUTPUT VOLTAGE COMPLIANCE)

 REFERENCE AMPLIFIER
COMMON-MODE RANGE

 OUTPUT COMPLIANCE
vs TEMPERATURE

 POWER SUPPLY CURRENT vs
POWER SUPPLY VOLTAGE

 POWER SUPPLY CURRENT
vs TEMPERATURE

 TRUE AND COMPLEMENTARY
OUTPUT OPERATION

 REFERENCE AMPLIFIER
SMALL-SIGNAL
FREQUENCY RESPONSE

 REFERENCE AMPLIFIER
LARGE-SIGNAL
FREQUENCY RESPONSE

 GAIN ACCURACY vs
REFERENCE CURRENT


BASIC CONNECTIONS

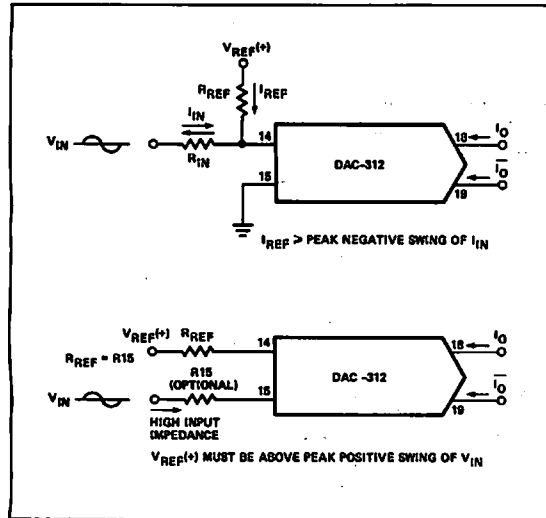
NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



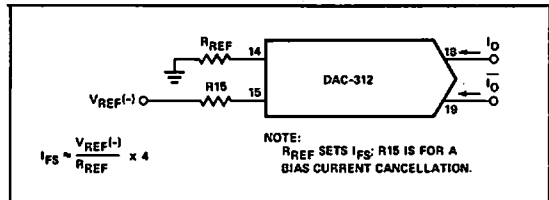
POSITIVE LOW IMPEDANCE OUTPUT OPERATION



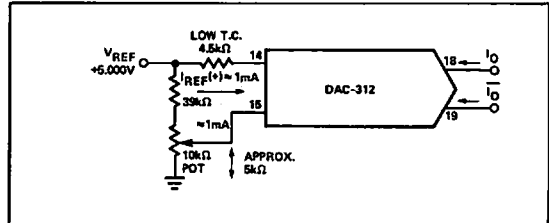
ACCOMMODATING BIPOLAR REFERENCES



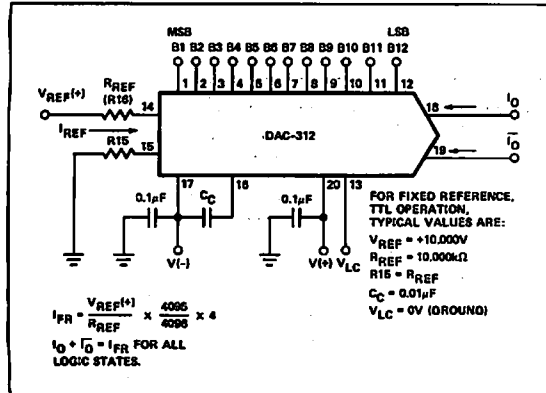
BASIC NEGATIVE REFERENCE OPERATION



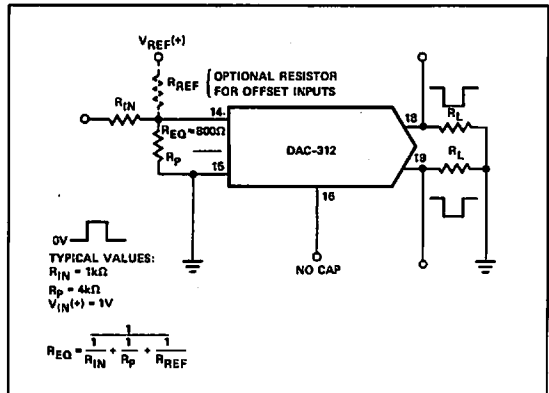
RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT



BASIC POSITIVE REFERENCE OPERATION



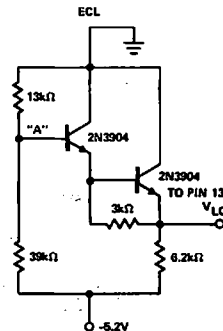
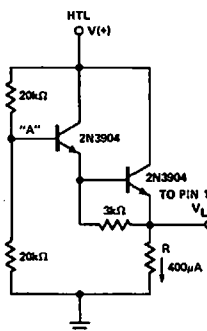
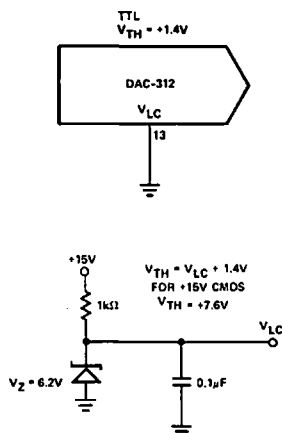
PULSED REFERENCE OPERATION





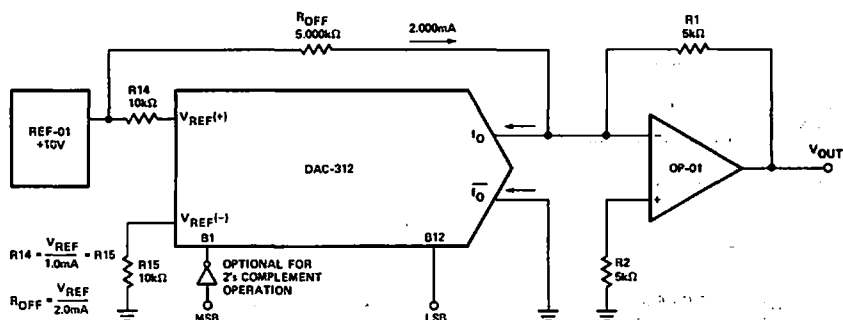
BASIC CONNECTIONS

INTERFACING WITH VARIOUS LOGIC FAMILIES



- NOTES:
1. SET THE VOLTAGE "A" TO THE DESIRED LOGIC INPUT SWITCHING THRESHOLD.
 2. ALLOWABLE RANGE OF LOGIC THRESHOLD IS TYPICALLY -5V TO +13.5V WHEN OPERATING THE DAC ON ±15V SUPPLIES.

BIPOLAR OFFSET (TRUE ZERO)

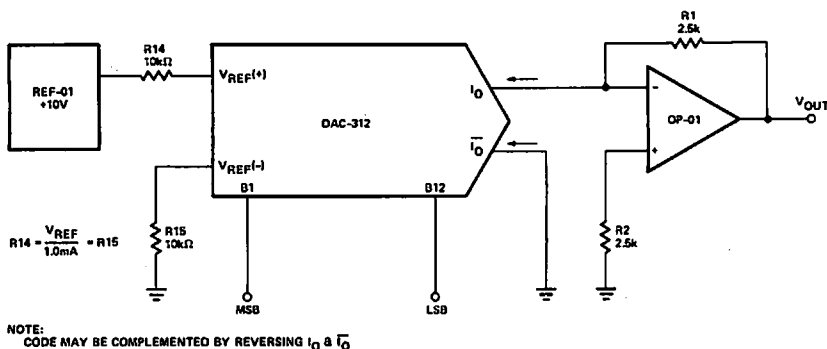


NOTE:
CODE MAY BE COMPLEMENTED BY REVERSING I_O & $\bar{I}_O$

CODE FORMAT	OUTPUT SCALE	MSB												LSB		I _O (mA)	I _O (mA)	V _{OUT}
		B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12					
Offset binary; true zero output.	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951	
	Positive full-scale -LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902		
	+LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049		
	Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000		
	-LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049		
	Negative full-scale +LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951		
	Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000		
2's complement; true zero output MSB complemented (Need inverter at B1).	Positive full-scale	0	0	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9951		
	Positive full-scale -LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9902		
	+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	0.0049		
	Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.000		
	-1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0049		
	Negative full-scale +LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9951		
	Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-10.000		

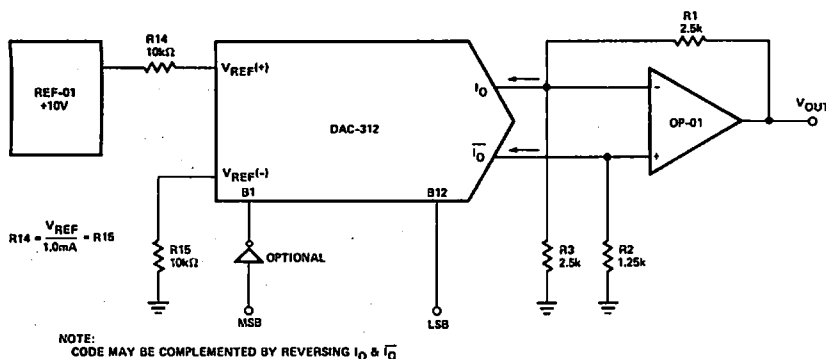
BASIC CONNECTIONS

BASIC UNIPOLAR OPERATION



CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_0 (mA)	$\bar{I}_0$ (mA)	V_{OUT}
Straight Binary; unipolar with true input code, true zero output.	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive full-scale - LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9951
	LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	0.0024
	Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	0.0000
Complementary binary; unipolar with complementary input code, true zero output.	Positive full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	9.9976
	Positive full-scale - LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	9.9951
	LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	0.0024
	Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	0.0000

SYMMETRICAL OFFSET OPERATION



CODE FORMAT	OUTPUT SCALE	MSB B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	LSB B12	I_0 (mA)	$\bar{I}_0$ (mA)	V_{OUT}
Straight offset binary; symmetrical about zero, no true zero output.	Positive full-scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	0.00	9.9976
	Positive full-scale - LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
	(+) Zero-scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(-) Zero-scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0024
	Negative full-scale - LSB	0	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9927
	Negative full-scale	0	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-9.9976
1's complement; symmetrical about zero, no true zero output. MSB complemented (need inverter at B1).	Positive full-scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	0.000	9.9976
	Positive full-scale - LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	0.001	9.9927
	(+) Zero-scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	0.0024
	(-) Zero-scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	-0.0024
	Negative full-scale - LSB	1	0	0	0	0	0	0	0	0	0	0	1	0.001	3.998	-9.9927
	Negative full-scale	1	0	0	0	0	0	0	0	0	0	0	0	0.000	3.999	-9.9976

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-312 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999 I_{REF}$$

$$\text{where } I_{REF} = I_{14}$$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V_-$ plus $(I_{REF} \times 3k\Omega)$ plus 1.23V. The positive common-mode range is V_+ less 1.8V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1 μ F capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF} . If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full-scale trimming which eliminates potentiometer T.C. effects is shown in the Recommended Full-Scale Adjustment circuit.

The reference amplifier must be compensated by using a capacitor from pin 16 to V_- . For fixed reference operation, a 0.01 μ F capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifier Compensation for Multiplying Applications."

MULTIPLYING OPERATION

The DAC-312 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1 μ A. Monotonic operation is maintained over a typical range of I_{REF} from 100 μ A to 1.0mA. Although some degradation of gain accuracy will be realized

at reduced values of I_{REF} . (See Gain Accuracy vs Reference Current).

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V_- . The value of this capacitor depends on the impedance presented to pin 14 for R14 values of 1.0, 2.5 and 5.0k Ω , minimum values of C_C are 5, 10, and 25pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For R14 = 1k Ω and C_C = 5pF, the reference amplifier slews at 4mA/ μ s enabling a transition from $I_{REF} = 0$ to $I_{REF} = 1$ mA in 250ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800 Ω and $C_C = 0$. This yields a reference slew rate of 8mA/ μ s which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-312 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40 μ A logic input current, and completely adjustable logic threshold voltage. For $V_- = -15$ V, the logic inputs may swing between -5 and +10V. This enables direct interface with +15V CMOS logic, even when the DAC-312 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V_- plus $(I_{REF} \times 3k\Omega)$ plus 1.8V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC} . For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq 1$ mA is recommended. For interfacing other logic families, see block titled "Interfacing With Various Logic Families". For general setup of the logic control circuit, it should be noted that pin 13 will sink 7mA typical; external circuitry should be designed to accommodate this current.



ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{RF}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{RF} ; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V_- and is independent of the positive supply. Negative compliance is +10V above V_- .

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-312 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V_- supplies of -10V or less, $I_{REF} \leq 1\text{mA}$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at -9V with $I_{REF} = 1\text{mA}$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-312 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-312 are guaranteed to apply over the entire rated operating temperature range. Full-Scale output current drift is tight, typically $\pm 10\text{ppm}/^\circ\text{C}$, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for min-

imum overall full-scale drift. Settling times of the DAC-312 decrease approximately 10% at -55°C ; at $+125^\circ\text{C}$ an increase of about 15% is typical.

SETTLING TIME

The DAC-312 is capable of extremely fast settling times, typically 250ns at $I_{REF} = 1.0\text{mA}$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the DAC-312 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of the settling time requires the ability to accurately resolve $\pm 1/2$ LSB of current, which is $\pm 500\text{nA}$ for 4mA FSR. In order to assure the measurement is of the actual settling time and not the R.C. time of the output network, the resistive termination on the output of the DAC must be 500 ohms or less. This does, however, place certain limitations on the testing apparatus. At I_{REF} values of less than 0.5mA, it is difficult to prevent RC damping of the output and maintain adequate sensitivity. Because the DAC-312 has 8 equal current sources for the 3 most significant bits, the major carry occurs at the code change of 000111111111 to 111000000000. The worst case settling time occurs at the zero to full-scale transition and it requires 9.2 time constants for the DAC output to settle to within $\pm 1/2$ LSB (0.0125%) of its final value.

The DAC-312 switching transients or "glitches" are on the order of 500mV-ns. This is most evident when switching through the major carry and may be further reduced by adding small capacitive loads at the output with a minor sacrifice in transition speeds.

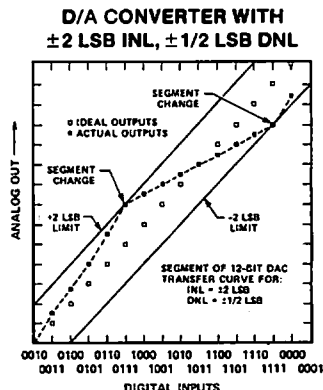
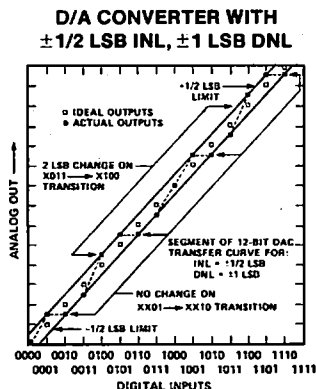
Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1 μF capacitors at the supply pins provide full transient protection.

DIFFERENTIAL vs INTEGRAL NONLINEARITY

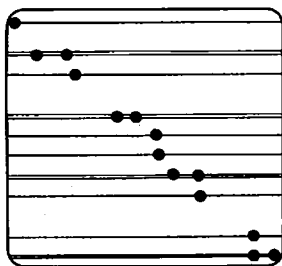
Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full-scale output or as fractional LSBs or both. The following figures define the manner in which these parameters are specified. The left figure shows a portion of the transfer curve of a DAC with 1/2 LSB INL and the (implied) DNL spec of 1 LSB. Below this is a graphic representation of the way this would appear on a CRT, for example, if the D/A Converter output were to be applied to the Y input of a CRT as shown in the application schematic titled "CRT Display Driver". On the right is a portion of the transfer curve of a DAC specified for 2 LSB INL with 1/2 LSB DNL specified and the graphic display below it.

One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e. the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2 LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, 2 LSB gaps can cause large errors at those input levels (assuming 1/2 LSB quantizing levels). It can be seen from the two figures that the DNL specified D/A converter will yield much finer grained data than the INL specified part, thus improving the ability of the A/D to resolve changes in the analog input.

DIFFERENTIAL LINEARITY COMPARISON

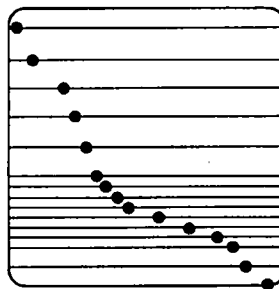


VIDEO DEFLECTION BY DACs



ENLARGED "POSITIONAL" OUTPUTS

VIDEO DEFLECTION BY DACs



ENLARGED "POSITIONAL" OUTPUTS

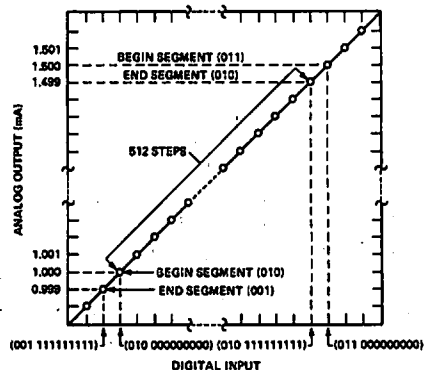


DESCRIPTION OF OPERATION

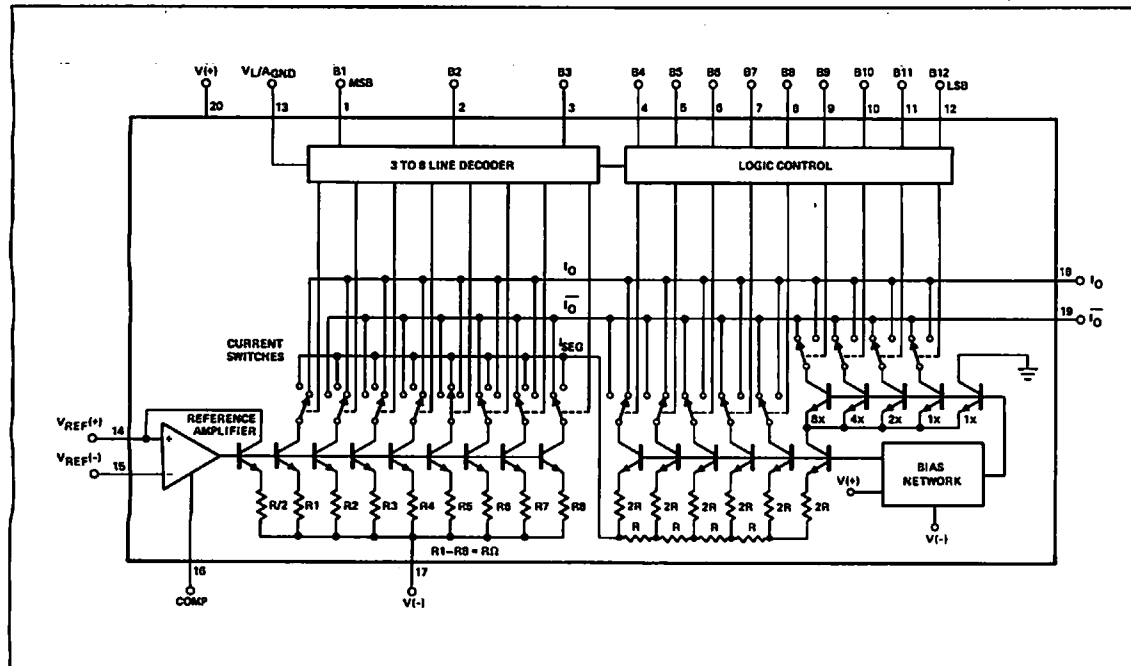
The DAC-312 is divided into two major sections, an 8-segment generator and a 9-bit master/slave D/A Converter. In operation the device performs as follows (See Simplified Schematic):

The three most significant bits (MSB's) are inputs to a 3-to-8 line decoder. The selected resistor (R_5 in the figure) is connected to the master/slave 9-bit D/A Converter. All lower order resistors (R_1 through R_4) are summed into the I_O line, while all higher order resistors (R_6 through R_8) are summed into the $\bar{I}_O$ line. The R_5 current supplies 512 steps of current (0 to 0.499mA for a 1mA reference current) which are also summed into the I_O or $\bar{I}_O$ lines depending on the bits selected. In the figure, the code selected is: 100 110000000. Therefore, 2mA ($4 \times 0.5\text{mA}/\text{segment}$) + 0.375mA (from master/slave D/A Converter) are summed into I_O giving an I_O of 2.375mA. $\bar{I}_O$ has a current of 1.625mA with this code. As the three MSB's are incremented, each successively higher code adds 0.5mA to I_O and subtracts 0.5mA from $\bar{I}_O$, with the selected resistor feeding its current to the master/slave D/A Converter; thus each increment of the 3 MSB's allows the current in the 9-bit D/A Converter to be added to a pedestal consisting of the sum of all lower order currents from the segment generator. This configuration guarantees monotonicity.

EXPANDED TRANSFER CHARACTERISTIC SEGMENT (001 010 011)

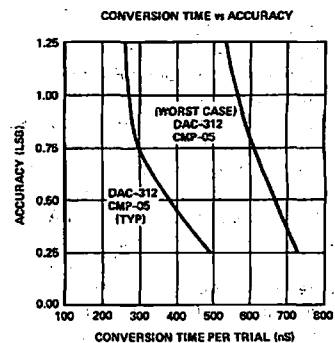
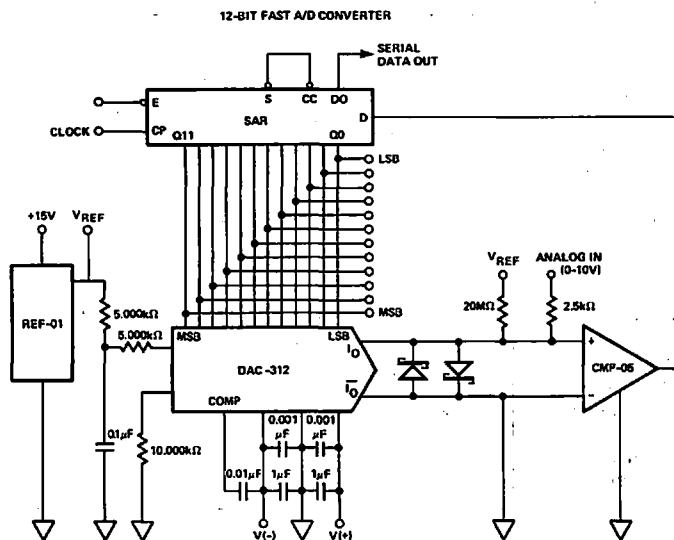


SIMPLIFIED SCHEMATIC





12-BIT FAST A/D CONVERTER



CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
CMP-05	92	125
TOTAL	375ns	680ns
x 13	4.9μs	8.8μs



DAC-888

BYTEDAC® 8-BIT HIGH-SPEED "MICROPROCESSOR COMPATIBLE"
MULTIPLYING D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- 8-Bit Level Triggered Latch
- 8-Bit μ P Compatible
- Easily Interfaced to All 8-Bit Processors
- TTL Logic Compatible
- CE and WR Inputs
- High Output Impedance and Compliance
- Proven DAC-08 Analog Flexibility and Reliability
- Nonlinearity to $\pm 0.1\%$ Max
- Low Power Dissipation 134mW

ORDERING INFORMATION†

18-PIN HERMETIC DUAL-IN-LINE PACKAGE

NL %FS	MILITARY TEMP.	INDUSTRIAL TEMP.
0.1	DAC888AX*	DAC888EX
0.10	DAC888BX*	DAC888FX

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-In is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

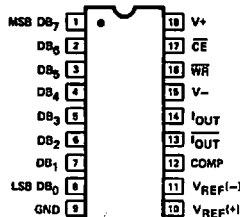
The BYTEDAC® DAC-888 is a buffered 8-bit digital-to-analog converter designed specifically for 8-bit bus oriented systems. The data inputs are connected to level-triggered latches. Two active-low control pins are provided for ease of interface to virtually all available microprocessors. The

latches may also be operated in a transparent mode by holding both control pins low. Additionally, the DAC-888 has a data hold time requirement of zero nanoseconds.

The Analog section consists of a "Field-Proven" DAC-08 D/A Converter. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates full-scale adjustment in most applications.

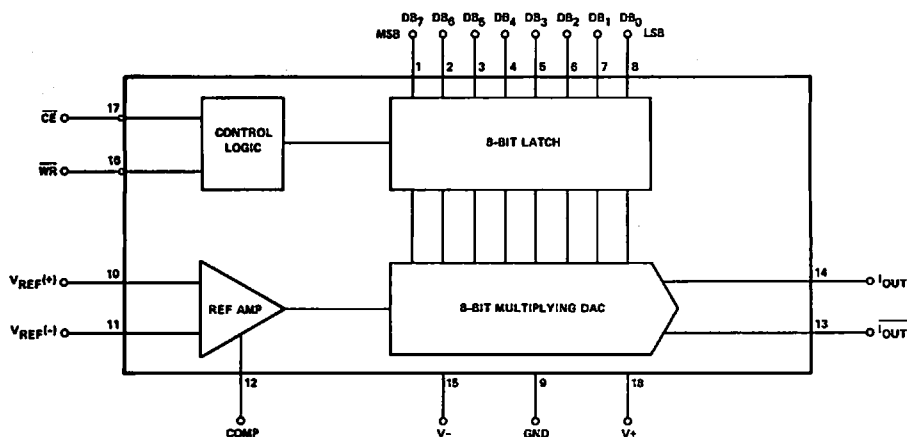
DAC-888 applications include graphic display drivers, high-speed modems, A/D converters, programmable waveform generators and power supplies, analog meter drivers, audio encoders and programmable attenuators; and other applications where low cost, high speed and buffered flexibility are required.

PIN CONNECTIONS



18-PIN HERMETIC
DUAL-IN-LINE
PACKAGE
(X-Suffix)

FUNCTIONAL DIAGRAM



Manufactured under one or more of the following patents: 4,055,773; 4,058,740; 4,092,639

**ABSOLUTE MAXIMUM RATINGS****Operating Temperature**

DAC-888 A/B	-55°C to +125°C
DAC-888 E/F	-25°C to +85°C
DICE Junction Temperature (T _J)	-65°C to +150°C
Storage Temperature	-65°C to +150°C
Power Dissipation	300mW
Derate above 100°C	10mW/°C
Lead Temperature (Soldering, 60 sec)	300°C
V+ Supply to V- Supply	18.1V

Logic Inputs	0V to 5.5V
Analog Current Outputs	-5mA
Reference Inputs (V ₁₀ to V ₁₁)	V- to V+
Reference Input Differential Voltage (V ₁₀ to V ₁₁)	±15V
Reference Input Current	5mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V+ = +5V, V- = -12V, I_{REF} = 2mA, T_A = -55°C to +125°C for DAC-888A/B, unless otherwise noted. T_A = 25°C to +85°C apply for DAC-888E/F. Output characteristics refer to both I_{OUT} and I_{OUT}.

PARAMETER	SYMBOL	CONDITIONS	DAC-888A/E			DAC-888B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			8	—	—	8	—	—	Bits
Monotonicity			8	—	—	8	—	—	Bits
Nonlinearity	NL		—	—	±0.1	—	—	±0.19	%FS
Full-Scale Tempco	TCI _{FS}	(See note)	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance	V _{OC}	Full-Scale Current Change < 1/2 LSB	-5	—	+5	-5	—	+5	V
Output Impedance	R _{OUT}		—	>20	—	—	>20	—	MΩ
Full Range Current	I _{FR}	V _{REF} = 10.000V R ₁₁ , R ₁₀ = 5.000kΩ T _A = 25°C	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I _{FRS}	I _{FR14} - I _{FR13}	—	±1	±8	—	±1	±8	μA
Zero-Scale Current	I _{ZS}		—	0.2	2	—	0.2	2	μA
Output Current Range	I _{FSR}	I _{REF} = 3mA	2.1	2.9	—	2.1	2.9	—	mA
Reference Bias Current	I _B		—	-1	-3	—	-1	-3	μA
Power Supply Sensitivity	PSSI _{FR+}	V+ = 4.5V to 5.5V	—	±0.0003	±0.01	—	±0.0003	±0.01	%ΔI _{FS} /ΔV+
	PSSI _{FR-}	V- = -10.8V to -13.2V I _{REF} = 1mA	—	±0.0002	±0.01	—	±0.0002	±0.01	%ΔI _{FS} /ΔV-
Power Supply Current	I+	I _{REF} = 2mA	—	12	16	—	12	16	mA
	I-		—	6	9	—	6	9	
Power Dissipation	P _d	I _{REF} = 2mA	—	134	190	—	134	190	mW
Logic Input Levels									
Logic Input "0"	V _{IL}		—	—	0.8	—	—	0.8	V
Logic Input "1"	V _{IH}		2	—	—	2	—	—	
Logic Input Current									
Logic Input "0"	I _{IL}	V _{IN} = 0V	—	-2	-10	—	-2	-10	μA
Logic Input "1"	I _{IH}	V _{IN} = 5.25V	—	0.1	1	—	0.1	1	

NOTE: Guaranteed by design.

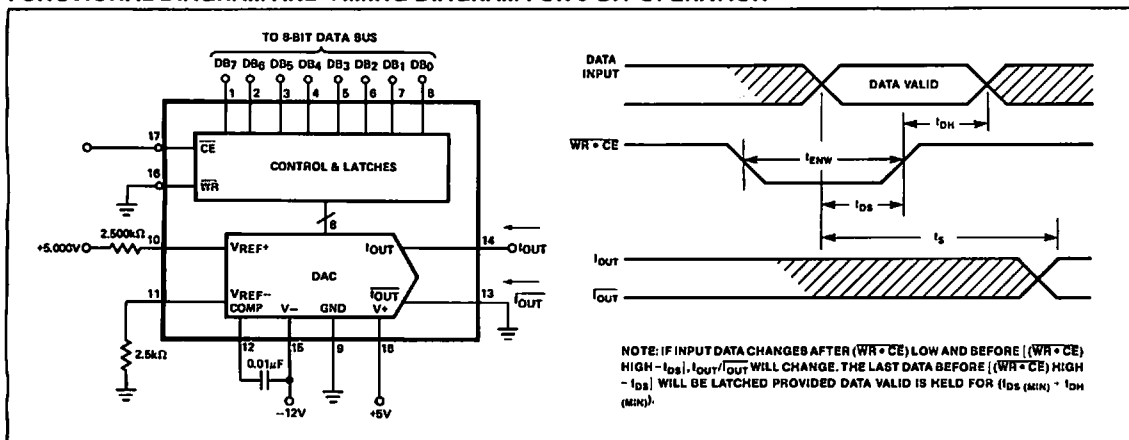
**ELECTRICAL CHARACTERISTICS — A.C. PARAMETERS** $V_S = +5V, -12V, I_{REF} = 2mA, T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	DAC-888A/E			DAC-888B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Settling Time	t_s	From $\overline{CE}$ & $\overline{WR}$ Negative Level to $\pm 1/2LSB$, All Bits Switched ON or OFF. (See note)	—	300	400	—	300	400	ns
Reference Input Slew Rate	dI/dt	(See Note)	4	8	—	4	8	—	mA/ μs
Data Input Setup Time	t_{DS}	(See note)	150	—	—	150	—	—	ns
Data Input Hold Time	t_{DH}	(See note)	10	—	—	10	—	—	ns
Chip Enable/Write Pulse Width	t_{ENW}	(See note)	250	—	—	250	—	—	ns

NOTE: Guaranteed by design.

DAC-888 PIN DESCRIPTION

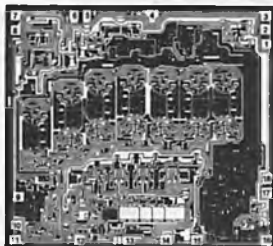
SYMBOL	DESCRIPTION	
DB ₀ - DB ₇	DATA BIT — Bits 0-7 are digital, active-high inputs. DB ₇ is assigned as the MSB.	PINS 1-8
$\overline{CE}$	CHIP ENABLE — An active low input control which is the device enable input terminal.	PIN 17
$\overline{WR}$	WRITE CONTROL — An active low control which enables the microprocessor to write data to the DAC.	PIN 18
$I_{OUT+} \cdot I_{OUT-}$	CURRENT OUTPUT — Complementary current outputs, which when added, equal I_{FS} .	PINS 13-14
V_{REF+}, V_{REF-}	VOLTAGE REFERENCE — Differential inputs that accept a negative, positive, or bipolar input and are used to set I_{FS} .	PINS 10-11
COMP	COMPENSATION — The reference amplifier frequency compensating terminal.	PIN 12

FUNCTIONAL DIAGRAM AND TIMING DIAGRAM FOR 8-BIT OPERATION**OPERATION TABLE**

$\overline{CE}$	$\overline{WR}$	OUTPUT
1	X	NO CHANGE
0	1	NO CHANGE
0	0	UPDATE LATCHES (TRANSPARENT)



DICE CHARACTERISTICS

DIE SIZE 0.141 × 0.127 inch, 17, 907 sq. mils
(3.58 × 3.23 mm, 11.56 sq. mm)

- | | |
|--------------|--------------------------|
| 1. DB7 (MSB) | 10. V _{REF} (+) |
| 2. DB6 | 11. V _{REF} (-) |
| 3. DB5 | 12. COMP |
| 4. DB4 | 13. I _{OUT} |
| 5. DB3 | 14. I _{OUT} |
| 6. DB2 | 15. V- |
| 7. DB1 | 16. W _R |
| 8. DB0 (LSB) | 17. CE |
| 9. GROUND | 18. V+ |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at V_S = +5, -12V, I_{REF} = 2mA, T_A = 25°C, unless otherwise noted. Output characteristics refer to both I_{OUT} and I_{OUT}.

PARAMETER	SYMBOL	CONDITIONS	DAC-888N LIMIT	DAC-888G LIMIT	UNITS
Resolution			8	8	Bits MIN
Monotonicity			8	8	Bits MIN
Nonlinearity			±0.1	±0.19	%FS MAX
Output Voltage Compliance	V _{OC}	Full-Scale Current Change < 1/2 LSB R _{OUT} > 20MΩ Typ.	+5	+5	V MAX
			-5	-5	V MIN
Full Range Current	I _{FR14}	V _{REF} = 10.000V R ₁₁ , R ₁₀ = 5.000kΩ T _A = 25°C	2.04	2.04	mA MAX
			1.94	1.94	mA MIN
Full Range Symmetry	I _{FRS}	I _{FR14} - I _{FR13}	±8	±8	μA MAX
Zero-Scale Current	I _{ZS}		2	2	μA MAX
Output Current Range	I _{FSR}	I _{REF} = 3mA	2.1	2.1	mA MIN
Reference Bias Current	I _B		-3	-3	μA MAX
Power Supply Sensitivity	PSSI _{FR+} PSSI _{FR-}	V+ = 4.5V to 5.5V	±0.01	±0.01	%ΔV _{FS} /ΔV+ MAX
		V- = -10.8V to -13.2V, I _{REF} = 1mA	±0.01	±0.01	%ΔV _{FS} /ΔV- MAX
Power Supply Current	I+ I-	I _{REF} = 2mA	16	16	mA MAX
			9	9	mA MAX
Power Dissipation	P _d	I _{REF} = 2mA	190	190	mW MAX
Logic Input Levels	V _{IL} V _{IH}		0.8	0.8	V MAX
			2	2	V MIN
Logic Input Current	I _{IL} I _{IH}	V _{IN} = 0V	-10	-10	μA MAX
		V _{IN} = 5.25V	1	1	μA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS V+ = +5V, -12V, I_{REF} = 2mA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-888 TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8.0	mA/μs
Settling Time	t _S	From CE Negative Edge to ±1/2 LSB, All bits Switched ON or OFF	300	ns
Data Input Setup Time	t _{DS}		100	ns
Data Input Hold Time	t _{DH}		0	ns
Chip Enable Write Pulse Width	t _{ENW}		200	ns



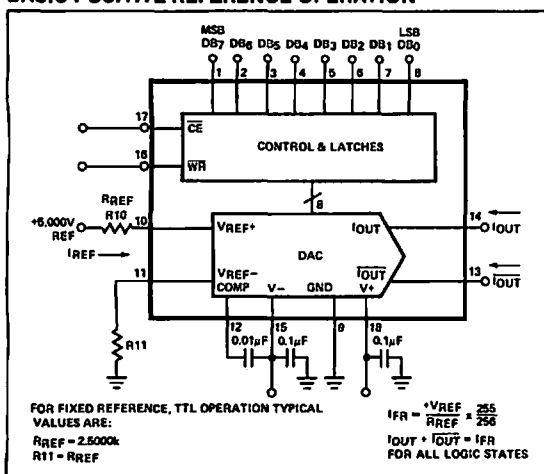
DIGITAL INFORMATION

The BYTEDAC® DAC-888 is a monolithic microprocessor compatible D/A converter consisting of an 8-bit level triggered latch, control circuitry and one 8-bit multiplying D/A converter housed in an 18-pin dual in line package (DIP).

The DAC-888 accepts 8-bit binary bytes at the data inputs. Data access is accomplished when $\overline{WR}$ and $\overline{CE}$ are low. During the low state of $\overline{CE}$ and $\overline{WR}$, the latches are transparent, therefore, data should be valid from 100ns prior to $\overline{WR}$ and $\overline{CE}$ low until $\overline{CE}$ or $\overline{WR}$ high. When $\overline{CE}$ or $\overline{WR}$ goes high, the data stored in the latches will hold the selected output indefinitely.

ANALOG INFORMATION

BASIC POSITIVE REFERENCE OPERATION



REFERENCE AMPLIFIER SET-UP

The DAC-888 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed

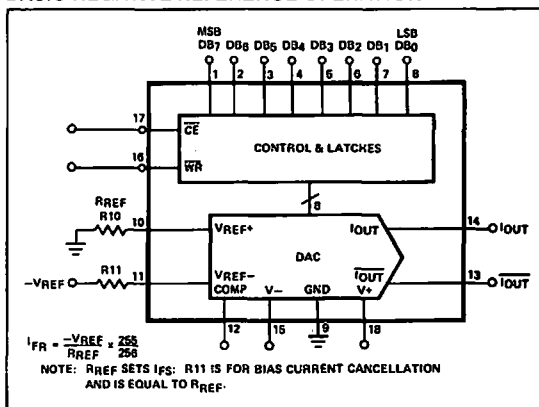
or may vary from nearly 0 to +4.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = 1_{10}$$

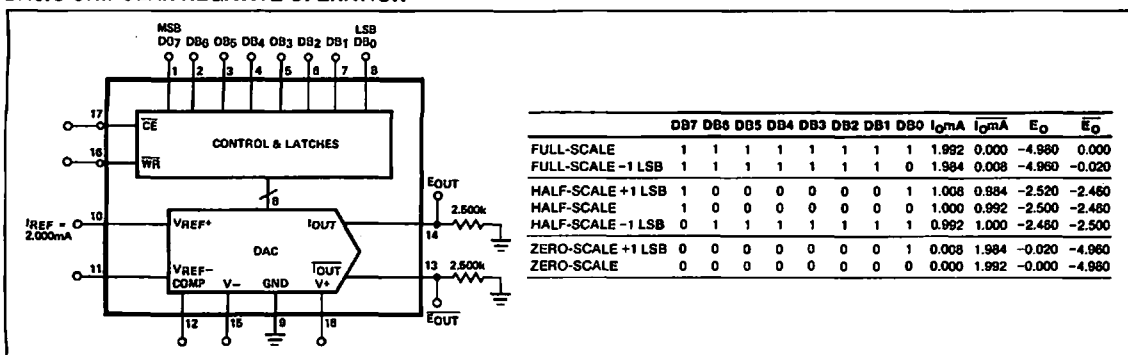
In positive reference applications, an external positive reference voltage current flows through R_{10} into the $V_{REF(+)}$ terminal of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$; reference current flows from ground through R_{10} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 11. The voltage at pin 10 is equal to and tracks the voltage at pin 11 due to the high gain of the internal reference amplifier. R_{11} (nominally equal to R_{10}) is used to cancel bias current errors; R_{11} may be eliminated with only a minor increase in error.

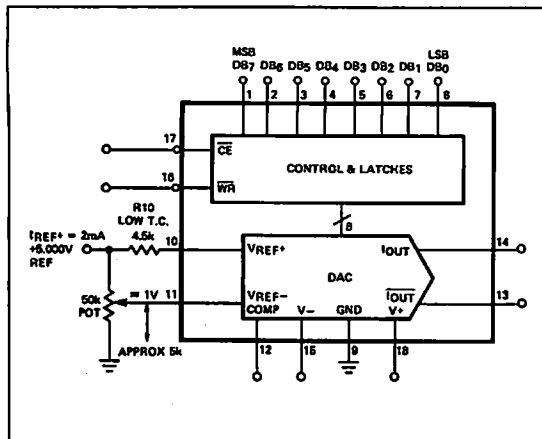
For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF} . If required, full-scale trimming may be accomplished by adjusting the value of R_{10} or by using a potentiometer for R_{10} . An improved method of full-scale trimming which eliminates potenti-

BASIC NEGATIVE REFERENCE OPERATION



BASIC UNIPOLAR NEGATIVE OPERATION



RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT


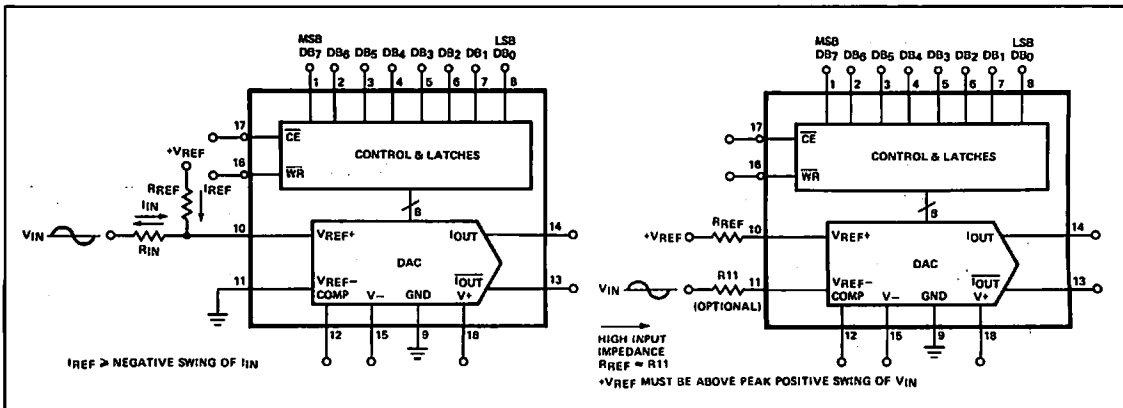
meter TC effects is shown in the Recommended Full Scale Adjustment Circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 12 to V-. For fixed reference operation a 0.01μF capacitor is recommended. For variable reference applications, see "Reference Amplifier Compensation for Multiplying Applications" section.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 12 to V-. The value of this capacitor depends on the impedance presented to pin 10 (see Table 1).

ACCOMMODATING BIPOLAR REFERENCES

TABLE 1. REFERENCE AMPLIFIER COMPENSATION

REF. INPUT RESISTANCE	SUGGESTED C_C
1kΩ	15pF
2.5kΩ	37pF
5kΩ	75pF

NOTE: A 0.01μF capacitor is suggested for fixed references.

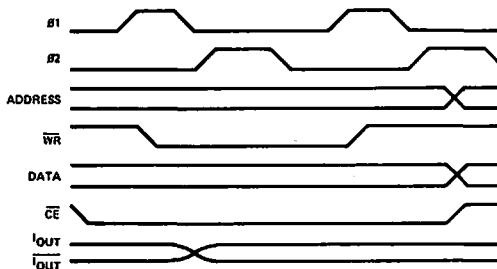
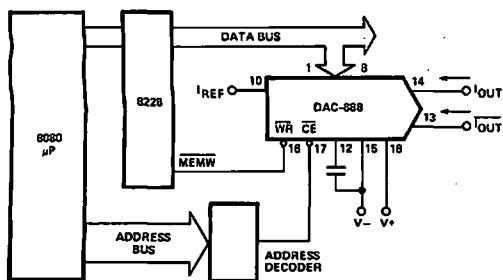
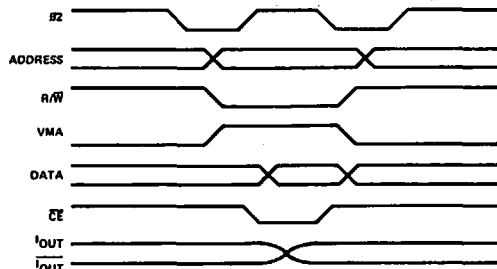
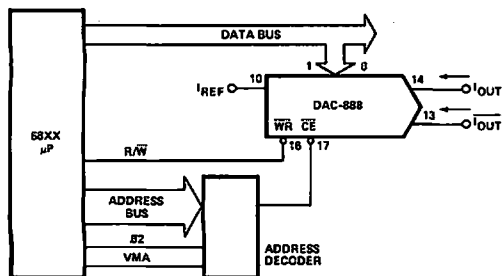
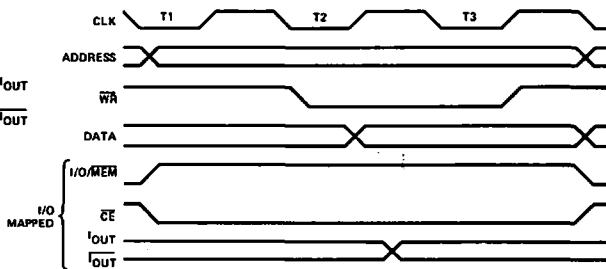
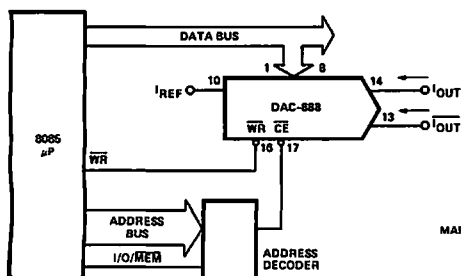
For fastest response to a pulse, low values of R_{10} , enabling small C_C values, should be used. If pin 10 is driven by a high current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For $R_{10} = 1kΩ$ and $C_C = 15pF$, the reference amplifier slews at 4mA/μs, enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns (see Figure, pulsed reference operation).

Bipolar references may be accommodated by offsetting V_{REF} or pin 11, as shown in Figure below. The negative common-mode range of the reference amplifier is given by $V_{CM} = V_-$ plus $(I_{REF} \times 1kΩ)$ plus 2.5V. The positive common-mode range is V_+ less 1.5V.

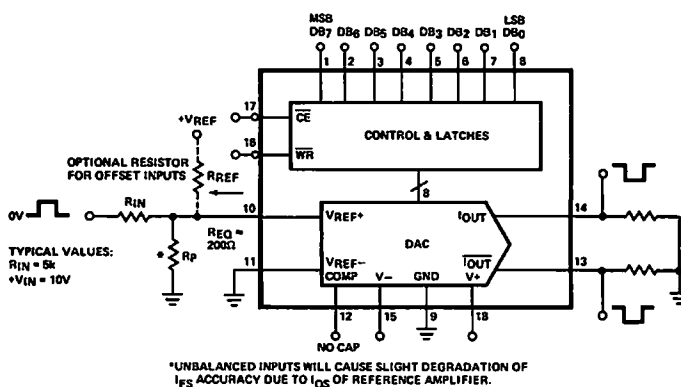
When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL Logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{10} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

ANALOG OUTPUT CURRENTS

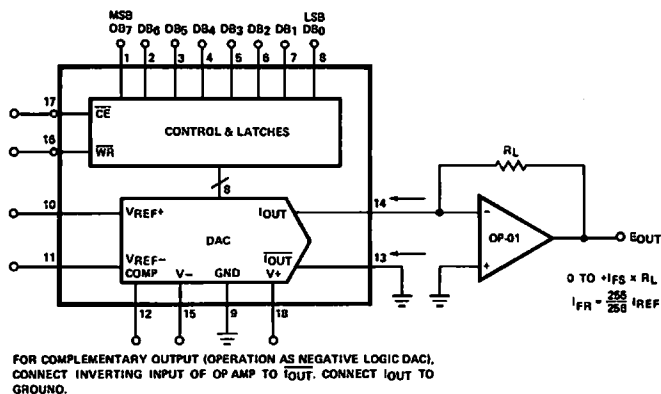
Both true and complemented output sink currents are provided, where $I_O + \bar{I}_O = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 14 increases proportionally in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 14 and turned on at pin 13. A decreasing logic count increases $\bar{I}_O$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS} ; do not leave an unused output pin open.

8080 INTERFACE

6800, 6801, 6809 INTERFACE

8085 INTERFACE


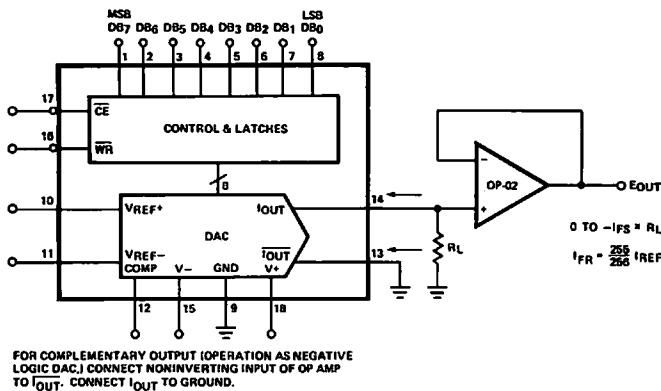
PULSED REFERENCE OPERATION



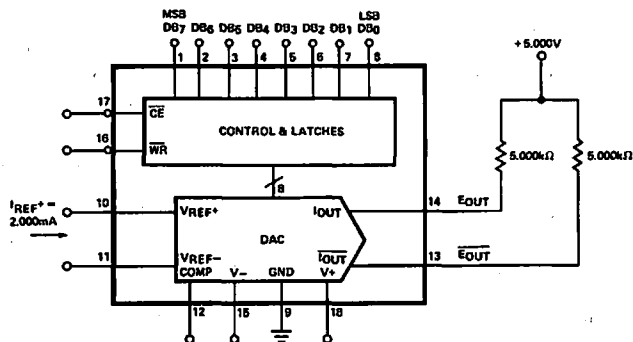
POSITIVE LOW IMPEDANCE OUTPUT OPERATION



NEGATIVE LOW IMPEDANCE OUTPUT OPERATION

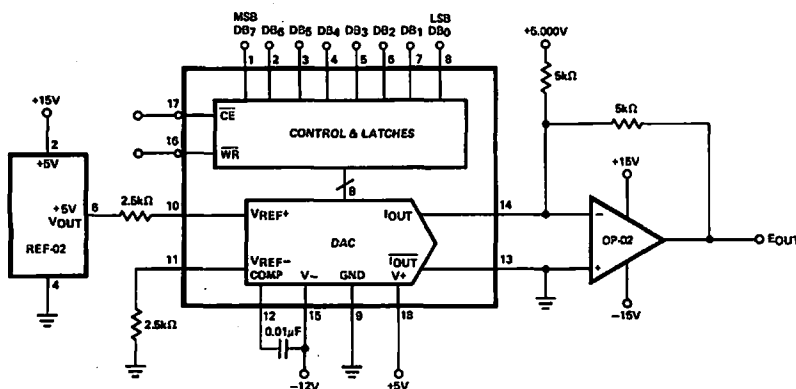


BASIC BIPOLAR OUTPUT OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O	E_O^-
POSITIVE FULL-SCALE	1	1	1	1	1	1	1	1	-4.960	5.000
POSITIVE FULL-SCALE -1LSB	1	1	1	1	1	1	1	0	-4.920	4.960
ZERO-SCALE +1LSB	1	0	0	0	0	0	0	1	-0.040	0.080
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000	0.040
ZERO-SCALE -1LSB	0	1	1	1	1	1	1	1	0.040	0.000
NEGATIVE FULL-SCALE +1LSB	0	0	0	0	0	0	0	1	4.900	-4.920
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	5.000	-4.960

OFFSET BINARY OPERATION



	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	E_O
POSITIVE FULL-SCALE	1	1	1	1	1	1	1	1	4.960
POSITIVE FULL-SCALE -1LSB	1	1	1	1	1	1	1	0	4.920
ZERO-SCALE	1	0	0	0	0	0	0	0	0.000
NEGATIVE ZERO-SCALE +1LSB	0	0	0	0	0	0	0	1	-4.960
NEGATIVE FULL-SCALE	0	0	0	0	0	0	0	0	-5.000



BASIC BIPOLAR OUTPUT OPERATION

Both outputs have an extremely wide voltage compliance, enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 18V above V_- and is independent of the positive supply. Negative compliance is given by V_- plus $(I_{REF} \times 1k\Omega)$ plus 2.5V.

POWER SUPPLIES

The DAC-888 operates over a wide range of power supply voltages from a total supply of 9V to 15V. When operating at supplies of $\pm 5V$ or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at $-4.5V$ with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower

supplies is possible. However, at least 8V must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-888 is quite insensitive to variations in supply voltage.

Power consumption may be calculated as follows:

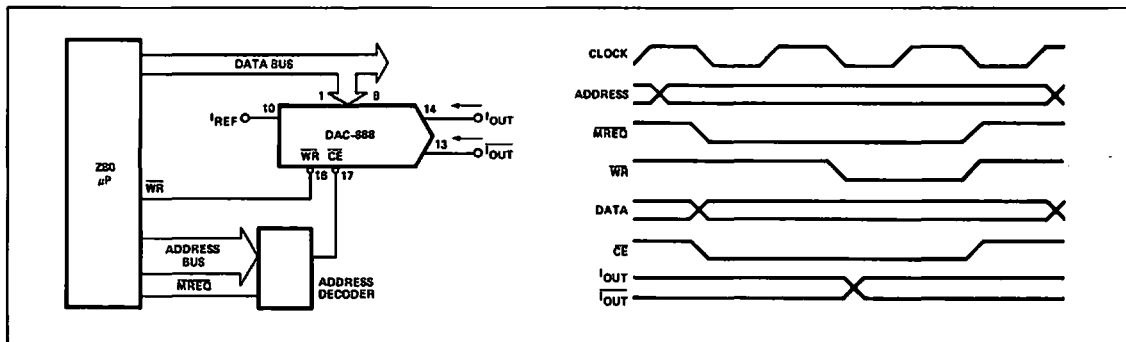
$$P_d = (I_+) (V_+) + (I_-) (V_-).$$

TEMPERATURE PERFORMANCE

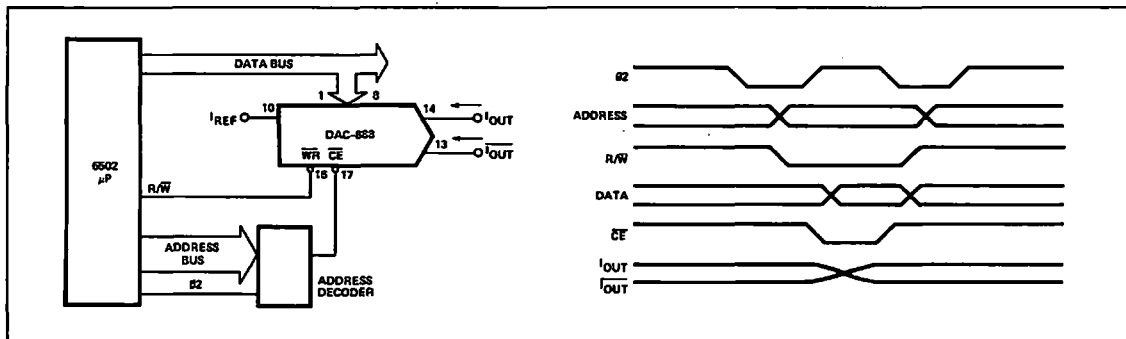
The nonlinearity and monotonicity specifications of the DAC-888 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically $\pm 10ppm/^{\circ}C$, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{10} should match and track that of the output resistor for minimum overall full-scale drift. Settling times of the DAC-888 decrease approximately 10% at $-55^{\circ}C$; at $+125^{\circ}C$ an increase of about 15% is typical.

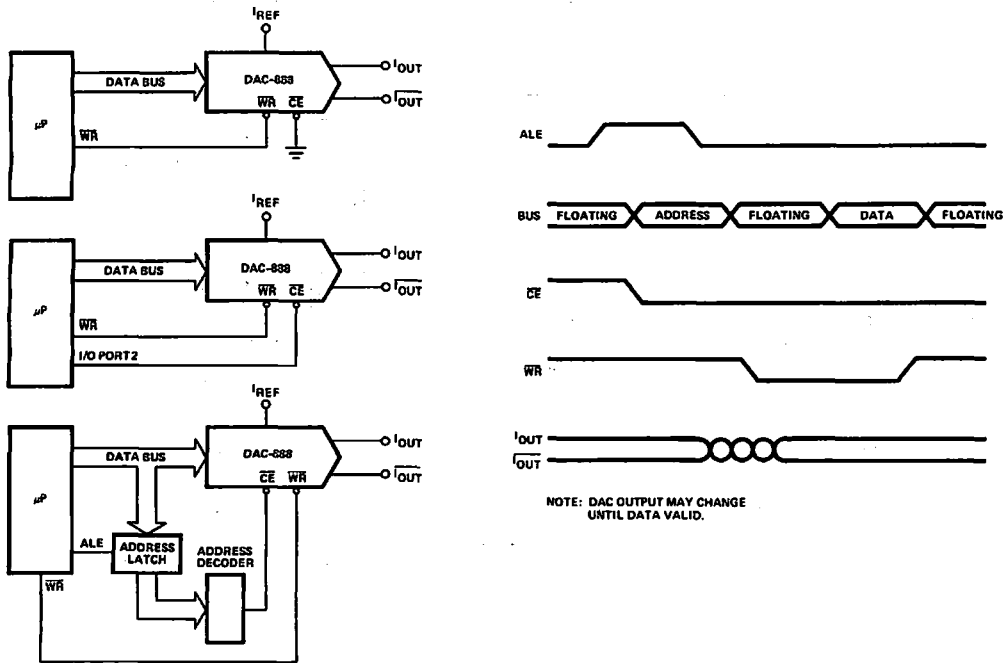
Z80 INTERFACE



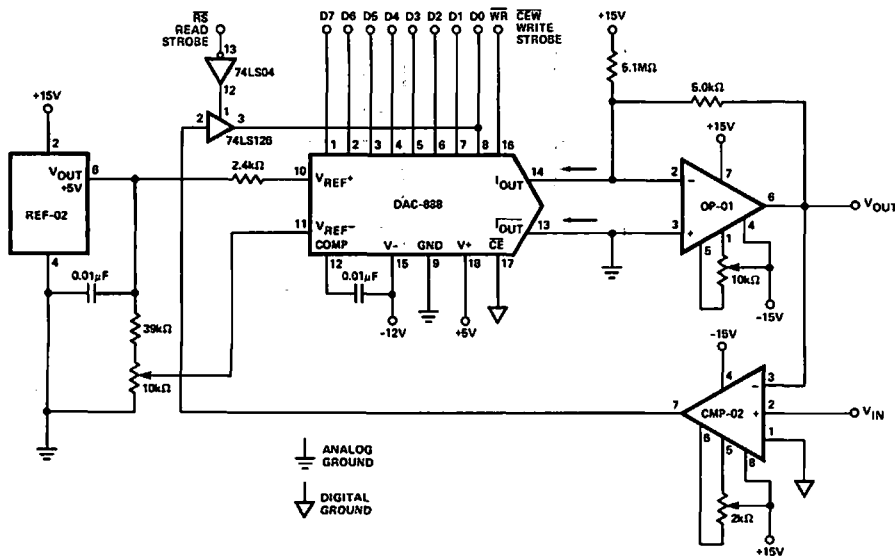
6502 INTERFACE



8048 INTERFACE

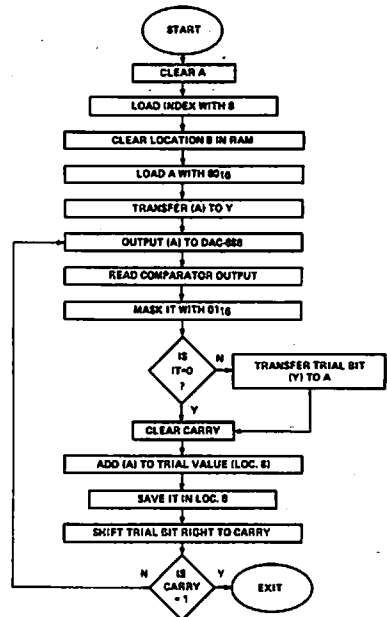
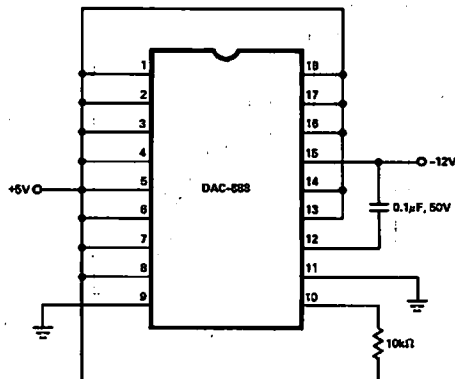


'SOFTWARE SAR' A/D CONVERTER (WITH 8048 MICROPROCESSOR)



**SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERSION PROGRAM
LISTING USING DAC-888 AND SYM 1 PCB WITH 6502 μ P WITH FLOW CHART**

LOCATION	DATA	MNEMONIC	COMMENTS
500	A9 00	LDA #00	Clear
502	A2 08	LDX #08	Set Index Register
504	95 00	STA ,X	Clear Memory at 08 _H
506	A9 80	LDA #80	Trial Bit
508	A8	TAY	TO Y
509	8D 00 10	STA 1000 (Cont.)	Output
50C	AD 00 1C	LDA 1C00	Read Comp.
50F	29 01	AND A, #01	Mask it
511	F0 01	BEQ * +1	Branch if CMP = 0
513	98	TYA	Get Trial Bit
514	18	CLC	Clear Carry
515	75 00	ADC ,X	Result Summed With Previous Test
517	95 00	STA ,X	Save it
519	98	TYA	Get Trial Value
51A	4A	LSR	Next Bit
51B	A8	TAY	Save it
51C	15 00	ORA ,X	Next Data
51E	90 E9	BCC *-23	Continue For 8 Trials
520	4C 00 05	JMP 500	Do Over

NOTE: 32 Bytes 260 μ s**BURN-IN CIRCUIT**



DAC-1508A/1408A

8-BIT MULTIPLYING
D/A CONVERTERS

Precision Monolithics Inc.

FEATURES

- Improved Direct Replacement for MC1508/MC1408
- 0.19% Nonlinearity Maximum Over Temperature Range
- Improved Settling Time 250ns, Typ
- Improved Power Consumption 157mW, Typ
- Compatible with TTL, CMOS Logic
- Standard Supply Voltages +5.0V and -5.0V to -15V
- Output Voltage Swing +0.5V to -5.0V
- High-Speed Multiplying Input 4.0mA/ μ s

ORDERING INFORMATION†

RELATIVE ACCURACY % FS	16-PIN DUAL-IN-LINE PACKAGE		
	MILITARY	HERMETIC COMMERCIAL	PLASTIC COMMERCIAL
$\pm 0.19\%$	DAC1508A-8Q*	DAC1408A-8Q	DAC1408A-8P
$\pm 0.39\%$	—	DAC1408A-7Q	DAC1408A-7P
$\pm 0.78\%$	—	DAC1408A-6Q	DAC1408A-6P

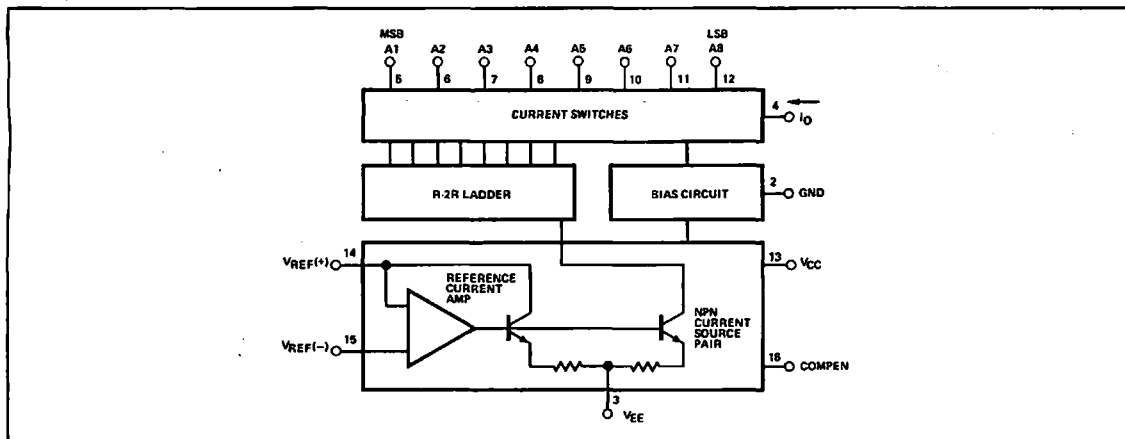
*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The DAC-1508A/1408A are 8-bit monolithic multiplying digital-to-analog converters consisting of a reference current amplifier, R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added. Improvements in design and processing techniques provide faster settling times combined with lower power consumption while retaining direct interchangeability with MC1508/1408 devices.

SIMPLIFIED SCHEMATIC

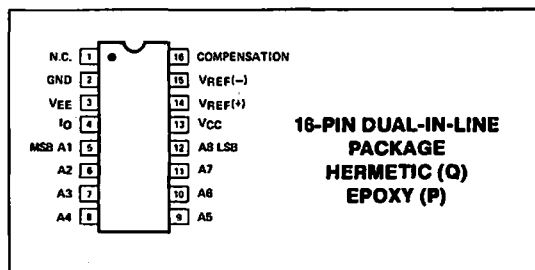


The R-2R ladder divides the reference current into eight binary-related components which are fed to the switches. A remainder current equal to the least significant bit is always shunted to ground, therefore the maximum output current is 255/256 of the reference amplifier input current. For example, a full-scale output current of 1.992mA would result from a reference input current of 2.0mA.

The DAC-1508A/1408A is useful in a wide variety of applications, including waveform synthesizers, digitally programmable gain and attenuation blocks, CRT character generation, audio digitizing and decoding, stepping motor drives, programmable power supplies and in building tracking and successive approximation analog-to-digital converters.

For significantly improved speed and applications flexibility your attention is directed to the DAC-08 8-bit high-speed multiplying D/A converter data sheet. For D/A converters, which include precision voltage references on the chip, please refer to the DAC-210 or the DAC-100 data sheet.

PIN CONNECTIONS



DIGITAL-TO-ANALOG CONVERTERS

**ABSOLUTE MAXIMUM RATINGS**

Power Supply Voltage	
V _{CC}	+5.5Vdc
V _{EE}	-16.5Vdc
Digital Input Voltage, V ₅ through V ₁₂	+5.5, 0Vdc
Applied Output Voltage	+0.5, -5.2Vdc
Reference Current, I ₁₄	5mA
Power Dissipation (Package Limitation), P _d	
Ceramic Package (or Epoxy B Package)	100mW
Derate above T _A = +25°C	6.7mW/°C

Derate above T _A = +100°C for	
Epoxy B Package	5.3mW/°C
Operating Temperature Range, T _A	
DAC-1508A	-55°C to +125°C
DAC-1408A	0°C to +75°C
DICE Junction Temperature (T _J)	-65°C to +150°C
Storage Temperature Range, T _{stg}	-85°C to +150°C
Plastic Package Only	-85°C to +125°C

NOTE: Ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at V_{CC} = +5Vdc, V_{EE} = -15Vdc, V_{REF}/R₁₄ = 2mA, -55°C ≤ T_A ≤ +125°C for DAC-1508A-8, 0°C ≤ T_A ≤ +75°C for DAC-1408A, unless otherwise noted. All digital inputs at logic high level.

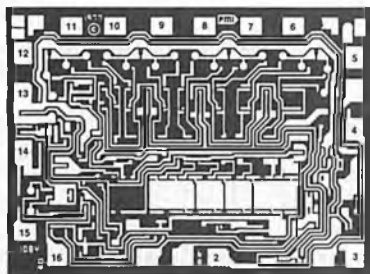
PARAMETER	SYMBOL	CONDITIONS	DAC-1508A/1408A			UNITS
			MIN	TYP	MAX	
Relative Accuracy (error relative to Full-Scale I _O)						
DAC-1508A-8, DAC-1408A-8	E _r		—	—	±0.18	%IFS
DAC-1408A-7			—	—	±0.39	
DAC-1408A-6			—	—	±0.78	
Settling Time to within 1/2 LSB (includes t _{PLH})	t _S	T _A = +25°C	—	250	—	ns
Propagation Delay Time	t _{PLH} , t _{PHL}	T _A = +25°C, (Note 1)	—	30	100	ns
Output Full-Scale Current Drift	TCI _O		—	±20	—	ppm/°C
Digital Input Logic Levels (MSB)						
High Level, Logic "1"	V _{IH}		2	—	—	Vdc
Low Level, Logic "1"	V _{IL}		—	—	0.8	
Digital Input Current (MSB)	I _{IH} I _{IL}	High Level, V _{IH} = 5.0V Low Level, V _{IL} = 0.8V	— —	0 -0.4	0.04 -0.8	mA
Reference Input Bias Current (Pin 15)	I ₁₅		—	-1	-3	
Output Current Range	I _{OR}	V _{EE} = -5V V _{EE} = -15V	0 0	2.0 2.0	2.1 4.2	mA
Output Current	I _O	V _{REF} = 2.000V, R ₁₄ = 1000Ω	1.9	1.99	2.1	
Output Current	I _{O, min.}	All bits low	—	0	4	μA
Output Voltage Compliance (E _r ≤ 0.19% at T _A = +25°C)	V _O	I _{REF} = 1mA V _{EE} = -5V V _{EE} = -10V	-0.6 -5	— —	+0.5 +0.5	Vdc
Reference Current Slow Rate	SRI _{REF}		—	4	—	
Output Current Power Supply Sensitivity	PSSI _O		—	0.5	2.7	μA/V
Power Supply Current	I _{CC} I _{EE}	All bits low	— —	+9 -7.5	+14 -13	mA
Power Supply Voltage	V _{CCR} V _{EER}	T _A = +25°C	+4.5 -4.5	+5 -15	+5.5 -16.5	
Power Dissipation	P _d	All bits low	—	—	—	mW
		V _{EE} = -5Vdc	—	82	135	
		V _{EE} = -15Vdc	—	157	285	
		All bits high	—	—	—	
		V _{EE} = -5Vdc	—	70	—	
		V _{EE} = -15Vdc	—	132	—	

NOTE:

1. Guaranteed by design.



DICE CHARACTERISTICS

DIE SIZE 0.087 × 0.063 inch, 5481 sq. mils
(2.21 × 1.60 mm, 3.54 sq. mm)

- | | |
|--------------------|--------------------------|
| 1. N.C. | 9. A5 |
| 2. GROUND | 10. A6 |
| 3. V _{EE} | 11. A7 |
| 4. I _O | 12. A8 (LSB) |
| 5. A1 (MSB) | 13. V _{CC} |
| 6. A2 | 14. V _{REF} (+) |
| 7. A3 | 15. V _{REF} (-) |
| 8. A4 | 16. COMP |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFFER TEST LIMITS at V₊ = 5V, V₋ = 15V, I_{REF} = 2mA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-1408A-G LIMIT	UNITS
Resolution			8	Bits MIN
Monotonicity			8	Bits MIN
Nonlinearity			±0.19	%FS MAX
Output Voltage Compliance	V _O	Full-Scale Current Change, I _{REF} = 1mA	+0.5	V MAX
		< 1/2 LSB V ₋ = -5V	-0.6	V MIN
		V ₋ = -10V	-5	V MIN
Full-Scale Current	I _{FS}	V _{REF} = 2.000V, R ₁₄ , R ₁₅ = 1.000kΩ	2, ±0.1	mA MAX
Zero-Scale Current	I _{ZS}	(All Bits Low)	4	μA MAX
Output Current Range	I _{OR}	V ₋ = -5V	2.1	mA MAX
		V ₋ = -15V	4.2	mA MAX
Logic "0" Input Level	V _{IL}		0.8	V MAX
Logic "1" Input Level	V _{IH}		2	V MIN
Logic Input Current	I _{IL} , I _{IH}	Low Level, V _{IL} = -0.8V	±10	μA MAX
		High Level, V _{IH} = 5V	±10	μA MAX
Reference Bias Current	I _{IS}		-3	μA MAX
Output Current Power Supply Sensitivity	PSSI _{O-}		2.7	μA/V MAX
Power Supply Current (All Bits Low)	I ₊ , I ₋		+14	mA MAX
			-13	mA MAX
Power Supply Voltage Range	V _{CCR} , V _{EE}		+5, ±0.5	V MAX/MIN
			-16.5, -4.5	V MAX/MIN
Power Dissipation (All Bits Low)	P _d	V ₋ = 5V	135	mW MAX
		V ₋ = -15V	265	mW MAX

NOTE:

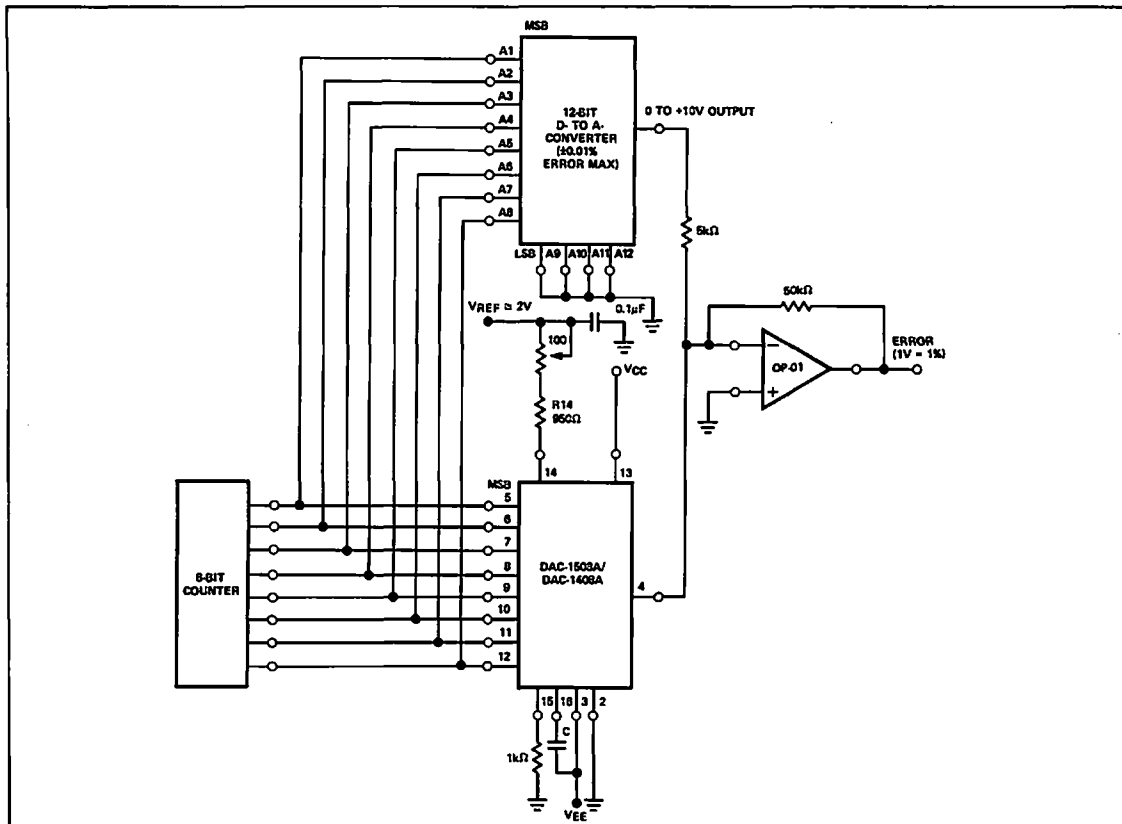
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V₊ = +5V, V₋ = -15V, T_A = 25°C, V_{LC} and I_{OUT} connected to ground, and I_{REF} = 2mA, unless otherwise noted. Output characteristics refer to I_{OUT} only.

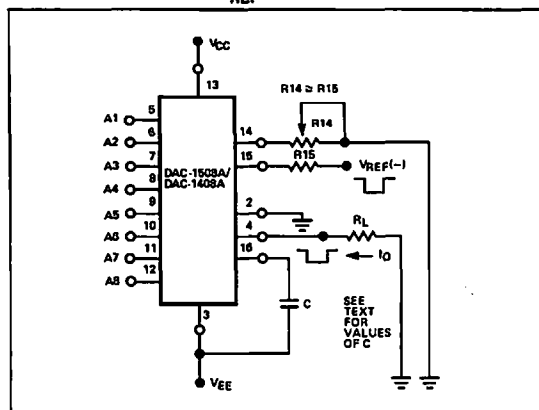
PARAMETER	SYMBOL	CONDITIONS	DAC-1408G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		4	mA/μs
Propagation Delay	t _{PLH} , t _{PHL}	Any Bit	30	ns
Settling Time	t _S	To ±1/2 LSB, All Bits Switched ON or OFF	250	ns

APPLICATIONS

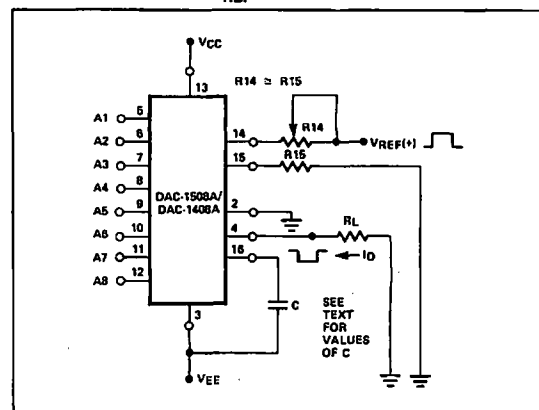
RELATIVE ACCURACY TEST CIRCUIT



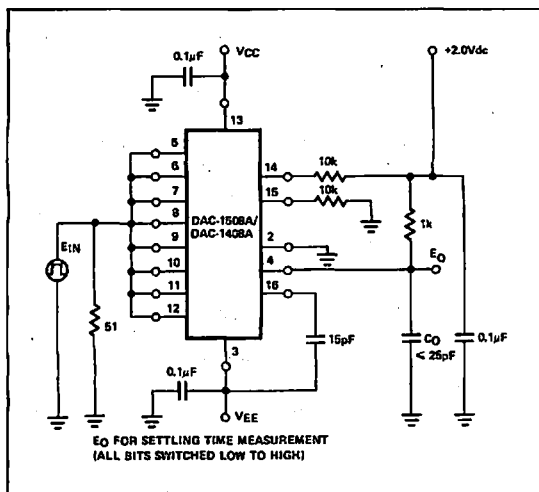
USE WITH NEGATIVE V_{REF}



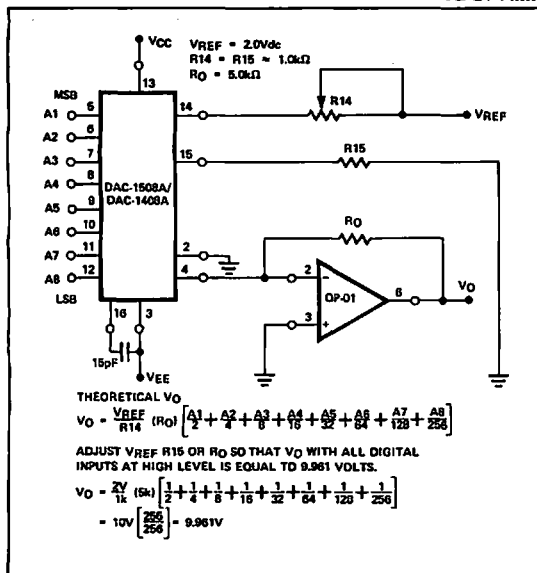
USE WITH POSITIVE V_{REF}



TRANSIENT RESPONSE AND SETTLING TIME TEST CIRCUIT



USE WITH CURRENT-TO-VOLTAGE CONVERTING OP AMP



GENERAL INFORMATION AND APPLICATION NOTES

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at Pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14} , must always flow into

Pin 14 regardless of the setup method or reference voltage polarity. Connections for a positive voltage are shown on the preceding page. The reference voltage source supplies the full current I_{14} . For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R_{15} with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R_{14} to maintain proper phase margin; for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on Pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic is to be used as the reference, R_{14} should be decoupled by connecting it to +5.0V through another resistor and bypassing the junction of the two resistors with 0.1µF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between Pin 14 and ground.

If Pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on Pin 4 is restricted to a range of -0.6V to +0.5V when $V_{EE} = -5V$ due to the current switching methods employed in the DAC-1508A-8.

The negative output voltage compliance of the DAC-1508A-8 is extended to -5.0V where the negative supply voltage is more negative than -10V. Using a full-scale current of 1.992mA and load resistor of 2.5kΩ between Pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980V. The value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500Ω do not significantly affect performance but a 2.5kΩ load increases "worst case" settling time to 1.2µs (when all bits are switched on). Refer to the subsequent text section of Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than -7.0V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC-1508A-8 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC-1508A-8 has a very low full-scale current drift with temperature.

The DAC-1508A-8/DAC-1408A series is guaranteed accurate to within $\pm 1/2$ LSB at a full-scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of one LSB (8.0 μ A), which is the ladder remainder shunted to ground. The input current to Pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. Testing relative accuracy is accomplished by the circuit labelled "Relative Accuracy Test Circuit". The 12-bit converter is calibrated for a full-scale output current of 1.992mA. This is an optional step since the DAC-1508A-8 accuracy is essentially the same between 1.5 and 2.5mA. Then the DAC-1508A-8 circuit's full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D/A converters may not be used to construct a 16-bit accuracy D/A converter. 16-bit accuracy implies a total error of $\pm 1/2$ of one part in 65,536, or $\pm 0.00076\%$ which is much more accurate than the $\pm 0.19\%$ specification provided by the DAC-1508A-8.

MULTIPLYING ACCURACY

The DAC-1508A-8 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μ A to 4.0mA, the additional error contributions are less than 1.6 μ A. This is well within eight-bit accuracy when referred to full scale.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC-1508A-8 is monotonic for all values of reference current above 0.5mA. The recommended range for operation with a DC reference current is 0.5 to 4.0mA.

SETTLING TIME

The "worst case" switching condition occurs when all bits are switched "ON", which corresponds to a low-to-high transition for all bits. This time is typically 250ns for settling to within $\pm 1/2$ LSB, for 8-bit accuracy, and 200ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25pF$.

The slowest single switch is the least significant bit. In applications where the D/A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 250ns may be realized.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μ F supply bypassing for low frequencies, and a minimum scope lead length are all mandatory.



DAC-8012

CMOS 12-BIT MULTIPLYING
D/A CONVERTER "WITH MEMORY"

Precision Monolithics Inc.

FEATURES

- Data Readback Capability for System Self Check
- Fast TTL/CMOS Compatible Data Register
- $\pm 1/2$ LSB Max Linearity Error Over the Full Operating Temperature Range
- ± 1 LSB Max Gain Error — No User Adjustment Required
- Less Than 0.04 LSB Max Zero Scale Error (10nA)
- Single +5V to +15V Supply
- Small 20-Pin 0.3" Wide DIP
- Improved ESD Resistance
- Latch-Up Resistant
- Adds Data Readback Feature to PM-7545 Pinout

GENERAL DESCRIPTION

The DAC-8012 is a monolithic 12-bit CMOS multiplying DAC with internal data latches and three-state data readback buffers. The latches and readback buffers perform like a "memory" location. Data loads into the latches as a single 12-bit wide word allowing direct connection to 12-bit and 16-bit busses.

Four-quadrant multiplying capability and 12-bit linearity simplifies wide-bandwidth, low-distortion, digitally-controlled precision attenuator and filter applications.

The powerful data readback function allows users to perform data path verification between the controlling processor and the DAC-8012. System self check results after writing a data word to the DAC-8012, then reading it back to the processor, verifying no change in data takes place. The readback function simplifies the design of automatic test equipment, industrial automation, robotics, and processor-controlled instrumentation. Reduction of software coding results with processors using direct memory execution instructions. In remote systems, data set-points are held in the DAC register which can be interrogated upon system fault recovery.

ORDERING INFORMATION†

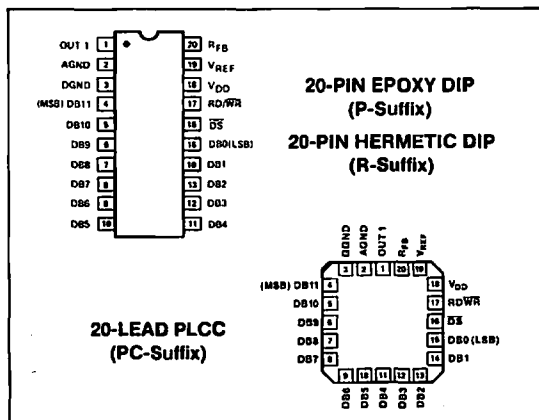
RELATIVE ACCURACY	PACKAGE: 20-PIN			
	MAXIMUM GAIN ERROR	MILITARY* TEMP	INDUSTRIAL TEMP	COMMERCIAL TEMP
	$T_A = +25^\circ\text{C}$ $V_{DD} = +5\text{V}$	-55°C to $+125^\circ\text{C}$	-25°C to $+85^\circ\text{C}$	0°C to $+70^\circ\text{C}$
$\pm 1/2$ LSB	± 1 LSB	DAC8012AR	DAC8012ER	DAC8012GP
± 1 LSB	± 3 LSB	DAC8012BR	DAC8012FR	DAC8012HP
± 1 LSB	± 3 LSB	—	—	DAC8012HPC††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

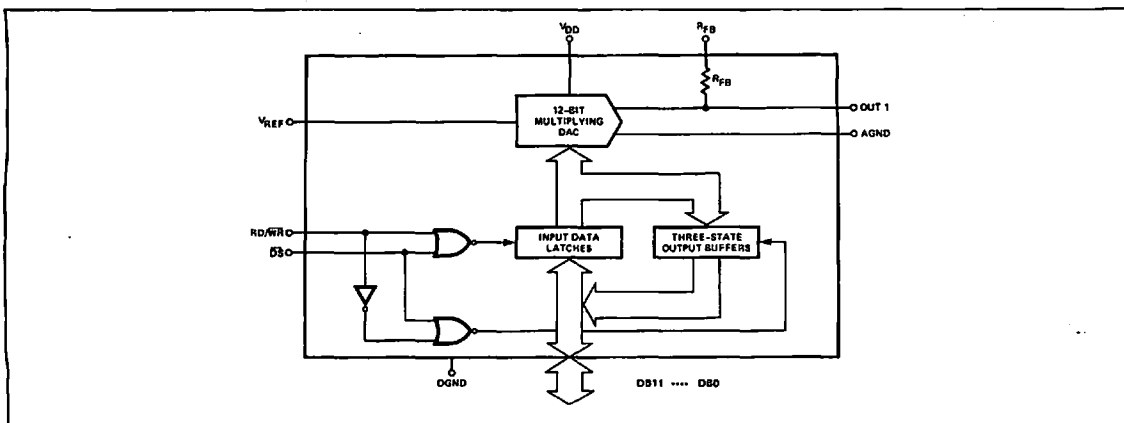
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**(T_A = 25°C, unless otherwise noted.)

V _{DD} to DGND	-0.3V, +17V
Digital Input Voltage to DGND	-0.3V, V _{DD}
AGND to DGND	-0.3V, V _{DD}
V _{REF} , V _{REF} to DGND	±25V
V _{PIN 1} to DGND	-0.3V, V _{DD}
Power Dissipation (Any Package) to +75°C	450mW
Derates Above +75°C by	6mW/°C
Operating Temperature Range	
Military (AR, BR) Grades	-55°C to +125°C
Industrial (ER, FR) Grades	-25°C to +85°C
Commercial (GP, HP, HPC) Grades	0°C to +70°C
Dice Junction Temperature	+150°C

Storage Temperature -65°C to +150°C

Lead Temperature (Soldering, 60 sec) +300°C

CAUTION:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
3. The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper anti-static handling procedures.
4. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REF} = +10V, V_{OUT 1} = 0V, AGND = DGND = 0V; T_A = -55°C to +125°C apply for DAC-8012AR/BR, T_A = -25°C to +85°C apply for DAC-8012ER/FR, T_A = 0°C to +70°C apply for DAC-8012GP/HP/HPC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G			DAC-8012B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY									
Resolution			12	—	—	12	—	—	Bits
Relative Accuracy	INL	T _A = Full Temp. Range	—	—	±1/2	—	—	±1	LSB
Differential Nonlinearity (Note 1)	DNL	T _A = Full Temp. Range	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G _{FSE}	T _A = +25°C T _A = Full Temp. Range	—	—	±1 ±2	—	—	±3 ±4	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature (Notes 4, 5)	TCG _{FS}		—	—	±5	—	—	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV _{DD} (Note 4)	PSR	T _A = +25°C T _A = Full Temp. Range (ΔV _{DD} = ±5%)	—	—	0.002 0.004	—	—	0.002 0.004	%/%
Output Leakage Current at OUT 1	I _{LKG}	T _A = +25°C, RD/WR = $\overline{DS}$ = 0V, All Digital Inputs = 0V T _A = Full Temp. Range A/B Versions E/F/G/H Versions	—	—	10 200 25	—	—	10 200 25	nA
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 6, & 7)	t _{PD}	T _A = +25°C (OUT 1 Load = 100Ω, C _{EXT} = 13pF)	—	—	300	—	—	300	ns
Current Settling Time (Notes 4, 7)	t _s	T _A = Full Temp. Range (To 1/2 LSB) I _{OUT 1} Load = 100Ω	—	—	1	—	—	1	μs
Glitch Energy (Note 4)	Q	T _A = +25°C T _A = Full Temp. Range V _{REF} = AGND	—	—	400 500	—	—	400 500	nVs
AC Feedthrough at I _{OUT 1} (Note 4)	FT	T _A = Full Temp. Range V _{REF} = ±10V, f = 10kHz	—	—	5	—	—	5	mV _{p-p}
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R _{REF}	T _A = Full Temp. Range Input Resistance	7	11	15	7	11	15	kΩ



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{REF} = +10V$, $V_{OUT1} = 0V$, $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8012AR/BR, $T_A = -25^\circ C$ to $+85^\circ C$ apply for DAC-8012ER/FR, $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8012GP/HP/HPC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G			DAC-8012B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUTS									
Output Capacitance (Note 4) C_{OUT1}	C_{OUT}	$V_{DD} = +5V$ or $+15V$ $T_A = \text{Full Temp. Range}$ $DB0-DB11 = 0V$, $RD/\overline{WR} = \overline{DS} = 0V$ $DB0-DB11 = V_{DD}$, $RD/\overline{WR} = \overline{DS} = 0V$	—	—	70 150	—	—	70 150	pF
DIGITAL INPUTS									
Input High Voltage	V_{INH}	$T_A = \text{Full Temp. Range}$	2.4	—	—	2.4	—	—	V
Input Low Voltage	V_{INL}	$T_A = \text{Full Temp. Range}$	—	—	0.8	—	—	0.8	V
Input Current	I_{IN}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	1 10	—	—	1 10	μA
Input Capacitance DB0-DB11 RD/ $\overline{WR}$, $\overline{DS}$ (Note 4)	C_{IN}	$T_A = \text{Full Temp. Range}$	—	—	12 6	—	—	12 6	pF
DIGITAL OUTPUTS									
Output High Voltage	V_{OH}	$I_O = 400\mu A$	4.0	—	—	4.0	—	—	V
Output Low Voltage	V_{OL}	$I_O = -1.6mA$	—	—	0.4	—	—	0.4	V
Three-State Output Leakage Current			—	—	10	—	—	10	μA
SWITCHING CHARACTERISTICS (Note 8)		See Timing Diagram							
Write to Data Strobe Setup Time	t_{WSU}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0 0	—	—	0 0	—	—	ns
Data Strobe to Write Hold Time	t_{WH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0 0	—	—	0 0	—	—	ns
Read to Data Strobe Setup Time	t_{RSU}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0 0	—	—	0 0	—	—	ns
Data Strobe to Read Hold Time	t_{RH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0 0	—	—	0 0	—	—	ns
Write Mode Data Strobe Width	t_{WRS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	180 250	—	—	180 250	—	—	ns
Read Mode Data Strobe Width	t_{RDS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	220 290	—	—	220 290	—	—	ns
Data Setup Time	t_{DSU}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	210 250	—	—	210 250	—	—	ns
Data Hold Time	t_{OH}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	0 0	—	—	0 0	—	—	ns
Data Strobe to Data Valid Time (Notes 4, 9)	t_{CO}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	— —	—	300 400	— —	—	300 400	ns
Output Active Time from Deselection (Notes 4, 9)	t_{OTD}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	— —	—	215 375	— —	—	215 375	ns
POWER SUPPLY									
Supply Current	I_{DD}	$T_A = \text{Full Temp. Range}$ (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	$T_A = \text{Full Temp. Range}$ (All Digital Inputs 0V or V_{DD})	—	10	100	—	10	100	μA



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $V_{OUT1} = 0V$, $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8012AR/BR; $T_A = -25^\circ C$ to $+85^\circ C$ apply for DAC-8012ER/FR, $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8012GP/HP/HPC, unless otherwise noted.

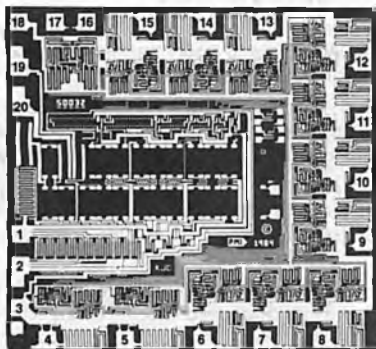
PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G			DAC-8012B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS									
Input High Voltage	V _{INH}	T _A = Full Temp. Range	13.5	—	—	13.5	—	—	V
Input Low Voltage	V _{INL}	T _A = Full Temp. Range	—	—	1.5	—	—	1.5	V
Input Current	I _{IN}	T _A = +25°C T _A = Full Temp. Range	—	—	1 10	—	—	1 10	μA
Input Capacitance DB0-DB11 RD/WR, DS (Note 4)	C _{IN}	T _A = Full Temp. Range	— —	— —	12 10	— —	— —	12 10	pF
DIGITAL OUTPUTS									
Output High Voltage	V _{OH}	I _O = 3mA	13.5	—	—	13.5	—	—	V
Output Low Voltage	V _{OL}	I _O = -3mA	—	—	1.5	—	—	1.5	V
Three-State Output Leakage Current			—	—	10	—	—	10	μA
SWITCHING CHARACTERISTICS (Note 8)		See Timing Diagram							
Write to Data Strobe Setup Time	t _{WSU}	T _A = +25°C T _A = Full Temp. Range	0 0	— —	— —	0 0	— —	— —	ns
Data Strobe to Write Hold Time	t _{WH}	T _A = +25°C T _A = Full Temp. Range	0 0	— —	— —	0 0	— —	— —	ns
Read to Data Strobe Setup Time	t _{RSU}	T _A = +25°C T _A = Full Temp. Range	0 0	— —	— —	0 0	— —	— —	ns
Data Strobe to Read Hold Time	t _{RH}	T _A = +25°C T _A = Full Temp. Range	0 0	— —	— —	0 0	— —	— —	ns
Write Mode Data Strobe Width	t _{WRS}	T _A = +25°C T _A = Full Temp. Range	100 120	— —	— —	100 120	— —	— —	ns
Read Mode Data Strobe Width	t _{RDS}	T _A = +25°C T _A = Full Temp. Range	110 150	— —	— —	110 150	— —	— —	ns
Data Setup Time	t _{DSU}	T _A = +25°C T _A = Full Temp. Range	90 120	— —	— —	90 120	— —	— —	ns
Data Hold Time	t _{DH}	T _A = +25°C T _A = Full Temp. Range	0 0	— —	— —	0 0	— —	— —	ns
Data Strobe to Output Valid Time (Note 9)	t _{CO}	T _A = +25°C T _A = Full Temp. Range	— —	— —	180 220	— —	— —	180 220	ns
Output Active Time for Deselection (Note 9)	t _{OTD}	T _A = +25°C T _A = Full Temp. Range	— —	— —	180 250	— —	— —	180 250	ns
POWER SUPPLY									
Supply Current	I _{DD}	T _A = Full Temp. Range (All Digital Inputs V _{INL} or V _{INH})	—	—	2	—	—	2	mA
	I _{OD}	T _A = Full Temp. Range (All Digital Inputs 0V or V _{DD})	—	10	100	—	10	100	μA

NOTES:

- 12-bit monotonic over full temperature range.
- Includes the effects of 5ppm max. gain T.C.
- Using internal R_{FB} . DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
- GUARANTEED but NOT TESTED.
- Typical value is 2ppm/ $^\circ C$ for $V_{DD} = +5V$.
- From digital input change to 90% of final analog output.
- All digital inputs = 0V to V_{DD} or V_{DD} to 0V.
- Sample tested at $+25^\circ C$ to ensure compliance.
- See load circuits for switching tests.



DICE CHARACTERISTICS



DIE SIZE 0.121×0.112 inch, 13,552 sq. mils
(3.07×2.85 mm, 8.75 sq. mm)

- | | |
|---------------|----------------------|
| 1. OUT 1 | 11. DB4 |
| 2. AGND | 12. DB3 |
| 3. DGND | 13. DB2 |
| 4. DB11 (MSB) | 14. DB1 |
| 5. DB10 | 15. DB0 (LSB) |
| 6. DB9 | 16. DS |
| 7. DB8 | 17. RD/WR |
| 8. DB7 | 18. V _{DD} |
| 9. DB6 | 19. V _{REF} |
| 10. DB5 | 20. R _{FB} |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at V_{DD} = +5V or +15V, V_{REF} = +10V, V_{OUT 1} = 0V, AGND = DGND = 0V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012G	UNITS
			LIMIT	
Relative Accuracy	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G _{FSE}	DAC Latches Loaded with 1111 1111 1111	±3	LSB MAX
Output Leakage	I _{LKG}	DAC Latches Loaded with 0000 0000 0000 Pad 1	±10	nA MAX
Input Resistance	R _{REF}	Pad 19	6/15	kΩ MIN/ kΩ MAX
Output High Voltage	V _{OH}	V _{DD} = 5V, I _O = 400μA	4.0	V MIN
Output Low Voltage	V _{OL}	V _{DD} = 5V, I _O = -1.6mA	0.4	V MAX
Digital Input High	V _{INH}	V _{DD} = 5V	2.4	V MIN
		V _{DD} = 15V	13.5	
Digital Input Low	V _{INL}	V _{DD} = 5V	0.8	V MAX
		V _{DD} = 15V	1.5	
Input Current	I _{IN}	V _{IN} = 0V or V _{DD}	±1	μA MAX
Supply Current	I _{DD}	All Digital Inputs V _{INL} or V _{INH}	2	mA MAX
		All Digital Inputs 0V or V _{DD}	0.1	
DC Supply Rejection (ΔGain/ΔV _{DD})	PSRR	V _{DD} = ±5%	0.004	%/% MAX

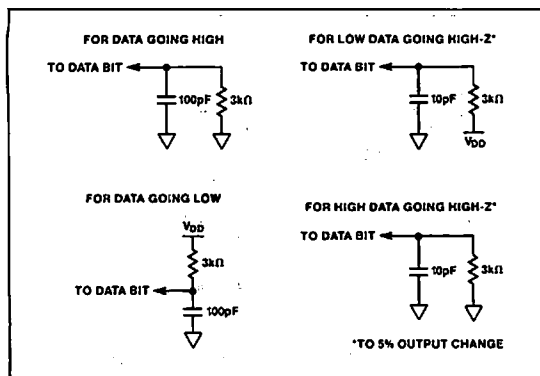
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REF} = +10V, V_{OUT 1} = 0V; T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012G	UNITS
			TYPICAL	
Digital Input Capacitance	C _{IN}		12	pF
Output Capacitance	C _{OUT 1}	DAC Latches Loaded with 0000 0000 0000	70	pF
	C _{OUT 1}	DAC Latches Loaded with 1111 1111 1111	150	pF
Propagation Delay	t _{PD}	V _{DD} = 15V V _{OD} = 5V	300	ns

LOAD CIRCUITS FOR SWITCHING TESTS



PARAMETER DEFINITIONS

RELATIVE ACCURACY

Sometimes referred to as endpoint nonlinearity, and is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Relative Accuracy is measured after the zero and full-scale points have been adjusted, and is normally expressed in LSB or as a percentage of full scale.

DIFFERENTIAL NONLINEARITY

This is the difference between the measured change and the ideal change between any two adjacent codes. A differential nonlinearity of ± 1 LSB maximum over the full operating temperature range will ensure that a device is monotonic (the output will not decrease for an increase in digital code applied).

GAIN ERROR

Gain or full scale error is the amount of output error between the ideal output and the actual output. The ideal output is V_{REF} minus 1 LSB. The gain error is adjustable to zero using external resistance.

OUTPUT CAPACITANCE

The capacitance from OUT1 to AGND.

PROPAGATION DELAY

This is measured from the digital input change to the analog output current reaching 90% of its final value.

FEEDTHROUGH GLITCH ENERGY

This is a measure of the amount of charge injected to the analog output from the digital inputs, when the digital inputs change states. It is the area of the glitch and is specified in nVsec; it is measured with $V_{REF} = AGND$.

LOGIC INFORMATION

D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A Converter section of the DAC-8012, and Figure 2 gives an approximate equivalent switch circuit. R is typically $11k\Omega$.

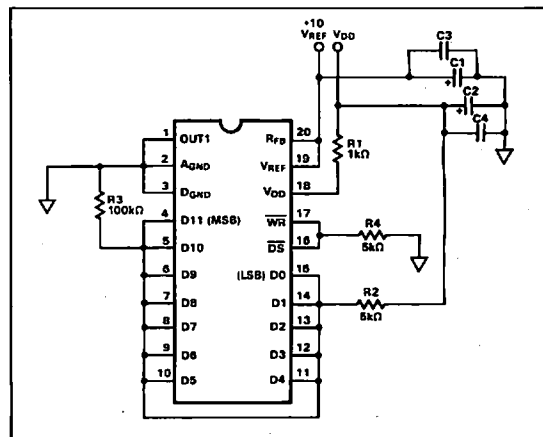
The binary-weighted currents are switched between OUT 1 and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT 1 terminal, C_{OUT1} , is code dependent and varies from 70pF (all switches to AGND) to 150pF (all switches to OUT 1). One of the current switches is shown in Figure 2.

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the $R/2R$ ladder characteristics resistance and is equal to value "R"). Since the input resistance at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} is recommended to define scale factor.)

The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves performance over temperature and power supply rejection; however, when the circuit is not powered up the switch assumes an open state.

BURN-IN CIRCUIT



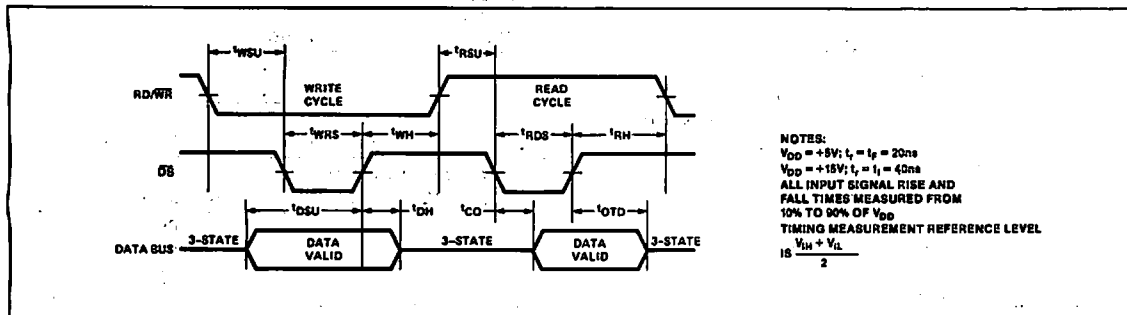
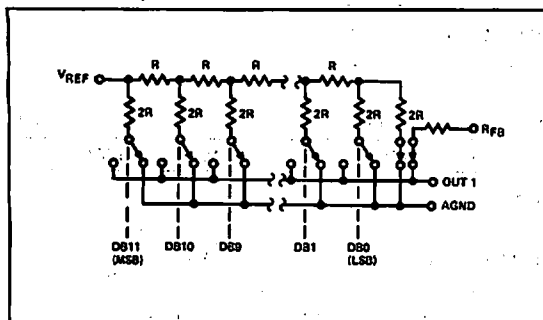
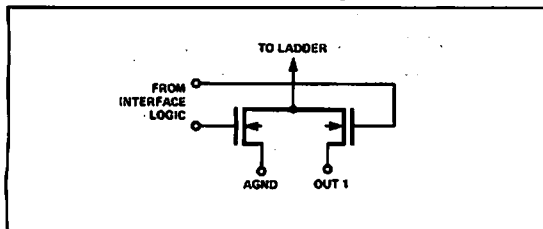
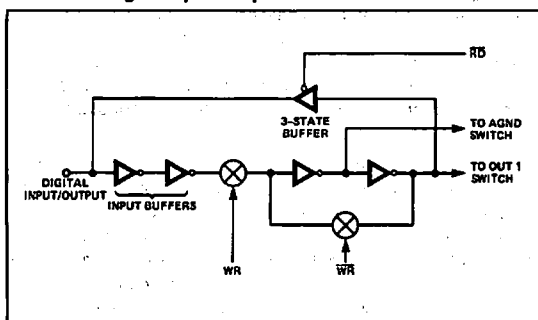
TIMING DIAGRAM

FIGURE 1: Simplified D/A Circuit of DAC-8012

FIGURE 2: N-Channel Current Steering Switch

DIGITAL SECTION

Figure 3 shows the digital I/O structure for one bit. When the data strobe ($\overline{DS}$) and the $\overline{RD}/\overline{WR}$ lines are held low, data at the digital input is fed through the input buffers and the data latches which control the DAC current output switches are transparent. Data is latched when either $\overline{DS}$ or $\overline{RD}/\overline{WR}$ go high. When the data strobe $\overline{DS}$ is held low and the $\overline{RD}/\overline{WR}$ line is held high, the three-state buffer becomes active and the data from the latches is

FIGURE 3: Digital Input/Output Structure


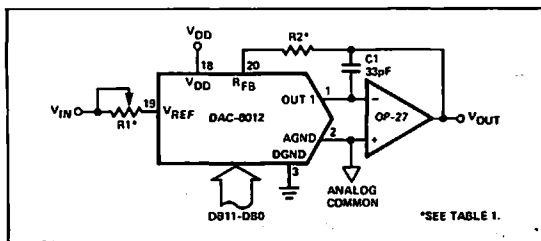
fed through the three-state buffers to the digital input/output lines. This is known as the Read Cycle, or data readback.

The input buffers are simple CMOS inverters designed such that when the DAC-8012 is operated with $V_{DD} = +5V$, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0V to 3.0V, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and D_{GND}) as is practically possible. The DAC-8012 may be operated with any supply voltage in the range $5V \leq V_{DD} \leq 15V$. With $V_{DD} = +15V$, the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

The three-state output buffers, in the active mode, provide TTL-compatible digital outputs with a fan-out of one TTL load when the DAC-8012 is operated with +5V power supply. When powered from +15V, the output buffers provide output logic levels of 1.5V and 13.5V. Three-state output leakage is typically 10nA.



FIGURE 4: Unipolar Binary Operation



BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the DAC-8012. Resistor R1 is used to trim for full scale. The following versions: DAC-8012AR, DAC-8012ER, DAC-8012GP, have a guaranteed maximum gain error of ± 1 LSB at $+25^{\circ}\text{C}$ and $V_{DD} = +5\text{V}$, and in many applications the gain trim resistors are not required. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuits of Figures 4 and 5 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (the inversion is introduced by the op amp); or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20\text{V} \leq V_{IN} \leq +20\text{V}$ (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD} . Table II shows the code relationship for the circuit of Figure 4.

Figure 5 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code, and inverter U_1 on the MSB line, converts 2's-complement input code to offset binary code. The inverter U_1 may be omitted if the inversion is done in software, using an exclusive OR instruction.

R3, R4 and R5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

FIGURE 5: Bipolar Operation (2's Complement Code)

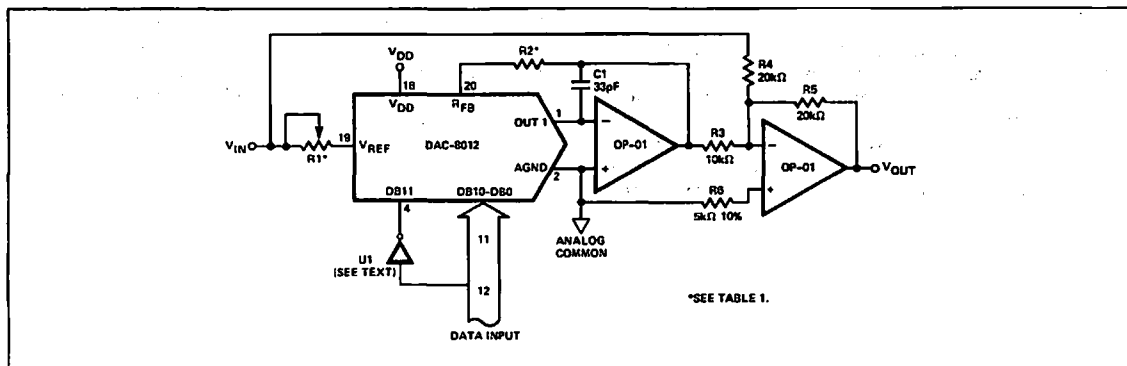


TABLE I: Recommended Trim Resistor Value vs. Grades

TRIM RESISTOR	HP/FR/BR	GP/ER/AR
R1	100 Ω	20 Ω
R2	83 Ω	6.8 Ω

TABLE II: Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN} \cdot \left(\frac{4095}{4096} \right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN} \cdot \left(\frac{2048}{4096} \right) = -1/2 V_{IN}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{IN} \cdot \left(\frac{1}{4096} \right)$
0 0 0 0 0 0 0 0 0 0 0 0	0 Volts

TABLE III: 2's Complement Code Table for Circuit of Figure 5

DATA INPUT	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN} \cdot \left(\frac{2047}{2048} \right)$
0 0 0 0 0 0 0 0 0 0 0 1	$+V_{IN} \cdot \left(\frac{1}{2048} \right)$
0 0 0 0 0 0 0 0 0 0 0 0	0 Volts
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN} \cdot \left(\frac{1}{2048} \right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN} \cdot \left(\frac{2048}{2048} \right)$

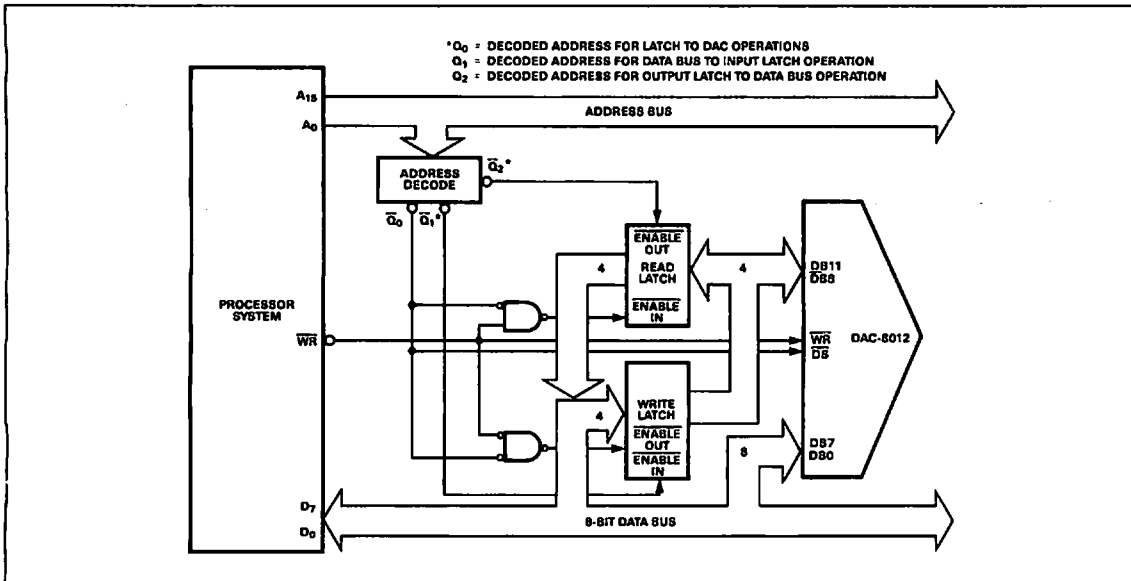
APPLICATIONS HINTS

Output Offset: CMOS D/A converters exhibit a code-dependent output resistance that causes a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is $0.67 V_{OS}$ where V_{OS} is the amplifier input-offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than 10% of 1 LSB over the temperature range of operation.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the DAC-8012. It is recommended that two diodes (1N914 or equivalent) be connected in inverse parallel between AGND and DGND pins in complex systems where AGND and DGND tie on the backplane.

Digital Glitches: When $RD/\overline{WR}$ and $\overline{DS}$ are both low, the latches are transparent and the D/A converter inputs follow the data inputs. Some bus systems do not always have data valid for the whole period during which $RD/\overline{WR}$ is low. This will allow invalid data to briefly appear at the DAC inputs during the write cycle. This can cause unwanted glitches at the DAC output. Retiming the write pulse $RD/\overline{WR}$, so that it only occurs when data is valid, will eliminate the problem.

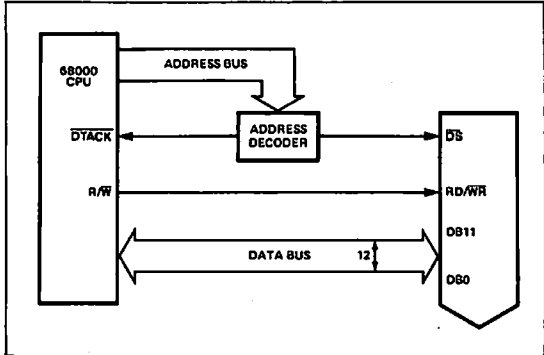
FIGURE 7: 8-Bit Processor to DAC-8012 Interface



INTERFACING THE DAC-8012 TO MICROPROCESSORS

Figure 6 shows the interface configuration for the 68000 16-bit microprocessor. No external logic is required to write data into the DAC or to readback data from the DAC-8012 latches. Analog circuitry has been removed for clarity.

FIGURE 6: 68000 16-Bit Microprocessor to DAC-8012 Interface





DAC-8043

12-BIT SERIAL INPUT

MULTIPLYING CMOS D/A CONVERTER IN 8-PIN PACKAGE

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- 12-Bit Accuracy in an 8-Pin Mini-Dip
- Fast Serial Data Input
- Double Data Buffers
- Low $\pm 1/2$ LSB Max INL and DNL
- Max Gain Error— ± 1 LSB
- Low 5ppm/ $^{\circ}$ C Max Tempco
- ESD Resistant

APPLICATIONS

- Auto-Calibration Systems
- Process Control and Industrial Automation
- Programmable Amplifiers and Attenuators
- Digitally-Controlled Filters

GENERAL DESCRIPTION

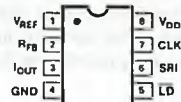
The DAC-8043 is a high accuracy 12-bit CMOS multiplying DAC in a space-saving 8-pin mini-DIP package. Featuring serial data input, double buffering, and excellent analog performance, the DAC-8043 is ideal for applications where PC board space is at a premium. Separate input strobe and load-DAC control lines allow full user control of data loading and analog output.

The circuit consists of a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial data is clocked into the input register on the rising edge of the CLOCK pulse. When the new data word has been clocked in, it is loaded into the DAC register with the LD input pin.

Operating from a single +5V power supply, the DAC-8043 is the ideal low power, small size, high performance solution to many applications problems.

For applications requiring an asynchronous CLEAR function or more versatile microprocessor interface logic, refer to the PM-7543.

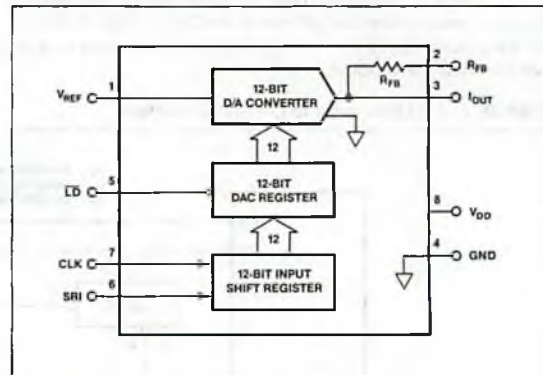
PIN CONNECTIONS



8-PIN EPOXY DIP
(P-Suffix)

8-PIN CERDIP
(Z-Suffix)

FUNCTIONAL BLOCK DIAGRAM



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



Precision Monolithics Inc.

DAC-8212

DUAL 12-BIT BUFFERED
MULTIPLYING CMOS D/A CONVERTER

FEATURES

- Two Matched 12-Bit DACs on One Chip
- Direct Parallel Load of All 12 Bits for High Data Throughput
- On-Chip Latches for Both DACs
- 12-Bit Endpoint Linearity ($\pm 1/2$ LSB)
- +5V to +15V Single Supply Operation
- DACs Matched to 1%
- Four-Quadrant Multiplication
- Low Power Consumption

APPLICATIONS

- Automatic Test Equipment
- Robotics
- Programmable Instrumentation Equipment
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION†

RELATIVE ACCURACY	GAIN ERROR	PACKAGE		
		MILITARY* TEMPERATURE -55°C to +125°C	INDUSTRIAL TEMPERATURE -25°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
$\pm 1/2$ LSB	± 2 LSB	DAC8212AV	DAC8212EV	DAC8212GP
± 1 LSB	± 4 LSB	DAC8212BV	DAC8212FV	DAC8212HP
± 1 LSB	± 4 LSB	—	—	DAC8212HPC††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

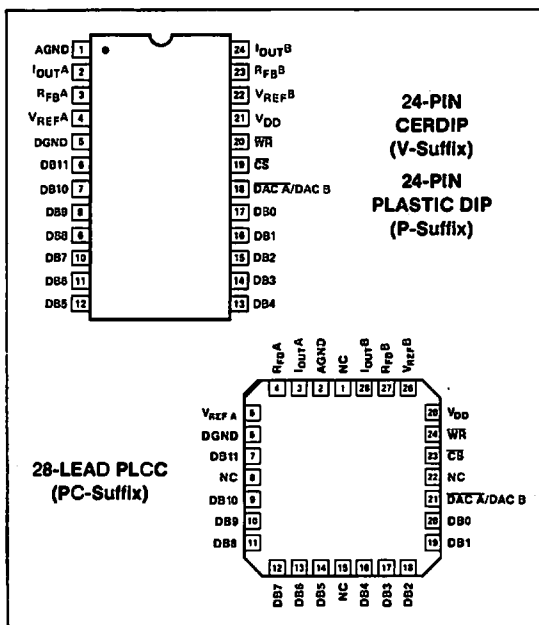
GENERAL DESCRIPTION

The DAC-8212 combines two identical 12-bit, multiplying, digital-to-analog converters into a single CMOS chip. Monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC-8212 consists of two thin-film R-2R resistor-ladder networks, two 12-bit data latches, one 12-bit input buffer, and control logic. The DAC-8212 can operate on a single supply from +5V to +15V. Maximum power dissipation with CMOS logic levels and a +5V supply is less than 0.5mW. The DAC-8212 is manufactured using PMI's highly-stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

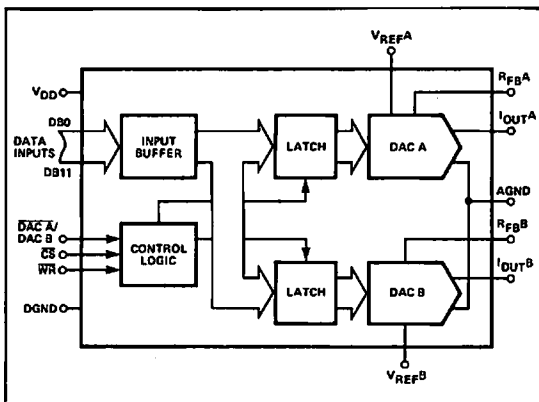
A common 12-bit (TTL/CMOS compatible) input port is used to load a 12-bit-wide word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. With

$\overline{WR}$ and $\overline{CS}$ lines at logic low, the input data latches are transparent. This allows direct unbuffered data to flow directly to the DAC output selected by $\overline{DAC\ A/DAC\ B}$ control input.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



DIGITAL-TO-ANALOG CONVERTERS

**ABSOLUTE MAXIMUM RATINGS**(T_A = +25°C, unless otherwise noted.)

V _{DD} to AGND	0V, +17V
V _{DD} to DGND	0V, +17V
AGND to DGND	-0.3V, V _{DD} + 0.3
Digital Input Voltage to DGND	-0.3V, V _{DD} + 0.3
I _{OUTA} , I _{OUTB} to AGND	-0.3V, V _{DD} + 0.3
V _{REFA} , V _{REFB} to AGND	±25V
V _{RFBA} , V _{RFBB} to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derate Above +75°C by	6mW/°C
Operating Temperature Range	
AV, BV Versions	-55°C to +125°C
EV, FV Versions	-25°C to +85°C
GP, HP, HPC Versions	0°C to +70°C

Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

CAUTION:

- Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
- The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
- Do not insert this device into powered sockets; remove power before insertion or removal.
- Use proper anti-static handling procedures.
- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REFA} = V_{REFB} = +10V, V_{OUTA} = V_{OUTB} = 0V; AGND = DGND = 0V; T_A = -55°C to +125°C apply for DAC-8212AV/BV; T_A = -25°C to +85°C apply for DAC-8212EV/FV; T_A = 0°C to +70°C apply for DAC-8212GP/HP/HPC, unless otherwise noted. Specifications apply for DAC A and DAC B.

			DAC-8212				
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
STATIC ACCURACY		Specifications apply to both DAC A and DAC B					
Resolution	N		12	—	—	Bits	
Relative Accuracy	INL	Endpoint Linearity Error	DAC-8212A/E/G DAC-8212B/F/H		±1/2 ±1	LSB	
Differential Nonlinearity	DNL	All Grades are Monotonic	—	—	±1	LSB	
Full Scale Gain Error (Note 1)	G _{FSE}	T _A = +25°C	DAC-8212A/E/G DAC-8212B/F/H		±2 ±4	LSB	
		T _A = Full Temp. Range	DAC-8212A/E/G DAC-8212B/F/H		±3 ±6		
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG _{FS}	(Notes 2, 7)	—	±2	±5	ppm/°C	
Output Leakage Current I _{OUTA} (Pin 2), I _{OUTB} (Pin 24)	I _{LKG}	All Digital Inputs = 0000 0000 0000	T _A = +25°C		±50	nA	
			T _A = Full Temp. Range		±100		
Input Resistance (V _{REFA} , V _{REFB})	R _{REF}		8	11	15	kΩ	
(V _{REFA} /V _{REFB}) (Input Resistance Match)	ΔV _{REFA, B}		—	±0.2	±1	%	
DIGITAL INPUTS							
Digital Input High	V _{INH}	V _{DD} = +5V	2.4	—	—	V	
		V _{DD} = +15V	13.5	—	—		
Digital Input Low	V _{INL}	V _{DD} = +5V	—	—	0.8	V	
		V _{DD} = +15V	—	—	1.5		
Input Current	I _{IN}	V _{IN} = 0V or V _{DD} and V _{INL} or V _{INH}	T _A = +25°C		±1	μA	
			T _A = Full Temp. Range		±10		
Input Capacitance (Note 2)	C _{IN}	DB0—DB11	—	—	10	pF	
		WR, CS, DAC A/DAC B	—	—	15		



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REFA} = V_{REFB} = +10V$, $V_{OUTA} = V_{OUTB} = 0V$; $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8212AV/BV; $T_A = -25^\circ C$ to $+85^\circ C$ apply for DAC-8212EV/FV; $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8212GP/HP/HPC, unless otherwise noted. Specifications apply for DAC A and DAC B. (Continued)

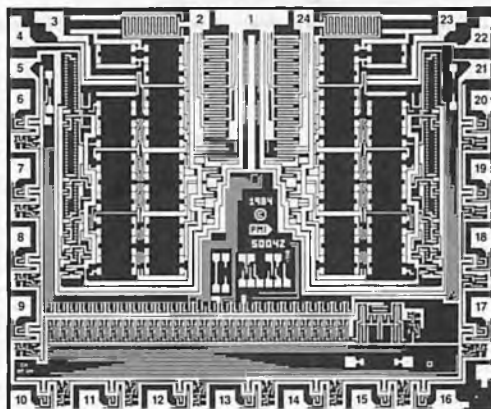
			DAC-8212			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
(Notes 2, 3)						
Chip Select to Write Set-Up Time	t _{CS}		230	—	—	ns
Chip Select to Write Hold Time	t _{CH}		30	—	—	ns
DAC Select to Write Set-Up Time	t _{AS}		230	—	—	ns
DAC Select to Write Hold Time	t _{AH}		30	—	—	ns
DAC Select Set-Up Write Time	t _{DSS}		0	—	—	ns
Data Valid to Write Set-Up Time	t _{DS}		230	—	—	ns
Data Valid to Write Hold Time	t _{DH}		0	—	—	ns
Write Pulse Width	t _{WR}		230	—	—	ns
POWER SUPPLY						
Supply Current	I _{DD}	All Digital Inputs V _{INL} or V _{INH}	—	—	2	mA
		All Digital Inputs 0V or V _{DD}	—	10	100	μA
DC Supply Rejection (ΔGain/ΔV _{DD})	PSR	ΔV _{DD} = ±5%	—	—	0.002	%/%
AC PERFORMANCE CHARACTERISTICS						
(Note 2)						
Propagation Delay (Notes 4, 5)	t _{pD}	T _A = +25°C	—	—	300	ns
Current Settling Time (Notes 5, 6)	t _s	T _A = +25°C	—	—	1	μs
Output Capacitance	C _{OUTA}	DAC Latches Loaded with 0000 0000 0000	—	—	90	pF
	C _{OUTB}	DAC Latches Loaded with 0000 0000 0000	—	—	90	
	C _{OUTA}	DAC Latches Loaded with 1111 1111 1111	—	—	120	
	C _{OUTB}	DAC Latches Loaded with 1111 1111 1111	—	—	120	
AC Feedthrough at I _{OUTA} or I _{OUTB}	FT _A	V _{REFA} to I _{OUTA} ; V _{REFA} = 20V _{p-p} ; f = 100kHz; T _A = +25°C	—	—	-70	dB
	FT _B	V _{REFB} to I _{OUTB} ; V _{REFB} = 20V _{p-p} ; f = 100kHz; T _A = +25°C	—	—	-70	

NOTES:

- Measured using internal R_{FEA} and R_{FEB} . Both DAC digital inputs = 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
- Guaranteed and not tested.
- See timing diagram.
- From 50% of digital input to 90% of final analog output current. $V_{REFA} = V_{REFB} = +10V$; OUT A, OUT B load = 100Ω , $C_{EXT} = 13pF$.
- $\overline{WR}$, $\overline{CS} = 0V$; $DB0-DB11 = 0V$ to V_{DD} or V_{DD} to $0V$.
- Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.
- Gain TC is measured from $+25^\circ C$ to T_{MIN} or from $+25^\circ C$ to T_{MAX} .



DICE CHARACTERISTICS



DIE SIZE 0.137×0.114 inch, 15,618 sq. mils
(3.48×2.90 mm, 10.10 sq. mm)

- | | |
|---------------|-----------------|
| 1. AGND | 13. DB4 |
| 2. I_{OUTA} | 14. DB3 |
| 3. R_{FBA} | 15. DB2 |
| 4. V_{REFA} | 16. DB1 |
| 5. DGND | 17. DB0 |
| 6. DB11 | 18. DAC A/DAC B |
| 7. DB10 | 19. CS |
| 8. DB9 | 20. WR |
| 9. DB8 | 21. V_{DD} |
| 10. DB7 | 22. V_{REFB} |
| 11. DB6 | 23. R_{FBB} |
| 12. DB5 | 24. I_{OUTB} |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +5V$ or $+15V$, $V_{REFA} = V_{REFB} = +10V$, $V_{OUTA} = V_{OUTB} = 0V$; AGND = DGND = 0V; $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	DAC-8212G	
			LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	± 1	LSB MAX
Differential Nonlinearity	DNL	(Note 1)	± 1	LSB MAX
Full Scale Gain Error (Note 2)	G _{FSE}	Digital Inputs = 1111 1111 1111	± 4	LSB MAX
Output Leakage (I_{OUTA} , I_{OUTB})	I_{LKG}	Digital Inputs = 0000 0000 0000 Pad 2 and 24	± 50	nA MAX
Input Resistance (V_{REFA} , V_{REFB})	R_{REF}	Pad 4 and 22	8/15	k Ω MIN/ k Ω MAX
V_{REFA}/V_{REFB} Input Resistance Match	$\Delta V_{REFA, B}$		± 1	% MAX
Digital Input High	V_{INH}	$V_{DD} = +5V$ $V_{DD} = +15V$	2.4 13.5	V MIN
Digital Input Low	V_{INL}	$V_{DD} = +5V$ $V_{DD} = +15V$	0.8 1.5	V MAX
Digital Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD} , V_{INL} or V_{INH}	± 1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	2 0.1	mA MAX
DC Supply Rejection ($\Delta \text{Gain}/\Delta V_{DD}$)	PSR	$\Delta V_{DD} = \pm 5\%$	0.002	%/% MAX

NOTES:

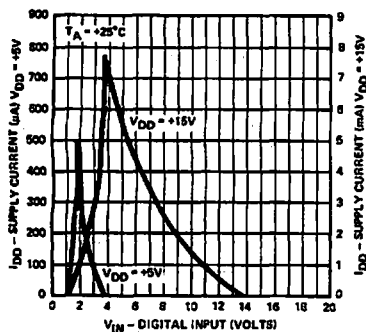
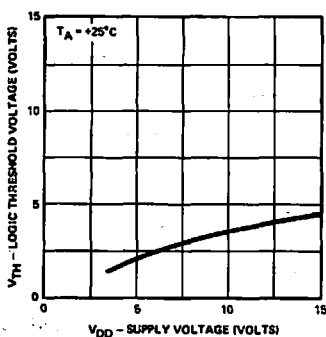
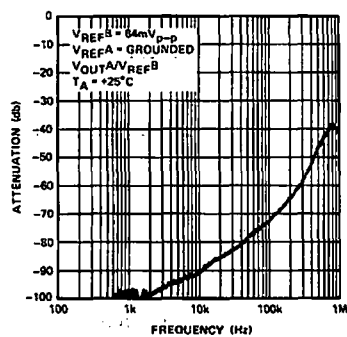
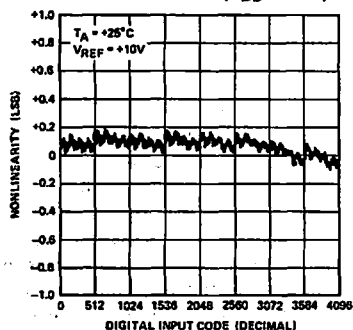
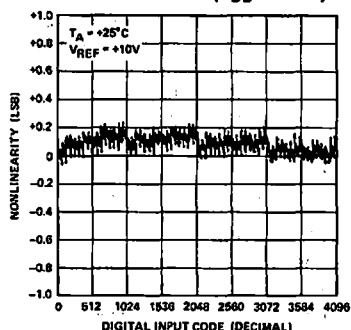
1. All grades are monotonic.

2. Measured using internal R_{FBA} and R_{FBB} .

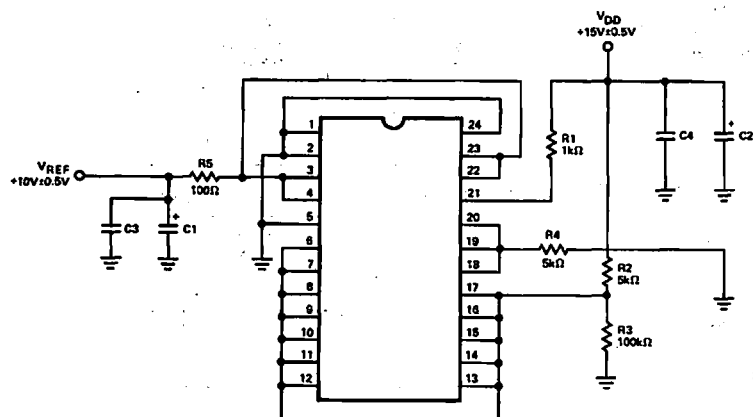
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



TYPICAL PERFORMANCE CHARACTERISTICS

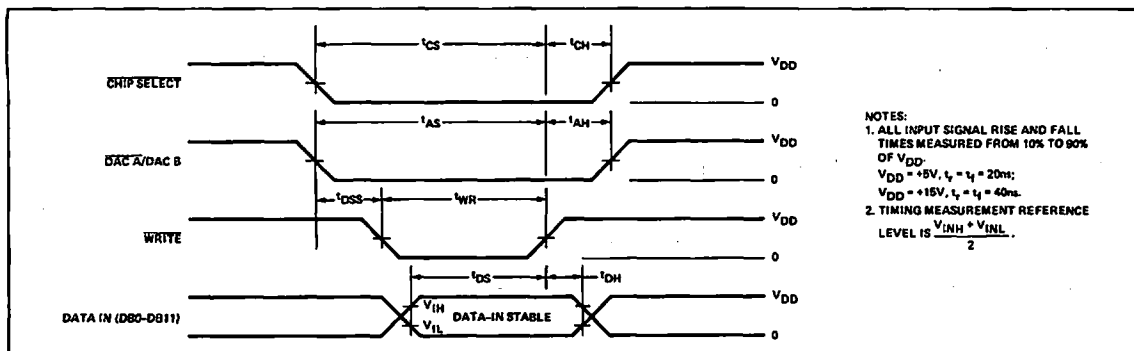
SUPPLY CURRENT vs
LOGIC LEVELLOGIC THRESHOLD VOLTAGE
vs SUPPLY VOLTAGEANALOG CROSSTALK
vs FREQUENCYNONLINEARITY vs
DIGITAL CODE ($V_{DD} = +5V$)NONLINEARITY vs
DIGITAL CODE ($V_{DD} = +15V$)

BURN-IN CIRCUIT



NOTES:
1. $C_1 = C_2$ 4.7 μF TANTALUM, 50V DC, EVERY 10TH DEVICE.
2. $C_3 = C_4$ 0.01 μF CERAMIC, 50V DC, EVERY 10TH DEVICE.
3. ALL MATERIAL TO WITHSTAND $150^\circ C$.

WRITE CYCLE TIMING DIAGRAM



PARAMETER DEFINITIONS

RESOLUTION (n)

The resolution of a DAC is the number of states (2^n) that the FSR is divided (or resolved) into, where n is equal to the number of bits.

INTEGRAL NONLINEARITY (INL) OR NONLINEARITY (NL)

This is the single most important DAC specification. PMI measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points, expressed as a percent of full-scale range or in terms of LSBs.

For DACs, a specification of $\pm 1/2$ LSB INL guarantees monotonicity and ± 1 LSB maximum differential nonlinearity.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog outputs from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called differential nonlinearity error or DNL. DACs with DNL greater than ± 1 LSB may be nonmonotonic. Maximum DNL error is less than or equal to twice the maximum INL.

GAIN ERROR (G_{FSE})

The difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal.

SETTLING TIME

Settling time is the elapsed time for the analog output to reach its final value within a specified error band after a digital input code change. It is usually specified for a full-scale change and measured from the 50% point of the logic input change to the time the output reaches its final value within the specified error band.

PROPAGATION DELAY

This is a measure of the internal delays of the DAC. It is defined as the time from a digital input change to the analog output-current reaching 90% of its final value.

OUTPUT CAPACITANCE

Output capacitance is that capacitance between I_{OUTA} , I_{OUTB} , and AGND.

A.C. FEEDTHROUGH

The ratio of the amplitude of signal at the DAC output to the reference input with all DAC switches off. This parameter is expressed in dBs.

D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A converter section of a single DAC. R is typically 11k Ω . Figure 2 gives an approximate equivalent switch circuit.

The binary-weighted currents are switched between I_{OUT} and AGND by N-channel MOS transistor switches. This maintains a constant current in each ladder leg independent of switch state. It is important that both N-channel switch "ON" resistances be matched so that the linearity errors can be kept at a minimum.

FIGURE 1: Simplified D/A Circuit

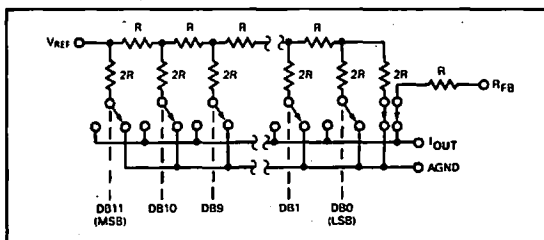
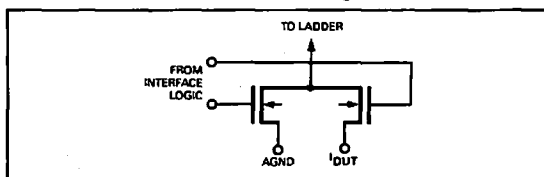


FIGURE 2: N-Channel Current Steering Switch



This also dictates that the voltage difference between I_{OUT} and AGND terminals be as close to zero as practical. This is easily accomplished by tying AGND to the noninverting input of an operational amplifier and I_{OUT} to the inverting input. The op amp feedback can then be tied directly to the R_{FB} terminal of the DAC; this will close the loop. The op amp, then, serves a two-fold function: it maintains the voltage difference between the DAC output terminals at virtual zero volts, and performs the current-to-voltage conversion for the DAC's output current. The output voltage is then dependent on the digital input code.

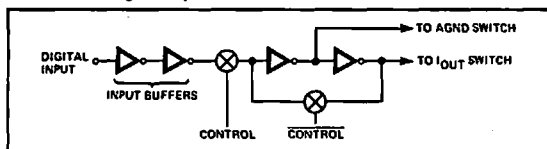
Input resistance at V_{REF} (Figure 1) is always equal to $R-LDR$ ($R-LDR$ is the $R/2R$ resistor ladder characteristic resistance and is equal to value "R"). Since the input resistance at V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or current, AC or DC, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} resistor is recommended to define scale factor).

The capacitance at I_{OUT} terminal, C_{OUT} , is code dependent and varies from 90pF (all digital inputs at AGND) to 120pF (all digital inputs HIGH).

DIGITAL SECTION

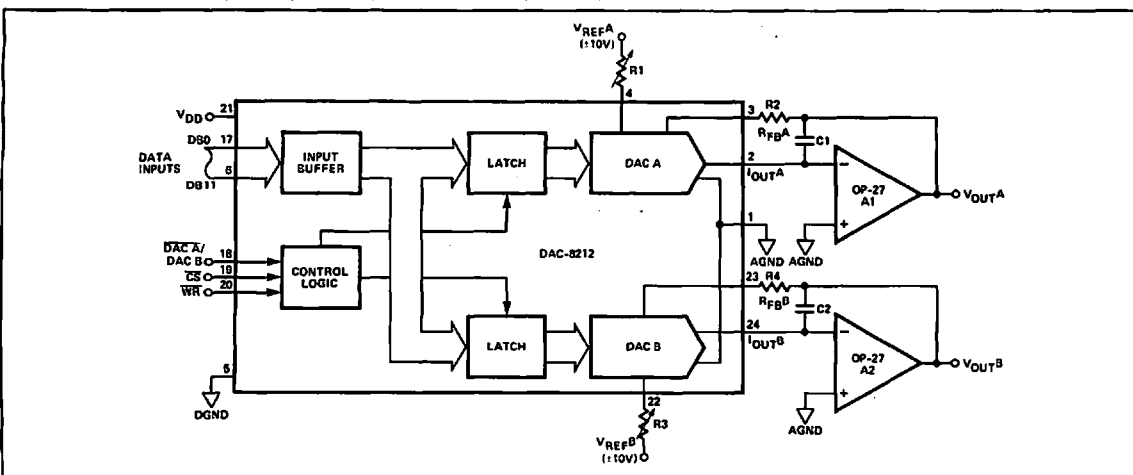
Figure 3 shows the digital structure for one bit. The digital signals CONTROL and CONTROL are generated from CS and WR.

FIGURE 3: Digital Input Structure



The input buffers are simple CMOS inverters designed such that when the DAC-8212 is operated with $V_{DD} = +5V$, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels.

FIGURE 4: Dual DAC Unipolar Operation (2-Quadrant Multiplication)



When the digital inputs are in the region of 1.2 to 2.8V with a +5V power supply, or 1.2 to 13.5V with a +15V power supply, the input buffers operate in their linear region and draw current from the power supply. It is, therefore, recommended that the digital input voltages be as close to the supply rails (V_{DD} and $DGND$) as is practically possible to keep supply currents at a minimum. The DAC-8212 may be operated with any supply voltage in the range $+5V \leq V_{DD} \leq +15V$. The input logic levels are CMOS compatible (1.5V and 13.5V) at $V_{DD} = +15V$.

BASIC APPLICATIONS

UNIPOLAR OUTPUT CIRCUIT

Figure 4 shows a simple unipolar (2-quadrant multiplication) circuit using the DAC-8212, and Table 1 shows the code table. Resistors R_1 , R_2 , and R_3 , R_4 , are used only if full-scale gain adjustments are required. Maximum full-scale error without these resistors for the top grade device and $V_{REF} = +10V$ is

TABLE 1: Unipolar Binary Code Table (Refer to Figure 4)

BINARY NUMBER IN DAC REGISTER		ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
MSB	LSB	
1111	1111 1111	$-V_{REF} \left(\frac{4095}{4096} \right)$
1000	0000 0000	$-V_{REF} \left(\frac{2048}{4096} \right) = -\frac{1}{2} V_{REF}$
0000	0000 0001	$-V_{REF} \left(\frac{1}{4096} \right)$
0000	0000 0000	0V

NOTE:
1 LSB = $(2^{-12}) (V_{REF}) = \frac{1}{4096} (V_{REF})$

0.048%, and 0.097% for the low grade device. See Table 3 for recommended values if using these resistors. Full-scale output voltage = $V_{REF} - 1 \text{ LSB} = V_{REF} \times (1 - 2^{-12})$ or $V_{REF} \times (4095/4096)$ with all digital inputs high. Low temperature coefficient (approximately 50ppm/°C) resistors or trimmers should be used. Full-scale can also be adjusted by varying V_{REF} voltage.

BIPOLAR OUTPUT CIRCUIT

Figure 5 shows how the DAC-8212 can be configured to operate in the bipolar mode (4-quadrant multiplication), and Table 2 shows the code table. As with the unipolar circuit of Figure 4, resistors R1, R2, and R3, R4, are used only if full-scale gain adjustment is required. Table 3 gives recommended values. R1 and R3 are used to adjust for zero voltage at the output of DAC A or DAC B respectively. The voltage is adjusted with the digital inputs set to 1000 0000 0000 for DAC A or DAC B. Matching and tracking is essential for resistor pairs R6, R7, and R9, R10. Capacitors C1 and C2 (10–15pF) provide phase compensation; they are required if using high speed op amps to prevent ringing or oscillations.

To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (244μV) over the operating temperature range.

PROGRAMMABLE WINDOW DETECTOR

Figure 6 shows the DAC-8212 used in a programmable window detector. The required upper and lower limits for the test are loaded into DAC A and DAC B. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero.

TABLE 2: Bipolar (Offset Binary) Code Table (Refer to Figure 5)

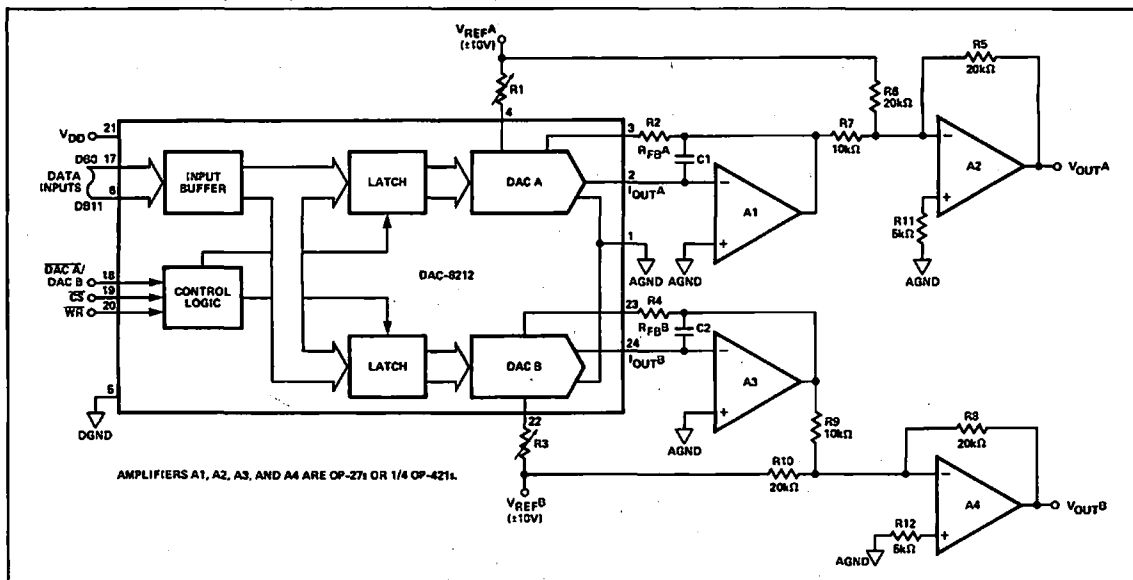
BINARY NUMBER IN DAC REGISTER		ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
MSB	LSB	
1111	1111 1111	$+V_{REF} \left(\frac{2047}{2048} \right)$
1000	0000 0001	$+V_{REF} \left(\frac{1}{2048} \right)$
1000	0000 0000	0V
0111	1111 1111	$-V_{REF} \left(\frac{1}{2048} \right)$
0000	0000 0000	$-V_{REF} \left(\frac{2048}{2048} \right)$

NOTE:
 $1 \text{ LSB} = (2^{-11}) (V_{REF}) = \frac{1}{2048} (V_{REF})$

TABLE 3: Recommended Trim Resistor Values vs Grade for Figures 4 and 5

TRIM RESISTOR	BV/FV/HP	AV/EV/GP
R1, R3	500Ω	200Ω
R2, R4	150Ω	82Ω

FIGURE 5: Dual DAC Bipolar Operation (4-Quadrant Operation)



APPLICATION HINTS

GROUND MANAGEMENT

Transient voltages between AGND and DGND can appear as noise at the DAC-8212's output. Figure 7 shows all analog grounds tied together and one connection from digital ground to analog ground. Note that AGND and DGND take off on their own ground paths, i.e., power grounds are kept separate from analog grounds. DGND pin is the return for supply currents and serves as the reference point for the digital inputs. Thus, DGND should be connected to the same ground as the circuitry which drives the digital inputs. AGND is the high-quality analog ground connection; this pin should serve as the reference point for all analog ground connections. It is recommended that any analog signal path carrying significant currents have its own return connection as shown in Figure 7.

POWER SUPPLY DECOUPLING

Power supplies used with the DAC-8212 should be well filtered and regulated. Local supply decoupling consisting of a 10 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic is highly recommended. The decoupling capacitors should be connected between the DAC-8212 supply pin (V_{DD}) and AGND pin.

WRITE ENABLE TIMING

During the period when both $\overline{CS}$ and $\overline{WR}$ are held low, the selected DAC latch is transparent and its analog output

responds directly to the data on the data bus line, DB0—DB11. Unwanted variations may appear at the input, therefore, the $\overline{WR}$ line should not go low until the data bus is fully settled (DATA VALID).

FIGURE 7: Recommended Ground Connections

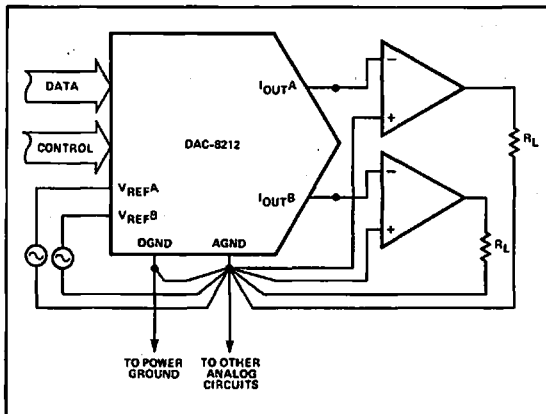
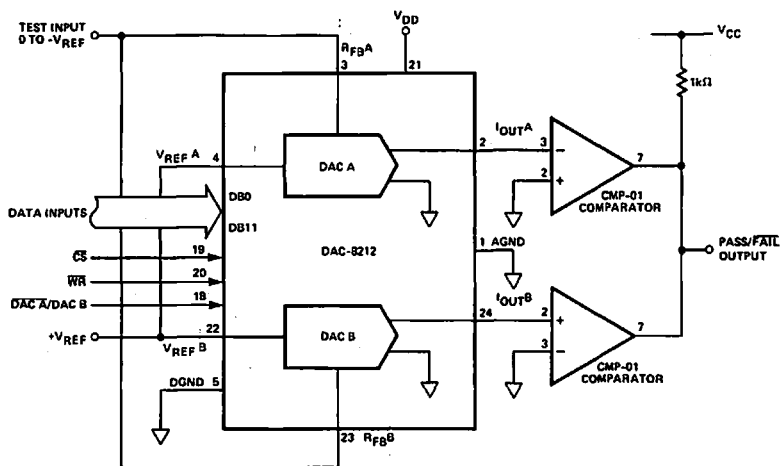


FIGURE 6: Digitally-Programmable Window Detector (Upper and Lower Limit Detector)



MICROPROCESSOR INTERFACE

Interfacing to an 8-bit or 16-bit bus system has been simplified by the loading structure versatility of the DAC-8212. Data loading into its 12-bit wide data latch is simplified by the use of only two control signals, $\overline{CS}$ and $\overline{WR}$.

8-BIT MICROPROCESSORS

8085A Microprocessor Interface: Loading data into the DAC-8212's 12-bit wide latch from an 8-bit bus will require two write cycles from the microprocessor. Data occupies two adjacent locations in the microprocessor's memory; several formats are possible and depends on the one desired. One scheme for interfacing the DAC-8212 to the 8085A 8-bit microprocessor is shown in Figure 8. Four MSBs are latched into the 74LS75 latch in the first cycle, and the entire 12-bit word is then loaded into the DAC-8212's data latch on the next write cycle. An alternate scheme would be to use an 8-bit latch so that the user can load the lower order bits in the first cycle. The 74LS139 is a dual 1 of 4 address decoder that supplies control signals for

DAC selection, $\overline{CS}$, high byte, and low byte. The NAND gate and inverter provides a constant chip select active-low signal while allowing the decoder to select either DAC A or DAC B.

6800 Microprocessor Interface: Because the DAC-8212 has a versatile data bus structure, interfacing it to the 6800 microprocessor is simplified and similar to that of the 8085A microprocessor circuit above. The circuit is shown in Figure 9.

16-BIT MICROPROCESSORS

Figures 10 and 11 show the DAC-8212's interface schemes for the 8086 and 68000 16-bit microprocessors. Circuit simplicity is achieved by connecting the DAC's data bus directly to the microprocessor. The 12-bit wide word is written to the DAC in one MOV instruction. The address decoder provides the DAC select and chip select signals and is programmed by the microprocessor.

FIGURE 8: DAC-8212 Dual DAC Interface with the 8085A 8-Bit Microprocessor

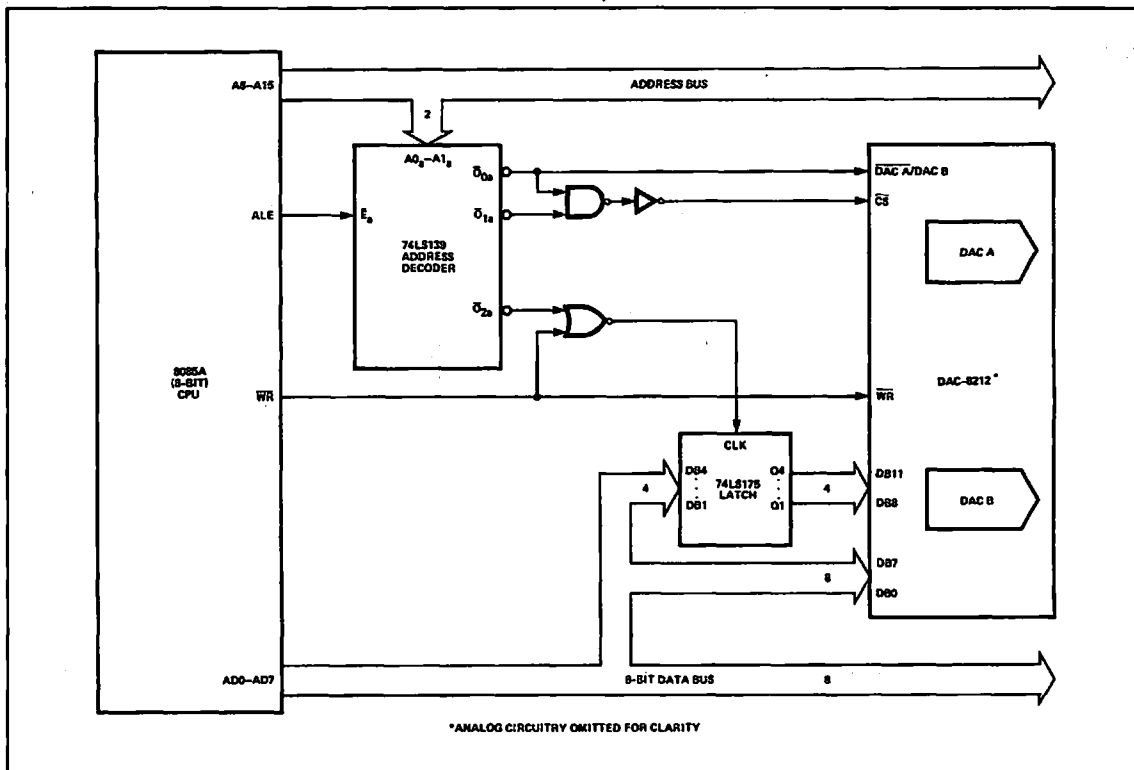


FIGURE 9: DAC-8212 Dual DAC Interface with the 6800 8-Bit Microprocessor

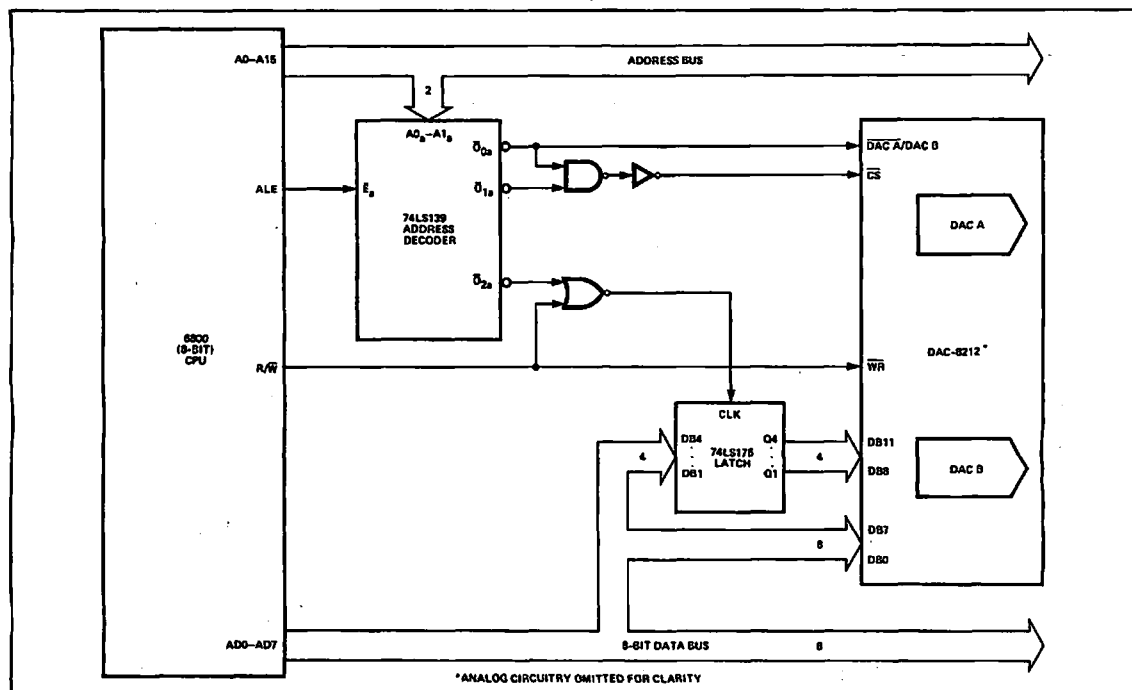


FIGURE 10: DAC-8212 Dual DAC Interface to the 8086 16-Bit Microprocessor

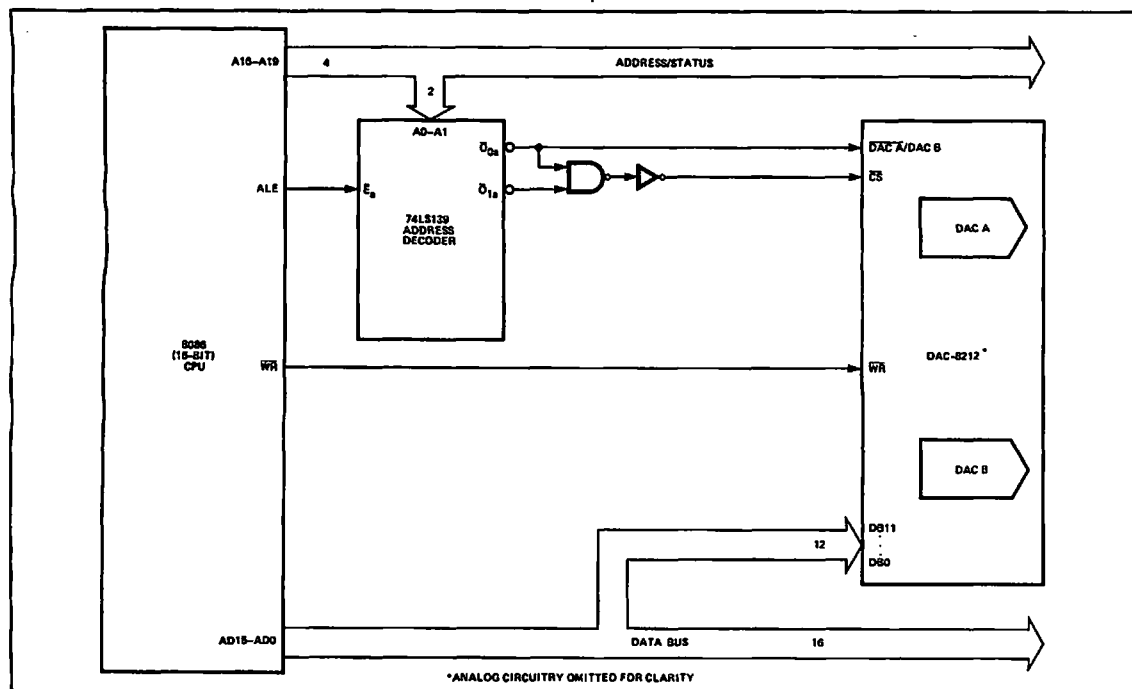
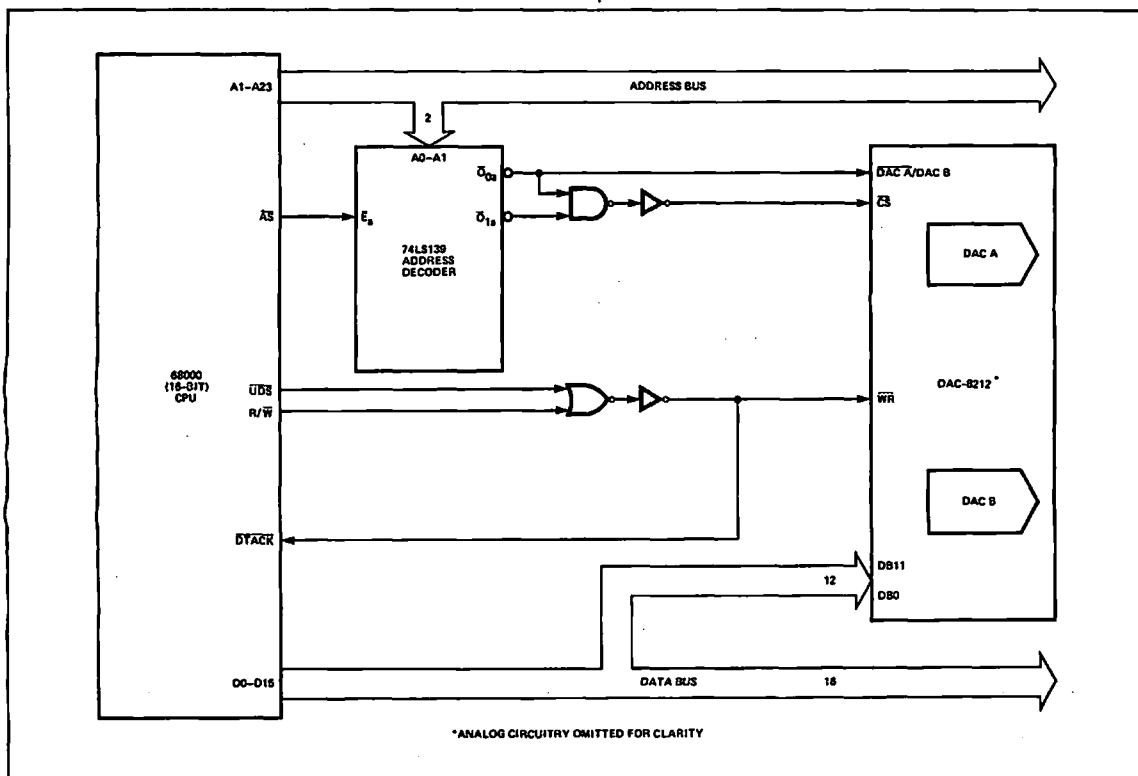


FIGURE 11: DAC-8212 Dual DAC Interface to the 68000 16-Bit Microprocessor





Precision Monolithics Inc.

DAC-8221

DUAL 12-BIT BUFFERED MULTIPLYING CMOS D/A CONVERTER

PRELIMINARY

FEATURES

- Two Matched 12-Bit DACs on One Chip
- Packaged in a Narrow 0.3" 24-Pin DIP
- Direct Parallel Load of All 12 Bits for High Data Throughput
- On-Chip Latches for Both DACs
- 12-Bit Endpoint Linearity ($\pm 1/2$ LSB) Over Temperature
- +5V to +15V Single Supply Operation
- DACs Matched to 1%
- Four-Quadrant Multiplication
- Improved ESD Resistance

APPLICATIONS

- Automatic Test Equipment
- Industrial Automation
- Robotics/Process Control
- Programmable Instrumentation Equipment
- Programmable Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION†

PACKAGE				
RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	MILITARY* TEMPERATURE -55°C to +125°C	INDUSTRIAL TEMPERATURE -40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
$\pm 1/2$ LSB	± 2 LSB	DAC8221AW	DAC8221EW	DAC8221GP
± 1 LSB	± 4 LSB	—	DAC8221FW	DAC8221HP
± 1 LSB	± 4 LSB	—	—	DAC8221HPC††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

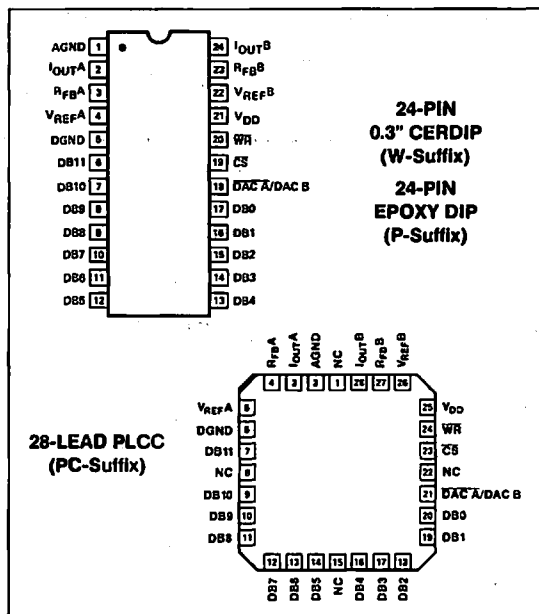
GENERAL DESCRIPTION

The DAC-8221 combines two identical 12-bit, multiplying, digital-to-analog converters into a single CMOS chip. This device is electrically similar to DAC-8212 with improved microprocessor interface timing and is packaged in a narrow 0.300" DIP. Monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC-8221 consists of two thin-film R-2R resistor-ladder networks, two 12-bit data latches, one 12-bit input buffer, and control logic. The DAC-8221 operates on a single supply from +5V to +15V. Maximum power dissipation with 0V and +5V logic levels and a +5V supply is less than 0.5mW. The DAC-8221 is manufactured using PMI's highly-stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

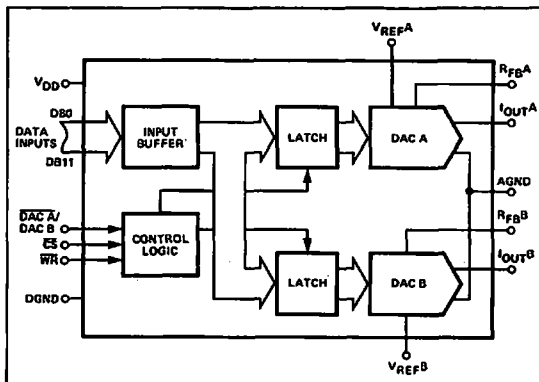
This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

A common 12-bit (TTL/CMOS compatible) input port is used to load a 12-bit-wide word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. With $\overline{WR}$ and $\overline{CS}$ lines at logic low, the input data latches are transparent. This allows direct unbuffered data to flow directly to the DAC output selected by DAC A/DAC B control input.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



DIGITAL-TO-ANALOG CONVERTERS

11

**ABSOLUTE MAXIMUM RATINGS**(T_A = +25°C, unless otherwise noted.)

V _{DD} to AGND	0V, +17V
V _{DD} to DGND	0V, +17V
AGND to DGND	-0.3V, V _{DD} +0.3V
Digital Input Voltage to DGND	-0.3V, V _{DD} +0.3
I _{OUTA} , I _{OUTB} to AGND	-0.3V, V _{DD} +0.3
V _{REFA} , V _{REFB} to AGND	±25V
V _{REFA} , V _{REFB} to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derate Above +75°C by	6mW/°C
Operating Temperature Range	
AW Version	-55°C to +125°C
EW, FW Versions	-40°C to +85°C
GP, HP, HPC Versions	0°C to +70°C

Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REFA} = V_{REFB} = +10V, V_{OUTA} = V_{OUTB} = 0V; AGND = DGND = 0V; T_A = -55°C to +125°C apply for DAC-8221AW; T_A = -40°C to +85°C apply for DAC-8221EW/FW; T_A = 0°C to +70°C apply for DAC-8221GP/HP/HPC, unless otherwise noted. Specifications apply for DAC A and DAC B.

				DAC-8221			
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY		Specifications apply to both DAC A and DAC B					
Resolution	N			12	—	—	Bits
Relative Accuracy	INL	Endpoint Linearity Error	DAC-8221A/E/G	—	—	±1/2	LSB
			DAC-8221F/H	—	—	±1	
Differential Nonlinearity	DNL	All Grades are Monotonic		—	—	±1	LSB
Full Scale Gain Error (Note 1)	G _{FSE}	T _A = +25°C	DAC-8221A/E/G	—	—	±2	LSB
			DAC-8221F/H	—	—	±4	
		T _A = Full Temp. Range	DAC-8221A/E/G	—	—	±3	
			DAC-8221F/H	—	—	±8	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG _{FS}	(Notes 2, 7)		—	±2	±5	ppm/°C
Output Leakage Current I _{OUTA} (Pin 2), I _{OUTB} (Pin 24)	I _{LKG}	All Digital Inputs = 0000 0000 0000	T _A = +25°C	—	±5	±50	nA
			T _A = Full Temp. Range	—	—	±100	
Input Resistance (V _{REFA} , V _{REFB})	R _{REF}			8	11	15	kΩ
(V _{REFA} /V _{REFB}) (Input Resistance Match)	ΔV _{REFA} , B			—	±0.2	±1	%
DIGITAL INPUTS							
Digital Input High	V _{INH}	V _{DD} = +5V		2.4	—	—	V
		V _{DD} = +15V		13.5	—	—	
Digital Input Low	V _{INL}	V _{DD} = +5V		—	—	0.8	V
		V _{DD} = +15V		—	—	1.5	
Input Current	I _{IN}	V _{IN} = 0V or V _{DD} and V _{INL} or V _{INH}	T _A = +25°C	—	±0.001	±1	μA
			T _A = Full Temp. Range	—	—	±10	
Input Capacitance (Note 2)	C _{IN}	DB0—DB11 WR, CS, DAC A/DAC B		—	—	10	pF
				—	—	15	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REFA} = V_{REFB} = +10V$, $V_{OUTA} = V_{OUTB} = 0V$; $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8221AW; $T_A = -40^\circ C$ to $+85^\circ C$ apply for DAC-8221EW/FW; $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8221GP/HP/HPC, unless otherwise noted. Specifications apply for DAC A and DAC B. (Continued)

			DAC-8221				
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
POWER SUPPLY							
Supply Current	I _{DD}	All Digital Inputs V _{INL} or V _{INH}	—	—	2	mA	
		All Digital Inputs 0V or V _{DD}	—	10	100	μA	
DC Power Supply Rejection Ratio (ΔGain/ΔV _{DD})	PSRR	ΔV _{DD} = ±5%	—	—	0.002	%/%	
AC PERFORMANCE CHARACTERISTICS (Note 2)							
Propagation Delay (Notes 4, 5)	t _{pD}	T _A = +25°C	—	—	300	ns	
Current Settling Time (Notes 5, 6)	t _s	T _A = +25°C	—	—	1	μs	
Output Capacitance	C _{OUTA}	DAC Latches Loaded with 0000 0000 0000	—	—	90	pF	
	C _{OUTB}	DAC Latches Loaded with 0000 0000 0000	—	—	120		
	C _{OUTA}	DAC Latches Loaded with 1111 1111 1111	—	—	120		
	C _{OUTB}	DAC Latches Loaded with 1111 1111 1111	—	—	90		
AC Feedthrough at I _{OUTA} or I _{OUTB}	FT _A	V _{REFA} to I _{OUTA} ; V _{REFA} = 20V _{p-p} ; f = 100kHz; T _A = +25°C	—	—	−70	dB	
	FT _B	V _{REFB} to I _{OUTB} ; V _{REFB} = 20V _{p-p} ; f = 100kHz; T _A = +25°C	—	—	−70		
SWITCHING CHARACTERISTICS (Notes 2, 3)			V _{DD} = +5V		V _{DD} = +15V		
			−40 TO +85°C (Note 8)		−55 TO +125°C		
			+25°C	ALL TEMPS			
Chip Select to Write Set-Up Time	t _{CS}		140	150	170	90	ns MIN
Chip Select to Write Hold Time	t _{CH}		0	0	0	0	ns MIN
DAC Select to Write Set-Up Time	t _{AS}		140	150	180	90	ns MIN
DAC Select to Write Hold Time	t _{AH}		0	0	0	0	ns MIN
Data Valid to Write Set-Up Time	t _{DS}		150	170	190	90	ns MIN
Data Valid to Write Hold Time	t _{DH}		0	0	0	0	ns MIN
Write Pulse Width	t _{WR}		120	150	170	90	ns MIN

NOTES:

- Measured using internal R_{fA} and R_{fB} . Both DAC digital inputs = 1111 1111 1111.
- Guaranteed and not tested.
- See timing diagram.
- From 50% of digital input to 80% of final analog output current. $V_{REFA} = V_{REFB} = +10V$; $OUT A, OUT B$ load = 100Ω , $C_{EXT} = 13pF$.
- $\overline{WR}, \overline{CS} = 0V$; $DB0-DB11 = 0V$ to V_{DD} or V_{DD} to $0V$.
- Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.
- Gain TC is measured from $+25^\circ C$ to T_{MIN} or from $+25^\circ C$ to T_{MAX} .
- These limits apply for the commercial and industrial grade products.

INTERFACE LOGIC INFORMATION

DAC SELECTION

Both DAC latches share a common 12-bit input port. The control input (DAC A/DAC B) selects which DAC can accept data from the input port.

MODE SELECTION

Inputs $\overline{CS}$ and $\overline{WR}$ control the operating mode of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{CS}$ and $\overline{WR}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0—DB11.

HOLD MODE

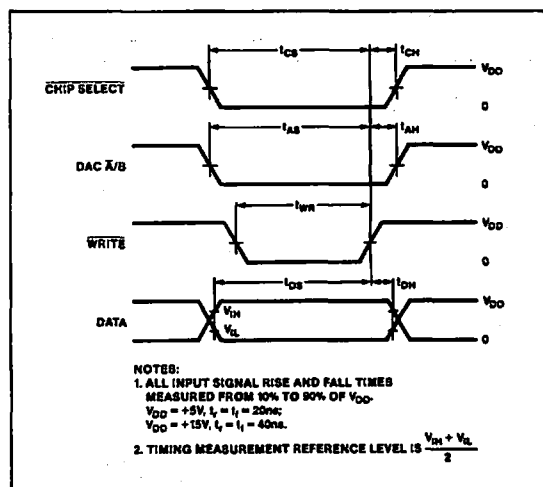
The selected DAC latch retains the data which was present on DB0—DB11 just prior to $\overline{CS}$ or $\overline{WR}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

MODE SELECTION TABLE

DAC A/ DAC B	$\overline{CS}$	$\overline{WR}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

WRITE CYCLE TIMING DIAGRAM





Precision Monolithics Inc.

DAC-8222

DUAL 12-BIT DOUBLE-BUFFERED
MULTIPLYING CMOS D/A CONVERTER

PRELIMINARY

FEATURES

- Two Matched 12-Bit DACs on One Chip
- Direct Parallel Load of All 12 Bits for High Data Throughput
- Double-Buffered Digital Inputs
- 12-Bit Endpoint Linearity ($\pm 1/2$ LSB) Over Temperature
- +5V to +15V Single Supply Operation
- DACs Matched to 1%
- Four-Quadrant Multiplication
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL package

APPLICATIONS

- Automatic Test Equipment
- Industrial Automation
- Robotics/Process Control
- Programmable Instrumentation Equipment
- Programmable Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

GENERAL DESCRIPTION

The DAC-8222 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has a 12-bit wide data port that allows a 12-bit word to be loaded directly. This achieves faster throughput time in stand-alone systems or when interfacing to a 16-bit

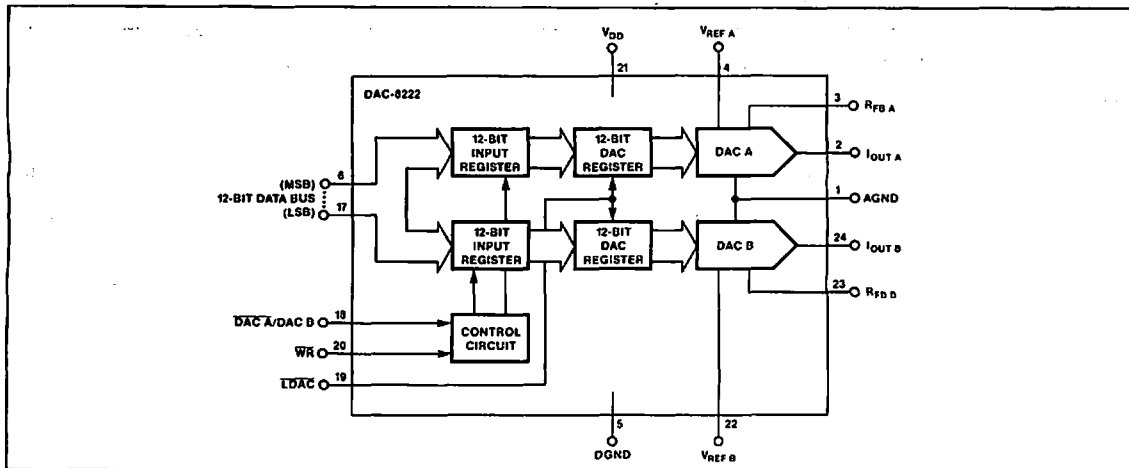
processor. A common 12-bit input TTL/CMOS compatible data port is used to load the 12-bit word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. (See PMI's DAC-8248 for a complete 8-bit data bus interface product.) A common bus allows the DAC-8222 to be packaged in a narrow 24-pin 0.3" wide DIP and save PCB space.

The DAC is controlled with two signals, $\overline{WR}$ and $\overline{LDAC}$. With logic low at these inputs, the DAC registers become transparent. This allows direct unbuffered data to flow directly to either DAC output selected by $\overline{DAC\ A/DAC\ B}$. The DAC's analog output can also be simultaneously updated using the $\overline{LDAC}$ control pin.

DAC-8222's monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The chip consists of two thin-film R-2R resistor ladder networks, four 12-bit data latches, and DAC control logic. It also has separate reference input and feedback resistors for each DAC and operates on a single supply from +5V to +15V. Maximum power dissipation at +5V using zero or V_{DD} logic levels is less than 0.5mW.

The DAC-8222 is manufactured with PMI's highly stable thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS technology. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

FUNCTIONAL DIAGRAM



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



ORDERING INFORMATION†

PACKAGE: 24-PIN DIP

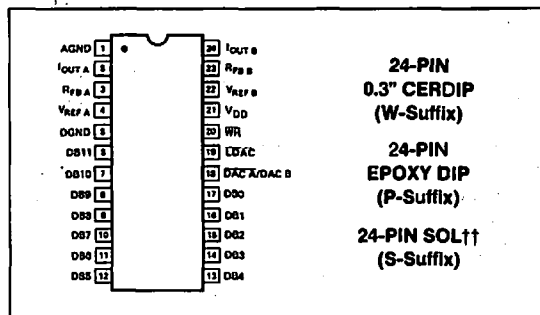
RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR	MILITARY* TEMPERATURE -55°C to +125°C	INDUSTRIAL TEMPERATURE -40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±2 LSB	DAC8222AW	DAC8222EW	DAC8222GP
±1 LSB	±4 LSB	—	DAC8222FW	DAC8222HP
±1 LSB	±4 LSB	—	—	DAC8222HSt†

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	-0.3V, $V_{DD} + 0.3\text{V}$
Digital Input Voltage to DGND	-0.3V, $V_{DD} + 0.3\text{V}$
$I_{OUT A}$, $I_{OUT B}$ to AGND	-0.3V, $V_{DD} + 0.3\text{V}$
$V_{REF A}$, $V_{REF B}$ to AGND	±25V
$V_{RFB A}$, $V_{RFB B}$ to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derate Above +75°C by	6mW/°C
Operating Temperature Range	
AW Version	-55°C to +125°C
EW, FW Versions	-40°C to +85°C
GP, HP Versions	0°C to +70°C
Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB} .
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5\text{V}$ or $+15\text{V}$, $V_{REF A} = V_{REF B} = +10\text{V}$, $V_{OUT A} = V_{OUT B} = 0\text{V}$; AGND = DGND = 0V; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ apply for DAC-8222AW; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ apply for DAC-8222EW/FW; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for DAC-8222GP/HP, unless otherwise noted. Specifications apply for DAC A and DAC B.

				DAC-8222			
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY		Specifications apply to both DAC A and DAC B					
Resolution	N			12	—	—	Bits
Relative Accuracy	INL	Endpoint Linearity Error	DAC-8222A/E/G	—	—	±1/2	LSB
			DAC-8222F/H	—	—	±1	
Differential Nonlinearity	DNL	All Grades are Monotonic		—	—	±1	LSB
Full Scale Gain Error (Note 1)	G _{FSE}	T _A = +25°C	DAC-8222A/E/G	—	—	±2	LSB
			DAC-8222F/H	—	—	±4	
		T _A = Full Temp. Range	DAC-8222A/E/G	—	—	±3	
			DAC-8222F/H	—	—	±6	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG _{FS}	(Notes 2, 7)		—	±2	±5	ppm/°C
Output Leakage Current I _{OUT A} (Pin 2), I _{OUT B} (Pin 24)	I _{LKG}	All Digital Inputs = 0000 0000 0000		T _A = +25°C T _A = Full Temp. Range	— —	±5 ±100	nA



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $V_{OUT A} = V_{OUT B} = 0V$; $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8222AW; $T_A = -40^\circ C$ to $+85^\circ C$ apply for DAC-8222EW/FW; $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8222GP/HP, unless otherwise noted. Specifications apply for DAC A and DAC B. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-8222			UNITS
			MIN	TYP	MAX	
Input Resistance ($V_{REF A}$, $V_{REF B}$)	R_{REF}		8	11	15	k Ω
($V_{REF A}/V_{REF B}$) (Input Resistance Match) $\Delta V_{REF A, B}$			—	± 0.2	± 1	%
DIGITAL INPUTS						
Digital Input High	V_{INH}	$V_{DD} = +5V$ $V_{DD} = +15V$	2.4 13.5	— —	— —	V
Digital Input Low	V_{INL}	$V_{DD} = +5V$ $V_{DD} = +15V$	— —	— —	0.8 1.5	V
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD} and V_{INL} or V_{INH}	— —	± 0.001 —	± 1 ± 10	μA
		$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$				
Input Capacitance (Note 2)	C_{IN}	DB0—DB11 WR, LDAC, DAC A/DAC B	— —	— —	10 15	pF
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	—	—	2	mA
		All Digital Inputs $0V$ or V_{DD}	—	10	100	μA
DC Power Supply Rejection Ratio ($\Delta \text{Gain}/\Delta V_{DD}$)	PSRR	$\Delta V_{DD} = \pm 5\%$	—	—	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 4, 5)	t_{pD}	$T_A = +25^\circ C$	—	—	300	ns
Current Settling Time (Notes 5, 6)	t_s	$T_A = +25^\circ C$	—	—	1	μs
Output Capacitance	$C_{OUT A}$	DAC Latches Loaded	—	—	90	pF
	$C_{OUT B}$	with 0000 0000 0000	—	—	90	
	$C_{OUT A}$	DAC Latches Loaded	—	—	120	
	$C_{OUT B}$	with 1111 1111 1111	—	—	120	
AC Feedthrough at $I_{OUT A}$ or $I_{OUT B}$	FT_A	$V_{REF A}$ to $I_{OUT A}$; $V_{REF A} = 20V_{p-p}$ $f = 100kHz$; $T_A = +25^\circ C$	—	—	-70	dB
	FT_B	$V_{REF B}$ to $I_{OUT B}$; $V_{REF B} = 20V_{p-p}$ $f = 100kHz$; $T_A = +25^\circ C$	—	—	-70	

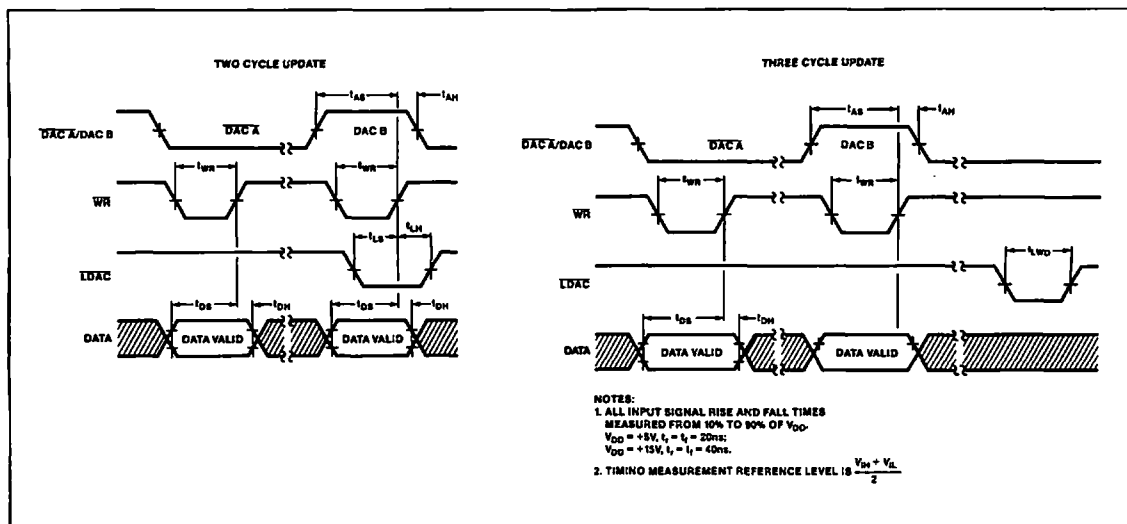


ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $V_{OUT A} = V_{OUT B} = 0V$; $AGND = DGND = 0V$; $T_A = -55^{\circ}C$ to $+125^{\circ}C$ apply for DAC-8222AW; $T_A = -40^{\circ}C$ to $+85^{\circ}C$ apply for DAC-8222EW/FW; $T_A = 0^{\circ}C$ to $+70^{\circ}C$ apply for DAC-8222GP/HP, unless otherwise noted. Specifications apply for DAC A and DAC B. (Continued)

		DAC-8222				
PARAMETER	SYMBOL	CONDITIONS				UNITS
SWITCHING CHARACTERISTICS (Notes 2, 3)			$V_{DD} = +5V$		$V_{DD} = +15V$	
			+25°C	-40 TO +85°C (Note 8)	-55 TO +125°C	
DAC Select to Write Set-Up Time	t_{AS}		140	170	170	90 ns MIN
DAC Select to Write Hold Time	t_{AH}		0	0	0	0 ns MIN
LDAC to Write Set-Up Time	t_{LS}		100	120	120	90 ns MIN
LDAC to Write Hold Time	t_{LH}		20	20	10	0 ns MIN
Data Valid to Write Set-Up Time	t_{DS}		160	180	190	90 ns MIN
Data Valid to Write Hold Time	t_{DH}		0	0	0	0 ns MIN
Write Pulse Width	t_{WR}		120	150	170	90 ns MIN
LDAC Pulse Width	t_{LWD}		90	90	90	90 ns MIN

NOTES:

- Measured using internal $R_{FB A}$ and $R_{FB B}$. Both DAC digital inputs = 1111 1111 1111.
- Guaranteed and not tested.
- See timing diagram.
- From 50% of digital input to 90% of final analog output current. $V_{REF A} = V_{REF B} = +10V$; OUT A, OUT B load = 100Ω , $C_{EXT} = 13pF$.
- $WR, LDAC = 0V$; DB0—DB11 = $0V$ to V_{DD} or V_{DD} to $0V$.
- Settling time is measured from 50% of the digital input change to where the output settles within 1/2 LSB of full scale.
- Gain TC is measured from $+25^{\circ}C$ to T_{MIN} or from $+25^{\circ}C$ to T_{MAX} .
- These limits apply for the commercial and industrial grade products.

WRITE CYCLE TIMING DIAGRAM

MODE SELECTION TABLE

DIGITAL INPUTS			DAC REGISTER STATUS			
DAC A/B	$\overline{WR}$	$\overline{LDAC}$	DAC A		DAC B	
			INPUT LATCH	DAC LATCH	INPUT LATCH	DAC LATCH
L	L	L	WRITE	WRITE	LATCHED	WRITE
H	L	L	LATCHED	WRITE	WRITE	WRITE
L	L	H	WRITE	LATCHED	LATCHED	LATCHED
H	L	H	LATCHED	LATCHED	WRITE	LATCHED
X	H	L	LATCHED	WRITE	LATCHED	WRITE
X	H	H	LATCHED	LATCHED	LATCHED	LATCHED

L = Low H = High X = Don't Care

INTERFACE CONTROL LOGIC

$\overline{DAC\ A/DAC\ B}$ (Pin 18) — DAC Selection. Active low for DAC A and active high for DAC B.

$\overline{WR}$ (Pin 20) — **WRITE**. Active Low. Used to write data into either DAC A or DAC B input registers, or active high latches data into the input registers.

$\overline{LDAC}$ (Pin 19) — **LOAD DAC**. Active Low. Used to simultaneously transfer data from DAC A and DAC B input registers to both DAC outputs, or active high latches data into the output registers.

WRITE TIMING CYCLES

Two timing diagrams are shown and are at the users discretion which to use.

The **TWO CYCLE UPDATE**, as the name implies, allows both DAC registers to be loaded and the outputs updated in two cycles. Data is first loaded into one DAC's input register on the first write cycle, and then new data loaded into the other DAC's input register while simultaneously updating both DAC outputs on the second cycle.

The **THREE CYCLE UPDATE** allows DAC A and DAC B registers to be loaded and analog output to be updated at a later time. The first two cycles loads both DACs as above, and the third cycle updates the outputs.

The $\overline{LDAC}$ and $\overline{DAC\ A/DAC\ B}$ control pins can be tied together and controlled with a single strobe. When using the DAC in this configuration, DAC B must be loaded first; this can be seen from the timing diagram.



DAC-8228

DUAL 8-BIT CMOS
D/A CONVERTER WITH VOLTAGE OUTPUT

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Fits 7528 Sockets, Eliminates External Op Amps
- Single +12 to +15V Operation
- 5 Microsecond Settling Time
- 8-Bit Accuracy
- Available in Small Outline Package

APPLICATIONS

- Programmable Instrumentation
- Disk Drive Servo Systems
- Process Control

GENERAL DESCRIPTION

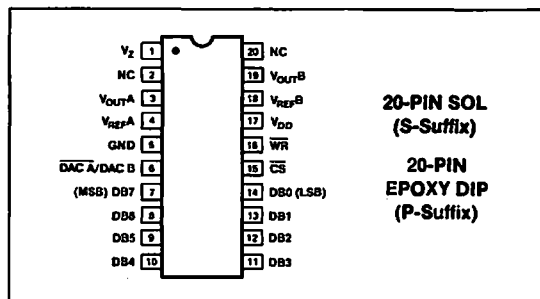
The DAC-8228 is a dual voltage-output monolithic multiplying CMOS D/A converter containing two high-accuracy R-2R ladder DACs and op amps. The REF input can be either grounded for DC voltage output applications or connected to an AC input signal for multiplying applications.

An internal regulator maintains TTL logic compatibility and fast microprocessor interface timing for all positive supply voltages.

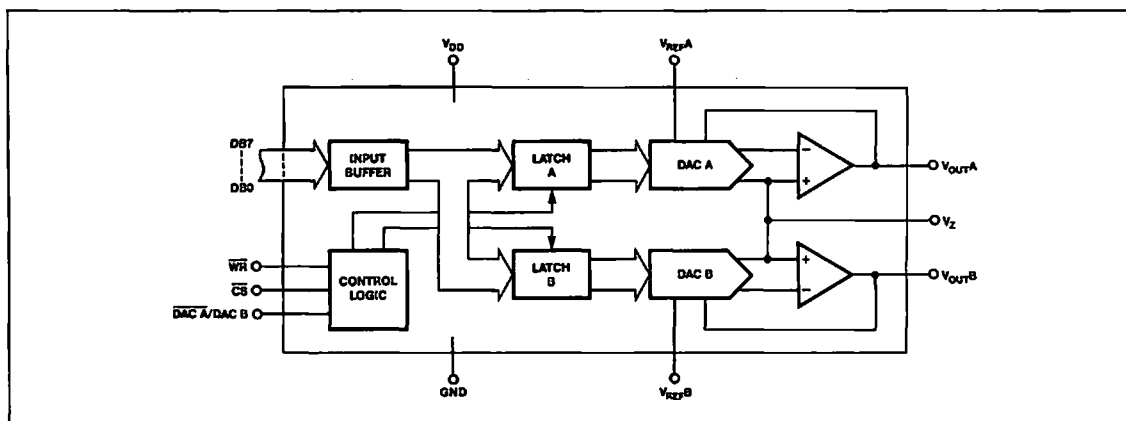
The DAC-8228 dissipates only 90mW in the space saving 20-pin 0.3" DIP or the 20-lead SO surface mount packages.

The pinout of the DAC-8228 fits directly into PM-7528 sockets and eliminates the need for external op amps.

PIN CONNECTIONS

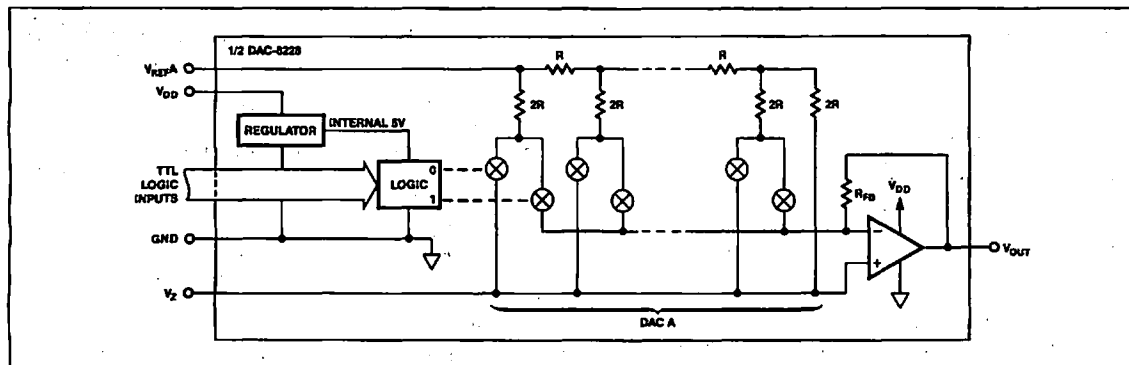


FUNCTIONAL DIAGRAM



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

FIGURE 1: Simplified Schematic (One-Half of DAC-8228)



APPLICATIONS INFORMATION

The DAC-8228 is optimized for operation in single-supply applications. Circuit operation is shown in the simplified schematic of Figure 1. The current-switching mode D/A converter is connected to the internal amplifier, resulting in a single inversion between reference input (V_{REF}) and the output (V_{OUT}) with respect to the virtual zero (V_Z).

Because of single-supply operation, this circuit is used as shown in Figure 2. The external reference is connected to the V_Z terminal which determines the zero-scale output voltage, i.e., V_{OUT} is derived from all zeros digital input. When the V_{REF} input is tied to ground (GND) this sets a nominal full-scale output voltage of $2 \times V_Z$. The full transfer characteristic of the DAC-8228 is described by the following equation:

$$V_{OUT}(D) = -[D/256 \times (V_{REF} - V_Z)] + V_Z$$

where D is the digital input in integer decimal. All voltages are referenced to ground (GND).

The following boundary conditions apply to circuit operation.

$$\begin{aligned} V_Z &< (V_{DD} - 2.5V) \\ V_{OUT} &< (V_{DD} - 2V) \\ -25V &< V_{REF} < +25V \\ V_{DD} &< 18V \end{aligned}$$

FIGURE 2: Typical Voltage Output Application

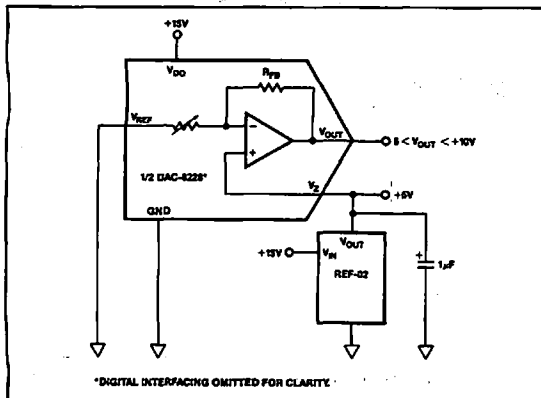


FIGURE 3: Typical Multiplying Application

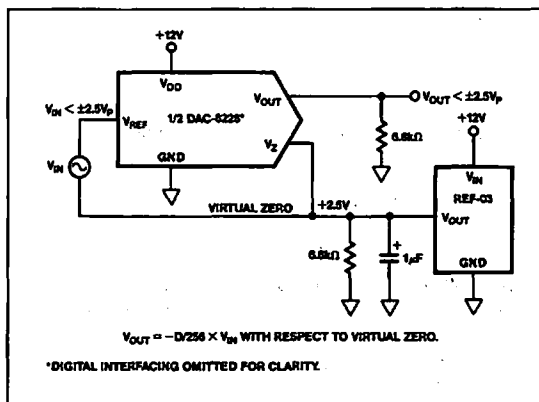
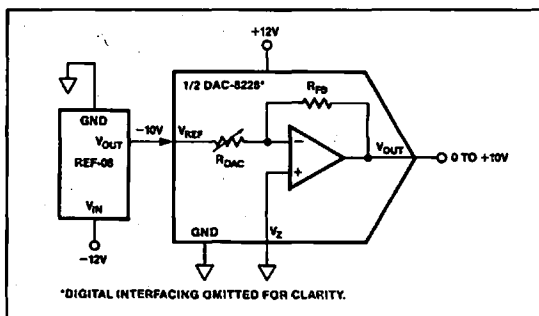


FIGURE 4: 0 to +10V Output Voltage Range





DAC-8248

DUAL 12-BIT (8-BIT BYTE)
DOUBLE-BUFFERED CMOS D/A CONVERTER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Two matched 12-bit DACs on One Chip
- 12-Bit Resolution with an 8-Bit Data Bus
- Direct Interface with 8-Bit Microprocessors
- Double-Buffered Digital Inputs
- RESET to Zero Pin
- 12-Bit Endpoint Linearity ($\pm 1/2$ LSB) Over Temperature
- Single +5V to +15V Supply
- Latch-Up Resistant
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL Package

APPLICATIONS

- Multi-Channel Microprocessor-Controlled Systems
- Industrial Automation
- Process Control
- Robotics
- Automatic Test Equipment
- Programmable Attenuator, Power Supplies, Window Comparators
- Instrumentation Equipment
- Battery Operated Equipment

GENERAL DESCRIPTION

The DAC-8248 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has an 8-bit wide input data port that

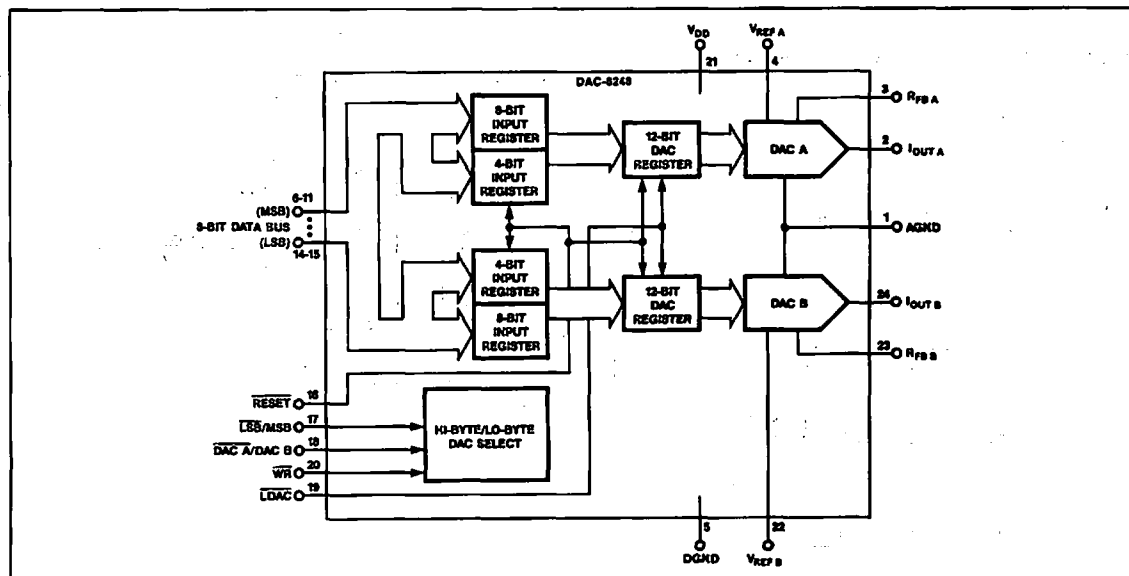
interfaces directly with most 8-bit microprocessors. It loads a 12-bit word in two bytes using a single control; it can accept either a least significant byte or most significant byte first. For designs with a 12-bit or 16-bit wide data path, choose the DAC-8222 or DAC-8221.

Outputs of DAC A and DAC B may be updated simultaneously. The DAC-8248 can also load new digital data into the DAC while simultaneously updating its output. These features are controlled with a separate LDAC control pin. A single pin resets both outputs to zero.

The monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The DAC consists of two thin-film R-2R resistor ladder networks, two 12-bit, two 8-bit, and two 4-bit data latches, and control logic. Separate reference input and feedback resistors are provided for each DAC. The DAC-8248 operates on a single supply from +5V to +15V, and it dissipates less than 0.5mW at +5V (using zero or V_{DD} logic levels). The device is packaged in a space-saving 0.3" 24-pin DIP.

The DAC-8248 is manufactured with PMI's highly-stable thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS technology. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

FUNCTIONAL DIAGRAM



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



ORDERING INFORMATION†

PACKAGE: 24-PIN DIP

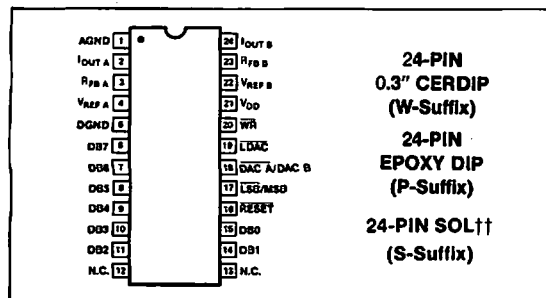
RELATIVE ACCURACY ERROR (+5V or +15V)	GAIN ERROR	MILITARY*	INDUSTRIAL	COMMERCIAL
		TEMPERATURE -55°C TO +125°C	TEMPERATURE -40°C TO +85°C	TEMPERATURE 0°C TO 70°C
±1/2 LSB	±2 LSB	DAC8248AW	DAC8248EW	DAC8248GP
±1 LSB	±4 LSB	—	DAC8248FW	DAC8248HP
±1 LSB	±4 LSB	—	—	DAC8248HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for /883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$, unless otherwise noted.)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	-0.3V, $V_{DD} + 0.3\text{V}$
Digital Input Voltage to DGND	-0.3V, $V_{DD} + 0.3\text{V}$
$I_{OUT A}$, $I_{OUT B}$ to AGND	-0.3V, $V_{DD} + 0.3\text{V}$
$V_{REF A}$, $V_{REF B}$ to AGND	±25V
$V_{REF A}$, $V_{REF B}$ to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derate Above +75°C by	6mW/°C
Operating Temperature Range	
AW Version	-55°C to +25°C
EW, FW Versions	-40°C to +85°C
GP, HP Versions	0°C to +70°C
Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

CAUTION:

- Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB} .
- The digital control inputs are Zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
- Do not insert this device into powered sockets; remove power before insertion or removal.
- Use proper anti-static handling procedures.
- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5\text{V}$ or $+15\text{V}$; $V_{REF A} = V_{REF B} = +10\text{V}$; $V_{OUT A} = V_{OUT B} = 0\text{V}$; AGND = DGND = 0V; $T_A = -55^\circ\text{C}$ to $+25^\circ\text{C}$ apply for DAC-8248AW; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ apply for DAC-8248EW/FW; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for DAC-8248GP/HP, unless otherwise noted. Specifications apply for DAC A and DAC B.

			DAC-8248			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Relative Accuracy	INL	DAC-8248A/E/G	—	—	±1/2	LSB
		DAC-8248F/H	—	—	±1	
Differential Nonlinearity	DNL	All Grades are Monotonic	—	—	±1	LSB
Full Scale Gain Error (Note 1)	G _{FSE}	T _A = ±25°C	—	—	—	LSB
		DAC-8248A/E/G	—	—	±2	
		DAC-8248F/H	—	—	±4	
		T _A = Full Temp. Range	—	—	—	
		DAC-8248A/E/G	—	—	±3	
		DAC-8248F/H	—	—	±6	
Gain Temperature Coefficient (ΔGain/ΔTemperature)	TCG _{FS}	(Notes 2, 6)	—	±2	±5	ppm/°C
Output Leakage Current I _{OUT A} (Pin 2), I _{OUT B} (Pin 24)	I _{LKG}	All Digital Inputs = 0s	—	—	—	nA
		T _A = +25°C	—	±5	±50	
		T _A = Full Temp. Range	—	—	±100	
Input Resistance (V _{REF A} , V _{REF B})	R _{REF}		8	11	15	kΩ
Input Resistance Match (V _{REF A} /V _{REF B})	ΔV _{REF A, B}		—	±0.2	±1	%
DIGITAL INPUTS						
Digital Input High	V _{INH}	V _{DD} = +5V	2.4	—	—	V
		V _{DD} = +15V	13.5	—	—	



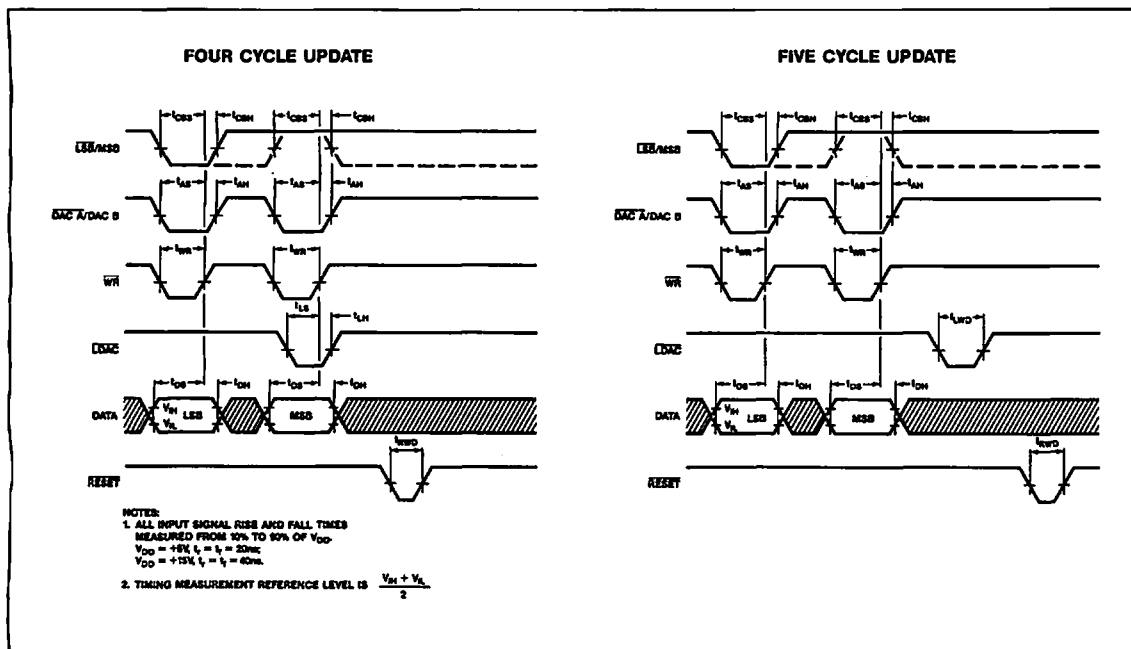
ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$; $V_{REF A} = V_{REF B} = +10V$; $V_{OUT A} = V_{OUT B} = 0V$; $AGND = DGND = 0V$; $T_A = -55^{\circ}C$ to $+25^{\circ}C$ apply for DAC-8248AW; $T_A = -40^{\circ}C$ to $+85^{\circ}C$ apply for DAC-8248EW/FW; $T_A = 0^{\circ}C$ to $+70^{\circ}C$ apply for DAC-8248GP/HP, unless otherwise noted. Specifications apply for DAC A and DAC B. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-8248			UNITS
			MIN	TYP	MAX	
Digital Input Low	V_{INL}	$V_{DD} = +5V$ $V_{DD} = +15V$	—	—	0.8 1.5	V
Input Current ($V_{IN} = 0V$ or V_{DD} and V_{INL} or V_{INH})	I_{IN}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	—	± 0.001 —	± 1 ± 10	μA
Input Capacitance (Note 2)	C_{IN}	DB0-DB11 WR, LDAC, DAC A/DAC B, LSB/MSB, RESET	—	—	10 15	pF
POWER SUPPLY						
Supply Current	I_{DD}	Digital Inputs = V_{INL} or V_{INH} Digital Inputs = $0V$ or V_{DD}	—	— 10	2 100	mA μA
DC Power Supply Rejection Ratio ($\Delta \text{Gain}/\Delta V_{DD}$)	PSRR	$\Delta V_{DD} = \pm 5\%$	—	—	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 3, 4)	t_{PD}	$T_A = +25^{\circ}C$	—	—	300	ns
Output Current Settling Time (Notes 4, 5)	t_S	$T_A = +25^{\circ}C$	—	—	1	μs
Output Capacitance	C_O	Digital Inputs = all 0s C_{OUTA}, C_{OUTB}	—	—	90	pF
		Digital Inputs = all 1s C_{OUTA}, C_{OUTB}	—	—	120	
AC Feedthrough at $I_{OUT A}$ or $I_{OUT B}$	FT_A	$V_{REF A}$ to $I_{OUT A}$; $V_{REF A} = 20V_{P-P}$ $f = 100kHz$; $T_A = +25^{\circ}C$	—	—	-70	dB
	FT_B	$V_{REF B}$ to $I_{OUT B}$; $V_{REF B} = 20V_{P-P}$ $f = 100kHz$; $T_A = +25^{\circ}C$	—	—	-70	
			$V_{DD} = +5V$		$V_{DD} = +15V$	
SWITCHING CHARACTERISTICS (Notes 2, 7)			$+25^{\circ}C$	-40 to $+85^{\circ}C$ (Note 8)	-55 to $+125^{\circ}C$	ALL TEMPS
LSB/MSB Select to Write Set-up Time	t_{CBS}	140	170	180	90	ns MIN
LSB/MSB Select to Write Hold Time	t_{CBH}	0	0	0	0	ns MIN
DAC Select to Write Set-up Time	t_{AS}	140	170	180	90	ns MIN
DAC Select to Write Hold Time	t_{AH}	0	0	0	0	ns MIN
LDAC to Write Set-up Time	t_{LS}	100	120	120	90	ns MIN
LDAC to Write Hold Time	t_{LH}	10	0	0	0	ns MIN
Data Valid to Write Set-up Time	t_{DS}	150	170	190	90	ns MIN
Data Valid to Write Hold Time	t_{DH}	0	0	0	0	ns MIN
Write Pulse Width	t_{WR}	120	150	170	90	ns MIN
LDAC Pulse Width	t_{LWD}	90	90	90	90	ns MIN
Reset Pulse Width	t_{RWD}	70	70	70	70	ns MIN

NOTES:

- Measured using internal $R_{FB A}$ and $R_{FB B}$. Both DAC digital inputs = 1111 1111 1111.
- Guaranteed and not tested.
- From 50% of digital input to 90% of final analog output current. $V_{REF A} = V_{REF B} = +10V$; $OUT A$, $OUT B$ load = 100Ω ; $C_{EXT} = 13pF$.
- WR, LDAC = $0V$; DB0-DB11 = $0V$ to V_{DD} or V_{DD} to $0V$.
- Settling time is measured from 50% of the digital input change to where the output settles within 1/2 LSB of full scale.
- Gain TC is measured from $+25^{\circ}C$ to T_{MIN} or from $+25^{\circ}C$ to T_{MAX} .
- See Timing Diagram.
- These limits apply for the commercial and industrial grade products.

WRITE TIMING CYCLE DIAGRAM



INTERFACE CONTROL LOGIC

LSB/MSB—(PIN 17) LEAST SIGNIFICANT BIT (Active Low)/ MOST SIGNIFICANT BIT (Active High). Selects lower 8-bits (LSBs) or upper 4-bits (MSBs); either can be loaded first. It is used with the $\overline{WR}$ signal to load data into the input registers. Data is loaded in a right justified format.

DAC A/DAC B—(PIN 18) DAC SELECTION. Active Low for DAC A and Active High for DAC B.

$\overline{WR}$ —(PIN 20) WRITE—Active Low. Used with the $\overline{LSB/MSB}$ signal to load data into the input registers, or Active High to latch data into the input registers.

$\overline{LDAC}$ —(PIN 19) LOAD DAC. Used to transfer data simultaneously from DAC A and DAC B input registers to both DAC output registers, or Active High to latch data into the output registers.

$\overline{RESET}$ —(PIN 16)—Active Low. Functions as a zero override; all registers are forced to zero when the $\overline{RESET}$ signal is low. All

registers are latched to zeros when the write signal is high and $\overline{RESET}$ goes high.

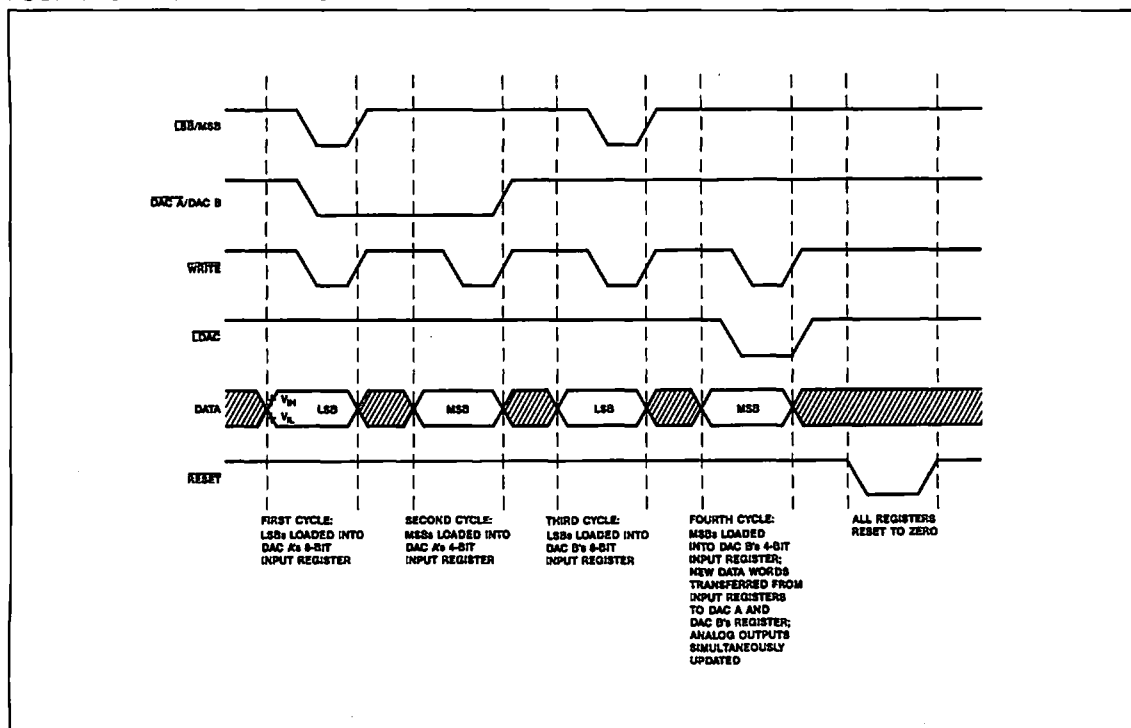
WRITE TIMING CYCLES

Four timing diagrams are shown: two are for the switching specification reference, and two are for DAC update timing reference. The modes are at the users discretion which to use.

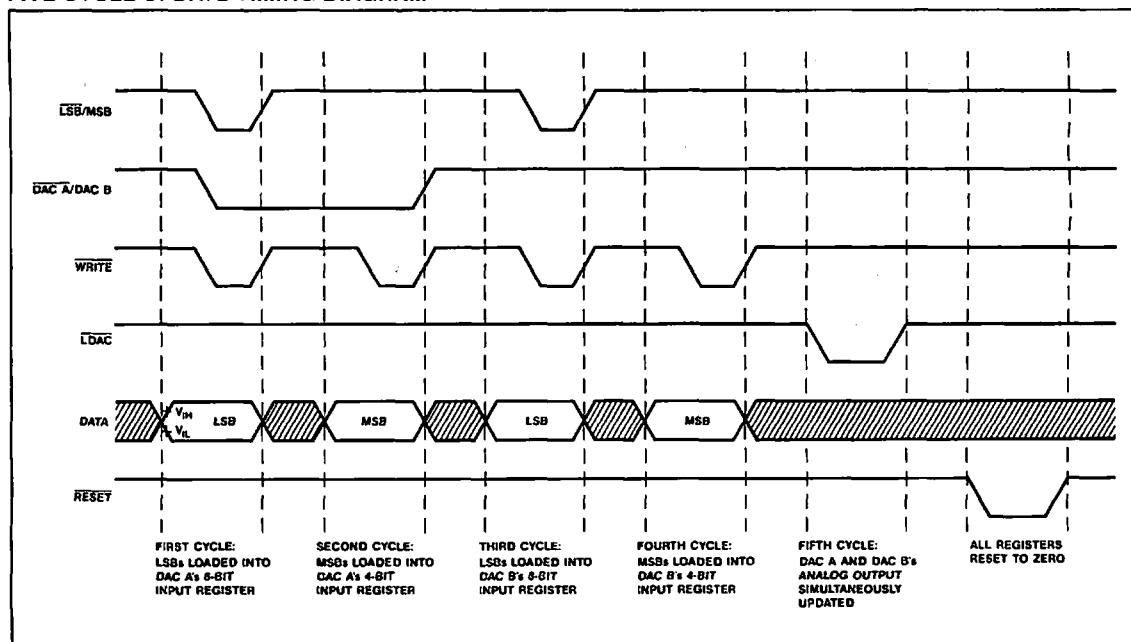
The **FOUR CYCLE UPDATE**, as the name implies, allows both DACs to be loaded and the outputs updated in four cycles. New data is first loaded into one DAC's input registers on the first two write cycles, and then new data loaded into the other DAC's input registers on the second two write cycles while simultaneously updating both DAC outputs on the fourth cycle.

The **FIVE CYCLE UPDATE** allows DAC A and DAC B input registers to be loaded on the first four cycles as above, and the DAC outputs updated on the fifth cycle at a later time.

FOUR CYCLE UPDATE TIMING DIAGRAM



FIVE CYCLE UPDATE TIMING DIAGRAM





MODE SELECTION TABLE

DIGITAL INPUTS					DAC REGISTER STATUS					
DAC A/B	$\overline{WR}$	LSB/MSB	$\overline{RESET}$	$\overline{LDAC}$	DAC A			DAC B		
					LSB	MSB	LDAC	LSB	MSB	LDAC
L	L	L	H	H	WR	LAT	LAT	LAT	LAT	LAT
L	L	L	H	L	WR	LAT	WR	LAT	LAT	WR
L	L	H	H	H	LAT	WR	LAT	LAT	LAT	LAT
L	L	H	H	L	LAT	WR	WR	LAT	LAT	WR
H	L	L	H	H	WR	LAT	LAT	LAT	LAT	LAT
H	L	L	H	L	WR	LAT	WR	LAT	LAT	WR
H	L	H	H	H	LAT	WR	LAT	LAT	LAT	LAT
H	L	H	H	L	LAT	WR	WT	LAT	LAT	WR
X	H	X	H	H	LAT	LAT	LAT	LAT	LAT	LAT
X	H	X	H	L	LAT	LAT	WR	LAT	LAT	WR
X	X	X	L	X	ALL REGISTERS ARE RESET TO ZEROS.					
X	H	X	$\overline{\uparrow}$	X	ALL REGISTERS ARE LATCHED TO ZEROS.					

L = Low H = High X = Don't Care WR = Registers Being Loaded LAT = Registers Latched



DAC-8408

QUAD 8-BIT MULTIPLYING CMOS
D/A CONVERTER WITH MEMORY

Precision Monolithics Inc.

FEATURES

- Four DACs in a 28 Pin, 0.6 Inch Wide DIP or 28 Pin JEDEC Plastic Chip Carrier
- $\pm 1/4$ LSB End-Point Linearity
- Guaranteed Monotonic
- DACs Matched to Within 1%
- Microprocessor Compatible
- Read/Write Capability (with Memory)
- TTL/CMOS Compatible
- Four-Quadrant Multiplication
- Single-Supply Operation (+5V)
- Low Power Consumption
- Latch-Up Resistant

ORDERING INFORMATION†

INL	DNL	PACKAGE		
		COMMERCIAL TEMPERATURE 0°C to +70°C	INDUSTRIAL TEMPERATURE -25°C to +85°C	MILITARY* TEMPERATURE -55°C to +125°C
$\pm 1/4$ LSB	$\pm 1/2$ LSB	DAC8408GP	DAC8408ET	DAC8408AT
$\pm 1/2$ LSB	± 1 LSB	DAC8408HP	DAC8408FT	DAC8408BT
$\pm 1/2$ LSB	± 1 LSB	DAC8408HPC††	—	—

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

APPLICATIONS

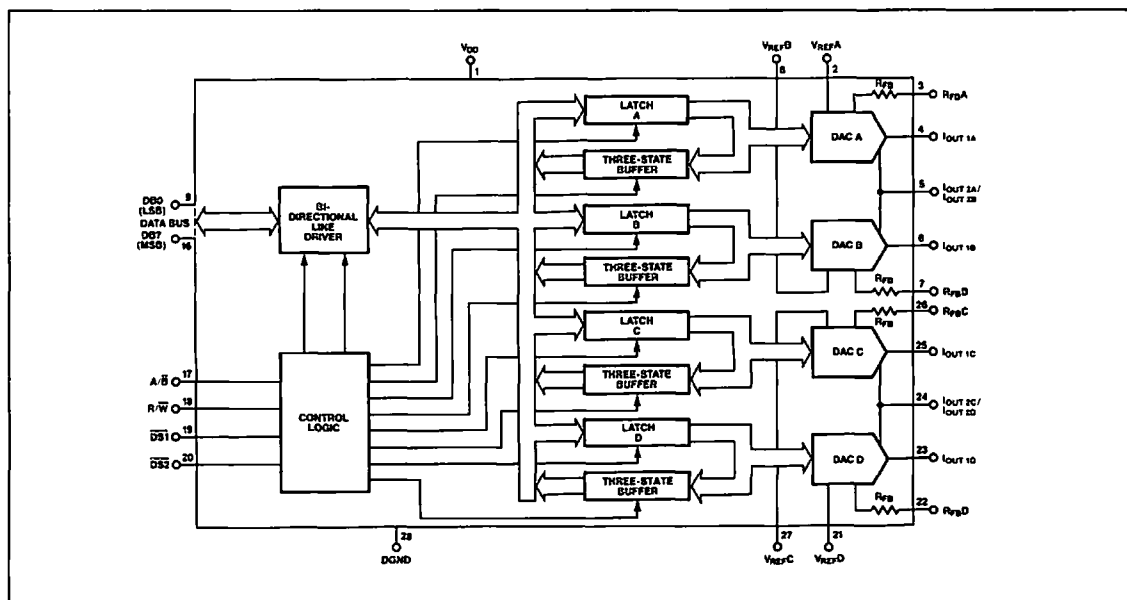
- Voltage Set Points in Automatic Test Equipment
- Systems Requiring Data Access for Self-Diagnostics
- Industrial Automation
- Multi-Channel Microprocessor-Controlled Systems
- Digitally Controlled Op Amp Offset Adjustment
- Process Control
- Digital Attenuators

GENERAL DESCRIPTION

The DAC-8408 is a monolithic quad 8-bit multiplying digital-to-analog CMOS converter. Each DAC has its own reference input, feedback resistor, and on-board data latches that feature read/write capability. The readback function serves as memory for those systems requiring self-diagnostics.

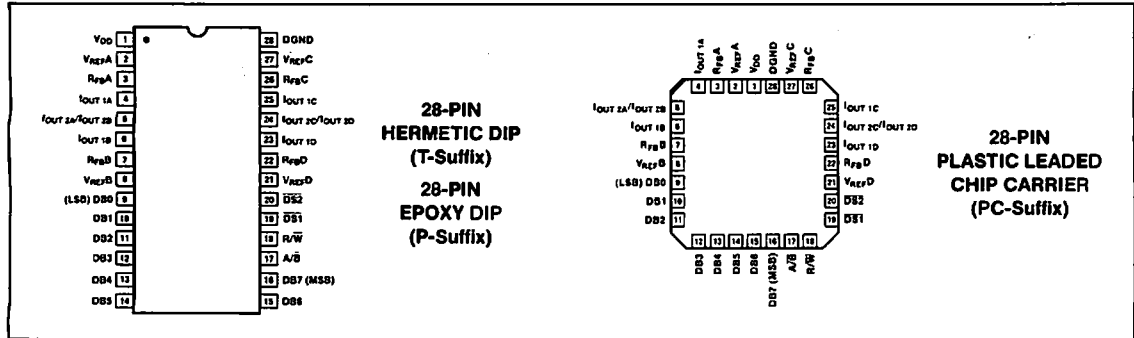
A common 8-bit TTL/CMOS compatible input port is used to load data into any of the four DAC data-latches. Control lines DS1, DS2, and A/B determine which DAC will accept data. Data loading is similar to that of a RAM's write cycle. Data can be read back onto the same data bus with control line R/W. The DAC-8408 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80. The DAC-8408 operates on a single +5 volt supply and dissipates less than 20mW. The DAC-8408 is manufactured using PMI's highly stable, thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS process. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

FUNCTIONAL DIAGRAM





PIN CONNECTIONS

**ABSOLUTE MAXIMUM RATINGS** ($T_A = +25^\circ\text{C}$ unless otherwise noted.)

V_{DD} to IOUT 2A, IOUT 2B, IOUT 2C, IOUT 2D	0, +7V
V_{DD} to DGND	0, +7V
IOUT 1A, IOUT 1B	
IOUT 1C, IOUT 1D to DGND	-0.3V to $V_{DD} + 0.3V$
$R_{FB}A, R_{FB}B, R_{FB}C, R_{FB}D$ to IOUT	$\pm 25V$
IOUT 2A, IOUT 2B	
IOUT 2C, IOUT 2D to DGND	-0.3V to $V_{DD} + 0.3V$
DB0 through DB7 to DGND	-0.3V to $V_{DD} + 0.3V$
Control Logic	
Input Voltage to DGND	-0.3V to $V_{DD} + 0.3V$
$V_{REF}A, V_{REF}B, V_{REF}C, V_{REF}D$, to	
IOUT 2A, IOUT 2B, IOUT 2C, IOUT 2D	$\pm 25V$
Power Dissipation (Any Package) to $+75^\circ\text{C}$	450mW
Derates Above $+75^\circ\text{C}$ by	6mW/ $^\circ\text{C}$

Operating Temperature Range

Commercial Grade (GP, HP, HPC)	0°C to $+70^\circ\text{C}$
Industrial Grade (ET, FT)	-25°C to $+85^\circ\text{C}$
Military Grade (AT, BT)	-55°C to $+125^\circ\text{C}$
Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$

CAUTION:

- Do not apply voltages higher than $V_{DD} + 0.3V$ or less than $-0.3V$ potential on any terminal except V_{REF} and R_{FB} .
- The digital control inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep in conductive foam at all times until ready to use.
- Use proper anti-static handling procedures.
- Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = \pm 10V$; $V_{OUT}A, B, C, D = 0V$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ apply for DAC-8408AT/BT, $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ apply for DAC-8408ET/FT; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for DAC-8408GP/HP/HPC, unless otherwise noted. Specifications apply for DAC A, B, C, & D.

			DAC-8408			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		8	—	—	Bits
Nonlinearity (Notes 1, 2)	INL	DAC-8408A/E/G DAC-8408B/F/H	— —	— —	±1/4 ±1/2	LSB
Differential Nonlinearity	DNL	DAC-8408A/E/G DAC-8408B/F/H	— —	— —	±1/2 ±1	LSB
Gain Error	G _{FSE}	(Using Internal R _{FB})	—	—	±1	LSB
Gain Tempco (Notes 3, 6)	TC _{GFS}		—	±2	±40	ppm/°C
Power Supply Rejection (ΔV _{DD} = ±10%)	PSR		—	—	0.001	%FSR/%
I _{OUT} 1A, B, C, D Leakage Current (Note 13)	I _{LKG}	T _A = +25°C	—	—	±30	nA
		T _A = Full Temp. Range	—	—	±100	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = \pm 10V$; $V_{OUTA, B, C, D} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8408AT/BT, $T_A = -25^\circ C$ to $+85^\circ C$ apply for DAC-8408ET/FT; $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8408GP/HP/HPC, unless otherwise noted. Specifications apply for DAC A, B, C, & D. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-8408			UNITS
			MIN	TYP	MAX	
REFERENCE INPUT						
Input Voltage Range			—	—	±20	V
Input Resistance Match (Note 4)		R _A , B, C, D	—	—	±1	%
Input Resistance	R _{IN}		6	10	14	kΩ
DIGITAL INPUTS						
Digital Input Low	V _{IL}		—	—	0.8	V
Digital Input High	V _{IH}		2.4	—	—	V
Input Current (Note 5)	I _{IN}	T _A = +25°C T _A = Full Temp. Range	—	±0.01	±1.0	μA
			—	—	±10.0	
Input Capacitance (Note 6)	C _{IN}		—	—	8	pF
DATA BUS OUTPUTS						
Digital Output Low	V _{OL}	1.6mA Sink	—	—	0.4	V
Digital Output High	V _{OH}	400μA Source	4	—	—	V
Output Leakage Current	I _{LKG}	T _A = +25°C T _A = Full Temp. Range	—	±0.005	±1.0	μA
			—	±0.075	±10.0	
DAC OUTPUTS (Note 6)						
Propagation Delay (Note 7)	t _{PD}		—	150	180	ns
Settling Time (Notes 11, 12)	t _s		—	190	250	ns
Output Capacitance	C _{OUT}	DAC Latches All "0's" DAC Latches All "1's"	—	—	30	pF
			—	—	50	
AC Feedthrough	FT	(20V _{p-p} @ F = 100kHz)	54	—	—	dB
SWITCHING CHARACTERISTICS (Notes 6, 10)						
Write to Data Strobe Time	t _{DS1} or t _{DS2}	T _A = +25°C T _A = Full Temp. Range	90 145	—	—	ns
Data Valid to Strobe Set-Up Time	t _{DSU}	T _A = +25°C T _A = Full Temp. Range	150 175	—	—	ns
Data Valid to Strobe Hold Time	t _{DH}		10	—	—	ns
DAC Select to Strobe Set-Up Time	t _{AS}		0	—	—	ns
DAC Select to Strobe Hold Time	t _{AH}		0	—	—	ns
Write Select to Strobe Set-Up Time	t _{WSU}		0	—	—	ns
Write Select to Strobe Hold Time	t _{WH}		0	—	—	ns



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = \pm 10V$; $V_{OUTA, B, C, D} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for DAC-8408AT/BT, $T_A = -25^\circ C$ to $+85^\circ C$ apply for DAC-8408ET/FT; $T_A = 0^\circ C$ to $+70^\circ C$ apply for DAC-8408GP/HP/HPC, unless otherwise noted. Specifications apply for DAC A, B, C, & D. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-8408			UNITS
			MIN	TYP	MAX	
Read to Data Strobe Width	t_{RDS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	220 350	—	—	ns
Data Strobe to Output Valid Time	t_{CO}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	320 430	—	—	ns
Output Data to Deselect Time	t_{OTD}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	200 270	—	—	ns
Read Select to Strobe Set-Up Time	t_{RSU}		0	—	—	ns
Read Select to Strobe Hold Time	t_{RH}		0	—	—	ns
POWER SUPPLY						
Voltage Range	V_{DD}		4.5	—	5.5	V
Supply Current (Note 8)	I_{DD}		—	—	50	μA
Supply Current (Note 9)	I_{DD}	$T_A = +25^\circ C$ $T_A = \text{Full Temp. Range}$	—	—	1.0 1.5	mA

NOTES:

1. This is an end-point linearity specification.
2. Guaranteed to be monotonic over the full operating temperature range.
3. ppm/ $^\circ C$ of FSR (FSR = Full Scale Range = $V_{REF} - 1 \text{ LSB}$).
4. Input Resistance Temperature Coefficient = $+300 \text{ ppm}/^\circ C$.
5. Logic Inputs are MOS gates. Typical input current at $+25^\circ C$ is less than 10 nA .
6. Guaranteed by design.

7. From Digital Input to 90% of final analog output current.

8. All Digital Inputs "0" or V_{DD} .

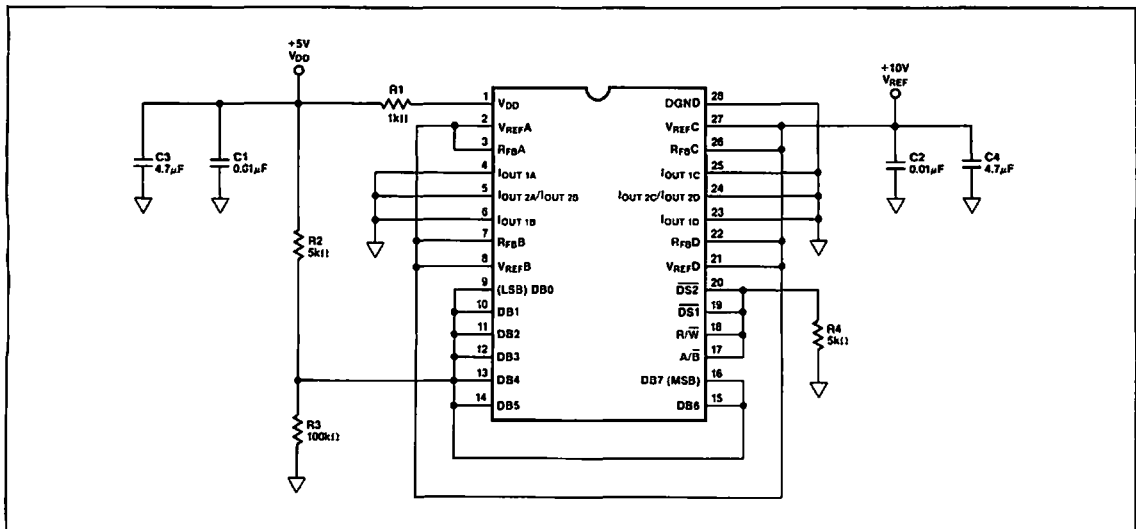
9. All Digital Inputs V_{IH} or V_{IL} .

10. See Timing Diagram.

11. Digital Inputs = $0V$ to V_{DD} or V_{DD} to $0V$.

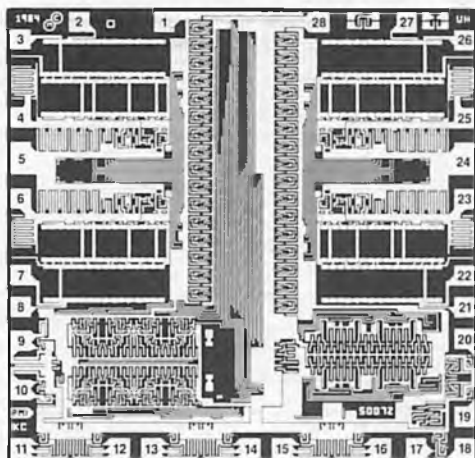
12. Extrapolated: $t_d (1/2 \text{ LSB}) = t_{pD} + 6.2\tau$ where τ = the measured first time constant of the final RC decay.

13. All Digital Inputs = $0V$; $V_{REF} = +10V$.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.130 × 0.124 inch, 16,120 sq. mils
(3.30 × 3.15 mm, 10.4 sq. mm)

- | | |
|----------------------------|-----------------------------|
| 1. V_{DD} | 15. DB6 |
| 2. V_{REFA} | 16. DB7 (MSB) |
| 3. R_{FBA} | 17. A/B |
| 4. $I_{OUT 1A}$ | 18. R/W |
| 5. $I_{OUT 2A}/I_{OUT 2B}$ | 19. DS1 |
| 6. $I_{OUT 1B}$ | 20. DS2 |
| 7. R_{FBB} | 21. V_{REFD} |
| 8. V_{REFB} | 22. R_{FBD} |
| 9. DB0 (LSB) | 23. $I_{OUT 1D}$ |
| 10. DB1 | 24. $I_{OUT 2C}/I_{OUT 2D}$ |
| 11. DB2 | 25. $I_{OUT 1C}$ |
| 12. DB3 | 26. R_{FBC} |
| 13. DB4 | 27. V_{REFC} |
| 14. DB5 | 28. DGND |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +5V$; $V_{REF} = \pm 10V$; $V_{OUTA, B, C, D} = 0V$; $T_A = +25^\circ C$, unless otherwise noted. Specifications apply for DAC A, B, C, & D.

PARAMETER	SYMBOL	CONDITIONS	DAC-8408G LIMITS	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits MIN
Nonlinearity (Note 1)	INL		$\pm 1/2$	LSB MAX
Differential Nonlinearity	DNL		± 1	LSB MAX
Gain Error	G_{FSE}	Using Internal R_{FB}	± 1	LSB MAX
Power Supply Rejection $\Delta V_{DD} = \pm 10\%$ (Note 2)	PSR	Using Internal R_{FB}	0.001	%FSR/% MAX
$I_{OUT 1A, B, C, D}$ Leakage Current	I_{LKG}	All Digital Inputs = 0V $V_{REF} = +10V$	± 30	nA MAX
REFERENCE INPUT				
Reference Input Resistance (Note 3)	R_{IN}		6/14	k Ω MIN/MAX
Input Resistance Match	R_{IN}		± 1	% MAX
DIGITAL INPUTS				
Digital Input Low	V_{IL}		0.8	V MAX
Digital Input High	V_{IH}		2.4	V MIN
Input Current (Note 4)	I_{IN}		± 1.0	μA MAX



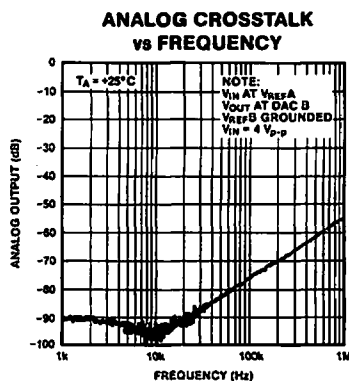
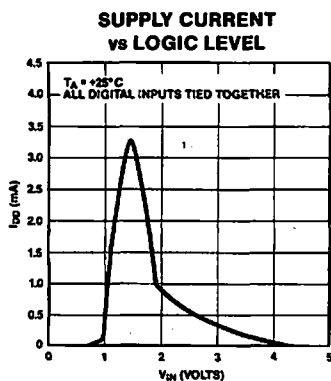
WAFER TEST LIMITS at $V_{DD}=+5V$; $V_{REF}=\pm 10V$; $V_{OUTA, B, C, D}=0V$; $T_A=+25^\circ C$, unless otherwise noted. Specifications apply for DAC A, B, C, & D. (Continued)

PARAMETER	SYMBOL	CONDITIONS	DAC-8408G LIMITS	UNITS
DATA BUS OUTPUTS				
Digital Output Low	V_{OL}	1.8mA Sink	0.4	V MAX
Digital Output High	V_{OH}	400 μA Source	4	V MIN
Output Leakage Current	I_{LKG}		± 1.0	μA MAX
POWER SUPPLY				
Supply Current (Note 5)	I_{DD}		50	μA MAX
Supply Current (Note 6)	I_{DD}		1.0	mA MAX

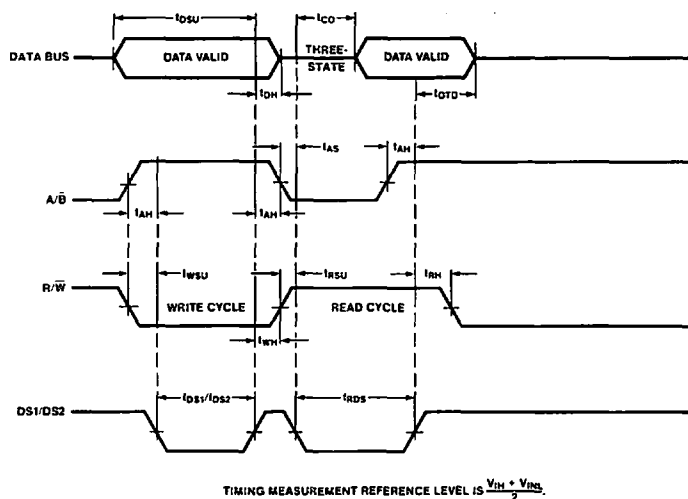
NOTES:

1. This is an endpoint linearity specification.
2. FSR is Full Scale Range = $V_{REF} - 1 \text{ LSB}$.
3. Input Resistance Temperature Coefficient approximately equals $+300 \text{ ppm}/^\circ C$.
4. Logic inputs are MOS gates. Typical input current at $+25^\circ C$ is less than 10 nA .
5. All Digital Inputs are either "0" or V_{DD} .
6. All Digital Inputs are either V_{IH} or V_{IL} .

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

TIMING DIAGRAM



PARAMETER DEFINITIONS

RESOLUTION

Resolution is the number of states (2^n) that the full-scale range (FSR) of a DAC is divided (or resolved) into.

NONLINEARITY

Nonlinearity (Relative Accuracy) is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in LSB, %, or ppm of full-scale range.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the worst case deviation of any adjacent analog outputs from the ideal 1LSB step size. A specified differential nonlinearity of ± 1 LSB maximum over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain Error (full-scale error) is a measure of the output error between the ideal and actual DAC output. The ideal full-scale output is $V_{REF} - 1$ LSB.

OUTPUT CAPACITANCE

Output Capacitance is that capacitance between $I_{OUT\ 1A}$, $I_{OUT\ 1B}$, $I_{OUT\ 1C}$, or $I_{OUT\ 1D}$ and AGND.

AC FEEDTHROUGH ERROR

This is the error caused by capacitance coupling from V_{REF} to the DAC output with all switches off.

SETTLING TIME

Settling Time is the time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input signal.

PROPAGATION DELAY

This is a measure of the internal delays of the DAC. It is defined as the time from a digital input change to the analog output-current reaching 90% of its final value.

CHANNEL-TO-CHANNEL ISOLATION

This is the portion of input signal that appears at the output of a DAC from another DAC's reference input. It is expressed as a ratio in dB.

DIGITAL CROSSTALK

Digital Crosstalk is the glitch energy transferred to the output of one DAC due to a change in digital input code from other DACs. It is specified in nVs.

CIRCUIT INFORMATION

The DAC-8408 combines four identical 8-bit CMOS DACs onto a single monolithic chip. Each DAC has its own reference input, feedback resistor, and on-board data latches. It also features a read/write function that serves as an accessible memory location for digital-input data words. The DAC's three-state readback drivers place the data word back onto the data bus.

D/A CONVERTER SECTION

Each DAC contains a highly stable, silicon-chromium, thin-film, $R-2R$ resistor ladder network and eight pairs of current steering switches. These switches are in series with each ladder resistor and are single-pole, double-throw NMOS transistors; the gates of these transistors are controlled by CMOS inverters. Figure 1 shows a simplified circuit of the $R-2R$ resistor ladder section, and Figure 2 shows an approximate equivalent switch circuit. The current through each resistor leg is switched between I_{OUT1} and I_{OUT2} . This maintains a constant current in each leg, regardless of the digital input logic states.

Each transistor switch has a finite "ON" resistance that can introduce errors to the DAC's specified performance. These resistances must be accounted for by making the voltage drop across each transistor equal to each other. This is done by binarily-scaling the transistor's "ON" resistance from the most significant bit (MSB) to the least significant bit (LSB). With 10 volts applied at the reference input, the current through the MSB switch is 0.5mA, the next bit is 0.25mA, etc.; this maintains a constant 10mV drop across each switch and the converter's accuracy is maintained. It also results in a constant resistance appearing at the DAC's reference input terminal; this allows the DAC to be driven by a voltage or current source, AC or DC of positive or negative polarity.

Shown in Figure 3 is an equivalent output circuit for DAC A. The circuit is shown with all digital inputs high. The leakage current source is the combination of surface and junction leakages to the substrate. The $1/256$ current source represents the constant 1-bit current drain through the ladder terminating resistor. The situation is reversed with all digital inputs low, as shown in Figure 4. The output capacitance is code dependent, and therefore, is modulated between the low and high values.

FIGURE 1: Simplified D/A Circuit of DAC-8408

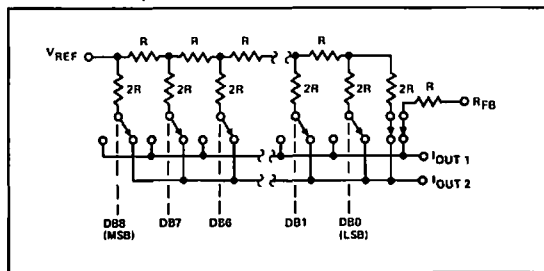


FIGURE 2: N-Channel Current Steering Switch

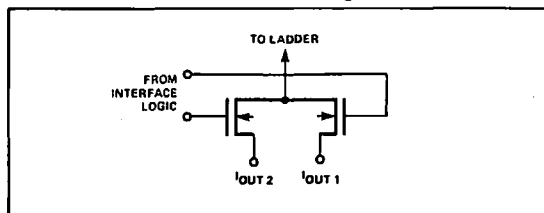


FIGURE 3: Equivalent DAC Circuit (All digital inputs HIGH)

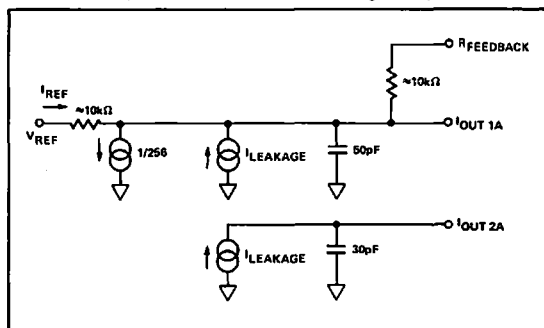
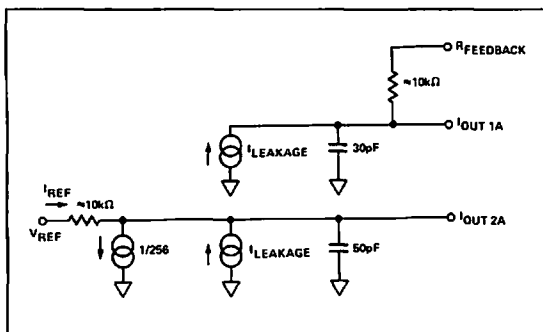
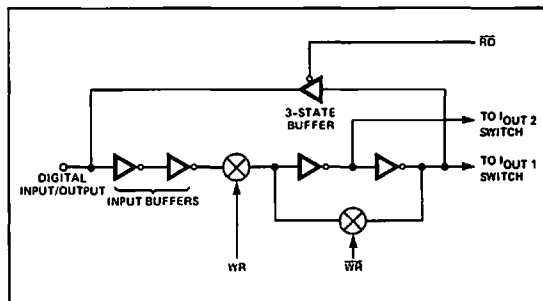


FIGURE 4: Equivalent DAC Circuit (All digital inputs LOW)


DIGITAL SECTION

Figure 5 shows the digital input/output structure for one bit. The digital $\overline{WR}$, WR , and $\overline{RD}$ controls shown in the figure are internally generated from the external $A/\overline{B}$, $R/\overline{W}$, $\overline{DS1}$, and $\overline{DS2}$ signals. The combination of these signals decide which DAC is selected. The digital inputs are CMOS inverters, designed such that TTL input levels (2.4V and 0.8V) are converted into CMOS logic levels. When the digital input is in the region of 1.2 to 1.8V, the input stages operate in their linear region and draw current from the +5V supply (see Typical Supply Current vs Logic Level curve on page 6). It is recommended that the digital input voltages be as close to V_{DD} and DGND as is practical in order to minimize supply currents. This allows maximum savings in power dissipation inherent with CMOS devices. The three-state readback digital output drivers (in the active mode) provide TTL-compatible digital outputs with a fan-out of one TTL load. The three-state digital readback leakage-current is typically 5nA.

FIGURE 5: Digital Input/Output Structure


INTERFACE LOGIC SECTION

DAC Operating Modes

- All DACs in HOLD MODE.
- DAC A, B, C, or D individually selected (WRITE MODE).
- DAC A, B, C, or D individually selected (READ MODE).
- DACs A and C simultaneously selected (WRITE MODE).
- DACs B and D simultaneously selected (WRITE MODE).

DAC Selection: Control inputs, $\overline{DS1}$, $\overline{DS2}$, and $A/\overline{B}$ select which DAC can accept data from the input port (see Mode Selection Table).

Mode Selection: Control inputs $\overline{DS}$ and $R/\overline{W}$ control the operating mode of the selected DAC.

Write Mode: When the control inputs $\overline{DS}$ and $R/\overline{W}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent, and its analog output responds to activity on the data inputs DB0—DB7.

Hold Mode: The selected DAC latch retains the data that was present on the bus line just prior to $\overline{DS}$ or $R/\overline{W}$ going to a high state. All analog outputs remain at the values corresponding to the data in their respective latches.

Read Mode: When $\overline{DS}$ is low and $R/\overline{W}$ is high, the selected DAC is in the read mode, and the data held in the appropriate latch is put back onto the data bus.

MODE SELECTION TABLE

CONTROL LOGIC				MODE	DAC
$\overline{DS1}$	$\overline{DS2}$	$A/\overline{B}$	$R/\overline{W}$		
L	H	H	L	WRITE	A
L	H	L	L	WRITE	B
H	L	H	L	WRITE	C
H	L	L	L	WRITE	D
L	H	H	H	READ	A
L	H	L	H	READ	B
H	L	H	H	READ	C
H	L	L	H	READ	D
L	L	H	L	WRITE	A&C
L	L	L	L	WRITE	B&D
H	H	X	X	HOLD	A/B/C/D
L	L	H	H	HOLD	A/B/C/D
L	L	L	H	HOLD	A/B/C/D

L = LOW STATE H = HIGH STATE X = IRRELEVANT

BASIC APPLICATIONS

Some basic circuit configurations are shown in Figures 6 and 7. Figure 6 shows the DAC-8408 connected in a unipolar configuration (2-Quadrant Multiplication), and Table I shows the Code Table. Resistors R1, R2, R3, and R4 are used to trim full scale output. Full-scale output voltage = $V_{REF} - 1 \text{ LSB} = V_{REF} (1 - 2^{-8})$ or $V_{REF} \times (255/256)$ with all digital inputs high. Low temperature coefficient (approximately 50ppm/°C) resistors or trimmers should be selected if used. Full scale can also be adjusted using V_{REF} voltage. This will eliminate resistors R1, R2, R3, and R4. In many applications, R1 through R4 are not required, and the maximum gain error will then be that of the DAC.

Each DAC exhibits a variable output resistance that is code-dependent. This produces a code-dependent, differential nonlinearity term at the amplifier's output which can have a maximum value of $0.67 \times$ the amplifier's offset voltage. This differential nonlinearity term adds to the R-2R resistor ladder differential nonlinearity; the output may no longer be monotonic. To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB ($1 \text{ LSB} = 2^{-8} \times V_{REF}$ or $1/256 \times V_{REF}$), or less than 3.9mV over the operating temperature range. Zero-scale output voltage (with all digital inputs low) may be adjusted using the op amp offset adjustment. Capacitors C1, C2, C3, and C4 provide phase compensation and help prevent overshoot and ringing when using high speed op amps.

Figure 7 shows the recommended circuit configuration for the bipolar operation (4-quadrant multiplication), and Table II shows the Code Table. Trimmer resistors R17, R18, R19, and R20

are used only if gain error adjustments are required and range between 50 and 1000Ω. Resistors R21, R22, R23, and R24 will range between 50 and 500Ω. If these resistors are used, it is essential that resistor pairs R9—R13, R10—R14, R11—R15, R12—R16 are matched both in value and tempco. They should be within 0.01%; wire wound or metal foil types are preferred for best temperature coefficient matching. The circuits of Figure 6 and 7 can either be used as a fixed reference D/A converter, or as an attenuator with an AC input voltage.

TABLE I: Unipolar Binary Code Table (Refer to Figure 6.)

DAC DATA INPUT								ANALOG OUTPUT
MSB						LSB		
1	1	1	1	1	1	1	1	$-V_{REF} \left(\frac{255}{256} \right)$
1	0	0	0	0	0	0	1	$-V_{REF} \left(\frac{129}{256} \right)$
1	0	0	0	0	0	0	0	$-V_{REF} \left(\frac{128}{256} \right) = -\frac{V_{IN}}{2}$
0	1	1	1	1	1	1	1	$-V_{REF} \left(\frac{127}{256} \right)$
0	0	0	0	0	0	0	1	$-V_{REF} \left(\frac{1}{256} \right)$
0	0	0	0	0	0	0	0	$-V_{REF} \left(\frac{0}{256} \right) = 0$

NOTE:
 $1 \text{ LSB} = (2^{-8}) (V_{REF}) = \frac{1}{256} (V_{REF})$

FIGURE 6: Quad DAC Unipolar Operation (2-Quadrant Multiplication)

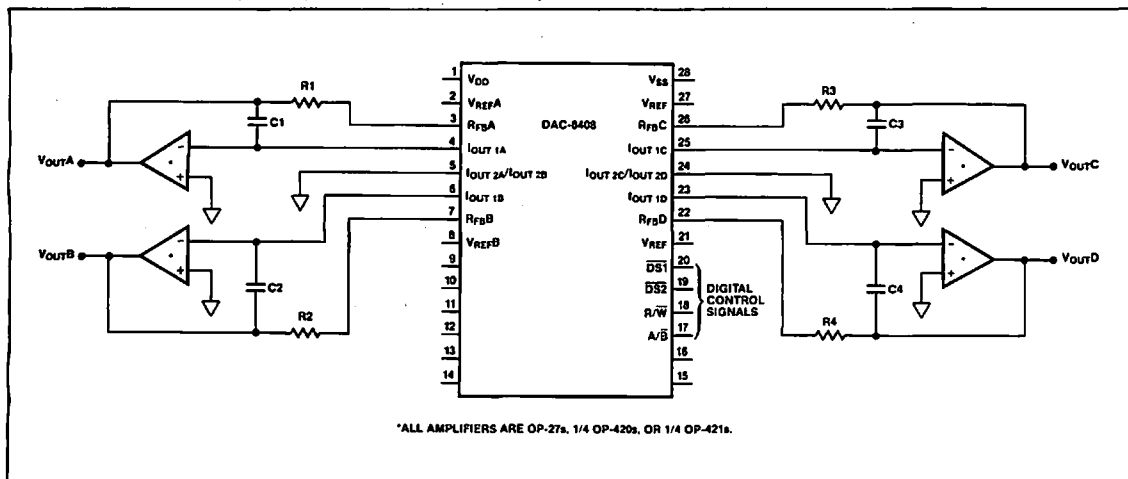


FIGURE 7: Quad DAC Bipolar Operation (4-Quadrant Multiplication)

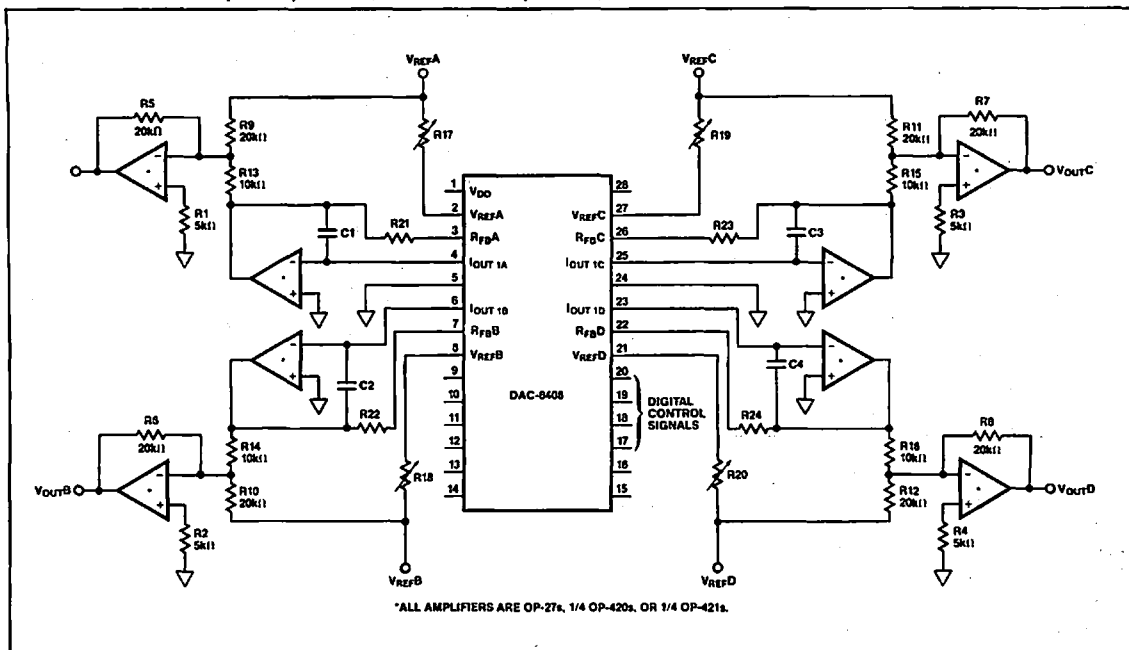


TABLE II: Bipolar (Offset Binary) Code Table (Refer to Figure 7.)

DAC DATA INPUT		ANALOG OUTPUT (DAC A OR DAC B)
MSB	LSB	
1	1	$+V_{REF} \left(\frac{127}{128} \right)$
1	0	$+V_{REF} \left(\frac{1}{128} \right)$
1	0	0
0	1	$-V_{REF} \left(\frac{1}{128} \right)$
0	0	$-V_{REF} \left(\frac{127}{128} \right)$
0	0	$-V_{REF} \left(\frac{128}{128} \right)$

NOTE:

$$1 \text{ LSB} = (2^{-7}) (V_{REF}) = \frac{1}{128} (V_{REF})$$

APPLICATION HINTS

General Ground Management: AC or transient voltages between AGND and DGND can appear as noise at the DAC-8408's analog output. Note that in Figures 5 and 6, I_{OUT2A}/I_{OUT2B} and I_{OUT2C}/I_{OUT2D} are connected to AGND. Therefore, it is recommended that AGND and DGND be tied together at the DAC-8408 socket. In systems where AGND and DGND are tied together on the backplane, two diodes (1N914 or equivalent) should be connected in inverse parallel between AGND and DGND.

Write Enable Timing: During the period when both $\overline{DS}$ and $\overline{RW}$ are held low, the DAC latches are transparent and the analog output responds directly to the digital data input. To prevent unwanted variations of the analog output, the $\overline{RW}$ should not go low until the data bus is fully settled (DATA VALID).

SINGLE SUPPLY, VOLTAGE OUTPUT OPERATION

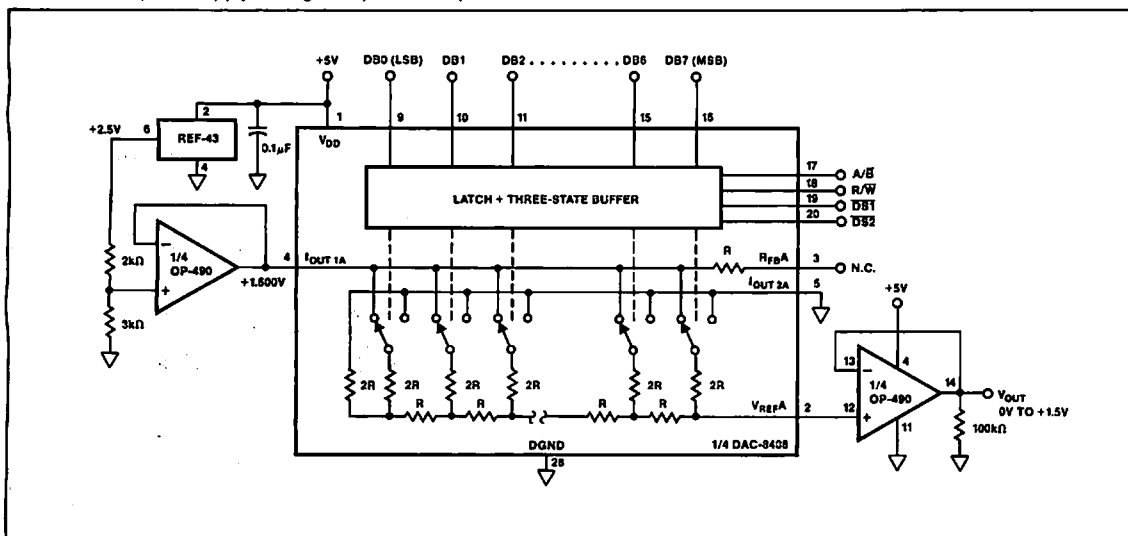
The DAC-8408 can be connected with a single +5V supply to produce DAC output voltages from 0V to +1.5V. In Figure 8, the DAC-8408 R-2R ladder is inverted from its normal connection. A +1.500V reference is connected to the current output pin 4 (I_{OUT1A}), and the normal V_{REF} input pin becomes the DAC output. Instead of a normal current output, the R-2R ladder outputs a voltage. The OP-490, consisting of four precision low-power op amps that can operate its inputs and outputs to zero volts, buffers the DAC to produce a low-impedance output voltage from 0V to +1.5V full-scale. Table III shows the code table.

With the supply and reference voltages as shown, better than 1/2 LSB differential and integral nonlinearity can be expected. To maintain this performance level, the +5V supply must not drop below 4.75V. Similarly, the reference voltage must be no higher than 1.5V. This is because the CMOS switches require a minimum level of bias in order to maintain the linearity performance.

TABLE III: Single Supply Binary Code Table (Refer to Figure 8)

DAC DATA INPUT		ANALOG OUTPUT
MSB	LSB	
1	1 1 1 1 1 1 1	$V_{REF} \left(\frac{255}{256} \right)$, +1.4941V
1	0 0 0 0 0 0 1	$V_{REF} \left(\frac{129}{256} \right)$, +0.7559V
1	0 0 0 0 0 0 0	$V_{REF} \left(\frac{128}{256} \right)$, +0.7500V
0	1 1 1 1 1 1 1	$V_{REF} \left(\frac{127}{256} \right)$, +0.7441V
0	0 0 0 0 0 0 1	$V_{REF} \left(\frac{1}{256} \right)$, +0.0059V
0	0 0 0 0 0 0 0	$V_{REF} \left(\frac{0}{256} \right)$, 0.0000V

FIGURE 8: Unipolar Supply, Voltage Output DAC Operation



The diagram illustrates a four-channel DAC system. At the core is DAC A (1/4 DAC-8408), which provides digital inputs (D0-D7, MSB to LSB), control signals (R/W, A/B, CS1, CS2), and outputs (I_O, V_O, V_{REF}). Three external DACs (DAC B, C, and D, all 1/4 DAC-8408) are connected to the system. DAC C's V_{REF} is connected to an input terminal. DAC B's V_{REF} is connected to DAC A's V_{REF}. DAC D's V_{REF} is connected to DAC A's V_{REF}. The circuit uses three OP-470 op-amp buffers to drive the DAC outputs. Two active filters, a Low Pass filter and a High Pass filter, are also shown, both using OP-470 op-amps and 1000pF capacitors. The system is powered by -15V and +5V rails with decoupling capacitors.

A powerful D/A converter application is a programmable active filter design as shown in Figure 9. The design is based on the state-variable filter topology which offers stable and repeatable filter characteristics. DAC B and DAC D can be programmed in tandem with a single digital byte load which sets the center frequency of the filter. DAC A sets the Q of the filter. DAC C sets the gain of the filter transfer function. The unique feature of this design is that varying the gain of filter does not affect the Q of the filter. Similarly, the reverse is also true. This makes the programmability of the filter extremely reliable and predictable. Note that low-pass, high-pass, and bandpass outputs are available. This sophisticated function is achieved in only two IC packages.

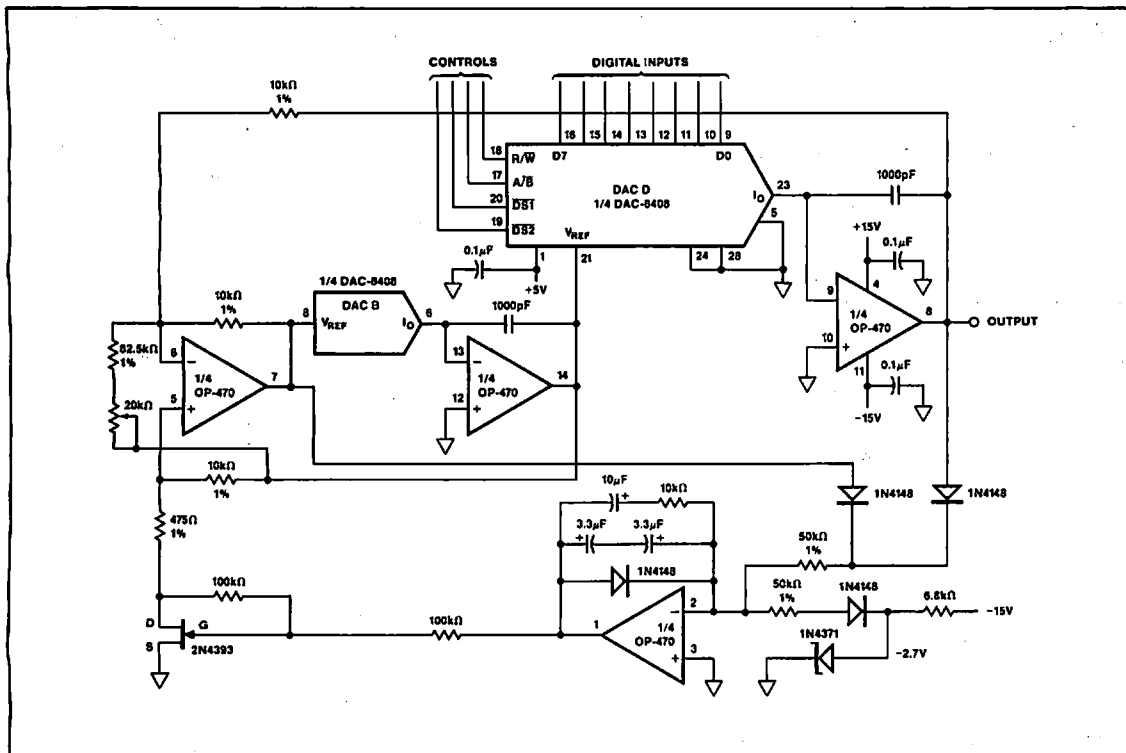
REF LEVEL
P0 P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15 P16 P17 P18 P19 P20 P21 P22 P23 P24 P25 P26 P27 P28 P29 P30 P31 P32 P33 P34 P35 P36 P37 P38 P39 P40 P41 P42 P43 P44 P45 P46 P47 P48 P49 P50 P51 P52 P53 P54 P55 P56 P57 P58 P59 P60 P61 P62 P63 P64 P65 P66 P67 P68 P69 P70 P71 P72 P73 P74 P75 P76 P77 P78 P79 P80 P81 P82 P83 P84 P85 P86 P87 P88 P89 P90 P91 P92 P93 P94 P95 P96 P97 P98 P99

START (0.000000) STOP (0.000000)

THE CIRCUIT PROVIDES FULL 8-BIT
(> 2 DECADE) DYNAMIC RANGE OF
FREQUENCY CONTROL

All components used are available off-the-shelf. Using low drift thin-film resistors, the DAC-8408 exhibits very stable performance over temperature. The wide bandwidth of the OP-470 produces excellent high frequency and high Q response. In addition, the OP-470's low input offset voltage assures an unusually low DC offset at the filter output.

FIGURE 11: A Digitally Programmable, Low-Distortion Sinewave Oscillator



A LOW-DISTORTION, PROGRAMMABLE SINEWAVE OSCILLATOR

By varying the previous state-variable filter topology slightly, one can obtain a very low distortion sinewave oscillator with programmable frequency feature as shown in Figure 11. Again, DAC B and DAC D in tandem control the oscillating frequency based on the relationship $f_c = 1/2\pi RC$. Positive feedback is accomplished via the 82.5kΩ and the 20kΩ potentiometer. The Q of the oscillator is determined by the ratio of

10kΩ and 475Ω in series with the FET transistor, which acts as an automatic gain control variable resistor. The AGC action maintains a very stable sinewave amplitude at any frequency. Again, only two ICs accomplish a very useful function.

At the highest frequency setting, the harmonic distortion level measures 0.016%. As the frequencies drop, distortion also drops to a low of 0.006%. At the lowest frequency setting, distortion came back up to a worst case of 0.035%.



DAC-8426

QUAD 8-BIT VOLTAGE OUT CMOS
D/A CONVERTER WITH INTERNAL 10V REFERENCE

Precision Monolithics Inc.

ADVANCE PRODUCT INFORMATION

FEATURES

- Four Voltage-Output DACs on a Single Chip
- Internal 10V Bandgap Reference
- Reference Output Supplies 10mA for Other Loads
- Operates from Single +15V Supply
- Microprocessor Compatible
- Fast 90ns Data Load Time, All Temperatures
- Direct Replacement for PM-7226

APPLICATIONS

- Process Controls
- Multi-Channel Microprocessor Controlled:
 - Variable Resistors
 - System Calibration
 - Op Amp Offset and Gain Adjust

GENERAL DESCRIPTION

The DAC-8426 is a complete quad voltage output D/A converter with internal reference. This product fits directly into any existing 7226 socket where the user currently has a 10V external reference. The external reference is no longer necessary. The internal reference of the DAC-8426 is laser-trimmed to $\pm 0.2\%$ ($\pm 1/2$ LSB) offering a 25ppm/ $^{\circ}\text{C}$ temperature coefficient and 10mA of load driving capability.

The DAC-8426 contains four 8-bit voltage-output CMOS D/A converters on a single chip. A 10V output bandgap reference sets the output full-scale voltage. The circuit also includes four input latches and interface control logic.

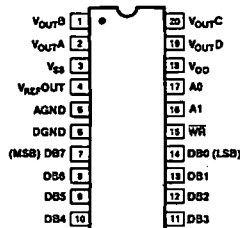
One of the four latches, selected by the address inputs, is loaded from the 8-bit data bus input when the write strobe is

active low. All digital inputs are TTL/CMOS (5V) compatible. The on-board amplifiers can drive up to 5mA from either a single or dual supply. The on-board reference that is always connected to the internal DACs has 10mA available to drive external devices.

Its compact size, low power, and economical cost-per-channel, make the DAC-8426 attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. System reliability is also increased due to reduced parts count.

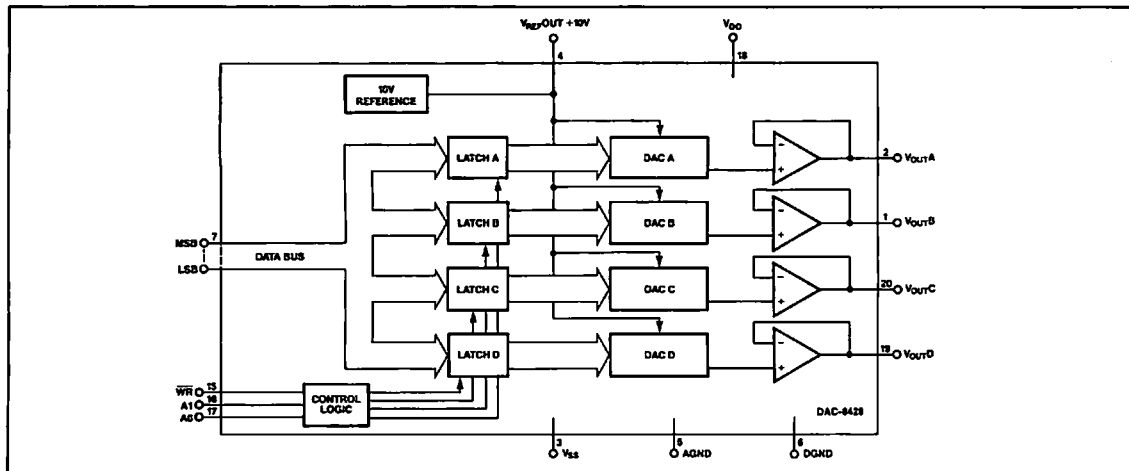
PMI's advanced oxide-isolated, silicon-gate, CMOS process allows the DAC-8426's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly-stable thin-film R-2R resistor ladder, aids in matching and temperature tracking between DACs.

PIN CONNECTIONS



20-PIN Cerdip
(R-Suffix)
20-PIN Epoxy Dip
(P-Suffix)
20-PIN Sol
(S-Suffix)

SIMPLIFIED SCHEMATIC



This advance product information describes a product in development at the time of this printing. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



PM-562

12-BIT MULTIPLYING CURRENT-OUTPUT D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- Nonlinearity $\pm 1/4$ LSB (Max)
- Settling Time $1.5 \mu s$ (Typ)
- No Laser Trimming Used In Fabrication
- Internal Range and Offset Scaling Resistors
- Guaranteed Monotonicity Over Temperature
- TTL or CMOS Logic Input Compatibility, Pin Selectable
- Low Power Consumption $130mW$ (Typ)
- Directly Pin Compatible with AD562

ORDERING INFORMATION†

NONLINEARITY @25°C (LSB)	PMI MODEL NO.	TEMP. RANGE
$\pm 1/4$	PM562AV*	-55°C/+125°C
$\pm 1/2$	PM562BV*	-55°C/+125°C
$\pm 1/2$	PM562FV	-25°C/+85°C
$\pm 1/4$	PM562GV	0°C/+70°C
$\pm 1/2$	PM562HV	0°C/+70°C

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

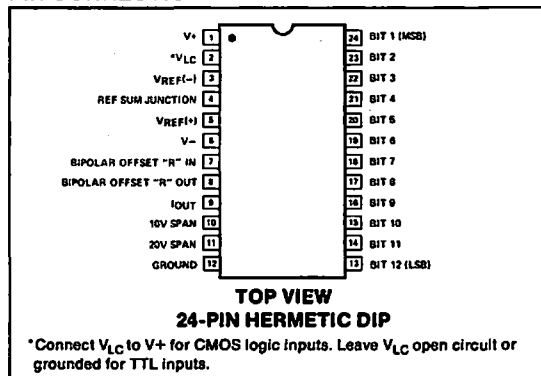
GENERAL DESCRIPTION

The PM-562 is a 12-bit monolithic multiplying digital-to-analog converter consisting of a reference current amplifier, an R-2R ladder network, range and offset scaling resistors, and 12 high-speed current switches. Improvements provided by the PM-562 include greater negative power supply range

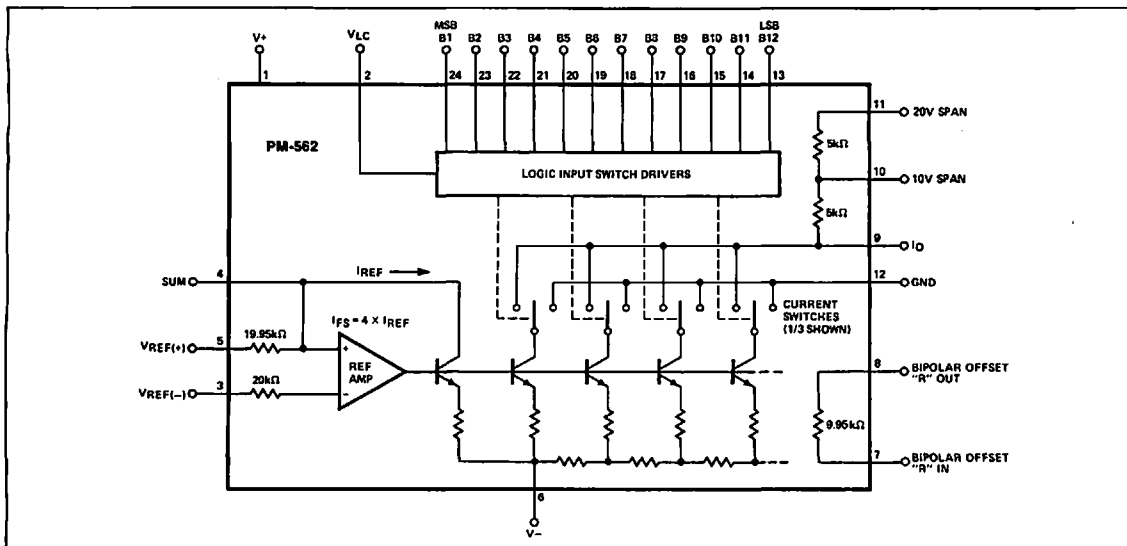
and increased output resistance. The PM-562 is pin compatible with the AD562.

A highly stable trim method; selective shorting of zener diodes, provides 13-bit accuracy without the need for laser trimming. Reliability of this trimming method has been proven in several other PMI products with many years of reliability history. Internal scaling resistors plus an external op amp simplifies construction in voltage output applications, while maintaining accuracy over wide operating temperature ranges. The PM-562 is recommended for 12-bit accuracy D/A applications where single-chip reliability, small size and low cost are primary considerations.

PIN CONNECTIONS



EQUIVALENT CIRCUIT



Manufactured under the following patent: 4,055,773.

**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature Range	
PM-562A/B	-55°C to +125°C
PM-562F	-25°C to +85°C
PM-562G/H	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation at $T_A = 125^\circ\text{C}$	1000mW
Lead Temperature (Soldering, 60 sec)	300°C

Supply Voltage (V_+)	+18V
Supply Voltage (V_-)	-18V
V_+ to V_-	36V
Logic Inputs	V_- to (V_- plus 36V)
Summing Junction (Pin 4)	V_- to V_+
CMOS/TTL Threshold (Pin 2)	V_- to V_+
I_{OUT} (Pin 9)	-5V to +18V
Span Resistors	36V

ELECTRICAL CHARACTERISTICS at $V_+ = 5V$, $V_- = -15V$, $V_{REF}(+) = +10.0000V$, $V_{REF}(-) = 0V$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-562A/G			PM-562B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution	N	$T_A = \text{Full Range}$	12	—	—	12	—	—	Bits
Monotonicity		$T_A = \text{Full Range}$	12	—	—	12	—	—	Bits
Nonlinearity	NL		—	—	$\pm 1/4$	—	—	$\pm 1/2$	LSB
Differential Nonlinearity	DNL		—	—	$\pm 1/2$	—	—	$\pm 1/2$	LSB
Settling Time	t_s	To $\pm 1/2$ LSB, all bits ON or OFF	—	1.5	—	—	1.5	—	μs
Output Voltage Compliance	V_{OC}		— +10/-1.5	—	—	— +10/-1.5	—	—	V
Full-Scale Output Current Range	I_{FR}	$V_{REF}(+) = +10.0000V$ Unipolar $R_2 = 50\Omega$ Bipolar	-1.6 ± 0.8	-2.0 ± 1.0	-2.4 ± 1.2	-1.6 ± 0.8	-2.0 ± 1.0	-2.4 ± 1.2	mA
Zero-Scale Current	I_{ZS}	All bits OFF	—	.005	0.05	—	.005	0.05	%FS
Output Resistance	R_O		—	2	—	—	2	—	M Ω
Output Capacitance	C_O		—	30	—	—	30	—	pF
Reference Input Impedance	Z_{IN}	Pin 5	—	20	—	—	20	—	k Ω
Gain Error	I_{FSE}	$R_2 = 50\Omega$, (Note 1)	—	± 0.2	—	—	± 0.2	—	%FS
Bipolar Zero-Scale Error	I_{BZSE}	$R_1 = 50\Omega$, (Note 1)	—	± 0.1	—	—	± 0.1	—	%FS
Full-Scale Gain Adjustment Range	ΔI_{FSR}	$R_2 = 100\Omega$ Trimpot, (Note 1)	—	± 0.25	—	—	± 0.25	—	%FS
Bipolar Zero-Scale Adjustment Range	ΔI_{BZSR}	$R_1 = 100\Omega$ Trimpot, (Note 1)	—	± 0.25	—	—	± 0.25	—	%FS
Power Supply Gain Sensitivity	$+P_{SS}$ $-P_{SS}$	$V_+ = 5V$ or $V_+ = 15V$ $V_- = -15V$	—	—	2 8	—	—	2 6	ppmFS/%
Supply Current	I_+ I_-	$V_+ = 4.75V$ to $15.8V$ $V_- = -15V \pm 10\%$	—	5 -7	18 -25	—	5 -7	18 -25	mA
TTL Logic Input Voltage	V_{IH} V_{IL}	Pin 2 Open Circuit	2.0	—	— 0.8	2.0	—	— 0.8	V
CMOS Voltage Logic Input	V_{IH} V_{IL}	Pin 2 tied to Pin 1	70	—	— 30	70	—	— 30	% V_+



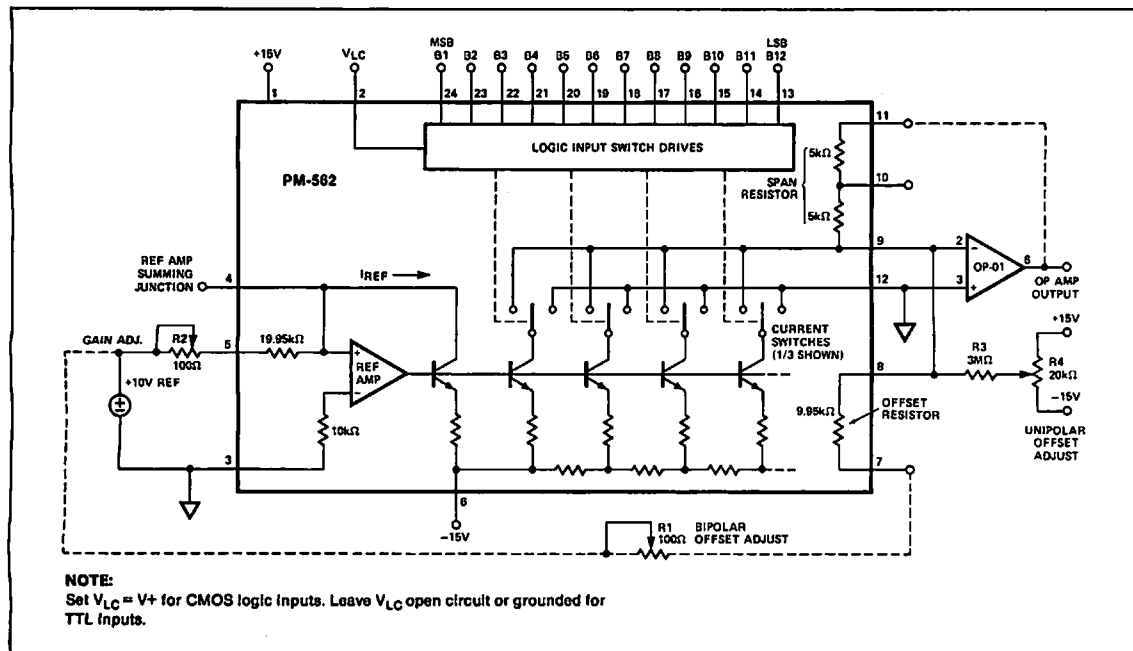
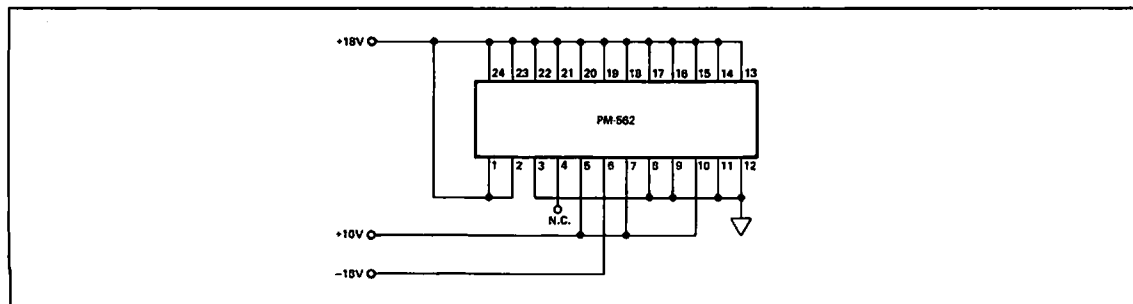
ELECTRICAL CHARACTERISTICS at $V^+ = 5V$, $V^- = -15V$, $V_{REF} (+) = +10.0000V$, $V_{REF} (-) = 0V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for PM-562A/B, $-25^\circ C \leq T_A \leq +85^\circ C$ for PM-562F, $0^\circ C \leq T_A \leq +70^\circ C$ for PM-562G/H, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-562A/G			PM-562B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Zero-Scale Temperature Coefficient	$TC_{I_{ZS}}$	Unipolar Leakage Current Change (Note 2)	—	—	2	—	—	2	ppmFS/ $^\circ C$
Bipolar Zero-Scale Temperature Coefficient	$TC_{I_{BZS}}$	Bipolar (Note 2)	—	—	4	—	—	4	ppmFS/ $^\circ C$
Full-Scale Gain Temperature Coefficient	$TC_{I_{FS}}$	Excludes V_{REF} (Note 2)	—	—	5	—	—	5	ppmFS/ $^\circ C$
Differential Nonlinearity Temperature Coefficient	TC_{DNL}	(Note 2)	—	1	—	—	2	—	ppmFS/ $^\circ C$

NOTES:

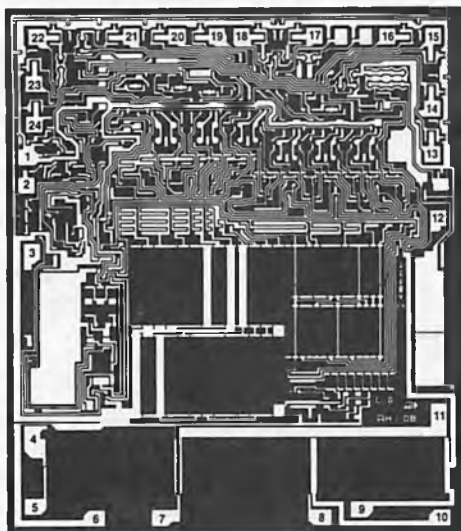
1. See connection diagram.

2. Guaranteed by design.

CONNECTION DIAGRAM**BURN-IN CONFIGURATION**



DICE CHARACTERISTICS



DIE SIZE 0.163×0.142 inch, 23,146 sq. mils
(4.140×3.607 mm, 14,933 sq. mm)

- | | |
|---------------------------|------------------|
| 1. V_+ | 13. BIT 12 (LSB) |
| 2. V_{LC} | 14. BIT 11 |
| 3. $V_{REF} (-)$ | 15. BIT 10 |
| 4. REF SUM JUNCTION | 16. BIT 9 |
| 5. $V_{REF} (+)$ | 17. BIT 8 |
| 6. V_- | 18. BIT 7 |
| 7. BIPOLAR OFFSET "R" IN | 19. BIT 6 |
| 8. BIPOLAR OFFSET "R" OUT | 20. BIT 5 |
| 9. I_{OUT} | 21. BIT 4 |
| 10. 10V SPAN | 22. BIT 3 |
| 11. 20V SPAN | 23. BIT 2 |
| 12. GROUND | 24. BIT 1 (MSB) |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = 5V$, $V_- = -15V$, $V_{REF} = 10.0000V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-562G LIMITS	UNITS
Nonlinearity	NL		$\pm 1/2$	LSB
Differential Nonlinearity	DNL		$\pm 1/2$	LSB
Zero-Scale Current	I_{ZS}	All Bits OFF	0.05	%FS
Full-Scale Output Current Range	I_{FR}	$I_{REF} = 0.5mA$ Unipolar	-1.6/-2.4	mA
Logic Input High	V_{IH}	$I_{IH} = 100nA$	2	V
Logic Input Low	V_{IL}	$I_{IL} = -100\mu A$	0.8	V
Positive Supply Current	I_+	$V_+ = 4.75$ to $15.8V$	18	mA
Negative Supply Current	I_-	$V_- = -13.5$ to $-16.5V$	-25	mA

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications bases on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = 5V$, $V_- = -15V$, $V_{REF} = 10.0000V$, $T_A = 25^\circ C$, unless otherwise noted.

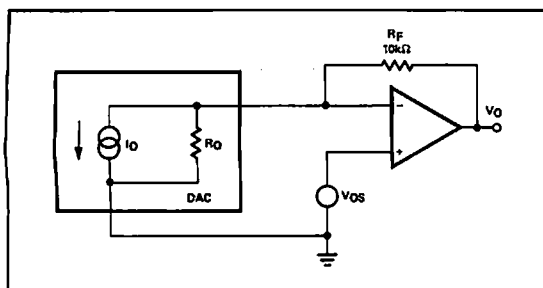
PARAMETER	SYMBOL	CONDITIONS	PM-562G TYPICAL	UNITS
Settling Time	t_s	to $\pm 1/2$ LSB, $V_O = 0V$	1.5	μs
Full-Scale Gain Temperature Coefficient	TCI_{FS}	Excludes V_{REF}	5	ppmFS/ $^\circ C$
Output Voltage Compliance	V_{OC}		-1.5/+10	V
Output Resistance	R_O		2	$M\Omega$
Output Capacitance	C_O		30	pF
Power Supply Gain Sensitivity	$+P_{SS}$	$V_+ = +5V$ or $+15V$	2	ppmFS/%
Power Supply Gain Sensitivity	$-P_{SS}$	$V_- = -15V$	6	ppmFS/%

APPLICATIONS INFORMATION

R_O EFFECT ON ACCURACY

The D/A converter equivalent circuit and output voltage equations show that a low output resistance (R_O) can provide a significant error term due to V_{OS} drift of the output amplifier. Note that the higher R_O (2M Ω) offered by the PM-562 gives an apparent V_{OS} drift that is one-half as large as that resulting from the 6.6k Ω R_O of the standard AD562 when using a 10k Ω span resistor (R_F).

$$\begin{aligned}\Delta V_O &= \Delta I_O R_F + \Delta V_{OS} \\ \text{Since: } \Delta I_O &= \Delta V_{OS} / R_O \\ \text{Then: } \Delta V_O &= \Delta V_{OS} (R_F / R_O + 1)\end{aligned}$$



LAYOUT SUGGESTIONS

Good layout practice appropriate for a 12-bit resolution analog system provides the overriding guideline. Power supplies should have small high frequency noise content. The V_- (-15V) supply should be the cleanest since it has the most direct effect on I_{OUT} . The PM-562 should have bypass capacitors on both V_+ and V_- supplies. A tantalum or electrolytic 1 to 10 micro Farad in parallel with a ceramic 0.01 micro Farad bypass capacitor adequately attenuate high frequency supply noise.

The ground line between Pin-3 and Pin-12 should not conduct any other current paths. Placing the common ground point at Pin-12 provides good results. Pin-9 is the most sensitive node to high frequency noise pickup. Keep the signal path between Pin-9 and the current-to-voltage converter (op amp or resistor) as short as possible.

LOGIC INTERFACING (TTL OR CMOS)

The PM-562 digital inputs (BIT 1 through BIT 12) can be programmed by the V_{LC} (Pin-2) for TTL or CMOS logic input compatibility.

For TTL input compatibility leave Pin-2 open circuit or ground it to Pin-12. The logic threshold trip point stays at 1.4V for V_+ set anywhere from 4.75 to 15.8V.

For CMOS input compatibility tie V_{LC} (Pin-2) to V_+ . This establishes the CMOS Logic threshold trip point at 1/2 of V_+ . Therefore V_+ should be set to the same V_{DD} voltage used by the CMOS driving logic.

MULTIPLYING MODE

The output current of the PM-562 is the product of the reference voltage input and the number represented by the digital input code divided by 4096. The reference voltage V_{REF} (+) must be positive with respect to V_{REF} (-). The PM-562 typically maintains 12-bit linearity with reference voltages as small as one volt. Reference signal feedthrough is typically 60dB down at 10kHz with a digital input of zero. The DAC output typically takes 20 microseconds to settle to within 1/2 LSB for a 5 volt step on the reference input. The small signal bandwidth for a 100mVpp reference input signal is typically 65kHz, and the typical large signal bandwidth for a 5Vpp reference input signal is 20kHz.

UNIPOLAR OPERATION (0 to +10V OUTPUT)

Figure 1 shows the simplest unipolar setup for 0 to +10V operation. The output should be buffered since the output resistance is 5k Ω . The digital input code is complemented in this configuration. That is, binary "0" in produces +10V full-scale out. And all binary one's in produces 0V out.

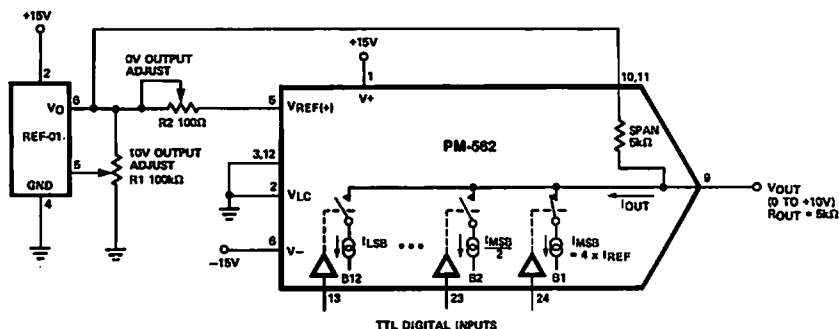
Figure 2 shows the best configuration to achieve a 0V to 10V output digital-to-analog converter. In this configuration digital "0" in produces 0V out. All one's in produces 10V out.

Calibration of Figure 2 is accomplished by placing digital "0" on all input bits and adjusting R1 until 0V appears at V_{OUT} . Next the span (or full-scale) is adjusted by R2 for an output voltage of 9.9976V.

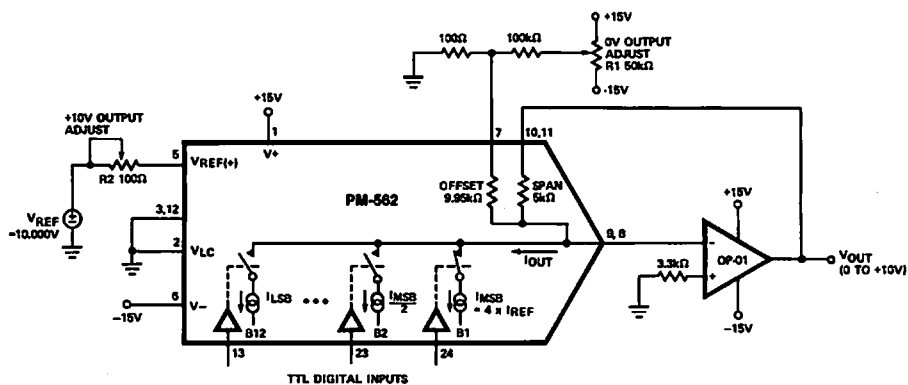
BIPOLAR OPERATION ($\pm 10V$ OUTPUT)

The bipolar configuration of Figure 3 provides positive and negative output voltage under control of one's complement digital input coding. Calibration is accomplished by turning all bits OFF (digital zero input code) and adjusting trimmer R1 for -10.000V output. Next turn ON the MSB (digital 1000 0000 0000 input code) and adjust R2 for 0.0000V.

This circuit can easily be converted to $\pm 5V$ output by connecting Pin-10 to the OP-01 output, making the span resistor 5k Ω .

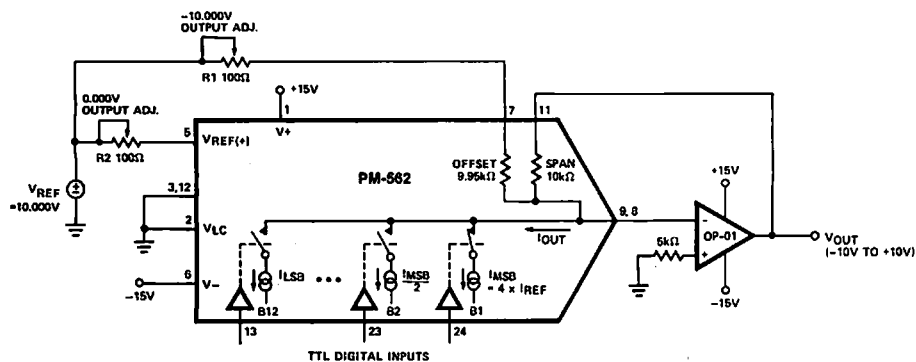
**NOTES:**

1. This simple configuration presents a high output resistance of $8k\Omega$.
2. Calibration Procedure: First set digital inputs B_1 thru B_{12} to digital zero and adjust R_1 until $V_{OUT} = 10.0000V$. Next set digital inputs B_1 thru B_{12} to digital one's and adjust R_2 until $V_{OUT} = 0.0000V$. Use a high input resistance DVM to calibrate to avoid resistor divider error.
3. Bypass $V+$ and $V-$ supplies with $0.01\mu F$ in parallel with $1\mu F$ capacitors.

FIGURE 1: Unbuffered Unipolar 0 to +10V Output**NOTES:**

1. Calibration Procedure: First set digital inputs B_1 thru B_{12} to digital zero and adjust R_1 until $V_{OUT} = 0.0000V$. Next set digital inputs B_1 thru B_{12} to digital one's and adjust R_2 until $V_{OUT} = 9.9876V$.
2. Bypass $V+$ and $V-$ supplies with $0.01\mu F$ in parallel with $1\mu F$ capacitors.

FIGURE 2: +10V Unipolar Voltage Output



NOTES:

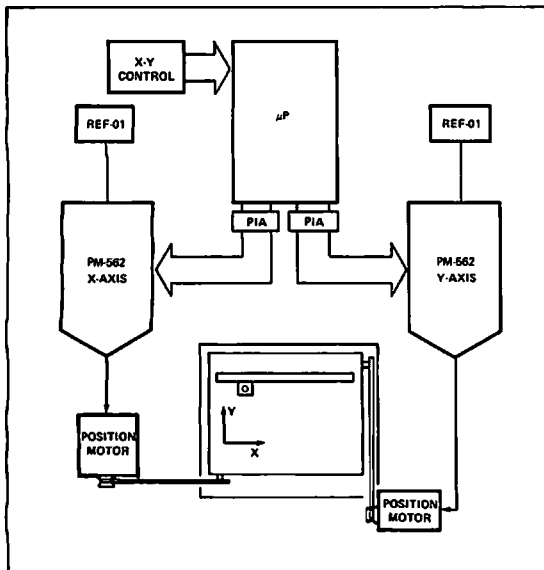
1. **Calibration Procedure:** Set $V_{REF} = 10.0000V$. Next set digital inputs B_1 thru B_{12} to digital zero and adjust R_1 until $V_{OUT} = -10.0000V$. Set digital inputs B_1 thru B_{12} to 1000 0000 0000 (i.e. only turn ON MSB)

and adjust R_2 until $V_{OUT} = 0.0000V$.

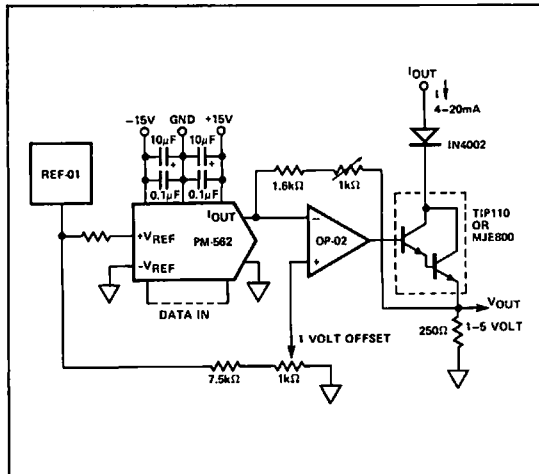
2. Bypass V^+ and V^- supplies with $0.01\mu\text{F}$ in parallel with $1\mu\text{F}$ capacitors.

FIGURE 3: $\pm 10\text{V}$ Bipolar Voltage Output

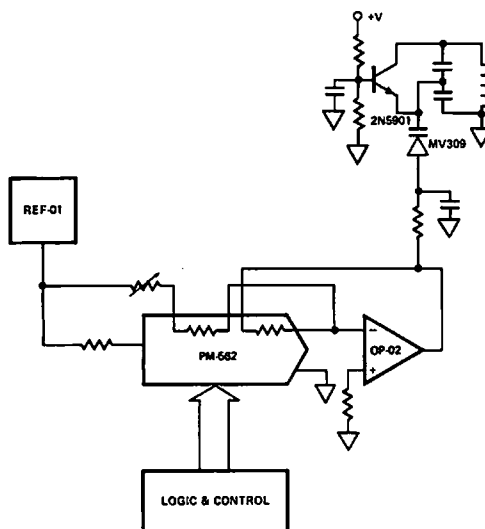
PRECISION X-Y POSITIONING SYSTEM



4-20mA TRANSMITTER



DIGITALLY CONTROLLED R.F. OSCILLATOR





PM-7224

8-BIT CMOS D/A CONVERTER WITH VOLTAGE OUTPUT

Precision Monolithics Inc.

FEATURES

- Internal Output Amplifier
- Double-Buffered Data Inputs
- Microprocessor Compatible
- Adjustment Free ($\pm 1/2$ LSB Total Error)
- Guaranteed Monotonicity
- Single or Dual Supply Operation
- Space Saving 0.3" Wide 18-Pin Dip
- TTL/5V CMOS Compatible
- Fast Data Load, $t_{WR} = 90$ ns (All Temperatures)
- Single Specification Table for Both Dual and Single Power Supply Operation

APPLICATIONS

- Process/Industrial Controls
- Automatic Test Equipment
- Op Amp Offset Adjust
- Gain Adjust
- Attenuation
- Medical Equipment

ORDERING INFORMATION†

TOTAL UNADJUSTED ERROR	PACKAGE: 18-PIN		
	MILITARY* TEMP	INDUSTRIAL TEMP	COMMERCIAL TEMP
$\pm 1/2$ LSB	PM7224AX	PM7224EX	PM7224GP
± 1 LSB	PM7224BX	PM7224FX	PM7224HP

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

CROSS REFERENCE

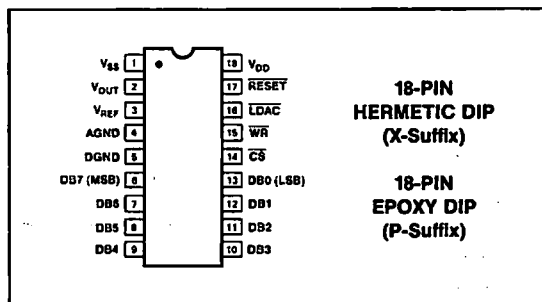
PMI	ADI	TEMPERATURE RANGE
PM7224AX PM7224BX	AD7224UQ AD7224TQ	MIL
PM7224EX PM7224FX	AD7224CQ AD7224BQ	IND
PM7224GP PM7224HP	AD7224LN AD7224KN	COM

GENERAL DESCRIPTION

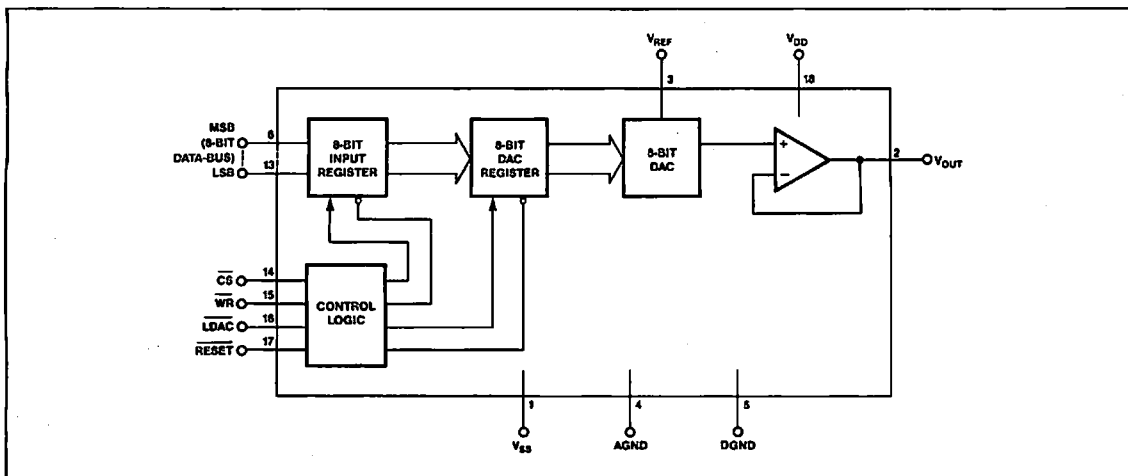
The PM-7224 is an improved version of the AD7224, which is an 8-bit, double-buffered, voltage output, CMOS digital-to-analog converter. It consists of a CMOS output amplifier, two 8-bit registers, interface control logic, and an R-2R resistor ladder network on a single monolithic chip.

PC board-space and costs are greatly reduced by eliminating the need for an external amplifier and associated trim circuitry.

PIN CONNECTIONS



FUNCTIONAL BLOCK DIAGRAM





Excellent zero code error is achieved for both single and dual supply operation by laser trimming the offset during manufacturing. The internal amplifier can deliver up to 5mA into a 2k Ω load and can drive a 3300pF capacitive load.

A reset pin simplifies system power-up and/or calibration cycles. It allows the DAC to momentarily be reset to 0V and function like a zero-override when both registers are transparent; however, the DAC output will remain at 0V when both registers are latched.

The PM-7224 can be operated with either a single or dual supply; however, zero code error can be improved using dual supplies.

PMI's advanced oxide-isolated, silicon-gate, CMOS process allows the PM-7224's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly-stable thin-film R-2R resistor ladder, aids in the PM-7224's excellent full-scale and zero-code error temperature coefficients. It also results in an inherently reliable DAC and output amplifier.

The PM-7224 is a CMOS monolithic chip that fits into a space saving 18-pin, 0.3" wide, DIP package. With faster AC timing and tighter single and dual supply operation specifications, it is an improved replacement for the AD7224.

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} to AGND or DGND		-0.3V, +17V
V_{SS} to AGND or DGND		-7V, V_{DD}
V_{DD} to V_{SS}		-0.3V, +24V
AGND to DGND		-0.3V, V_{DD}
Digital Input Voltage to DGND		-0.3V, V_{DD}
V_{REF} to AGND		-0.3V, V_{DD}
V_{OUT} to AGND (Note 1)		V_{SS} , V_{DD}
Power Dissipation (any package) to $+75^\circ\text{C}$		450mW
Derates above $+75^\circ\text{C}$ by		6.0mW/ $^\circ\text{C}$
Operating Temperature		
Military, AX/BX		-55°C to $+125^\circ\text{C}$
Industrial, EX/FX		-25°C to $+85^\circ\text{C}$
Commercial, GP/HP		0°C to $+70^\circ\text{C}$
Dice Junction Temperature		$+150^\circ\text{C}$
Storage Temperature		-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)		$+300^\circ\text{C}$

NOTES:

1. Outputs may be shorted to AGND provided the package power dissipation is not exceeded. Typical output short circuit current to AGND is 50mA.
2. The digital inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep device in conductive foam at all times until ready for use.
3. Use proper anti-static handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: $V_{DD} = +11.4\text{V}$ to $+16.5\text{V}$; $V_{SS} = -5\text{V} \pm 10\%$; AGND = DGND = 0V; $V_{REF} = +2\text{V}$ to ($V_{DD} - 4\text{V}$); or SINGLE SUPPLY: $V_{DD} = +15\text{V} \pm 5\%$; $V_{SS} = \text{AGND} = \text{DGND} = 0\text{V}$; $V_{REF} = +10\text{V}$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ apply for PM-7224AX/BX; $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ apply for PM-7224EX/FX; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for PM-7224GP/HP, unless otherwise noted.

			PM-7224			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		8	—	—	Bits
Total Unadjusted Error (Note 1)	TUE	PM-7224A/E/G PM-7224B/F/H	— —	— —	±1/2 ±1	LSB
Relative Accuracy	INL	PM-7224A/E/G PM-7224B/F/H	— —	— —	±1/2 ±1	LSB
Differential Nonlinearity (Note 2)	DNL	PM-7224A/E/G PM-7224B/F/H	— —	— —	±1/2 ±1	LSB
Full Scale Error	G _{FSE}	PM-7224A/E/G PM-7224B/F/H	— —	— —	±1/2 ±1	LSB
Full Scale Temperature Coefficient (Note 3)	T _{CGFS}		—	±1	±20	ppm/°C
Zero Code Error	V _{ZSE}	DUAL SUPPLY: PM-7224A/E/G	—	—	±5	mV
		PM-7224B/F/H	—	—	±20	
		SINGLE SUPPLY: PM-7224A/E/G	—	—	±10	mV
		PM-7224B/F/H	—	—	±20	
Zero Code Error Temperature Coefficient (Note 3)	TCV _{ZS}		—	±10	—	μV/°C



Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: $V_{DD} = +11.4V$ to $+16.5V$; $V_{SS} = -5V \pm 10\%$; $AGND = DGND = 0V$; $V_{REF} = +2V$ to $(V_{DD} - 4V)$; or SINGLE SUPPLY: $V_{DD} = +15V \pm 5\%$; $V_{SS} = AGND = DGND = 0V$; $V_{REF} = +10V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7224AX/BX; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7224EX/FX; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7224GP/HP, unless otherwise noted. (Continued)

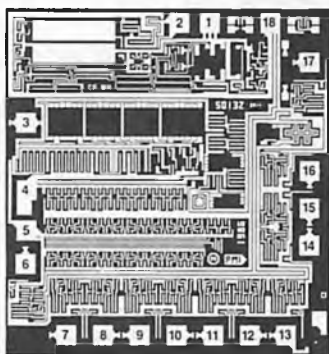
			PM-7224			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUT						
Voltage Range (Note 4)		DUAL SUPPLY ONLY	2	—	(V _{DD} − 4)	V
Input Resistance	R _{IN}		8	—	—	kΩ
Input Capacitance (Note 3)	C _{IN}	Digital Inputs = all 1's	—	—	100	pF
DIGITAL INPUTS						
Digital Input High	V _{INH}		2.4	—	—	V
Digital Input Low	V _{INL}		—	—	0.8	V
Input Current	I _{IN}	V _{IN} = 0V or V _{DD}	—	—	±1	μA
Input Capacitance (Note 3)	C _{IN}		—	—	8	pF
Input Coding				BINARY		
POWER SUPPLIES						
Power Supply Rejection Ratio	PSRR		—	—	0.005%	%/%
Positive Supply Current (Note 5)	I _{DO}	T _A = +25°C T _A = Full Temp Range	— —	— —	4 6	mA
Negative Supply Current (Note 5)	I _{SS}	DUAL SUPPLY ONLY T _A = +25°C T _A = Full Temp Range	— —	— —	3 5	mA
DYNAMIC PERFORMANCE						
V _{OUT} Slow Rate (Note 3)	SR		2.5	—	—	V/μS
V _{OUT} Settling Time Positive or Negative (Note 3, 6)	t _S		—	—	5	μS
Digital Feedthrough (Note 3)	Q		—	10	—	nVs
Minimum Load Resistance	R _{L(MIN)}	V _{OUT} = +10V	2	—	—	kΩ
SWITCHING CHARACTERISTICS (Note 3)						
Chip Select/Load DAC Pulse-Width	t ₁		90	—	—	ns
Write/Reset Pulse-Width	t ₂		90	—	—	ns
Chip Select/Load DAC to Write Setup Time	t ₃		0	—	—	ns
Chip Select/Load DAC to Write Hold Time	t ₄		0	—	—	ns
Data Valid to Write Setup Time	t ₅		90	—	—	ns
Data Valid to Write Hold Time	t ₆		10	—	—	ns

NOTES:

- Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
- All devices guaranteed monotonic over the full operating temperature range.
- Guaranteed by design and not subject to production test.
- $V_{DD} - 4$ volts is the maximum reference voltage for the above specifications.
- $V_{IN} = V_{INL}$ or V_{INH} ; outputs unloaded.
- $V_{REF} = +10V$; to where output settles to 1/2 LSB.



DICE CHARACTERISTICS



DIE SIZE 0.094×0.099 inch, 9306 sq. mils
(2.39×2.52 mm, 6.0 sq. mm)

- | | |
|--------------|--------------|
| 1. V_{SS} | 10. DB3 |
| 2. V_{OUT} | 11. DB2 |
| 3. V_{REF} | 12. DB1 |
| 4. AGND | 13. DB0(LSB) |
| 5. DGND | 14. CS |
| 6. DB7(MSB) | 15. WR |
| 7. DB6 | 16. LDAC |
| 8. DB5 | 17. RESET |
| 9. DB4 | 18. V_{DO} |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

WAFER TEST LIMITS: DUAL SUPPLY: $V_{DD} = +11.4V$ to $+16.5V$; $V_{SS} = -5V \pm 10\%$; AGND = DGND = 0V; $V_{REF} = +2V$ to $(V_{DD} - 4V)$. SINGLE SUPPLY: $V_{DD} = +15V \pm 5\%$; $V_{SS} =$ AGND = DGND = 0V; $V_{REF} = +10V$; unless otherwise noted.

PM-7224GBC				
PARAMETER	SYMBOL	CONDITIONS	LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits
Total Unadjusted Error (Note 1)	TUE		± 1	LSB MAX
Relative Accuracy	INL		± 1	LSB MAX
Differential Nonlinearity (Note 2)	DNL		± 1	LSB MAX
Full Scale Error	G_{FSE}		± 1	LSB MAX
Zero Code Error	V_{ZSE}		± 20	mV MAX
REFERENCE INPUT				
Voltage Range (Note 3)	V_{REF}	DUAL SUPPLY ONLY	2 to $(V_{DD} - 4V)$	V
Reference Input Resistance	R_{IN}		8	k Ω MIN
DIGITAL INPUTS				
Digital Inputs High	V_{INH}		2.4	V MIN
Digital Inputs Low	V_{INL}		0.8	V MAX
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD}	± 1	μA MAX
Input Coding			BINARY	
POWER SUPPLIES				
Positive Supply Current (Note 4)	I_{DD}		4	mA MAX
Negative Supply Current (Note 4)	I_{SS}	DUAL SUPPLY ONLY	3	mA MAX

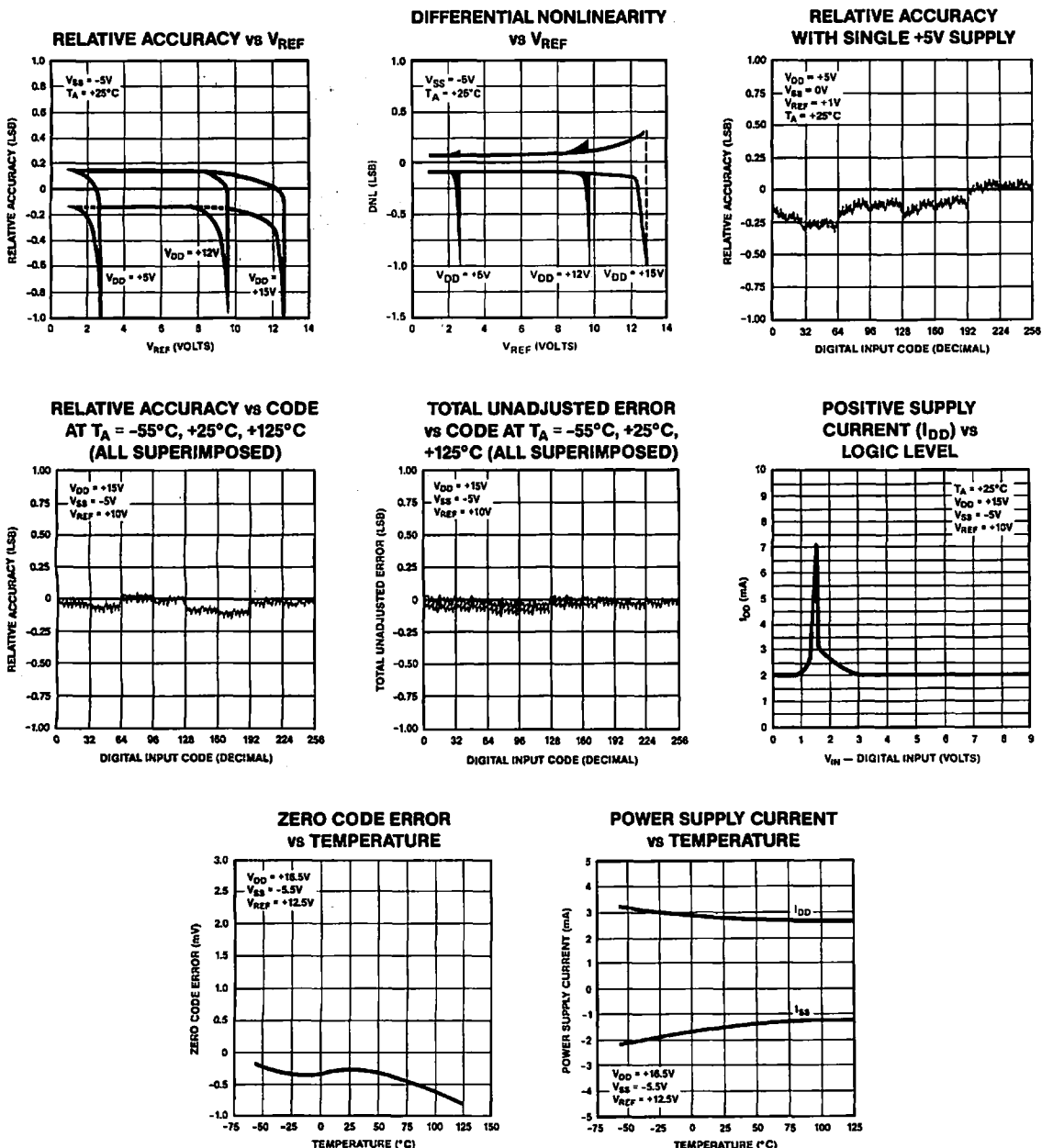
NOTES:

- Includes Full Scale Error, Relative Accuracy, and Zero Code Error
- All dice guaranteed monotonic over the full operating temperature range.
- $V_{DD} - 4$ volts is the maximum reference voltage for the above specifications.
- $V_{IN} = V_{INL}$ or V_{INH} ; output unloaded.

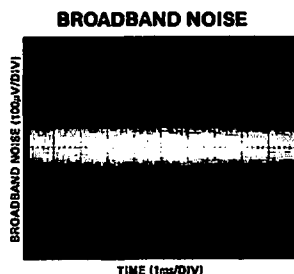
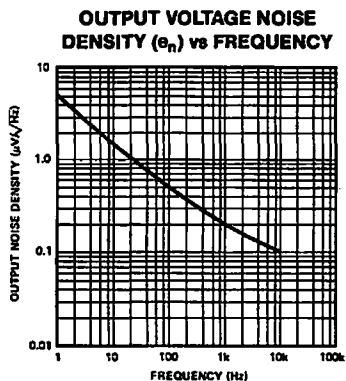
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



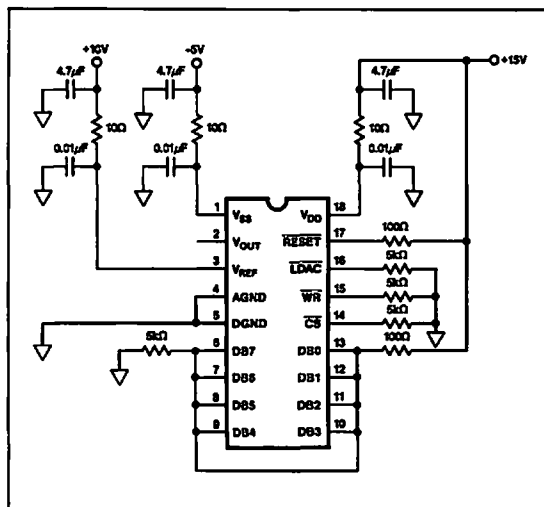
TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS



BURN-IN CIRCUIT



PARAMETER DEFINITIONS

TOTAL UNADJUSTED ERROR

This specification includes Full-Scale-Error, Relative Accuracy, and Zero-Code-Error. Ideal full scale output is $V_{REF} - 1 \text{ LSB}$, and 1 LSB is $V_{REF} \times (2^{-n})$.

DIGITAL FEEDTHROUGH

Digital feedthrough are the switching transients coupled to the output of the DAC due to a change in digital input code. It is expressed in nano-Volt-seconds and measured with $V_{REF} = 0V$.

Refer to PMI 1986 Data Book Section 11 for additional digital-to-analog converter definitions.

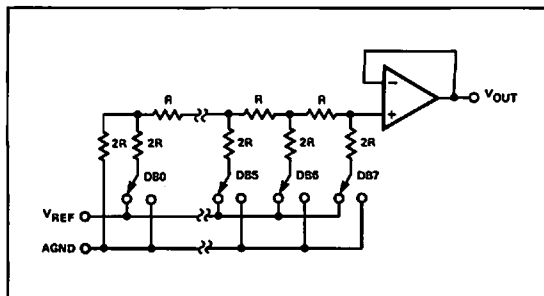
GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The PM-7224 contains an output buffer amplifier, a highly-stable, thin-film, R-2R resistor ladder network, 8-bit input and DAC registers, and interface control logic. Also included are eight single-pole double-throw NMOS transistor switches. These transistors were designed to switch between V_{REF} and AGND and are controlled by the digital input code.

A simplified circuit of the R-2R resistor ladder and output is illustrated in Figure 1. The ladder is shown connected to the amplifier in the voltage-mode configuration. The advantages gained in operating the ladder in the voltage mode are two-fold: it allows the DAC to be operated with a single supply, and the ladder resistance/capacitance modulation encountered in the current mode configuration are eliminated. The modulation (caused by the varying digital code) is now presented to the low-impedance reference voltage source (most voltage reference output-impedances are low enough so that its output voltage will not be affected by the varying digital code). The

FIGURE 1: Simplified DAC Circuit Configuration. (Switches are shown for all "1's" on the digital inputs.)



amplifier's input terminal now "sees" a constant resistance/capacitance and thus, the output offset voltage modulation is eliminated. Also, digital glitches fed through the switch capacitance to the output will be greatly reduced; it will be absorbed by the low output-impedance of the external reference resulting in a "cleaner" output voltage.

Figure 1 also shows the amplifier configured to operate as a buffer amplifier resulting in no signal inversion from input to output (V_{REF} to V_{OUT}). Also, note that analog ground (AGND) is accessible and can be biased above digital ground (DGND) for some applications; more on this in the applications section under AGND biasing.

For proper operation, maximum V_{REF} should be limited to V_{DD} minus 4 volts. This means that in order to operate the DAC with +10V at the reference input terminal, V_{DD} must be at least +14V.

The voltage output equation is given by:

$$V_{OUT} = V_{REF} \times D/256$$

where D is the digital input code integer number that is between 0 and 255.

BUFFER AMPLIFIER SECTION

The R-2R resistor ladder network has a typical resistance of 10k Ω ; a 100k Ω load would cause a 23 LSB gain error. Therefore, in order to drive a 2k Ω load, the R-2R ladder was terminated with a stable CMOS buffer amplifier. The amplifier can drive 10 volts across a 2k Ω load delivering 5mA, and can easily drive a 3300pF capacitive load. The PM-7224's output can also withstand an indefinite short-circuit to AGND to typically 50mA. The output may also be shorted to any voltage between V_{DD} and V_{SS} ; however, care must be taken to not exceed the device maximum power dissipation.

The amplifier's output stage is an intrinsic NPN bipolar transistor. It is derived from the P⁻ well and the substrate. This transistor provides a low-impedance high-output current capability using only a small part of the chip area. The emitter of this NPN transistor is loaded with a 400 μ A NMOS current-source referenced to V_{SS} . This current is sunk into the negative supply allowing the amplifier's output to go directly to ground.

A simplified schematic of the output amplifier is shown in Figure 2. It shows the current-source connection between the NPN output transistor's emitter and V_{SS} . Figure 3 depicts a typical plot for the dual and single supply current sink capability of the DAC versus output voltage. Let's take a closer look at what happens to its behavior by referring to Figures 2 and 3.

It can be seen that with dual supplies the current-source is still in its high impedance (saturation) state when the output reaches 0 volts. This is due to the 5 volts (V_{SS}) across the current-source that is sinking the 400 μ amps. When $V_{SS} = 0$ volts, however, the current sink capability is reduced as the output voltage approaches 0 volts; the current-source is coming out of its saturation region and starts appearing resistive.

The amplifier's current-limiting and buffering abilities are achieved with an NMOS transistor and a series resistor, see

Figure 2. The transistor operates as a source follower driving the resistor and output transistor.

The amplifier's internal gain stages were designed so that they maintain sufficient gain over its common mode range; this results in good offset performance over the specified voltage range. In addition, the amplifier's offset voltage is laser-trimmed during the manufacturing process; this eliminates offset trimming by the user in most applications. The amplifier's offset is included in the data sheet under "total unadjusted error" specification.

FIGURE 2: Amplifier Output Stage

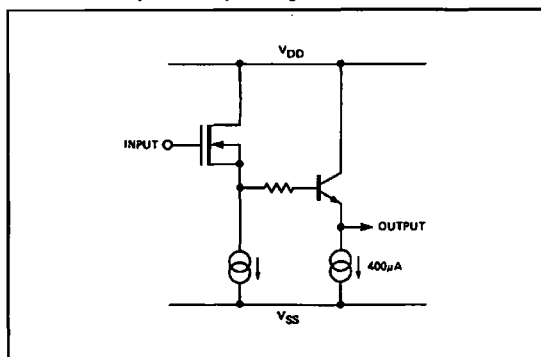
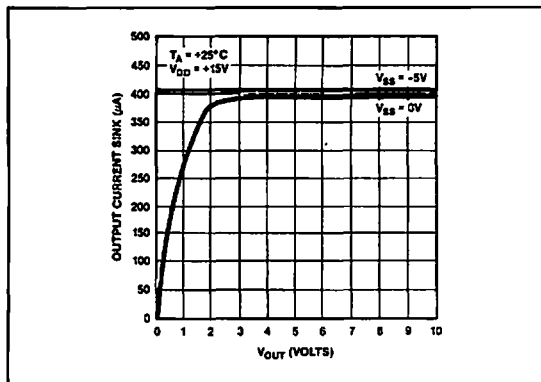


FIGURE 3: DAC Output Current Sink



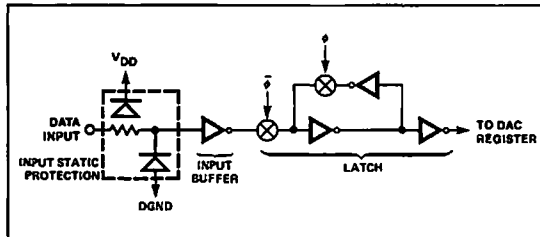
DIGITAL SECTION

The digital inputs are CMOS inverters. They were designed to convert TTL and 5V CMOS input logic levels into CMOS levels to drive the internal circuitry. A simple internal 5V regulator is used to ensure the high speed timing requirements.

The PM-7224's digital inputs are TTL and CMOS (5V) compatible between the V_{DD} range of +11.4V to +16.5V. As shown in Figure 4, these inputs are protected from electrostatic-discharge and build-up with two internal distributed-diodes; they are connected between V_{DD} and DGND. Each input has a typical input current of less than 1nA.

Figure 4 also shows the equivalent logic circuit for the digital data input register structure. This circuit drives the DAC register. The digital controls ϕ and $\bar{\phi}$ shown are controlled by the external $\overline{WR}$, and $\overline{CS}$ signals.

FIGURE 4: Input Register Structure



INTERFACE CONTROL LOGIC SECTION

Figure 5 shows the PM-7224's input control logic structure with its input register and DAC register, also shown is the equivalent logic circuitry. The $\overline{WR}$ signal is required when loading data into either register and is used in conjunction with either $\overline{CS}$ or $\overline{LDAC}$. $\overline{CS}$ loads data into the input register, and $\overline{LDAC}$ loads data into the DAC register. Data is latched in the input register on the rising edge of the $\overline{WR}$ pulse. The DAC's analog output voltage is determined by the data contained in the DAC register. See Table 1.

TABLE 1

RESET	LDAC	WR	CS	FUNCTION
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register is Transparent
H	H	$\uparrow$	L	Input Register is Latched
H	L	$\uparrow$	L	DAC Register is Transparent
H	L	$\uparrow$	H	DAC Register is Latched
L	X	X	X	Both Registers Loaded with all Zeros
$\uparrow$	H	H	H	Both Registers Loaded with all Zeros and the Output Remains at Zero
$\uparrow$	L	L	L	Both Registers are Transparent (output follows the input)

H = High State; L = Low State; X = Don't Care

Table 1 shows that the DAC is transparent when $\overline{WR}$, $\overline{CS}$, and $\overline{LDAC}$ are low, and the input register is transparent when $\overline{WR}$ and $\overline{CS}$ only are low. Also shown is the data being latched into the input register on the rising edge of the $\overline{WR}$ signal.

Also provided with the PM-7224 is a $\overline{RESET}$ pin as shown in Figure 5. A low $\overline{RESET}$ signal will reset both registers to zero. If

the DAC is in the transparent mode, the DAC output will go to 0V for as long as the reset line remains low. If the DAC is in the latched mode, the output will go to 0V (and remain there) on the rising edge of the reset signal.

Figure 6 shows the PM-7224 write timing diagram.

FIGURE 5: Input Control Logic

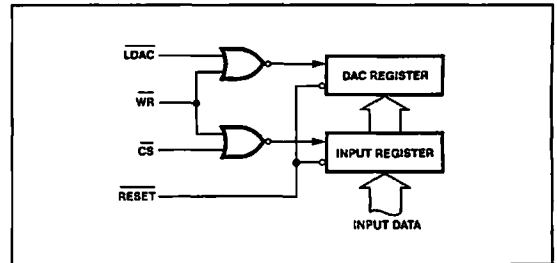
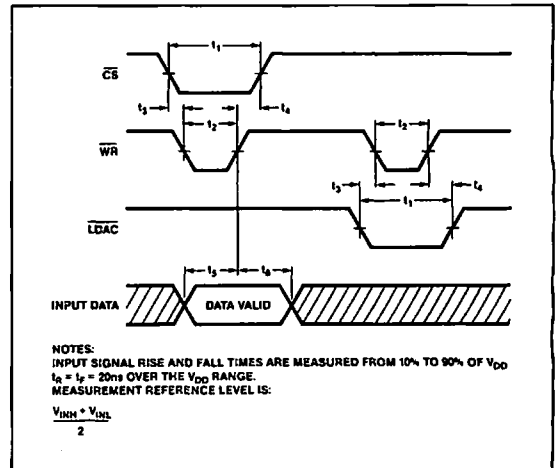


FIGURE 6: Write Timing Diagram



APPLICATIONS INFORMATION

POWER SUPPLY

The PM-7224 data sheet is specified with a dual or single power supply condition. The dual supply specifications are specified with a positive supply (V_{DD}) range of +11.4V to +16.5V and a negative supply (V_{SS}) of -5V. The specified reference voltage (V_{REF}) under these conditions range from +2V to $V_{DD} - 4V$. For those applications requiring +10 volts at the output ($V_{REF} = +10V$), V_{DD} must be +14V minimum to meet data sheet limits.

The specified V_{REF} for the single supply specifications is +10V. V_{REF} voltage limitation of $V_{DD} - 4V$ for dual or single power supply applications must be observed. This will ensure that the PM-7224's multiplying capabilities are preserved.

Although the PM-7224 can operate well with either a single or dual power supply, improved zero-code error can be achieved by using dual supplies.

DYNAMIC PERFORMANCE

The PM-7224's settling time is limited by the internal amplifier's slew rate; however, it sports an impressive settling time of 5 μ s using a dual or single power supply. Settling time is not affected by the DAC's output voltage polarity, positive or negative. The PM-7224 also has minimum signal overshoot or ringing.

AGND BIASING

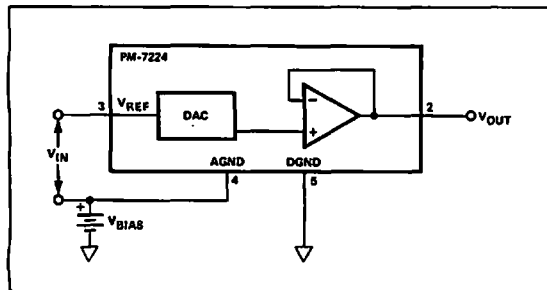
Some applications may require a DC offset voltage level at the DAC's output. This may be easily accomplished with the PM-7224; the desired DC offset voltage can be applied to the AGND pin as shown in Figure 7. The DAC's TTL/CMOS compatibility is not affected. Note that V_{DD} and V_{SS} must be referenced to DGND.

The DAC's output voltage expression under this condition is:

$$V_{OUT} = \text{AGND bias} + V_{IN} \times D/255$$

where AGND bias is the voltage level above DGND and D is the digital input code integer number that is between 0 and 255.

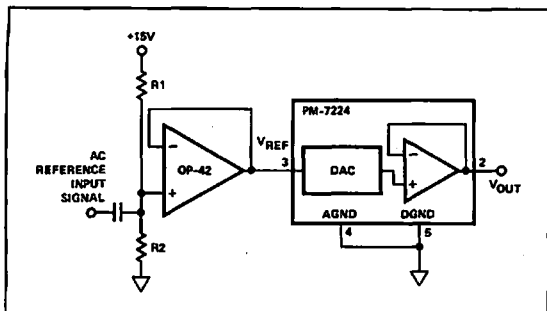
FIGURE 7: AGND Biasing Scheme



MULTIPLYING OPERATION

The PM-7224 has good multiplying capabilities if the reference input signal level is kept within +2V and $V_{DD} - 4V$, with V_{DD} of +16.5 V, the maximum input signal level is +12.5V; however, it is recommended that $V_{DD} = +15V \pm 5\%$ and the AC voltage swing between +2V and $V_{DD} - 4V$. The signal must be AC coupled and biased up with a voltage divider as shown in Figure 8. A buffer amplifier should be used to ensure that the DAC's V_{REF} impedance does not load the resistor divider, R1 and R2.

FIGURE 8: AC Signal Input Scheme

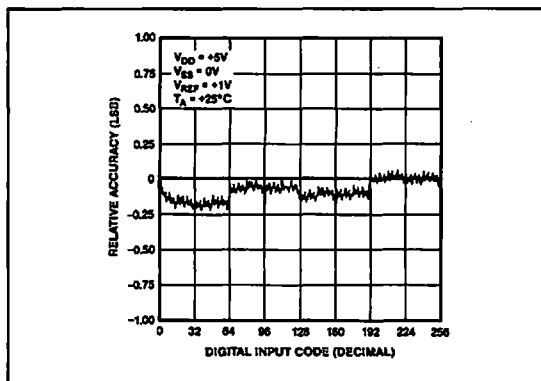


The V_{REF} small-signal frequency response ($-3dB$ bandwidth) for the PM-7224 is typically 1.5MHz. Its small-signal harmonic distortion is less than $-57dB$ at 1kHz and $-55dB$ at 100kHz.

+5V SINGLE SUPPLY OPERATION

Although a +5V performance specification table is not listed, the PM-7224 can operate well with only a single +5V supply (see Figure 9). This will then limit the reference input voltage level to a maximum of +1V; the $V_{DD} - 4V$ limitation must still be observed.

FIGURE 9: Relative Accuracy With Single +5V Operation



GENERAL GROUND MANAGEMENT

Digital transient voltages between AGND and DGND can appear as noise at the PM-7224's output. It is, therefore, recommended that AGND and DGND be tied together at the device socket; each ground is then brought out separately to their respective common ground points. A word of caution is worth mentioning here: ground loops can be created if both grounds are tied together at more than one location, i.e., at the device socket and back at the power supplies, or at any other location. These ground loops can cause noisy digital ground currents to flow through the analog ground paths and destroy its integrity. Analog ground should be maintained as a high quality ground.

If system requirements dictate the use of one common return line for each ground, then the DAC should be placed as close to the power supplies as possible. Also, for those systems that require both grounds be separated, two Schottky diodes should be tied in inverse parallel between AGND and DGND at the device socket.

POWER SUPPLY DECOUPLING

Power supply decoupling capacitors are important to suppress oscillations and noise transients from entering the system and causing system errors. Noise transients are generated from digital switching or switching power supplies; and oscillations on the power supply lines are caused by lead inductances combined with stray capacitance.

High and low frequency decoupling capacitors at the device socket is strongly recommended; a 0.01 μ F ceramic in parallel with a 1 to 10 μ F tantalum decoupling capacitors should be used.

BASIC APPLICATIONS

UNIPOLAR OPERATION

Figure 10 shows the PM-7224 configured to operate in the unipolar mode; the analog output voltage is of a single positive polarity only. Table 2 shows the code for this mode of operation.

FIGURE 10: Unipolar Operation

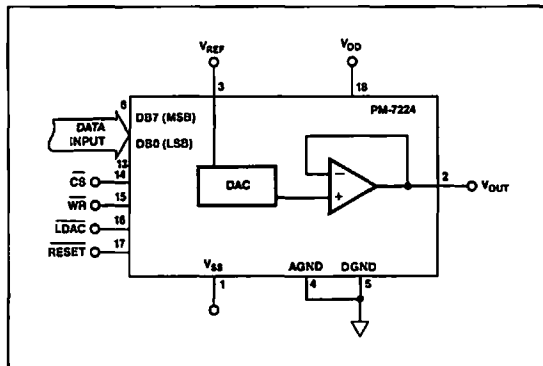


TABLE 2: Unipolar Code Table (Refer to Figure 10)

DAC DATA INPUT		ANALOG OUTPUT
MSB	LSB	
1	1 1 1 1 1 1 1	$+V_{REF} \left(\frac{225}{256} \right)$
1	0 0 0 0 0 0 1	$+V_{REF} \left(\frac{129}{256} \right)$
1	0 0 0 0 0 0 0	$+V_{REF} \left(\frac{128}{256} \right) = \frac{+V_{REF}}{2}$
0	1 1 1 1 1 1 1	$+V_{REF} \left(\frac{127}{256} \right)$
0	0 0 0 0 0 0 1	$+V_{REF} \left(\frac{1}{256} \right)$
0	0 0 0 0 0 0 0	0V

It shows no signal inversion between $+V_{REF}$ and V_{OUT} . Also note that the analog output voltage is equal to V_{REF} multiplied by the digital input code, hence, multiplying DAC.

The expression for 1 LSB and V_{OUT} is:

$$1 \text{ LSB} = V_{REF} \times 2^{-8}, \text{ or } V_{REF} \times 1/256$$

and

$$V_{OUT} = V_{REF} \times D/256$$

where D is the digital input integer between 0 and 255.

BIPOLAR OPERATION

Figure 11 illustrates the bipolar mode of operation for the PM-7224. This mode allows the output voltage to swing plus or minus and is determined by the digital input code; see Table 3 for $R1 = R2$. This configuration requires an external amplifier and two resistors.

The output voltage expression is given by:

$$V_{OUT} = ((1 + R2/R1) \times D/256 \times V_{REF}) - (R2/R1 \times V_{REF})$$

where D is the digital input code integer between 0 and 255. If $R1 = R2$, then V_{OUT} becomes:

$$V_{OUT} = (2 \times D/256 - 1) \times V_{REF}$$

To keep gain and offset errors at a minimum, $R1$ and $R2$ should be matched to $\pm 0.1\%$ and track over the operating temperature range of interest.

FIGURE 11: Bipolar Operation

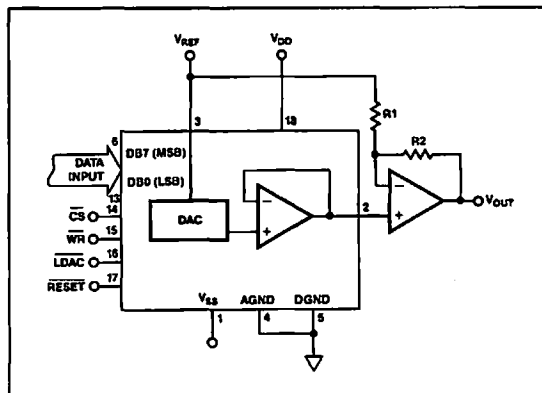


TABLE 3: Bipolar (Offset Binary) Code Table (Refer to Figure 11)

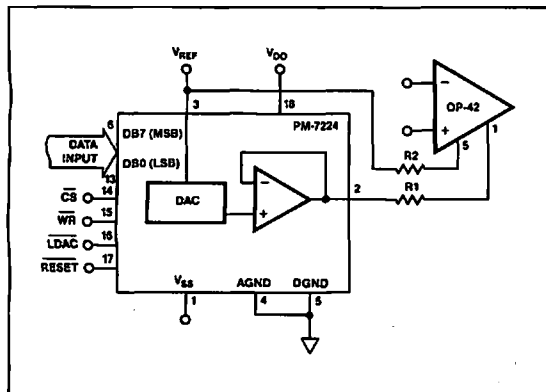
DAC DATA INPUT		ANALOG OUTPUT
MSB	LSB	
1	1 1 1 1 1 1 1	$+V_{REF} \left(\frac{127}{128} \right)$
1	0 0 0 0 0 0 1	$+V_{REF} \left(\frac{1}{128} \right)$
1	0 0 0 0 0 0 0	0V
0	1 1 1 1 1 1 1	$-V_{REF} \left(\frac{1}{128} \right)$
0	0 0 0 0 0 0 1	$-V_{REF} \left(\frac{127}{128} \right)$
0	0 0 0 0 0 0 0	$-V_{REF} \left(\frac{128}{128} \right) = -V_{REF}$

PROGRAMMABLE OP AMP OFFSET ADJUST

The PM-7224 can be used for op amp offset trim adjustments under microprocessor control. Offsets caused by temperature drifts can also be trimmed by the microprocessor during a periodic calibration cycle.

The PM-7224 uses the input offset voltage nulling pins normally provided on most amplifiers as shown in Figure 12. A fixed bias current is provided to pin 5 of the op amps offset null pin with $R2$, and $R1$ (connected to the DAC's voltage output pin) provides the variable current to pin 1.

FIGURE 12: Op Amp Offset Adjust (See Text)



For a plus or minus ($\pm$) offset adjust control, the current through R1 must equal the current through R2 when the PM-7224 is at half scale, binary code = 10000000.

The resistor values R1 and R2 should be chosen to give the required offset adjustment range desired. Lower values provide a larger range; however, resolution will be sacrificed. Reversing the op amp connections, pin 1 and 5, will reverse the offset adjustment direction.

Some op amps are not provided with offset adjustment pins. In these cases, the circuit configuration of Figure 13 can be used. Again, the current through resistor R4 must equal the current through R3 with the PM-7224 at half scale, digital code = 10000000. With the circuit components shown, the maximum adjustment range is $\pm 5\text{mV}$. Incremental adjustment resolution is $39\mu\text{V}$ per bit.

MICROPROCESSOR INTERFACING

Interfacing the PM-7224 to a microprocessor is simplified by virtue of its loading structure simplicity. Data from the processor is loaded into the DAC by use of only two control lines, the write strobe ($\overline{WR}$) and chip select ($\overline{CS}$). The data is then output with

the **WR** and **LDAC** signal. Figures 14 through 17 show various popular microprocessor interface configurations.

FIGURE 14: PM-7224 to 8085A Interface (Only digital interface portion of PM-7224 shown for clarity.)

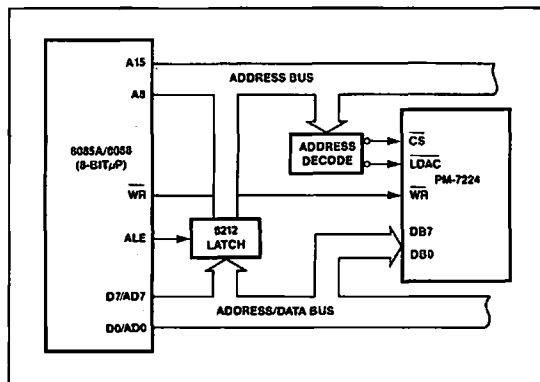


FIGURE 15: PM-7224 to Z-80 Interface (Only digital interface portion of PM-7224 shown for clarity.)

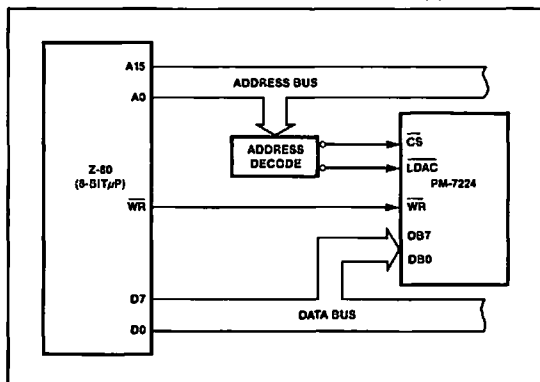


FIGURE 13: Alternate Offset Adjust (See Text)

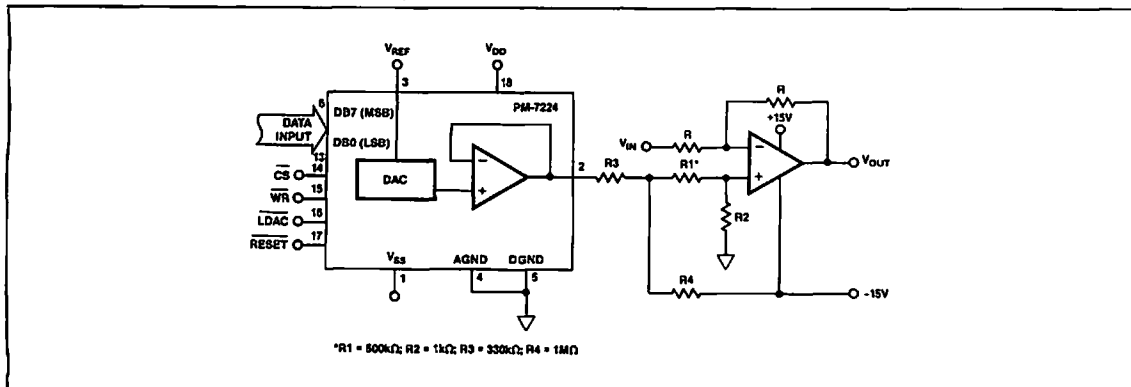


FIGURE 16: PM-7224 to 6809 Interface (Only digital interface portion of PM-7224 shown for clarity.)

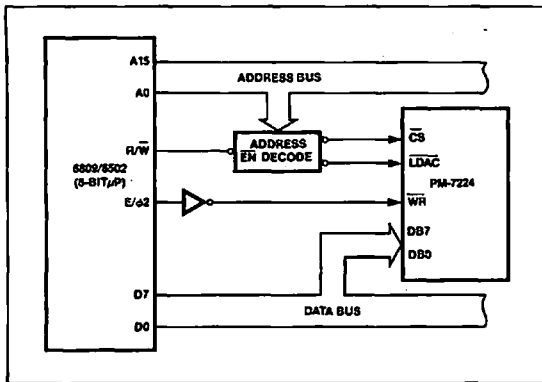
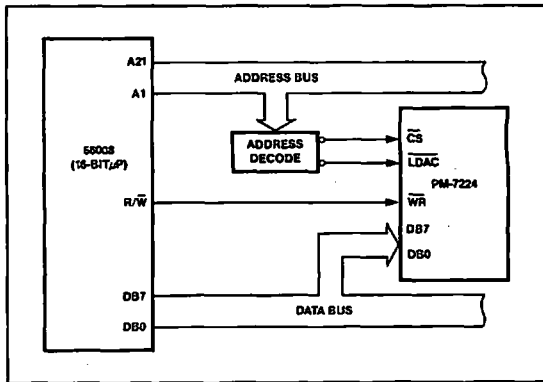


FIGURE 17: PM-7224 to 68008 Microprocessor (Only digital interface portion of PM-7224 shown for clarity.)





PM-7226

QUAD 8-BIT CMOS D/A CONVERTER
WITH VOLTAGE OUTPUT

Precision Monolithics Inc.

FEATURES

- Four Voltage Output DACs on a Single Chip
- Microprocessor Compatible
- Adjustment-Free $\pm 1/2$ LSB Total Error
- Guaranteed Monotonicity
- Single (+5V to +15V) or Dual Supply
- Space Saving 20-Pin 0.3 Inch DIP
- TTL/CMOS (5V) Compatible
- Single Specification Table for Both Dual and Single Power Supply Operation
- Fast Data Load, $t_{WR} = 90$ ns, All Temperatures

APPLICATIONS

- Automatic Test Equipment
- Process/Industrial Controls
- Energy Controls
- Scientific Instrumentation
- Medical Equipment
- Multi-Channel Microprocessor-Controlled:
 - Variable Resistors
 - System Calibration
 - Op Amp Offset and Gain Adjust

GENERAL DESCRIPTION

The PM-7226 contains four 8-bit voltage output CMOS digital-to-analog converters on a single chip. Also incorporated into this chip are four input latches and interface control logic.

The four latches are under control of one write and two address signals and are fed from a common 8-bit data bus. It allows the PM-7226 to be packaged into a narrow space-saving 20-pin, 300-mil DIR All digital inputs are TTL/CMOS (5V) compatible. Also, each DAC's input latch is addressable for easy microprocessor interface. The on-board output amplifiers can each drive up to 5mA from either a single or dual supply.

The PM-7226's compact size, low power, and economical cost-per-channel, make it attractive for applications requiring multi-

ple D/A converters without sacrificing circuit-board space. System reliability is also increased due to reduced parts count.

PMI's advanced oxide-isolated, silicon-gate, CMOS process allows the PM-7226's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly-stable thin-film R-2R resistor ladder, aids in matching and temperature tracking between DACs.

The PM-7226 is an improved replacement for the AD7226.

ORDERING INFORMATION†

TOTAL UNADJUSTED ERROR	PACKAGE: 20-PIN		
	MILITARY* TEMPERATURE	INDUSTRIAL TEMPERATURE	COMMERCIAL TEMPERATURE
$\pm 1/2$ LSB	PM7226AR	PM7226ER	PM7226GP
± 1 LSB	PM7226BR	PM7226FR	PM7226HP
± 1 LSB	—	—	PM7226HPC††
± 1 LSB	—	—	PM7226HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

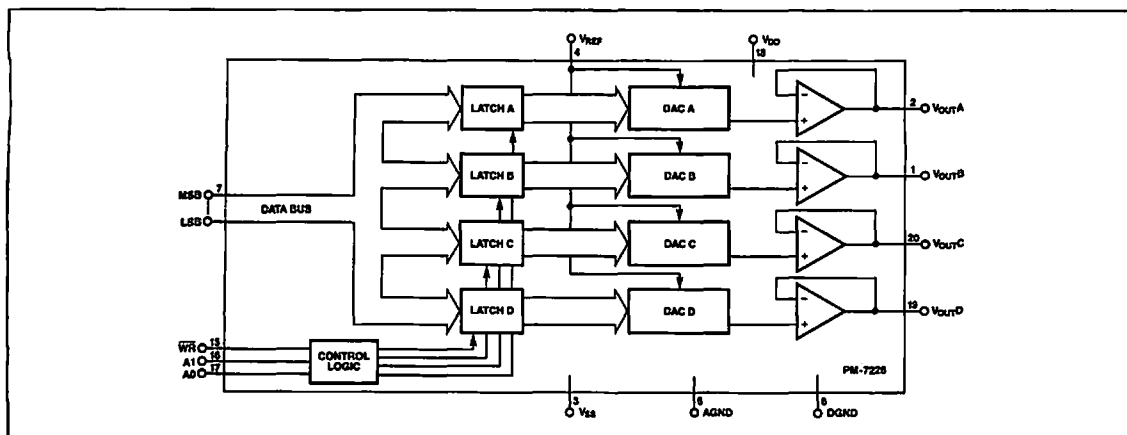
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

CROSS REFERENCE

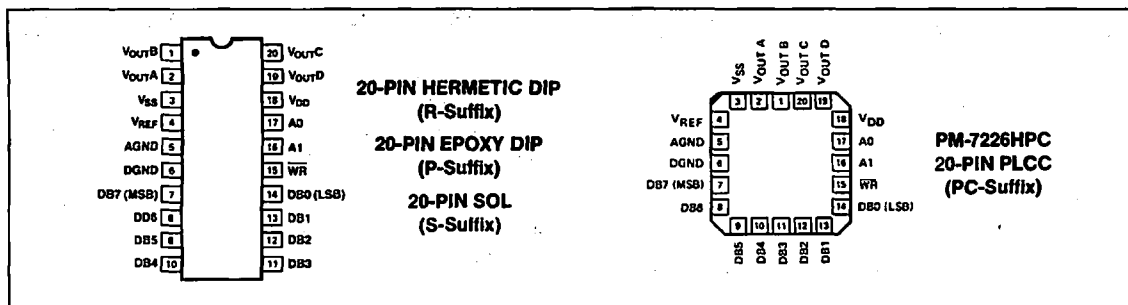
PMI	ADI	TEMPERATURE RANGE
PM7226AR PM7226BR	— AD7226TQ	MIL
PM7226ER PM7226FR	— AD7226BQ	IND
PM7226GP PM7226HP PM7226HPC	— AD7226KN AD7226KP	COM

FUNCTIONAL DIAGRAM





PIN CONNECTIONS



Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: $V_{DD} = +11.4\text{V to } +16.5\text{V}$; $V_{SS} = -5\text{V} \pm 10\%$; $AGND = DGND = 0\text{V}$; $V_{REF} = +2\text{V to } (V_{DD} - 4\text{V})$. SINGLE SUPPLY: $V_{DD} = +15\text{V} \pm 5\%$; $V_{SS} = AGND = DGND = 0\text{V}$; $V_{REF} = +10\text{V}$; unless otherwise specified. $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ apply for PM-7226AR/BR; $T_A = -25^\circ\text{C to } +85^\circ\text{C}$ apply for PM-7226ER/FR; $T_A = 0^\circ\text{C to } +70^\circ\text{C}$ apply for PM-7226GP/HP/HPC/HS. All specifications apply for DACs A, B, C, and D.

			PM-7226			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		8	—	—	Bits
Total Unadjusted Error (Note 1)	TUE	PM-7226A/E/G PM-7226B/F/H	— —	— —	±1/2 ±1	LSB
Relative Accuracy	INL	PM-7226A/E/G PM-7226B/F/H	— —	— —	±1/2 ±1	LSB
Differential Nonlinearity (Note 2)	DNL	PM-7226A/E/G PM-7226B/F/H	— —	— —	±1/2 ±1	LSB
Full Scale Error	G _{FSE}	PM-7226A/E/G PM-7226B/F/H	— —	— —	±1/2 ±1	LSB
Full Scale Temperature Coefficient (Note 4)	TCG _{FS}		—	1	±20	ppm/°C
Zero Code Error	V _{ZSE}	DUAL SUPPLY				
		PM-7226A/E/G	—	—	±5	mV
		PM-7226B/F/H	—	—	±20	
		SINGLE SUPPLY				
		PM-7226A/E/G	—	—	±10	
		PM-7226B/F/H	—	—	±20	
Zero Code Error Temperature Coefficient (Note 4)	TCV _{ZS}	DUAL SUPPLY ONLY	—	±10	—	μV/°C
REFERENCE INPUT						
Voltage Range (Note 3)			2	—	(V _{DD} - 4V)	V
Input Resistance	R _{IN}		2	—	—	kΩ
Input Capacitance (Note 4)	C _{IN}	Digital Inputs = all 0's	65	—	—	pF
		Digital Inputs = all 1's	—	—	300	



Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

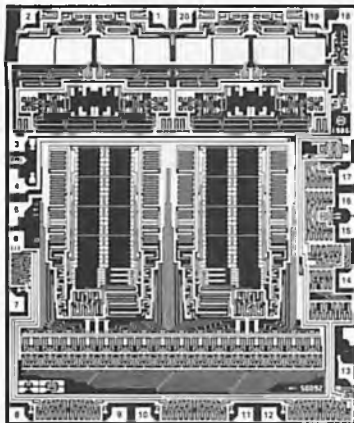
ELECTRICAL CHARACTERISTICS: DUAL SUPPLY: $V_{DD} = +11.4V$ to $+16.5V$; $V_{SS} = -5V \pm 10\%$; $AGND = DGND = 0V$; $V_{REF} = +2V$ to $(V_{DD} - 4V)$. SINGLE SUPPLY: $V_{DD} = +15V \pm 5\%$; $V_{SS} = AGND = DGND = 0V$; $V_{REF} = +10V$; unless otherwise specified. $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7226AR/BR; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7226ER/FR; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7226GP/HP/HPC/HS. All specifications apply for DACs A, B, C, and D. (Continued)

			PM-7226			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Digital Inputs High	V _{INH}		2.4	—	—	V
Digital Inputs Low	V _{INL}		—	—	0.8	V
Input Current	I _{IN}	V _{IN} = 0V or V _{DD}	—	—	±1	μA
Input Capacitance (Note 4)	C _{IN}		—	—	8	pF
Input Coding			BINARY			
POWER SUPPLIES						
Positive Supply Current (Note 6)	I _{DD}		—	—	12	mA
Negative Supply Current (Note 6)	I _{SS}	DUAL SUPPLY ONLY	—	—	10	mA
DYNAMIC PERFORMANCE						
V _{OUT} Slew Rate (Note 4)	SR		2.5	—	—	V/μs
V _{OUT} Settling Time (Positive or Negative) (Notes 4, 5)	t _s		—	—	5	μs
Digital Crosstalk (Note 4)	Q		—	10	—	nVs
Minimum Load Resistance	R _{L(min)}	V _{OUT} = +10V	2	—	—	kΩ
SWITCHING CHARACTERISTICS (Note 4)						
Address to Write Set-Up Time	t _{AS}		0	—	—	ns
Address to Write Hold Time	t _{AH}		0	—	—	ns
Data Valid to Write Set-Up Time	t _{DS}		90	—	—	ns
Data Valid to Write Hold Time	t _{DH}		10	—	—	ns
Write Pulse Width	t _{WR}		90	—	—	ns

- NOTES:**
- Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
 - All devices guaranteed monotonic over the full operating temperature range.
 - $V_{DD} - 4$ volts is the maximum reference voltage for the above specifications.
 - Guaranteed by design and not subject to production test.
 - $V_{REF} = +10V$; to where output settles to 1/2 LSB.
 - $V_{IN} = V_{INL}$ or V_{INH} ; outputs unloaded.



DICE CHARACTERISTICS



DIE SIZE: 0.129×0.152 , 19,608 sq. mils
(3.28 mm $\times$ 3.86 mm, 12.65 sq. mm)

- | | |
|---------------|----------------|
| 1. V_{OUTB} | 11. DB3 |
| 2. V_{OUTA} | 12. DB2 |
| 3. V_{SS} | 13. DB1 |
| 4. V_{REF} | 14. DB0(LSB) |
| 5. AGND | 15. WR |
| 6. DGND | 16. A1 |
| 7. DB7(MSB) | 17. A0 |
| 8. DB6 | 18. V_{DD} |
| 9. DB5 | 19. V_{OUTD} |
| 10. DB4 | 20. V_{OUTC} |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

WAFER TEST LIMITS: DUAL SUPPLY: $V_{DD} = +11.4V$ to $+16.5V$; $V_{SS} = -5V \pm 10\%$; AGND = DGND = 0V; $V_{REF} = +2V$ to ($V_{DD} - 4V$). SINGLE SUPPLY: $V_{DD} = +15V \pm 5\%$; $V_{SS} =$ AGND = DGND = 0V; $V_{REF} = +10V$; unless otherwise specified. $T_A = +25^\circ C$. All specifications apply for DACs A, B, C, and D.

			PM-7226GBC	
PARAMETER	SYMBOL	CONDITIONS	LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits
Total Unadjusted Error (Note 1)	TUE		±1	LSB MAX
Relative Accuracy	INL		±1	LSB MAX
Differential Nonlinearity (Note 2)	DNL		±1	LSB MAX
Full Scale Error	G _{FSE}		±1	LSB MAX
Zero Code Error	V _{ZSE}		±20	mV MAX
REFERENCE INPUT				
Voltage Range (Note 3)	V _{REF}		2 to (V _{DD} – 4V)	V
Input Resistance	R _{IN}		2	kΩ MIN



Specifications apply for DUAL or SINGLE SUPPLY, unless otherwise specified.

WAFER TEST LIMITS: DUAL SUPPLY: $V_{DD} = +11.4V$ to $+16.5V$; $V_{SS} = -5V \pm 10\%$; $AGND = DGND = 0V$; $V_{REF} = +2V$ to $(V_{DD} - 4V)$.
SINGLE SUPPLY: $V_{DD} = +15V \pm 5\%$; $V_{SS} = AGND = DGND = 0V$; $V_{REF} = +10V$; unless otherwise specified. $T_A = +25^\circ C$. All specifications apply for DACs A, B, C, and D. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7226GBC LIMIT	UNITS
DIGITAL INPUTS				
Digital Inputs High	V_{INH}		2.4	V MIN
Digital Inputs Low	V_{INL}		0.8	V MAX
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD}	± 1	μA MAX
Input Coding			BINARY	
POWER SUPPLIES				
Positive Supply Current (Note 4)	I_{DD}		12	mA MAX
Negative Supply Current (Note 4)	I_{SS}	DUAL SUPPLY ONLY	10	mA MAX

NOTES:

1. Includes Full Scale Error, Relative Accuracy, and Zero Code Error.
2. All dice guaranteed monotonic over the full operating temperature range.
3. $V_{DD} - 4$ volts is the maximum reference voltage for the above specifications.
4. $V_{IN} = V_{INL} = V_{INH}$; outputs unloaded.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

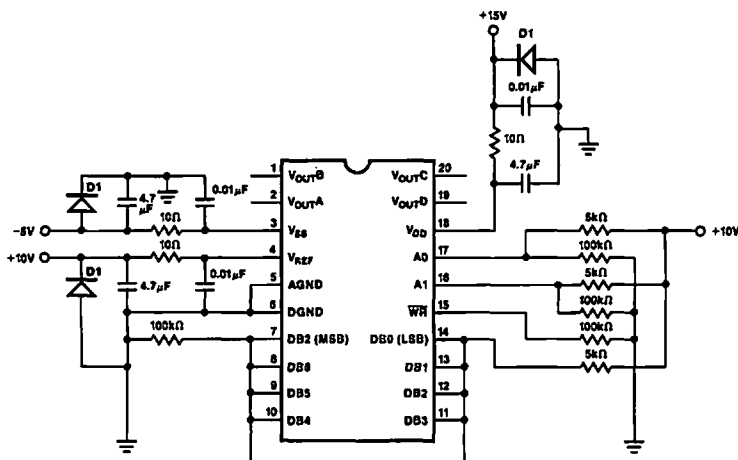
ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} to AGND or DGND	-0.3V, +17V
V_{SS} to AGND or DGND	-7V, V_{DD}
V_{DD} to V_{SS}	-0.3V, +24V
AGND to DGND	-0.3V, V_{DD}
Digital Input Voltage to DGND	-0.3V, V_{DD}
V_{REF} to AGND	-0.3V, V_{DD}
V_{OUT} to AGND (Note 1)	V_{SS} , V_{DD}
Power Dissipation (Any Package) to $+75^\circ\text{C}$	500mW
Derates above $+75^\circ\text{C}$	6.6mW/ $^\circ\text{C}$
Operating Temperature	
Military, AR/BR	-55°C to $+125^\circ\text{C}$
Industrial, ER/FR	-25°C to $+85^\circ\text{C}$
Commercial, GP/HP/HPC/HS	0°C to $+70^\circ\text{C}$

Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$+300^\circ\text{C}$

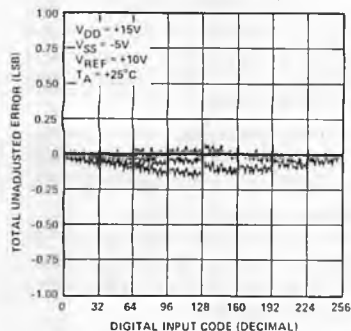
NOTES:

1. Outputs may be shorted to any terminal provided the package power dissipation is not exceeded. Typical output short circuit current to AGND is 50mA.
2. The digital inputs are diode-protected; however, permanent damage may occur on unconnected inputs from high-energy electrostatic fields. Keep device in conductive foam at all times until ready for use.
3. Use proper anti-static handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

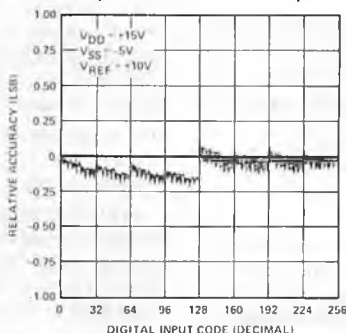
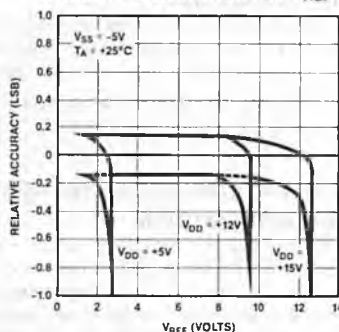
BURN-IN CIRCUIT


TYPICAL PERFORMANCE CHARACTERISTICS

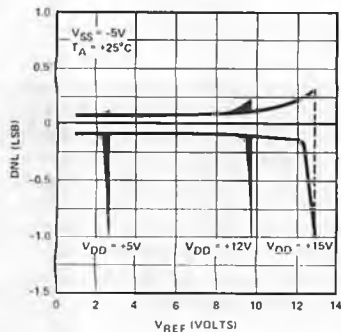
CHANNEL-TO-CHANNEL
MATCHING
(DACs A, B, C, D
SUPERIMPOSED)



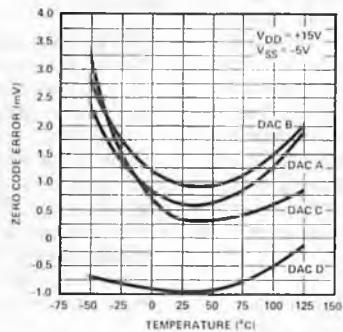
RELATIVE ACCURACY
vs CODE AT
 $T_A = -55^\circ\text{C}, +25^\circ\text{C}, +125^\circ\text{C}$
(ALL SUPERIMPOSED)

RELATIVE ACCURACY vs V_{REF} 

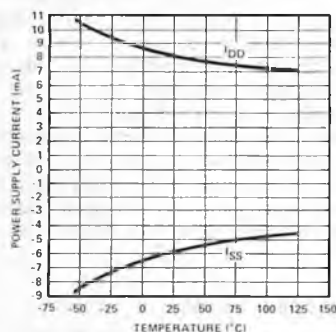
DIFFERENTIAL NONLINEARITY
vs V_{REF}



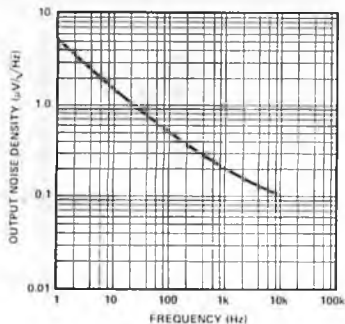
ZERO CODE ERROR
vs TEMPERATURE



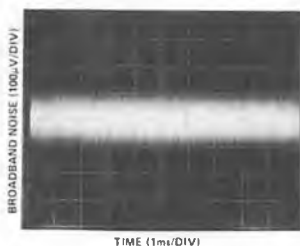
POWER SUPPLY CURRENT
vs TEMPERATURE



OUTPUT VOLTAGE NOISE
DENSITY (e_n) vs FREQUENCY



BROADBAND NOISE



PARAMETER DEFINITIONS

TOTAL UNADJUSTED ERROR

This specification includes Full-Scale-Error, Relative Accuracy, and Zero-Code-Error. Ideal full scale output is $V_{REF} - 1 \text{ LSB}$, and 1 LSB is $V_{REF} \times (2^{-n})$.

DIGITAL CROSSTALK

Digital Crosstalk is the signal coupled to the output of one DAC due to a change in digital input code from other DACs. It is specified in nano-Volt-seconds and measured with $V_{REF} = 0V$.

Refer to PMI 1988 Data Book, Section 11 for additional digital-to-analog converter definitions.

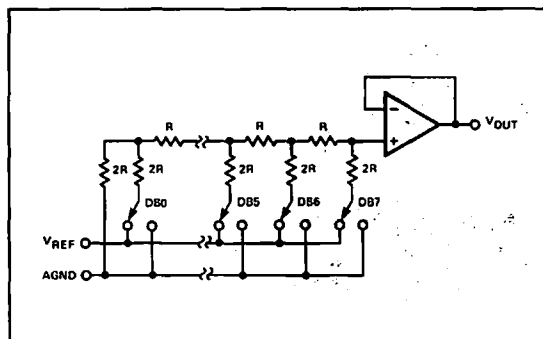
GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The PM-7226 contains four output amplifiers, four highly-stable, thin-film, R-2R resistor ladder networks, four input data latches, and interface control logic. Also included are thirty-two NMOS single-pole, double-throw switches. These switches select either V_{REF} or AGND and are controlled by the digital input code.

Figure 1 shows a simplified circuit for the R-2R ladder network. It is shown employed in the voltage mode configuration and connected to an amplifier. The advantages gained in operating the ladder in the voltage mode are two-fold: it allows the DAC to be operated with a single supply, and the ladder resistance/capacitance modulation encountered in the current mode configuration are eliminated. The modulation (caused by the varying digital code) is now presented to the low-impedance reference voltage source (most voltage reference output-impedances are low enough so that its output voltage will not be affected by the varying digital code). The amplifier's input terminal now "sees" a constant resistance/capacitance, thus

FIGURE 1: Simplified circuit configuration for one DAC.
(Switches are shown for all "1's" on the digital inputs.)



the output offset voltage modulation is eliminated. Also, digital glitches will not feed through the switch capacitance to the output; instead, it will be absorbed by the low output-impedance of the external reference source, thus, resulting in a "cleaner" output voltage.

Note in Figure 1 that the amplifier is configured to operate as a buffer amplifier, and so, no signal inversion takes place from input to output (V_{REF} to V_{OUT}). Also note that analog ground (AGND) is accessible and can be biased above digital ground (DGND) for some applications; more on this in the applications section on Page 11 under AGND biasing.

For proper operation, V_{REF} maximum should be limited to V_{DD} minus 4 volts. This means that in order to operate the DAC with +10V at the reference input terminal, V_{DD} must be at least +14V.

The PM-7226's reference input terminal is common to the four DACs. This puts each R-2R ladder resistance in parallel and its resistance can range from $2k\Omega$ to infinity; the value depends on the digital input code. The capacitance at this node also varies from 65pF to 300pF, and is code dependent.

The voltage output equation for each DAC is given by:

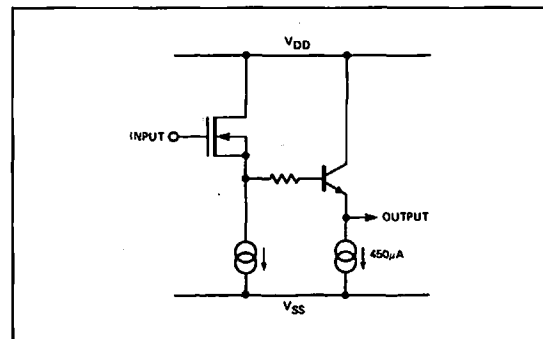
$$V_{OUT} = V_{REF} \times D/255$$

where D is the digital input code integer number that is between 0 and 255.

BUFFER AMPLIFIER SECTION

Each R-2R resistor ladder network has a typical resistance of $10k\Omega$; a $100k\Omega$ load would cause the gain error to rise to 23 LSB. Therefore, in order to drive a $2k\Omega$ load, the R-2R ladder was buffered with a stable CMOS amplifier configured to operate in the unity gain mode. The amplifier can drive 10 volts across a $2k\Omega$ load delivering 5mA, and can easily drive a 3300pF capacitive load. The PM-7226's output can also withstand an indefinite short-circuit to AGND (typical short-circuit current to AGND is 50 mA). The output may also be shorted to any voltage between V_{DD} and V_{SS} ; however, care must be taken to not exceed the device maximum power dissipation.

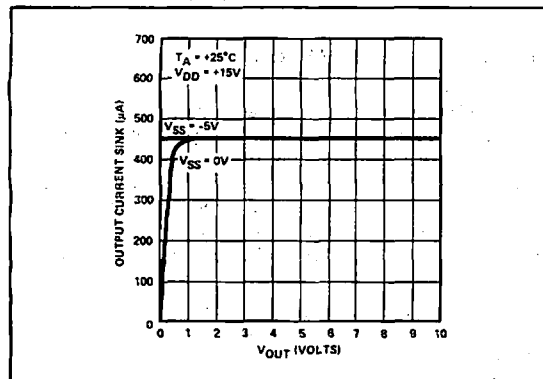
FIGURE 2: Amplifier Output Stage



The amplifier's output stage uses an intrinsic NPN bipolar transistor. This transistor provides a low-impedance, high-output current capability using a small part of the chip area. The transistor is derived from the P⁺ well and the substrate. The emitter of this NPN transistor is loaded with a 450 μ A NMOS current-source referenced to V_{SS}. This allows 450 μ A to be sunk to the negative supply allowing the amplifier's output to go directly to ground.

A simplified circuit of the output amplifier is shown in Figure 2. Note how the current-source is connected between the parasitic NPN output transistor's emitter and V_{SS}. Figure 3 shows a typical plot of the DAC's current sink capability versus output voltage; note that it is for a dual and single supply operation. Let's take a closer look at what happens to its behavior by referring to Figure 3.

FIGURE 3: DAC Output Current Sink



With a dual supply, the current-source is still in its high impedance (saturation) state when the output is at 0 volts. This is possible because 5 volts (V_{SS}) is across the current-source and is sinking 450 μ amps. When V_{SS} = 0 volts, however, the current sink capability is reduced as the output voltage approaches 0 volts; the current-source is coming out of its saturation region and starts appearing resistive.

The amplifier's current-limiting and buffering abilities are achieved by using an NMOS transistor and a series resistor. The transistor is configured as a source follower and is driving the resistor and NPN output transistor. This is also shown in Figure 2.

The amplifier's internal gain stages were designed so that they maintain good gain over its common mode range; the objective was to maintain good offset performance over the specified voltage range. The amplifiers offset voltage is laser-trimmed during the manufacturing process; this eliminates offset trimming by the user in most applications. The effect of amplifier offset is included in the data sheet under "total unadjusted error" specification.

DIGITAL SECTION

The digital inputs are CMOS inverters. They were designed such that TTL and CMOS (5V) input levels are converted into internal CMOS logic levels; they are used to drive the internal circuitry. A simple 5V regulator is used to ensure the high speed timing.

The PM-7228's digital inputs are TTL and CMOS (5V) compatible between the V_{DD} range of +11.4V to +16.5V. The inputs are protected from electrostatic-discharge and build-up with two internal distributed-diodes; they are connected from V_{DD} and DGND to each CMOS input gate. Each input has a typical input current of less than 1nA. A simplified input protection scheme is shown in Figure 4.

FIGURE 4: One Digital Input Structure

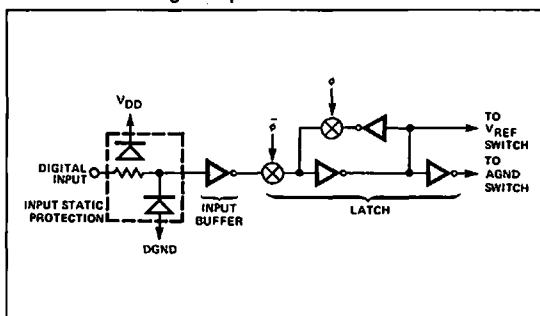
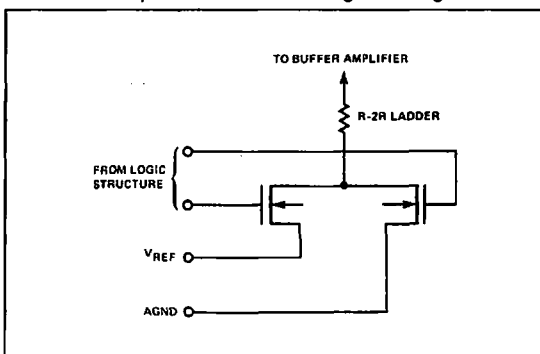


Figure 4 also shows an equivalent logic circuit for one digital input structure. This logic circuit drives the ladder switches shown in Figure 5, they also drive the control logic circuitry. The digital controls $\bar{\theta}$ and θ shown are internally generated from the external WR, A1, and A0 signals. The logic combination of A0 and A1 decide which DAC is selected.

FIGURE 5: Simplified N-Channel Voltage Steering Switches



INTERFACE CONTROL LOGIC SECTION

Figure 6 shows the PM-7226's input control logic, and Table 1 the DAC control table. The address lines A0 and A1 determines which DAC will accept the input data. The $\overline{WR}$ input determines whether the selected DAC is transparent (output follows the input), latched, or no operation.

FIGURE 6: Input Control Logic

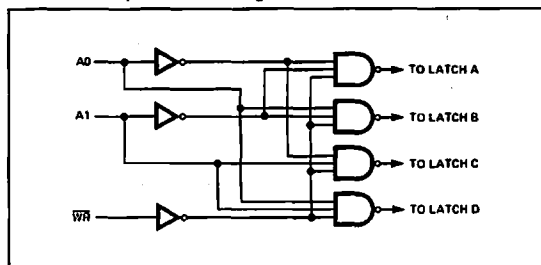


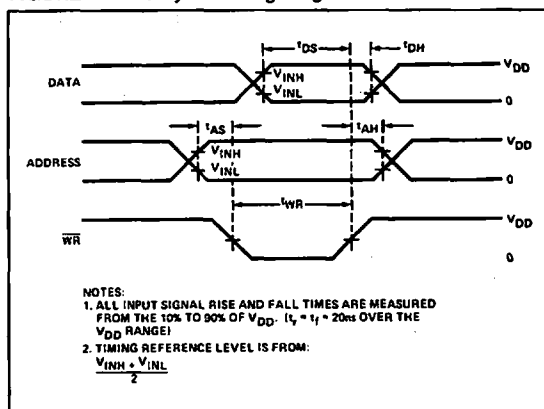
TABLE 1: DAC Control Table

LOGIC CONTROL			PM-7226 OPERATION
$\overline{WR}$	A1	A0	
H	X	X	No Operation Device Not Selected
L	L	L	DAC A Transparent
	L	L	DAC A Latched
L	L	H	DAC B Transparent
	L	H	DAC B Latched
L	H	L	DAC C Transparent
	H	L	DAC C Latched
L	H	H	DAC D Transparent
	H	H	DAC D Latched

L = Low State, H = High State, X = Don't Care

Figure 7 shows the PM-7226's write timing diagram. It shows that the selected DAC is transparent when the $\overline{WR}$ signal is low. Some bus systems do not always have data valid for the entire period during which the $\overline{WR}$ signal is low. This allows invalid data to briefly appear at the DAC's digital inputs and cause unwanted glitches at the output. Retiming the write pulse ($\overline{WR}$) so that it only occurs when data is valid will eliminate this problem.

FIGURE 7: Write Cycle Timing Diagram



APPLICATIONS INFORMATION

POWER SUPPLY

The PM-7226 data sheet is specified with a dual and single power supply conditions. The dual supply specifications are specified with a positive supply (V_{DD}) range of +11.4V to +16.5V, and a negative supply (V_{SS}) of -5V. The specified reference voltage (V_{REF}) under these conditions range from +2V to $V_{DD} - 4V$. For those applications requiring +10 volts at the output ($V_{REF} = +10V$), V_{DD} must be +14V minimum to meet data sheet limits.

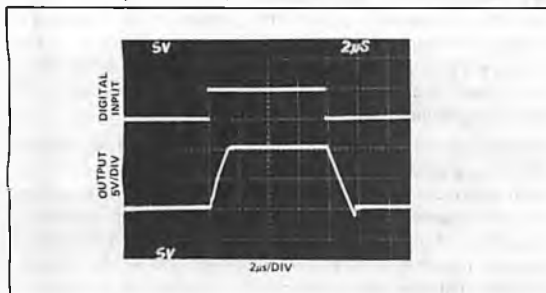
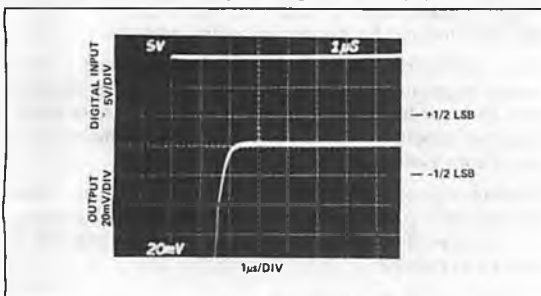
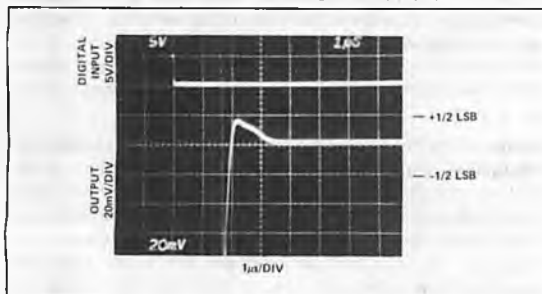
The specified V_{REF} for the single supply specifications is +10V. The V_{REF} voltage range for both dual and single power supply applications must be observed if the PM-7226's multiplying capabilities are to be preserved.

Although the PM-7226 can operate with either a single or dual power supply, improved zero-code error can be obtained by using dual supplies.

DYNAMIC PERFORMANCE

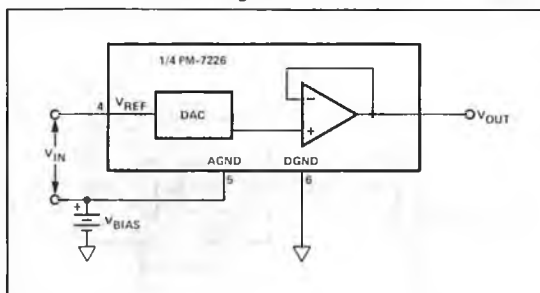
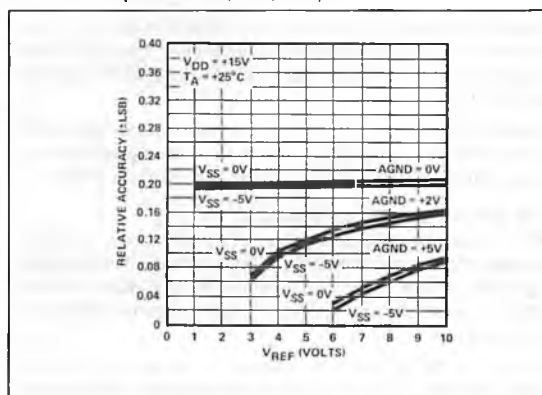
The PM-7226's settling time is limited by the internal amplifier's slew-rate as shown in Figure 8. Depicted is the dynamic response for a positive full-scale output voltage swing. Figure 9 shows the expanded view with no evidence of signal overshoot or ringing; note that the typical settling time is 1.85 μs . An expanded view of the negative full-scale output voltage swing is shown in Figure 10. It also shows overshoot or ringing at a minimum, and the typical settling time is 1.9 μs .

A special test fixture was used for the photographs of Figures 9 and 10. The 10V swing would have overloaded the oscilloscope's input resulting in erroneous indications.

FIGURE 8: Dynamic Response

FIGURE 9: Positive Swing Settling Time (1.85μs)

FIGURE 10: Negative Swing Settling Time (1.9μs)


AGND BIASING

Some applications may require the DAC's output voltage level to be offset above ground. This is easily accomplished with the PM-7226; the desired DC offset voltage can be applied to the AGND pin. Raising AGND above DGND affects all four DACs because AGND is common to them. The digital input voltage levels are not affected. Figure 11 shows the circuit configuration and Figure 12 shows the relative accuracy with AGND biased at

FIGURE 11: AGND Biasing Scheme

**FIGURE 12: Relative Accuracy vs V_{REF}
(AGND = 0V, +2V, +5V)**


0V, +2V, and +5V. The graph shows both a dual and single supply operation with V_{DD} at +15V. It is important to remember that other parameters degrade more pronouncedly than relative accuracy. Note, V_{DD} and V_{SS} must be referenced to DGND.

The DAC's output voltage expression under this condition is:

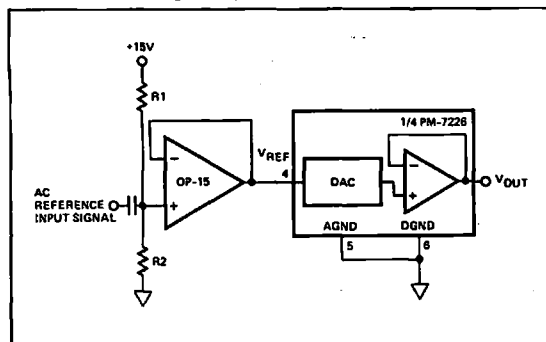
$$V_{OUT} = \text{AGND bias} + V_{IN} \times D/256$$

where AGND bias is the voltage level above DGND and D is the digital input code integer number that is between 0 and 255.

MULTIPLYING OPERATION

Good multiplying capabilities are realized with the PM-7226 if the reference signal level is kept within +2V and $V_{DD} - 4V$. The maximum input signal level is +12.5V for a V_{DD} supply voltage of +16.5V; however, it is recommended that $V_{DD} = +15V \pm 5\%$ and the AC voltage swing between +2V and +11V. The signal must be AC coupled and biased up with a voltage divider as

FIGURE 13: AC Signal Input Scheme



shown in Figure 13. A buffer amplifier should be used to ensure that the DAC's V_{REF} impedance (remember, the R-2R ladder input resistance varies from $2k\Omega$ to infinity) does not load the resistor divider.

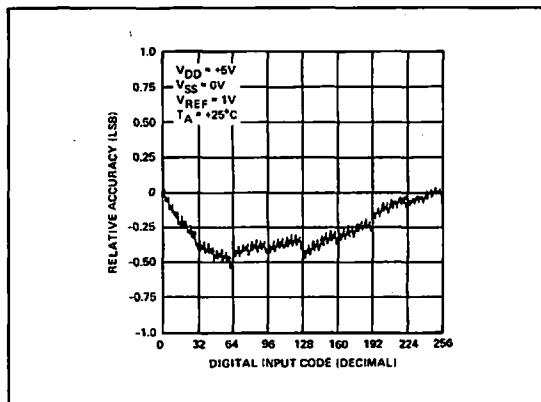
The V_{REF} small-signal frequency response ($-3dB$ bandwidth) for the PM-7226 is typically 1.5 MHz. Its small-signal harmonic distortion is less than $-57dB$ at 1kHz and $-55dB$ at 100kHz.

+5V SINGLE SUPPLY OPERATION

Although a +5V performance specification table is not listed, the PM-7226 can operate well with only a single +5V supply (see Figure 14). All performance parameters are degraded; however, DNL remains within the specified ± 1 LSB ensuring monotonic operation.

Using the PM-7226 with a single +5V supply will limit the reference input voltage level to a maximum of +1V. The $V_{DD}-4V$ limitation must still be observed.

FIGURE 14: Relative Accuracy with Single +5V Operation



GENERAL GROUND MANAGEMENT

Ground management implies the placement of a system's analog and digital ground currents. Analog and digital ground returns are a source of system errors and must be addressed. Remember, the analog signal is only as good as the integrity of its analog ground.

Different ground management techniques are used depending on the size and type of overall system. Proper grounding techniques require tying the analog and digital grounds together at the DAC's socket, and each ground return line be brought out separately to their respective power supply grounds. Tying the grounds together at the device socket and at the power supplies, or at more than one location, can create ground loops. This causes noisy digital ground currents to flow through the analog ground paths destroying the analog's ground integrity. Voltage differences of millivolts (and hundreds of millivolts in some systems) can be found in these ground paths.

Other sources of system errors can be introduced by the product of ground noise currents and ground bus impedances. Using large conductors or ground planes between the converter and power supplies will minimize the ground impedances and thus, reduce system errors.

If system requirements dictate the use of common return lines to the power supplies for both the analog and digital grounds, the converter should then be placed as close to the power supplies as possible.

POWER SUPPLY DECOUPLING

Power supply decoupling capacitors are important to suppress oscillations and noise transients from entering the system. Noise transients are generated from digital switching or switching power supplies; and oscillations on the power supply lines are caused by lead inductances combined with stray capacitance. These transients and oscillations can also cause system errors.

Bypassing the PM-7226 at the socket with only high frequency decoupling capacitors may not remove these oscillations. An LC tank circuit can be formed by the stray power lead inductance and capacitance. These reactive components can allow oscillations to occur during a digital current step. It is necessary, then, to remove or lower the tank's resonant frequency. The easiest method is to parallel the high frequency decoupling capacitor with a low frequency capacitor.

The high frequency decoupling capacitors should be ceramic and in the range of $0.01\mu F$; the low frequency decoupling capacitors should be tantalum and between 1 to $10\mu F$ as close as possible to the device socket.

BASIC APPLICATIONS

UNIPOLAR OPERATION

Figure 15 shows the PM-7226 configured in the unipolar mode of operation; the analog output voltage is of a single positive polarity only. Table 2 shows the code for this mode of operation. The table shows that there is no signal inversion between $+V_{REF}$ and V_{OUT} . Note that the analog output voltage is equal to

V_{REF} multiplied by the digital input code (hence, multiplying DAC).

The expression for 1 LSB and V_{OUT} is:

$$1 \text{ LSB} = V_{REF} \times 2^{-8}, \text{ or } V_{REF} \times 1/256$$

and

$$V_{OUT} = V_{REF} \times D/256,$$

where D is the digital input integer between 0 and 255.

FIGURE 15: Unipolar Operation

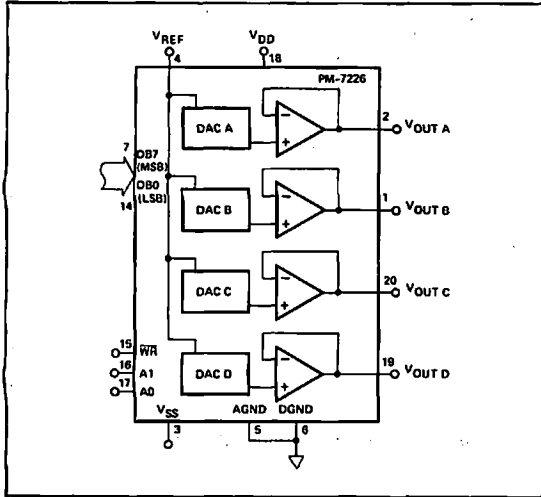


TABLE 2: Unipolar Code Table (Refer to Figure 15)

DAC DATA INPUT MSB	LSB	ANALOG OUTPUT (DAC A, B, C, or D)
1	1 1 1 1 1 1 1 1	$+V_{REF} \left(\frac{255}{256} \right)$
1	0 0 0 0 0 0 0 1	$+V_{REF} \left(\frac{129}{256} \right)$
1	0 0 0 0 0 0 0 0	$+V_{REF} \left(\frac{128}{256} \right) = \frac{+V_{REF}}{2}$
0	1 1 1 1 1 1 1 1	$+V_{REF} \left(\frac{127}{256} \right)$
0	0 0 0 0 0 0 0 1	$+V_{REF} \left(\frac{1}{256} \right)$
0	0 0 0 0 0 0 0 0	0V

BIPOLAR OPERATION

Figure 16 illustrates the PM-7226 in the bipolar mode of operation. This mode allows the output voltage to swing plus or minus and is determined by the digital input code; this can be seen in Table 3. This configuration requires an external amplifier and two resistors for each channel requiring bipolar operation.

The output voltage expression is given by:

$$V_{OUT} = \left((1 + R2/R1) \times D/256 \times V_{REF} \right) - (R2/R1 \times V_{REF})$$

where D is the digital input code integer between 0 and 255. If $R1 = R2$, then V_{OUT} becomes:

$$V_{OUT} = (2 \times D/256 - 1) \times V_{REF}$$

To keep gain and offset errors at a minimum, $R1$ and $R2$ should be matched to $\pm 0.1\%$ and track over the operating temperature range of interest.

TABLE 3: Bipolar (Offset Binary) Code Table (Refer to Figure 16)

DAC DATA INPUT MSB	LSB	ANALOG OUTPUT (DAC A, B, C, or D)
1	1 1 1 1 1 1 1 1	$+V_{REF} \left(\frac{127}{128} \right)$
1	0 0 0 0 0 0 0 1	$+V_{REF} \left(\frac{1}{128} \right)$
1	0 0 0 0 0 0 0 0	0V
0	1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{1}{128} \right)$
0	0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{127}{128} \right)$
0	0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{128}{128} \right) = -V_{REF}$

FIGURE 16: Bipolar Operation

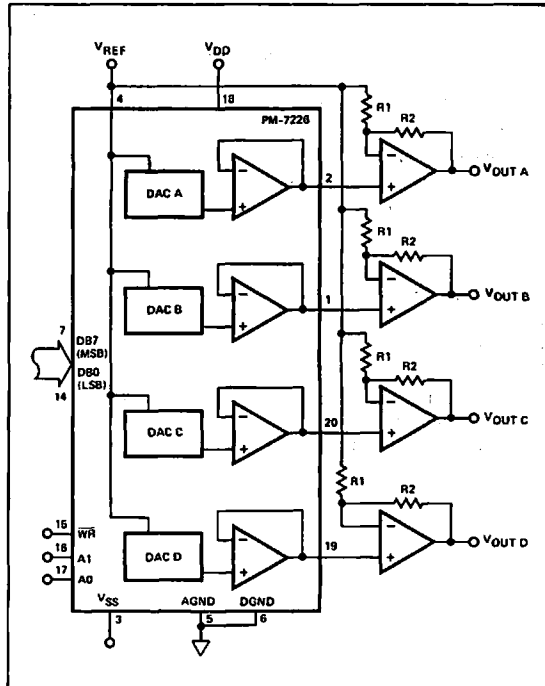
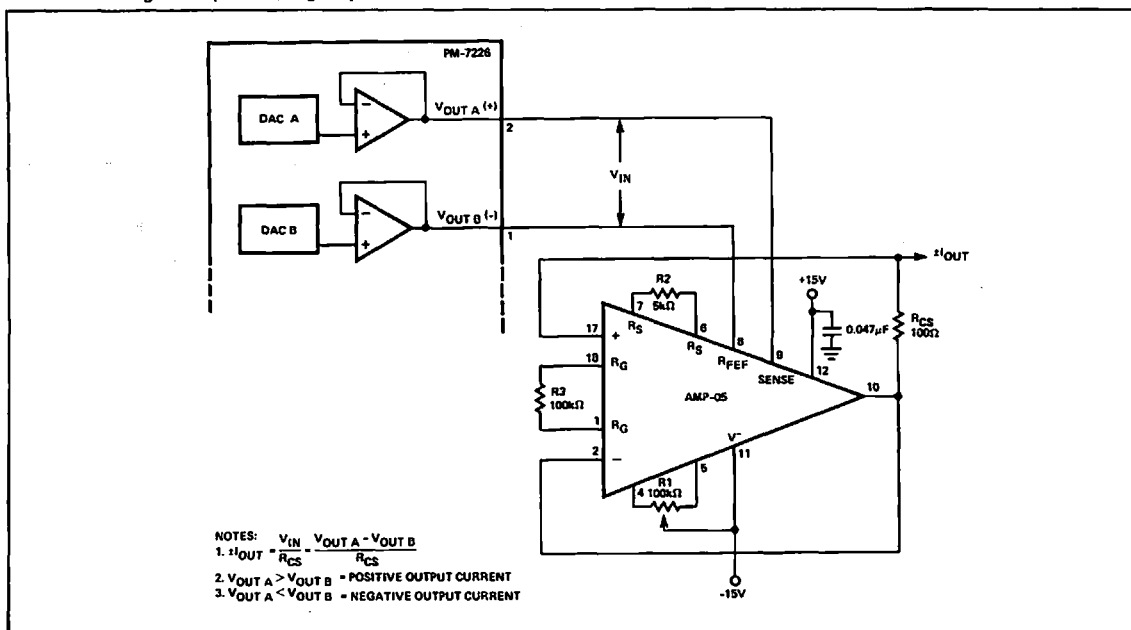


FIGURE 17: High Compliance, Digitally-Controlled, Current Source



HIGH-COMPLIANCE BIPOLAR PRECISION CURRENT-SOURCE

Figure 17 shows the PM-7226 controlling a high-compliance, bipolar precision current-source using PMI's AMP-05 instrumentation amplifier. The AMP-05's reference and sense pins become differential inputs, and the "old" inputs now monitor the voltage across a precision current-sense resistor, R_{CS} in Figure 17. Voltage gain is set at unity, so the transfer function is simply: $I_{OUT} = (V_{OUTA} - V_{OUTB})/R_{CS}$. Using a 100Ω resistor for R_{CS} limits the output current to $\pm 10mA$ with a $\pm 1V$ input.

Potentiometer R1 trims the output current to zero with the two inputs at 0V. Fine gain adjustment may be accomplished by trimming R2 or R3.

PROGRAMMABLE OP AMP OFFSET ADJUST

The PM-7226 can be used for op amp offset trimming adjustments under microprocessor control. Offsets caused by temperature drifts can be trimmed by the microprocessor during a periodic calibration cycle.

The PM-7226 uses the input offset voltage nulling pins normally provided on most amplifiers as shown in Figure 18. A fixed bias current is provided to pin 5 of the op amps offset null pin with R2, and R1 (connected to the DAC's voltage output pin) provides the variable current to pin 1.

FIGURE 18: OP AMP Offset Adjust (See Text)

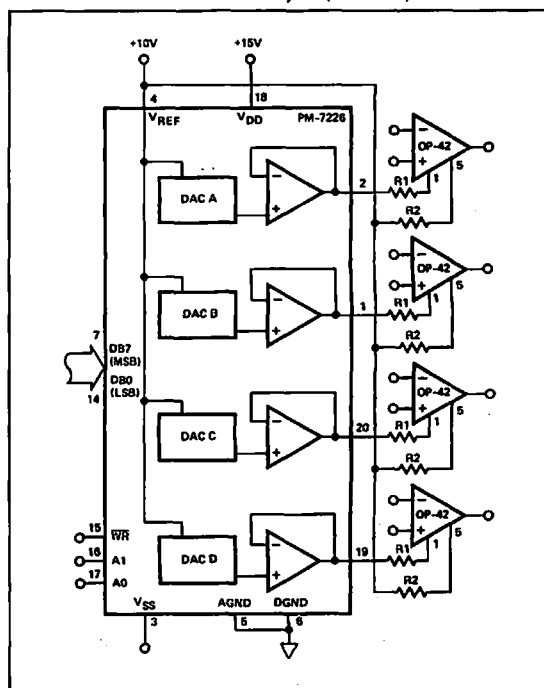
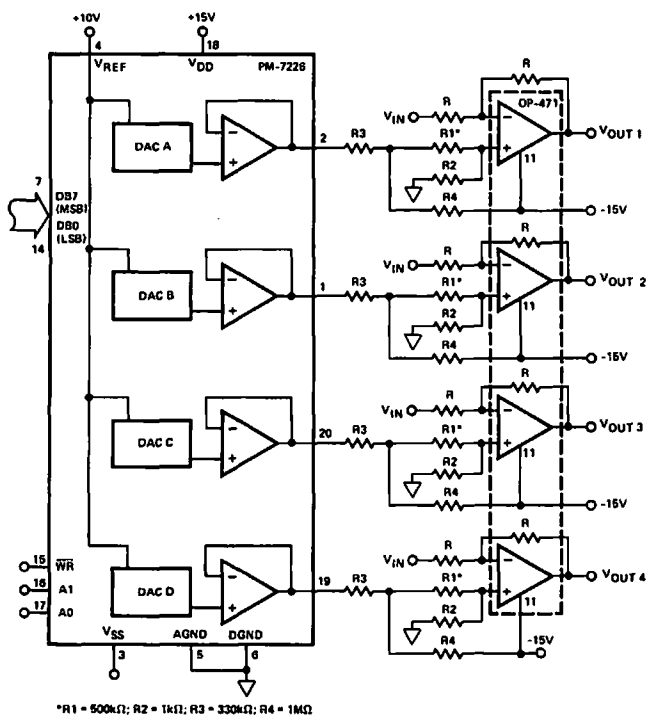
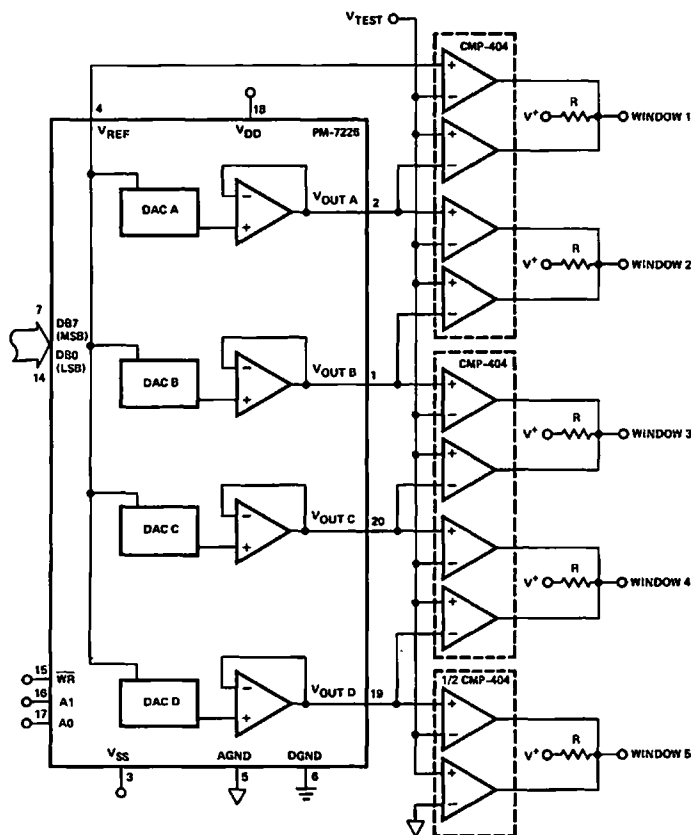


FIGURE 19: Alternate Offset Adjust (See Text)



The non-overlapping circuit uses one PM-7226 and ten comparators; this allows for five voltage windows. These windows

FIGURE 20: Non-Overlapping Window Comparator



range between V_{REF} and analog ground. Figure 20 shows that the first window is between V_{REF} and V_{OUTA} . V_{OUTA} is also the upper limit of window 2, the lower limit being V_{OUTB} , etc. These limits (window size) can be microprocessor controlled. The relationship $V_{REF} > V_{TEST} > AGND$ apply.

More versatility can be obtained by connecting the output of DAC D (V_{OUTD}) to V_{REF} ; this allows V_{REF} (which is common to all four DACs) to be under microprocessor control (see "Programmable DAC Reference Voltage" below). This, however, reduces the windows to four. Overlapping windows (Figure 21) will reduce the windows to three.

PROGRAMMABLE DAC REFERENCE-VOLTAGE

With the PM-7228's flexibility, one of the internal DACs can be used to control V_{REF} for all of the DACs, and under microprocessor control.

The circuit configuration is shown in Figure 22. The relationship of V_{REF} to V_{IN} is dependent upon the digital code and the ratio of R_1 and R_2 , and is given by:

$$V_{REF} = \left[(1 + R_1/R_2) / (R_1 \times D/256 + 1) \right] \times V_{IN}$$

where $R = R_2/R_1$ (Figure 22)

D = digital input code

Table 4 shows V_{REF} for various ratios of R_1 and R_2 .

FIGURE 21: Overlapping Window Comparator

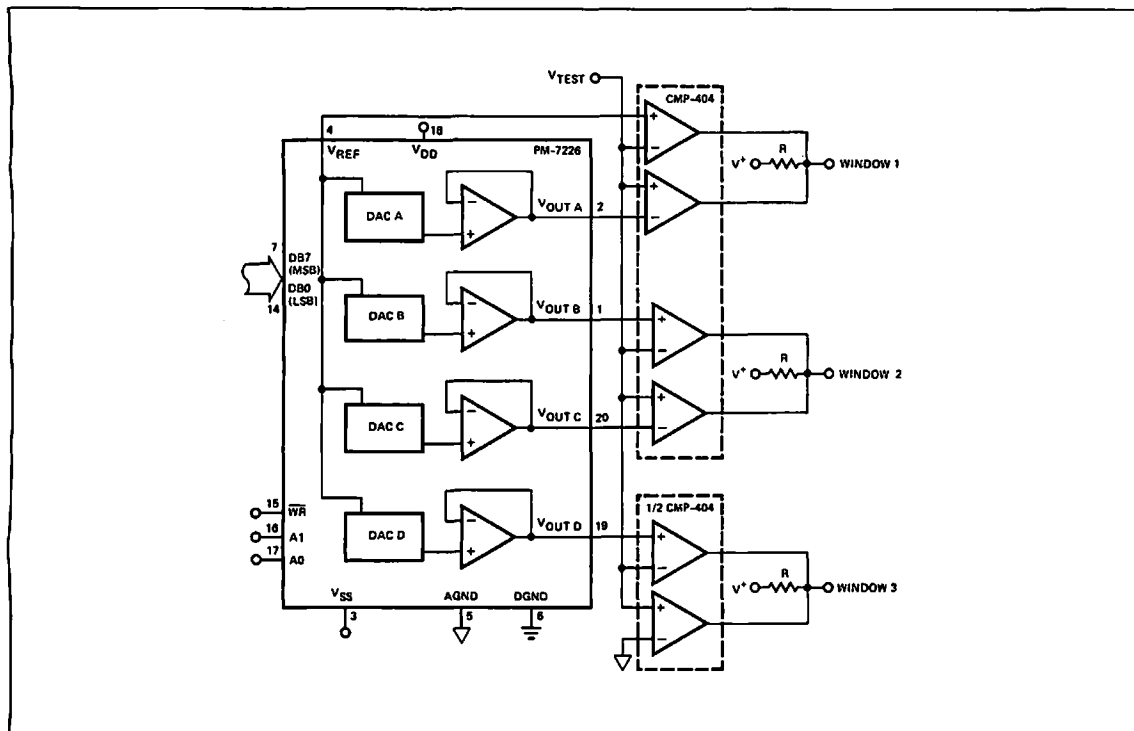
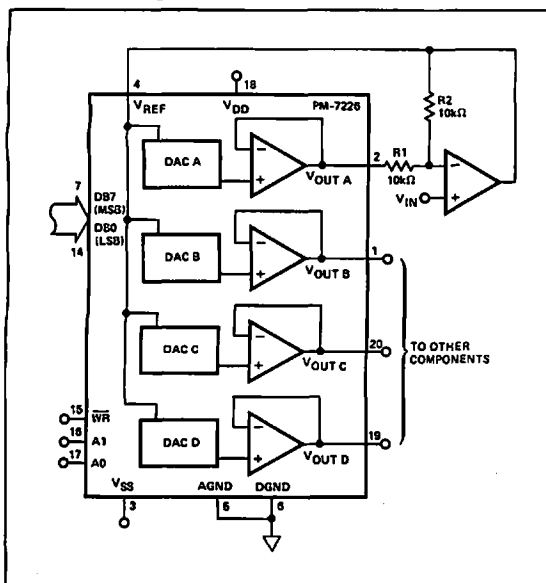


FIGURE 22: Programmable DAC Reference

TABLE 4: V_{REF} versus R_1, R_2 (see Figure 22)

R_1, R_2	DIGITAL INPUT CODE	V_{REF}
$R_1 = R_2$	00000000 (0/256)	$2 V_{IN}$
$R_1 = R_2$	10000000 (128/256)	$1.3 V_{IN}$
$R_1 = R_2$	11111111 (255/256)	V_{IN}
$R_2 = 3R_1$	00000000 (0/256)	$4 V_{IN}$
$R_2 = 3R_1$	10000000 (128/256)	$1.6 V_{IN}$
$R_2 = 3R_1$	11111111 (255/256)	V_{IN}

This application works best with dual supplies. This is due to the DAC's output-current sink capability as V_{OUT} approaches 0V.

3-PHASE SINEWAVE GENERATION

The PM-7226 is well suited for 3-phase sinewave generation and with amplitude control. These sinewaves can be used to control a shaft's rotational angle in small 3-phase synchro motors; some applications are antennas, robotics, and process controls. Other waveforms (such as triangular) may also be generated. The concept revolves around a PROM, counter, and a clock (or a microprocessor).

FIGURE 23: 3-Phase Sinewave Generator Circuit (Using Counter)

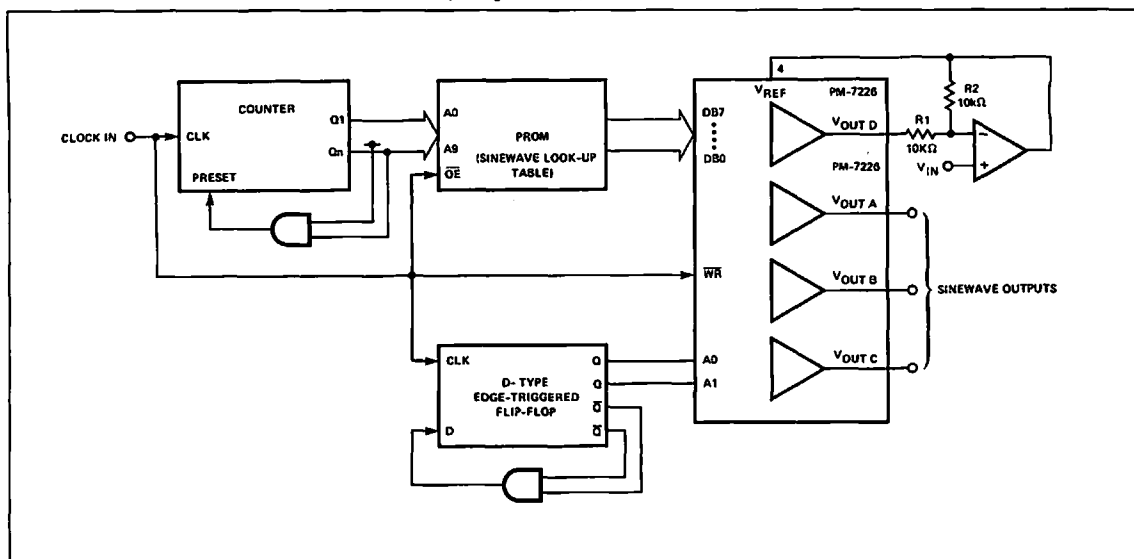
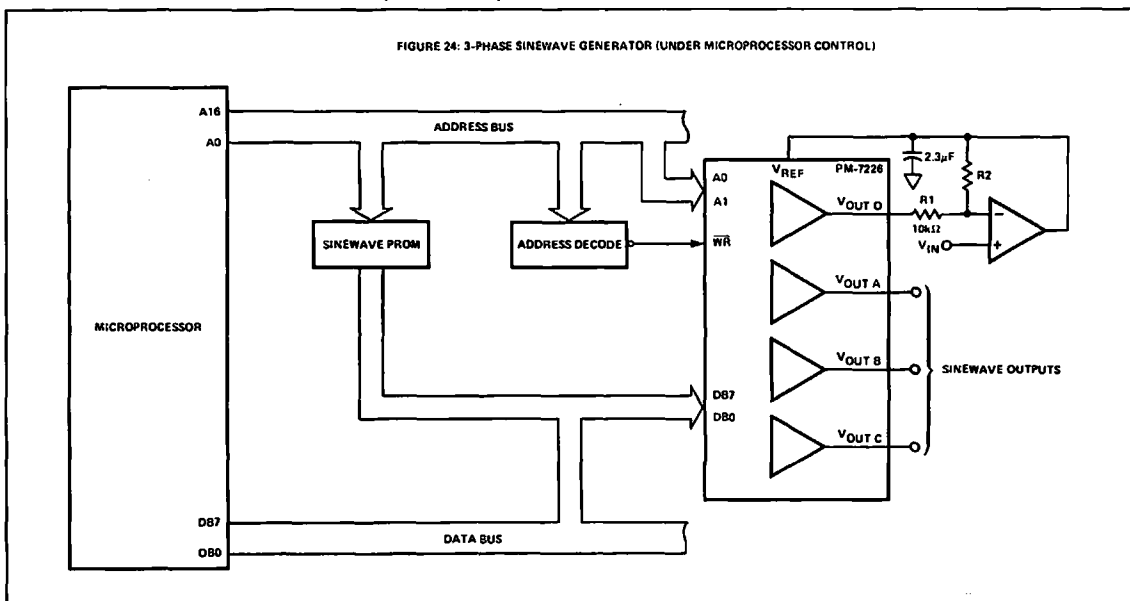


FIGURE 24: 3-Phase Sinewave Generator (Under Microprocessor Control)



The sinewave codes are stored in a PROM in sets of three. Each set is 120° apart and has a 1.4° resolution (360°/256). These codes will use 768 memory address spaces (256 × 3).

Figure 23 shows the circuit using a counter, flip-flop, and a PROM; note that a clock is used to control the circuit. The counter counts through the PROM's addresses until the counter

has stepped through the PROM's full look-up table, this completes a full cycle. The counter then resets and begins the cycle again when the last address data has been loaded into the PM-7226.

Sinewave generation can also be under microprocessor control, see Figure 24. The processor's software runs 3 phases to three DACs. Each phase is drawn from the PROM's look-up table.

Any combination of wave shapes may be simultaneously generated. It only requires the functions to be programmed into the PROM on an interface basis.

The output amplitudes can also be microprocessor controlled; see previous section on "PROGRAMMABLE DAC REFERENCE VOLTAGE".

MICROPROCESSOR INTERFACING

Interfacing the PM-7226 to a microprocessor is simplified by virtue of its loading structure simplicity. Data is loaded into the DAC by use of only three control lines, the write strobe (WR) and two DAC selection control signals (A0, A1).

Figures 25 through 29 show various popular microprocessor interface configurations.

FIGURE 25: PM-7226 to 8085A INTERFACE (Simplified circuit, only lines of interests are shown.)

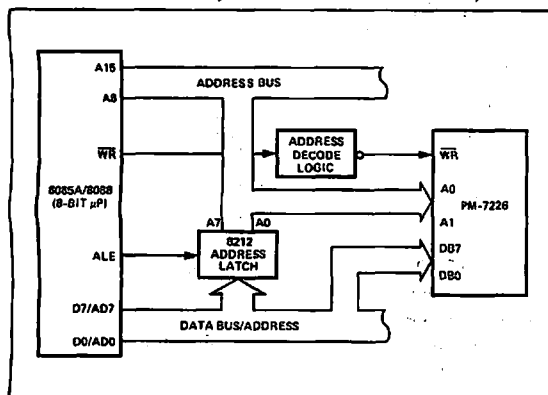


FIGURE 26: PM-7226 to Z-80 INTERFACE (Simplified circuit, only lines of interests are shown.)

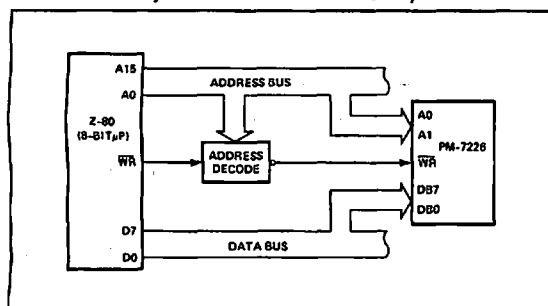


FIGURE 27: PM-7226 to 6809 INTERFACE (Simplified circuit, only lines of interest are shown.)

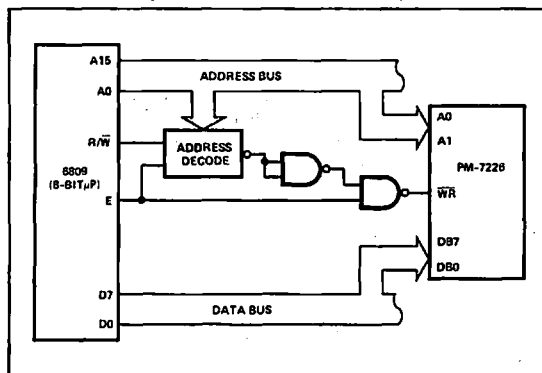


FIGURE 28: PM-7226 to 6502 INTERFACE (Simplified circuit, only lines of interest are shown.)

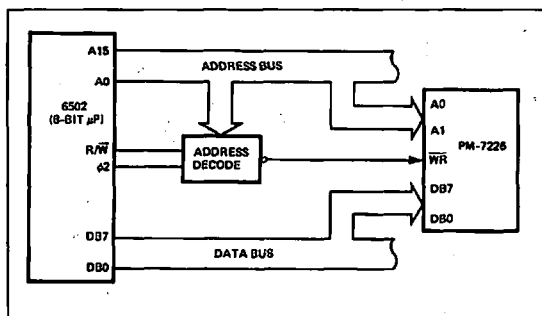
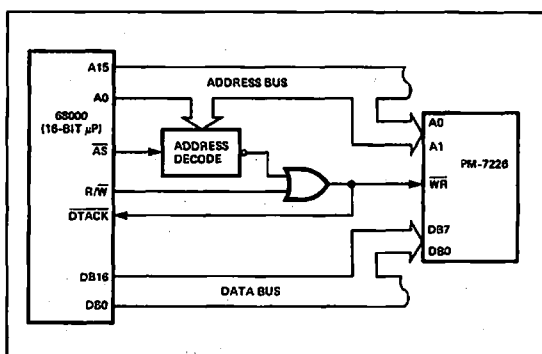


FIGURE 29: PM-7226 to 68000 INTERFACE (Simplified circuit, only lines of interest are shown.)





PM-7524

CMOS 8-BIT BUFFERED MULTIPLYING
D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- $\pm 1/8$ LSB Maximum Nonlinearity Over Temperature
- ± 0.002 LSB Maximum Zero-Scale Error (I_{LKG} 10nA)
- ± 1 LSB Maximum Gain Error Over Temperature
- Microprocessor Compatible
- Improved Resistance to ESD
- Latch-up Resistant; No Schottky Diodes Required
- 5mW @ +5V Maximum Power Consumption

APPLICATIONS

- Microprocessor Controlled Circuits
- Precision AGC Circuits
- Bus Structured Instruments
- Function Generators
- Digitally Controlled Attenuators and Power Supplies

ORDERING INFORMATION†

NON- LINEARITY $V_{DD} = +15V$	GAIN ERROR	TEMPERATURE (°C)		
		MILITARY*	INDUSTRIAL	COMMERCIAL
		-55 TO +125	-25 TO +85	0 TO +70
$\pm 1/8$ LSB	± 1 LSB	PM7524AQ	PM7524EQ	PM7524GP
$\pm 1/4$ LSB	± 1.5 LSB	PM7524BQ	PM7524FQ	PM7524HP
$\pm 1/4$ LSB	± 1.5 LSB	—	—	PM7524HPC††
$\pm 1/4$ LSB	± 1.5 LSB	—	—	PM7524HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The PM-7524 is an 8-bit monolithic multiplying digital-to-analog converter with input latches. It is compatible with all popular 8-bit microprocessors including the 6800, 8080, 8085, and Z80. Its load cycle is similar to that of a RAM's write cycle.

PMI's tightly controlled thin-film resistor processing provides $1/8$ LSB linearity without laser trimming. The design incorporates a matching MOS transistor switch in series with the R-2R ladder terminating resistor and output op amp's feedback resistor. This allows the DAC to achieve an excellent gain tempco and improved power supply rejection.

The PM-7524 exhibits excellent performance on a single +5V to +15V power supply. It is TTL compatible at +5V and dissipates less than 50mW; using 0V or V_{DD} at the digital inputs, the device dissipates less than $50\mu W$ at +5V and $150\mu W$ at +15V. At +15V it is CMOS compatible.

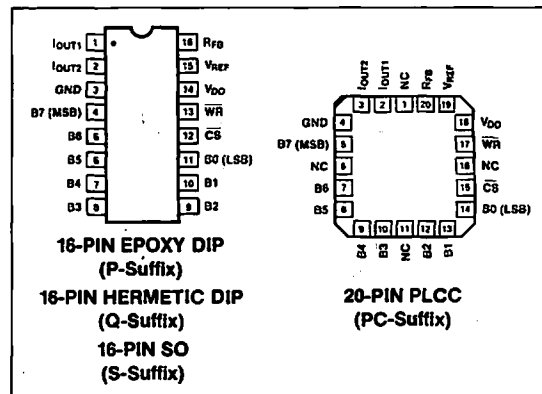
PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

The PM-7524 is manufactured using thin-film resistors on an advanced oxide-isolated silicon-gate CMOS process.

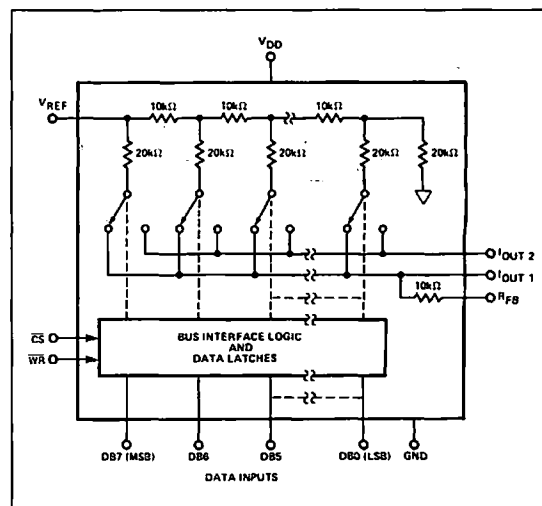
CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7524AQ PM7524BQ PM7524BQ	AD7524UD AD7524TD AD7524SD	MILITARY
PM7524EQ PM7524FQ PM7524FQ	AD7524CD AD7524BD AD7524AD	INDUSTRIAL
PM7524GP PM7524HP PM7524HP	AD7524LN AD7524KN AD7524JN	COMMERCIAL

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



**ABSOLUTE MAXIMUM RATINGS** ($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} (to GND)	−0.3V, +17V
V_{REF} (to GND)	±25V
R_{FB} (to GND)	±25V
Digital Input Voltage to GND	−0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2)	−0.3V to V_{DD}
Power Dissipation (Package)	
Ceramic (Suffix Q)	
To $+75^\circ\text{C}$	450mW
Derates Above $+75^\circ\text{C}$ By	6mW/ $^\circ\text{C}$
Plastic (Suffix P, PC, S)	
To $+70^\circ\text{C}$	670mW
Derates Above $+70^\circ\text{C}$ By	8.3mW/ $^\circ\text{C}$
Operating Temperature Range	
Military (AQ, BQ Versions)	−55 $^\circ\text{C}$ to $+125^\circ\text{C}$
Industrial (EQ, FQ Versions)	−25 $^\circ\text{C}$ to $+85^\circ\text{C}$
Commercial (GP, HP, HPC, HS Versions)	0 $^\circ\text{C}$ to $+70^\circ\text{C}$

Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	−65 $^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener protected, however, permanent damage may occur on unconnected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5\text{V}$ and $+15\text{V}$; $V_{REF} = +10\text{V}$; $V_{OUT1} = V_{OUT2} = 0\text{V}$; Limits apply to the Full Temperature Range for each grade shown: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ apply for PM-7524AQ/BQ/ARC/BRC; $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ apply for PM-7524EQ/FQ; $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for PM-7524GP/HP/HPC/HS; unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7524			UNITS		
			MIN	TYP	MAX			
STATIC ACCURACY								
Resolution	N		—	—	8	Bits		
Relative Accuracy (Notes 1, 2)	INL	$V_{DD} = +5V$						
		PM-7524A/E/G	—	—	±0.1	%FSR		
			—	—	(±1/4)	(LSB)		
		PM-7524B/F/H	—	—	±0.2	%FSR		
			—	—	(±1/2)	(LSB)		
		$V_{DD} = +15V$						
Gain Error (Note 3)	G_{FSE}	PM-7524A/E/G	—	—	±0.05	%FSR		
			—	—	(±1/8)	(LSB)		
		PM-7524B/F/H	—	—	±0.1	%FSR		
			—	—	(±1/4)	(LSB)		
		$V_{DD} = +5V$						
		PM-7524A/E/G	—	—	±0.4	%FSR		
Gain T.C. (Notes 4, 5)	TCG_{FS}		—	—	(±1)	(LSB)		
		PM-7524B/F/H	—	—	±0.8	%FSR		
			—	—	(±2)	(LSB)		
		$V_{DD} = +15V$						
		$T_A = +25^\circ C$	—	—	±0.4	%FSR		
			—	—	(±1)	(LSB)		
DC Power Supply Rejection ($\Delta\text{Gain}/\Delta V_{DD}$) (Notes 3, 6)	PSR	$T_A = \text{Full Temp. Range}$	—	—	±0.6	%FSR		
			—	—	(±1.5)	(LSB)		
		Output Leakage Current (I_{OUT1}, I_{OUT2}) (Notes 7, 8)	I_{LKG}	$T_A = +25^\circ C, V_{DD} = +5V, +15V$	—	—	10	
				$T_A = \text{Full Temp. Range}$				
REFERENCE INPUT	R_{IN}	$V_{DD} = +5V$	—	—	200	nA		
		$V_{DD} = +15V$	—	—	100			
		Input Resistance (Pin 15 to GND) (Note 11)		7	11	15	k Ω	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ and $+15V$; $V_{REF} = +10V$; $V_{OUT1} = V_{OUT2} = 0V$; Limits apply to the Full Temperature Range for each grade shown: $T_A = -55^{\circ}C$ to $+125^{\circ}C$ apply for PM-7524AQ/BQ/ARC/BRC; $T_A = -25^{\circ}C$ to $+85^{\circ}C$ apply for PM-7524EQ/FQ; $T_A = 0^{\circ}C$ to $+70^{\circ}C$ apply for PM-7524GP/HP/HPC/HS; unless otherwise noted. (Continued)

		PM-7524				
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current (Digital Inputs = X)	I _{DD}	X = V _{IL} or V _{IH}	—	—	1	mA
		X = 0V or V _{DD}	—	—	10	μA
		T _A = 25°C	—	—	25	
		T _A = Full Temp. Range	—	—		
ANALOG OUTPUTS						
Output Capacitance (Note 4)	C _O	DB0–DB7 = V _{DD} (Note 12)	—	—	120	pF
		C _{OUT1} (Pin 1)	—	—	30	
		C _{OUT2} (Pin 2)	—	—		
		DB0–DB7 = 0V (Note 13)	—	—	30	pF
		C _{OUT1}	—	—	120	
C _{OUT2}	—	—				
DIGITAL INPUTS						
Digital Inputs High	V _{IH}	V _{DD} = +5V V _{DD} = +15V	+2.4 +13.5	— —	—	V
Digital Inputs Low	V _{IL}	V _{DD} = +5V V _{DD} = +15V	— —	— —	+0.8 +1.5	V
Input Current (V _{IN} = 0V or V _{DD})	I _{IN}	T _A = 25°C T _A = Full Temp. Range	— —	— —	±1 ±10	μA
Input Capacitance (V _{IN} = 0V) (Note 4)	C _{IN}	DB0–DB7 WR, CS	— —	— —	5 20	pF
SWITCHING CHARACTERISTICS (Notes 4, 14)						
Chip Select to Write Setup Time (t _{WR} = t _{CS}) (Note 14)	t _{CS}	V _{DD} = +5V T _A = +25°C T _A = Full Temp. Range	170	—	—	nA
		PM-7524A/B	240	—	—	
		PM-7524E/F/G/H	220	—	—	
		V _{DD} = +15V T _A = +25°C T _A = Full Temp. Range	100	—	—	nA
		PM-7524A/B	150	—	—	
		PM-7524E/F/G/H	130	—	—	
Chip Select to Write Hold Time	t _{CH}		0	—	—	ns
Write Pulse Width (t _{CH} ≥ t _{WR} , t _{CH} ≥ 0)	t _{WR}	V _{DD} = +5V T _A = +25°C T _A = Full Temp. Range	150	—	—	ns
		PM-7524A/B	220	—	—	
		PM-7524E/F/G/H	200	—	—	
		V _{DD} = +15V T _A = +25°C T _A = Full Temp. Range	100	—	—	ns
		PM-7524A/B	150	—	—	
		PM-7524E/F/G/H	130	—	—	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ and $+15V$; $V_{REF} = +10V$; $V_{OUT1} = V_{OUT2} = 0V$; Limits apply to the Full Temperature Range for each grade shown: $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7524AQ/BQ/ARC/BRC; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7524EQ/FQ; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7524GP/HP/HPC/HS; unless otherwise noted. (Continued)

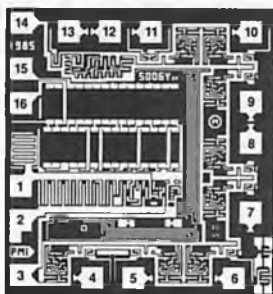
PARAMETER	SYMBOL	CONDITIONS	PM-7524			UNITS	
			MIN	TYP	MAX		
Data Setup Time	t_{OS}	$V_{DD} = +5V$					
		$T_A = +25^{\circ}C$	135	—	—	ns	
		$T_A = \text{Full Temp. Range}$	170	—	—		
		$V_{DD} = +15V$					
		$T_A = +25^{\circ}C$	60	—	—		
		$T_A = \text{Full Temp. Range}$				ns	
		PM-7524A/B	100	—	—		
		PM-7524E/F/G/H	80	—	—		
Data Hold Time	t_{DH}		10	—	—	ns	
DYNAMIC PERFORMANCE							
Propagation Delay (From Digital Input to 90% of Final Analog Output Current) (Notes 4, 9)	t_{PD}	$V_{DD} = +5V$					
		$T_A = +25^{\circ}C$	—	—	150		
		$T_A = \text{Full Temp. Range}$				ns	
		PM-7524A/B	—	—	200		
		PM-7524E/F/G/H	—	—	175		
		$V_{DD} = +15V$					
		$T_A = +25^{\circ}C$	—	—	65		
		$T_A = \text{Full Temp. Range}$				ns	
		PM-7524A/B	—	—	90		
		$V_{DD} = +5V$					
		$T_A = +25^{\circ}C$	—	—	300		
Output Current Settling Time (To 1/2 LSB) (Notes 4, 9, 15)	t_s	$T_A = \text{Full Temp. Range}$	—	—	350		
		$V_{DD} = +15V$				ns	
		$T_A = +25^{\circ}C$	—	—	200		
		$T_A = \text{Full Temp. Range}$	—	—	250		
		AC Feedthrough	FT	—	—	0.25	%FSR
		I_{OUT1}, I_{OUT2} (Note 4)					
Digital Charge Injection (Note 16)	Q	$V_{DD} = +5V$	—	50	—		
		$T_A = +25^{\circ}C$				nV/s	
		$V_{DD} = +15V$	—	55	—		
		$T_A = +25^{\circ}C$					

NOTES:

- Guaranteed monotonic over full temperature range and at $V_{DD} = +5V$ and $+15V$.
- FSR (Full Scale Range) = $V_{REF} - 1\text{LSB}$.
- Using internal feedback resistor.
- Guaranteed by design and not production tested.
- Gain TC measured from $+25^\circ C$ to T_{MIN} or from $+25^\circ C$ to T_{MAX} .
- $\Delta V_{DD} = \pm 10\%$.
- DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$; $V_{REF} = \pm 10V$, for I_{OUT1} .
- DB0-DB7 = V_{DD} ; $\overline{WR} = \overline{CS} = 0V$; $V_{REF} = \pm 10V$, for I_{OUT2} .
- I_{OUT1} load = 100Ω ; $C_{EXT} = 13pF$; $\overline{WR} = \overline{CS} = 0V$; DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V.
- $V_{REF} = \pm 10V$, $f = 100kHz$; DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$.
- Temperature coefficient approximately equals $+50ppm/^\circ C$.
- DB0-DB7 = V_{DD} ; $\overline{WR} = \overline{CS} = 0V$.
- DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$.
- See Timing Diagram.
- Extrapolated: t_s (1/2 LSB) = $t_{PD} + 6.2\tau$, where τ = the measured first time constant of the final RC decay.
- $V_{REF} = 0V$; Digital Inputs = 0V to V_{DD} .



DICE CHARACTERISTICS

DIE SIZE 0.070 × 0.076 inch, 5320 sq. mils
(1.78 × 1.93 mm, 3.43 sq. mm)

- | | |
|---------------|---------------------|
| 1. I_{OUT1} | 9. DB2 |
| 2. I_{OUT2} | 10. DB1 |
| 3. GND | 11. DB0 (LSB) |
| 4. DB7 (MSB) | 12. $\overline{CS}$ |
| 5. DB6 | 13. $\overline{WR}$ |
| 6. DB5 | 14. V_{DD} |
| 7. DB4 | 15. V_{REF} |
| 8. DB3 | 16. R_{FB} |

For additional DICE ordering information, refer to
1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +5V$ and $+15V$; $V_{REF} = +10V$; $V_{OUT1} = V_{OUT2} = 0V$; $T_A = +25^\circ C$.

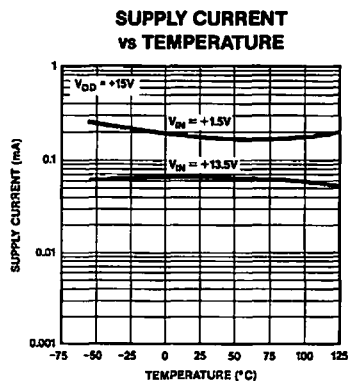
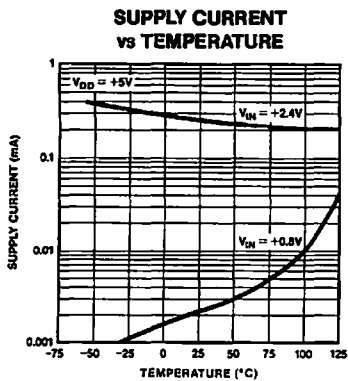
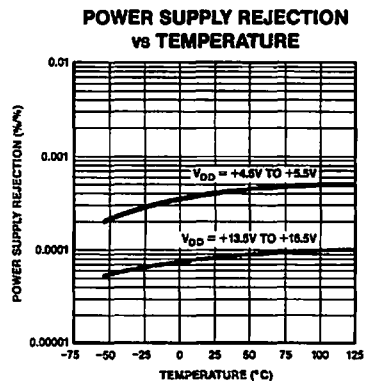
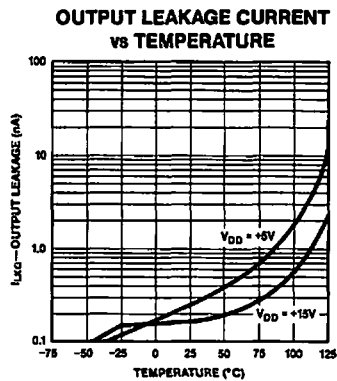
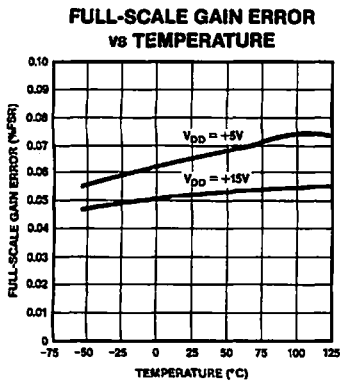
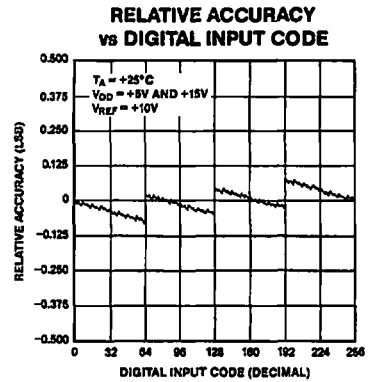
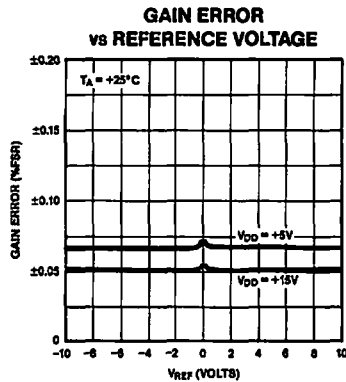
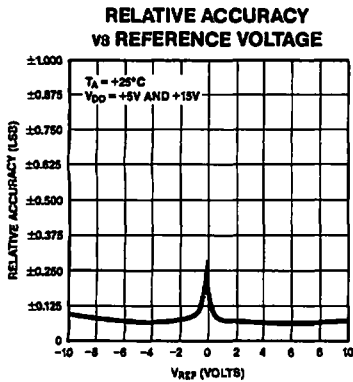
		PM-7524G	
PARAMETER	SYMBOL	CONDITIONS	UNITS
STATIC ACCURACY			
Resolution	N		8 Bits MIN
Relative Accuracy (Notes 1, 2)	INL	$V_{DD} = +5V$	± 0.2 %FSR (LSB) MAX
		$V_{DD} = +15V$	± 0.1 %FSR (LSB) MAX
Gain Error (Note 3)	G_{FSE}	$V_{DD} = +5V$	± 0.8 %FSR (LSB) MAX
		$V_{DD} = +15V$	± 0.4 %FSR (LSB) MAX
DC Power Supply Rejection Ratio ($\Delta \text{Gain}/\Delta V_{DD}$) (Notes 3, 4)	PSRR		0.01 %FSR/% MAX
Output Leakage Current (I_{OUT1}, I_{OUT2}) (Notes 5, 6)	I_{LKG}		10 nA MAX
REFERENCE INPUT			
Input Resistance	R_{IN}	(Note 7)	7/15 k Ω MIN/MAX
DIGITAL INPUTS			
Digital Inputs High	V_{IH}	$V_{DD} = +5V$ $V_{DD} = +15V$	+2.4 +13.5 V MIN
Digital Inputs Low	V_{IL}	$V_{DD} = +5V$ $V_{DD} = +15V$	+0.8 +1.5 V MAX
Input Current ($V_{IN} = 0V$ or V_{DD})	I_{IN}		± 1 μA
POWER SUPPLY			
Supply Current (Digital Inputs = X)	I_{DD}	X = V_{IL} or V_{IH}	1 mA
		X = 0V or V_{DD}	10 μA

NOTES:

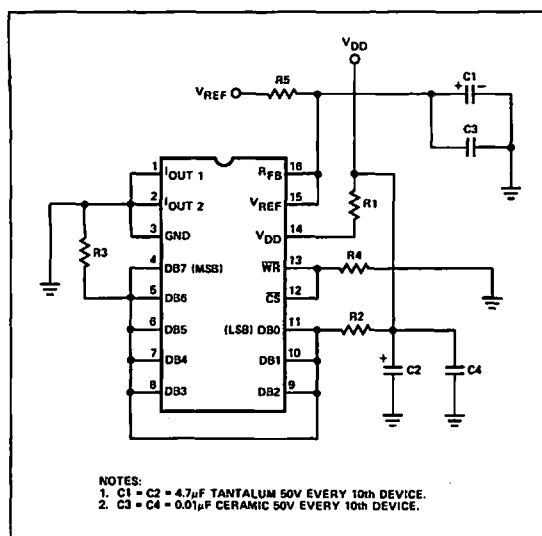
- Guaranteed monotonic over full temperature range and at $V_{DD} = +5V$ and $+15V$.
- FSR (Full Scale Range) = $V_{REF} - 1$ LSB.
- Using internal feedback resistor.
- $\Delta V_{DD} = \pm 10\%$.
- DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$; $V_{REF} = \pm 10V$, for I_{OUT1} .
- DB0-DB7 = V_{DD} ; $\overline{WR} = \overline{CS} = 0V$; $V_{REF} = \pm 10V$, for I_{OUT2} .
- Temperature coefficient approximately equals $+50\text{ppm}/^\circ C$.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS



BURN-IN CIRCUIT



DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where n is equal to the number of bits. Resolution in no way implies linearity.

RELATIVE ACCURACY

Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1 LSB.

PROPAGATION DELAY

The time for the output current to reach 90% of its final value from a given digital input signal.

SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when using the DAC's internal feedback resistor.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideal output is equal to $V_{REF} - 1$ LSB.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches off.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT

Current which appears on I_{OUT1} terminal with all digital inputs low or on I_{OUT2} terminal when all inputs are high.

CIRCUIT DESCRIPTION

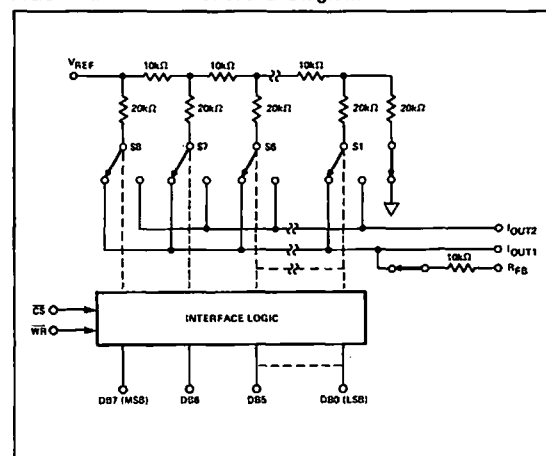
CIRCUIT INFORMATION

The PM-7524 is an 8-bit multiplying CMOS digital-to-analog converter with on-board data latches. It is fabricated using a highly stable thin-film R-2R resistor ladder network and eight N-channel current switches. A voltage or current reference and an operational amplifier are all that is required in the majority of applications.

Figure 1 shows a simplified circuit of the PM-7524 converter. The R-2R ladder, current steering switches, and interface logic are shown. The switches are binarily weighted and switch the ladder current between I_{OUT1} and I_{OUT2} bus lines; this switching allows a constant current to be maintained in each resistor leg regardless of the switch state.

The simplified circuit of Figure 1 also shows the matching switches in series with the ladder terminating and R_{FB} (feedback) resistors. These switches are designed to temperature-track the ladder current-steering switches and improve power supply rejection. Both switches are MOS transistors that have their gate turn-on voltage derived from V_{DD} supply. This means the terminating and feedback resistors are open-circuit when V_{DD} power is off. If R_{FB} is used as part of an op amp's feedback element, and the op amp's supply comes on before the DAC, the op amp's output will go to the rails. It remains in this open-loop condition until the DAC's V_{DD} is applied. In applications where the op amp's supply must come on before the DAC, a voltage clamp or external feedback resistor may be necessary.

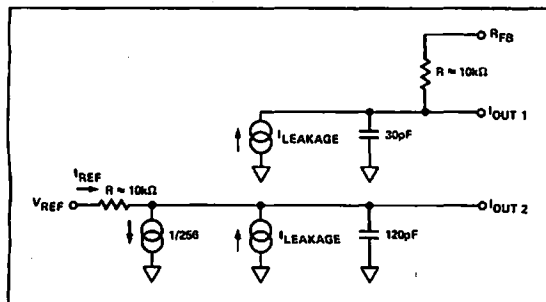
FIGURE 1: PM-7524 Functional Diagram



EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an equivalent circuit for the PM-7524 with all digital inputs LOW. The I_{OUT1} and I_{OUT2} leakage current source is the combination of surface and junction leakages to the substrate. The $1/256$ current source represents the constant 1-bit current drain through the ladder termination resistor. The situation is reversed with all digital inputs HIGH, i.e., the current output is now switched to the I_{OUT1} terminal. The output capacitance is dependent upon the digital input code, and is therefore modulated between the low and high values.

FIGURE 2: PM-7524 Equivalent Circuit
(All Digital Inputs LOW)



INTERFACE LOGIC

MODE SELECTION

The mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

The PM-7524 is in the WRITE mode when both the $\overline{CS}$ and $\overline{WR}$ are both LOW; the input latches are transparent and the output immediately follows the data input logic. See the MODE SELECTION TABLE.

MODE SELECTION TABLE

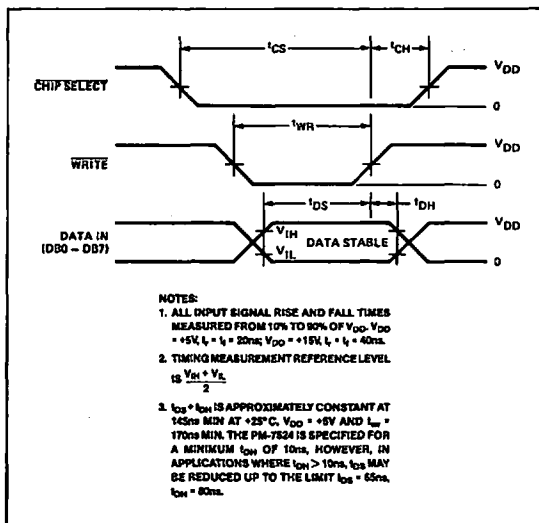
$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	WRITE	DAC responds to data bus (DB0—DB7) inputs (transparent)
H	X	HOLD	Data bus (DB0—DB7) is locked out
X	H	HOLD	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumes a HIGH state

L = Low State, H = High State, X = Don't Care.

HOLD MODE

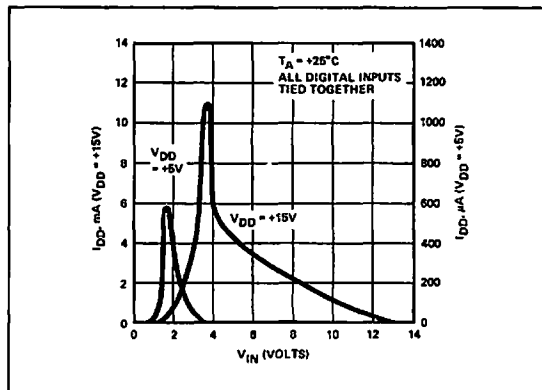
The MODE SELECTION TABLE shows the output results when either $\overline{CS}$ or $\overline{WR}$ is HIGH. The output holds the value corresponding to the last digital inputs prior to $\overline{CS}$ or $\overline{WR}$ assuming the HIGH state.

WRITE CYCLE TIMING DIAGRAM

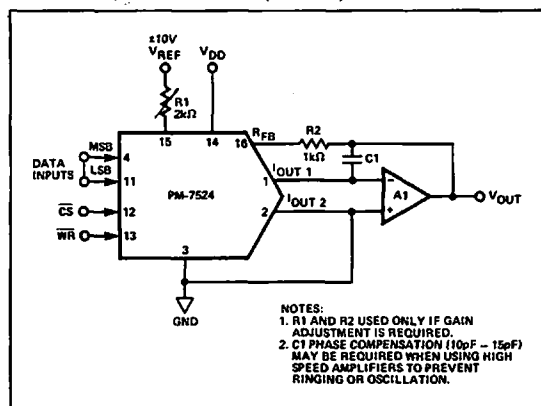


Supply current (I_{DD}) versus Logic input voltage (V_{IN}) is shown in Figure 3. This plot shows the supply current for both $V_{DD} = +5V$ and $V_{DD} = +15V$.

FIGURE 3: Supply Current vs Logic Level



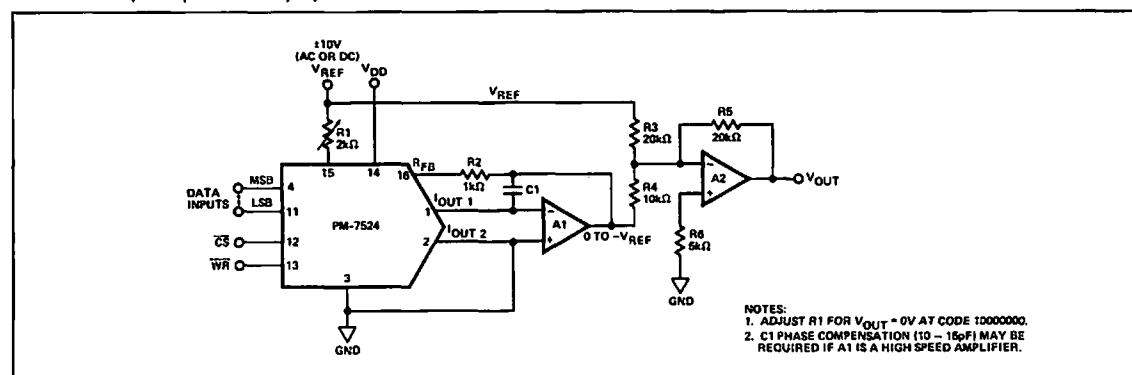
APPLICATIONS

**FIGURE 4: Unipolar Binary Operation
(2-Quadrant Multiplication)**

TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT		
MSB	LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1		$-V_{REF} \left(\frac{255}{256} \right)$
1 0 0 0 0 0 0 1		$-V_{REF} \left(\frac{129}{256} \right)$
1 0 0 0 0 0 0 0		$-V_{REF} \left(\frac{128}{256} \right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1		$-V_{REF} \left(\frac{127}{256} \right)$
0 0 0 0 0 0 0 1		$-V_{REF} \left(\frac{1}{256} \right)$
0 0 0 0 0 0 0 0		$-V_{REF} \left(\frac{0}{256} \right) = 0$

NOTE:

$$1\text{LSB} = (2^{-8}) (V_{REF}) = \frac{1}{256} (V_{REF})$$

FIGURE 5: Bipolar (4-Quadrant) Operation

TABLE 2: Bipolar (Offset Binary) Code Table

DIGITAL INPUT		
MSB	LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1		$+V_{REF} \left(\frac{127}{128} \right)$
1 0 0 0 0 0 0 1		$+V_{REF} \left(\frac{1}{128} \right)$
1 0 0 0 0 0 0 0		0
0 1 1 1 1 1 1 1		$-V_{REF} \left(\frac{1}{128} \right)$
0 0 0 0 0 0 0 1		$-V_{REF} \left(\frac{127}{128} \right)$
0 0 0 0 0 0 0 0		$-V_{REF} \left(\frac{128}{128} \right)$

NOTE:

$$1\text{LSB} = (2^{-7}) (V_{REF}) = \frac{1}{128} (V_{REF})$$

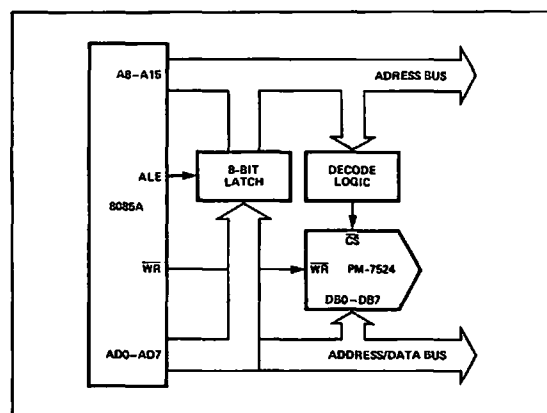
FIGURE 6: PM-7524/8085A Interface


FIGURE 7: PM-7524/MC6800 Interface

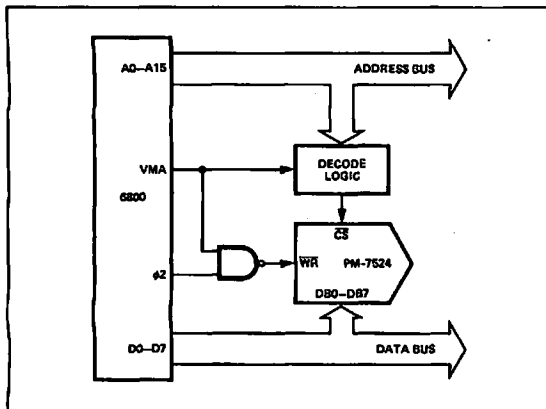
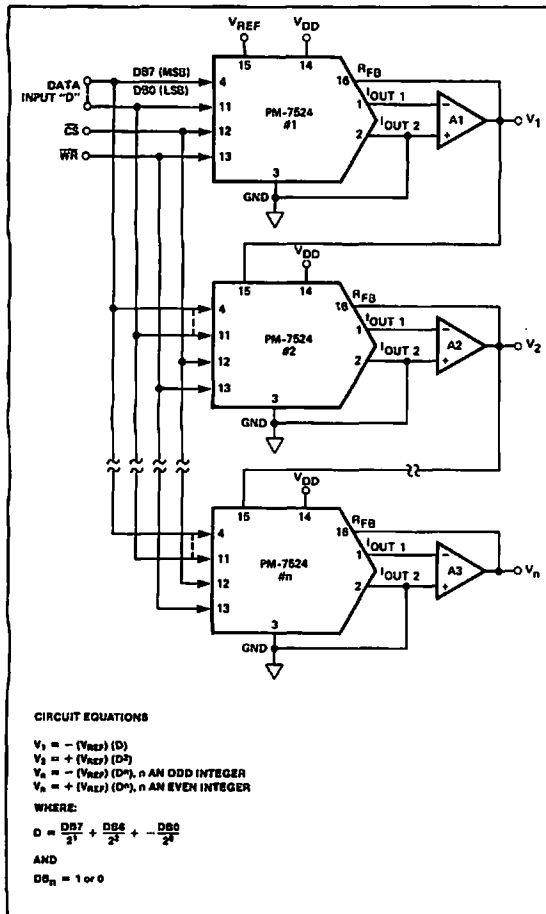
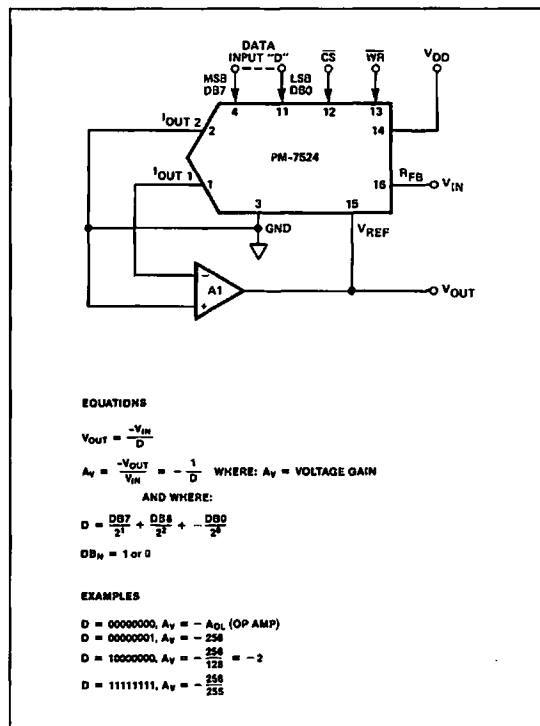


FIGURE 8: Power Generation Connection


 FIGURE 9: Divider
(Digitally Controlled Gain)




PM-7528

DUAL 8-BIT BUFFERED
MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- On-Chip Latches For Both DACs
- +5V To +15V Single Supply Operation
- DACs Matched To 1%
- Four-Quadrant Multiplication
- TTL/CMOS Compatible
- 8-Bit Endpoint Linearity ($\pm 1/2$ LSB)
- Full Temperature Operation
- Low Power Consumption
- Microprocessor Compatible
- Improved ESD Resistance
- Automatically Insertable Cerdip and Plastic Packages
- Available in Surface Mount SO, PLCC and LCC Packages

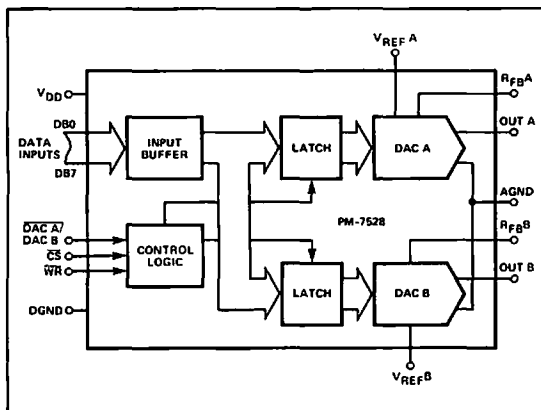
APPLICATIONS

- Digital Gain/Attenuation Control
- Digital Control Of Filter Parameters
- Digitally-Controlled Audio Circuits
- X-Y Graphics
- Digital/Synchro Conversion
- Robotics
- Ideal For Battery-Operated Equipment

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7528AR	AD7528UD	MILITARY
PM7528BR	AD7528TD	
PM7528BR	AD7528SD	
PM7528ER	AD7528CQ	INDUSTRIAL
PM7528FR	AD7528BQ	
PM7528FR	AD7528AQ	
PM7528GP	AD7528LN	COMMERCIAL
PM7528HP	AD7528KN	
PM7528HP	AD7528JN	
PM7528HPC	AD7528KP	
PM7528HPC	AD7528JP	

FUNCTIONAL DIAGRAM



ORDERING INFORMATION†

PACKAGE: 20-PIN				
RELATIVE ACCURACY	GAIN ERROR	MILITARY* TEMPERATURE -55°C TO +125°C	INDUSTRIAL TEMPERATURE -25°C TO +85°C	COMMERCIAL TEMPERATURE 0°C TO +70°C
$\pm 1/2$ LSB	± 1 LSB	PM7528AR	PM7528ER	PM7528GP
$\pm 1/2$ LSB	± 1 LSB	PM7528ARC/883	—	—
$\pm 1/2$ LSB	± 2 LSB	PM7528BR	PM7528FR	PM7528HP
$\pm 1/2$ LSB	± 2 LSB	PM7528BRC/883	—	PM7528HPC††
$\pm 1/2$ LSB	± 2 LSB	—	—	PM7528HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

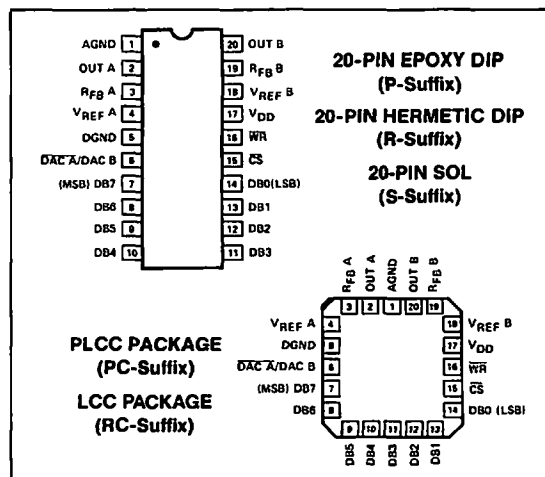
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The PM-7528 contains two 8-bit multiplying digital-to-analog converters. Excellent DAC-to-DAC matching and tracking results from monolithic construction. The PM-7528 consists of two thin-film R-2R resistor-ladder networks, tracking span resistors, two data latches, one input buffer, and control logic. Operation from a 5 to 15 volt single power supply dissipates only 20mW of power in a space saving 20-pin 0.3" wide DIP. The PM-7528 features circuitry designed to protect against damage from electrostatic discharges.

Digital input data is directed into one of the DAC data latches determined by the DAC selection control line $\overline{\text{DAC A/DAC B}}$. The 8-bit wide input data path provides TTL/CMOS compatibility. The data load cycle is similar to the write cycle of a random access memory. The PM-7528 is bus compatible with most 8-bit microprocessors, including the 6800, 8080, 8085, and Z80.

PIN CONNECTIONS



**ABSOLUTE MAXIMUM RATINGS**(T_A = +25°C, unless otherwise noted.)

V _{DD} to AGND	0V, +17V
V _{DD} to DGND	0V, +17V
AGND to DGND	0V, V _{DD}
Digital Input Voltage to DGND	-0.3V, +15V
V _{PIN 2} , V _{PIN 20} to AGND	-0.3V, +15V
V _{REF A} , V _{REF B} to AGND	±25V
V _{RFB A} , V _{RFB B} to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derate Above +75°C by	6mW/°C
Operating Temperature Range	
AR, ARC, BR, BRC Versions	-55°C to +125°C
ER, FR Versions	-25°C to +85°C
GP, HP, HPC, HS Versions	0°C to +70°C

Die Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets; remove power before insertion or removal.
4. Use proper anti-static handling procedures.
5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REF A} = V_{REF B} = +10V, OUT A = OUT B = 0V; T_A = -55°C to +125°C apply for PM-7528AR/ARC/BR/BRC; T_A = -25°C to +85°C apply for PM-7528ER/FR; T_A = 0°C to +70°C apply for PM-7528GP/HP/HPC/HS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7528			UNITS	
			MIN	TYP	MAX		
STATIC ACCURACY (Note 1)							
Resolution	N		8	—	—	Bits	
Relative Accuracy (Note 2)	NL		—	—	±1/2	LSB	
Differential Nonlinearity (Note 3)	DNL		—	—	±1	LSB	
Full Scale Gain Error (Note 4)	G _{FSE}	T _A = +25°C	PM7528A/E/G	—	—	±1	LSB
			PM7528B/F/H	—	—	±2	
		V _{DD} = +5V	PM7528A/E/G	—	—	±3	
		T _A = Full Temp. Range	PM7528B/F/H	—	—	±4	
		V _{DD} = +15V	PM7528A/E/G	—	—	±1	
		T _A = Full Temp. Range	PM7528B/F/H	—	—	±3	
Gain Temperature Coefficient (ΔGain/ΔTemperature) (Notes 4, 10)	TCG _{FS}	V _{DD} = +5V V _{DD} = +15V	— —	— —	±0.007 +0.0035	%/°C	
Output Leakage Current Out A (Pin 2)/Out B (Pin 20) (Note 5)	I _{LKG}	T _A = +25°C	—	5	±50	nA	
		V _{DD} = +5V	—	—	±400		
		T _A = Full Temp. Range	—	—	±400		
		V _{DD} = +15V	—	—	+200		
Input Resistance (V _{REF} A, V _{REF} B) (Note 6)	R _{REF}		8	—	15	kΩ	
V _{REF} A/V _{REF} B (Input Resistance Match)	ΔV _{REF} A, B		—	0.1	±1	%	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^{\circ}C$ to $+125^{\circ}C$ apply for PM-7528AR/ARC/BR/BRC; $T_A = -25^{\circ}C$ to $+85^{\circ}C$ apply for PM-7528ER/FR; $T_A = 0^{\circ}C$ to $+70^{\circ}C$ apply for PM-7528GP/HP/HPC/HS, unless otherwise noted. (Continued)

			PM-7528			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (Note 9)						
Digital Input High (Note 8)	V_{INH}	$V_{DD} = +5V$ $V_{DD} = +15V$	2.4 13.5	— —	— —	V
Digital Input Low (Note 8)	V_{INL}	$V_{DD} = +5V$ $V_{DD} = +15V$	— —	— —	0.8 1.5	V
Input Current (Note 7)	I_{IN}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	— —	.001 —	± 1 ± 10	μA
Input Capacitance (Note 10)	C_{IN}	DB0-DB7 WR, CS, DAC A/DAC B	— —	— —	10 15	pF
SWITCHING CHARACTERISTICS at $V_{DD} = +5V$ (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	200 230	— —	— —	ns
Chip Select to Write Hold Time	t_{CH}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	20 30	— —	— —	ns
DAC Select to Write Set-Up Time	t_{AS}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	200 230	— —	— —	ns
DAC Select to Write Hold Time	t_{AH}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	20 30	— —	— —	ns
Data Valid to Write Set-Up Time	t_{DS}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	110 130	— —	— —	ns
Data Valid to Write Hold Time	t_{DH}		0	—	—	ns
Write Pulse Width	t_{WR}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	180 200	— —	— —	ns
SWITCHING CHARACTERISTICS at $V_{DD} = +15V$ (Notes 10, 11)						
Chip Select to Write Set-Up Time	t_{CS}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	60 80	— —	— —	ns
Chip Select to Write Hold Time	t_{CH}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	10 15	— —	— —	ns
DAC Select to Write Set-Up Time	t_{AS}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	60 80	— —	— —	ns
DAC Select to Write Hold Time	t_{AH}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	10 15	— —	— —	ns
Data Valid to Write Set-Up Time	t_{DS}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	50 70	— —	— —	ns
Data Valid to Write Hold Time	t_{DH}		10	—	—	ns
Write Pulse Width	t_{WR}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	60 80	— —	— —	ns



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7528AR/ARC/BR/BRC; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7528ER/FR; $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7528GP/HP/HPC/HS, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7528			UNITS
			MIN	TYP	MAX	
POWER SUPPLY (Note 12)						
Supply Current (Note 21)	I _{DD}	All Digital Inputs V _{INL} or V _{INH}	—	—	1	mA
		All Digital Inputs 0V or V _{DD}	—	—	100	μA
AC PERFORMANCE CHARACTERISTICS (Note 13)						
DC Supply Rejection Ratio (ΔGain/ΔV _{DD}) (Note 14)	PSRR	V _{DD} = +5V	—	—	0.02	%/%
		T _A = +25°C	—	—	0.04	
		T _A = Full Temp. Range	—	—	0.01	
		V _{DD} = +15V	—	—	0.02	
Propagation Delay (Notes 15, 16, 17)	t _{pD}	T _A = +25°C	—	—	220	ns
		T _A = Full Temp. Range	—	—	270	
		V _{DD} = +15V	—	—	80	
		T _A = +25°C	—	—	100	
Current Settling Time (Notes 16, 17, 22)	t _s	T _A = Full Temp. Range	—	—	350	ns
		V _{DD} = +15V	—	—	400	
		T _A = +25°C	—	—	180	
		T _A = Full Temp. Range	—	—	200	
Digital Charge Injection (Note 18)	Q	T _A = +25°C	—	160	—	nC
		V _{DD} = +5V	—	440	—	
		V _{DD} = +15V	—	—	—	
Output Capacitance	C _{OUT A}	DAC Latches Loaded	—	—	50	pF
	C _{OUT B}	with 00000000	—	—	50	
	C _{OUT A}	DAC Latches Loaded	—	—	120	
	C _{OUT B}	with 11111111	—	—	120	
AC Feedthrough (Note 19)	FT _A	V _{REF A} to OUT A;	—	—	−70	dB
		T _A = +25°C	—	—	−65	
	FT _B	T _A = Full Temp. Range	—	—	−65	
		V _{REF B} to OUT B;	—	—	−70	
		T _A = +25°C	—	—	−70	
		T _A = Full Temp. Range	—	—	−65	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = -55^{\circ}C$ to $+125^{\circ}C$ apply for PM-7528AR/ARC/BR/BRC; $T_A = -25^{\circ}C$ to $+85^{\circ}C$ apply for PM-7528ER/FR; $T_A = 0^{\circ}C$ to $+70^{\circ}C$ apply for PM-7528GP/HP/HPC/HS, unless otherwise noted. (Continued)

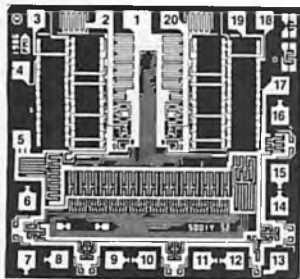
			PM-7528			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE CHARACTERISTICS						
(Note 13)						
Channel-to-Channel Isolation (Note 20)	CCI _{BA}	V _{REF} A to OUT B; V _{REF} A = 20V _{p-p} Sinewave @ f = 100kHz V _{REF} B = 0V. T _A = +25°C	—	−77	—	dB
	CCI _{AB}	V _{REF} B to OUT A; V _{REF} B = 20V _{p-p} Sinewave @ f = 100kHz V _{REF} A = 0V. T _A = +25°C	—	−77	—	
Digital Crosstalk	Q	For Code Transition From 00000000 to 11111111. T _A = +25°C	—	30	—	nVs
		V _{DD} = +5V V _{DO} = +15V	—	60	—	
Harmonic Distortion	THD	V _{IN} = 6Vrms @ f = 1kHz. T _A = +25°C	—	−85	—	dB

NOTES:

- Specifications apply to both DAC A and DAC B.
- This is an endpoint linearity specification.
- All grades guaranteed to be monotonic over the full operating temperature range.
- Measured using internal $R_{FB A}$ and $R_{FB B}$. Both DAC latches loaded with 11111111. Gain error is adjustable using circuits of Figures 5 and 6.
- DAC loaded with 00000000.
- Input resistance $TC = +50ppm/^{\circ}C$; typical input resistance = 11k Ω .
- $V_{IN} = 0V$ or V_{DD} .
- For all data bits DB0-DB7, $\overline{WR}$, $\overline{CS}$, $\overline{DAC A}$ /DAC B.
- Logic inputs are MOS gates. Typical input current ($+25^{\circ}C$) is less than 1nA.
- Guaranteed and not tested.
- See timing diagram.
- See Figure 3.
- These characteristics are for design guidance only and are not subject to test.
- $\Delta V_{DD} = \pm 5\%$.
- From digital input to 90% of final analog-output current.
- $V_{REF A} = V_{REF B} = +10V$; $OUT A$, $OUT B$ load = 100 Ω , $C_{EXT} = 13pF$.
- $\overline{WR}$, $\overline{CS} = 0V$, DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V.
- For code transition 00000000 to 11111111.
- $V_{REF A}$, $V_{REF B} = 20V_{p-p}$ Sinewave @ $f = 100kHz$.
- Both DAC latches loaded with 11111111.
- $I_{DD} = 500\mu A$ at $T_A = Full$ Temp. Range.
- Extrapolated: $t_b (1/2 LSB) = t_p D + 6.2\tau$, where τ = the measured first time constant of the final RC decay.



DICE CHARACTERISTICS



DIE SIZE 0.086 × 0.092 Inch, 7,192 sq. mils
(2.184 × 2.337 mm, 5,105 sq. mm)

- | | |
|---|--|
| 1. ANALOG GROUND (AGND) | 11. DIGITAL INPUT DB3 |
| 2. OUTPUT A (OUT A) | 12. DIGITAL INPUT DB2 |
| 3. DAC A FEEDBACK RESISTOR ($R_{FB A}$) | 13. DIGITAL INPUT DB1 |
| 4. DAC A REFERENCE INPUT ($V_{REF A}$) | 14. DIGITAL INPUT DB0 (LSB) |
| 5. DIGITAL GROUND (DGND) | 15. CHIP SELECT ($\overline{CS}$) |
| 6. DIGITAL SELECTION (DAC A/DAC B) | 16. WRITE ($\overline{WR}$) |
| 7. DIGITAL INPUT DB7 (MSB) | 17. POSITIVE POWER SUPPLY (V_{DD}) |
| 8. DIGITAL INPUT DB6 | 18. DAC B REFERENCE INPUT ($V_{REF B}$) |
| 9. DIGITAL INPUT DB5 | 19. DAC B FEEDBACK RESISTOR ($R_{FB B}$) |
| 10. DIGITAL INPUT DB4 | 20. OUTPUT B (OUT B) |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7528G	UNITS
			LIMIT	
Relative Accuracy	NL	Endpoint Linearity Error	$\pm \frac{1}{2}$	LSB MAX
Differential Nonlinearity	DNL		± 1	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 11111111	± 2	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 00000000 Pad 2 and 20	± 50	nA MAX
Input Resistance	R_{REF}	Pad 4 and 18	8/15	K Ω MIN/ K Ω MAX
$V_{REF A}/V_{REF B}$ Input Resistance Match	$\Delta V_{REF A, B}$		± 1	% MAX
Digital Input High	V_{IH}	$V_{DD} = 5V$ $V_{DD} = 15V$	2.4 13.5	V_{MIN}
Digital Input Low	V_{IL}	$V_{DD} = 5V$ $V_{DD} = 15V$	0.8 1.5	V_{MAX}
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD}	± 1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs $0V$ or V_{DD}	1 0.1	mA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSRR	$V_{DD} = \pm 5\%$	0.02	%/% MAX

NOTE:

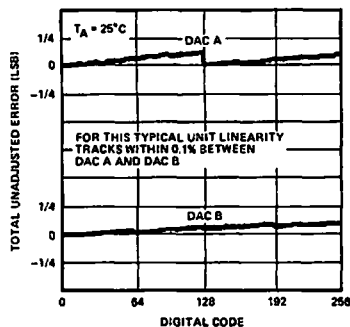
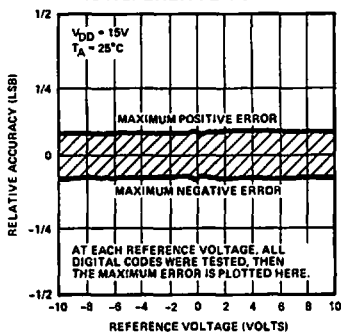
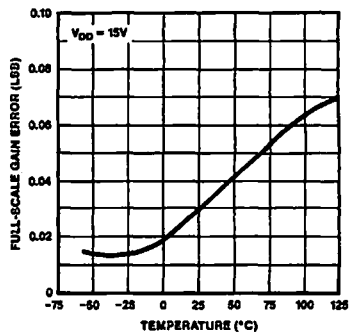
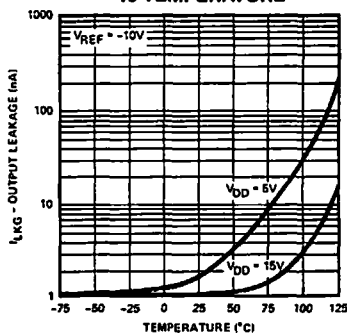
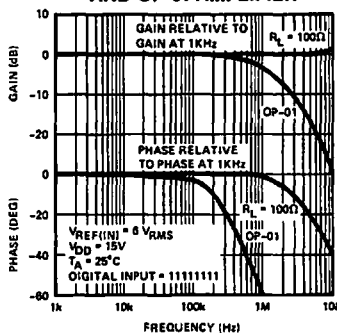
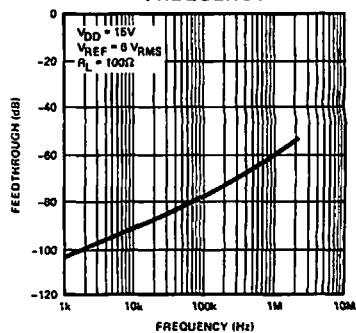
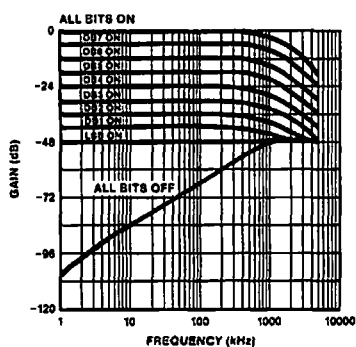
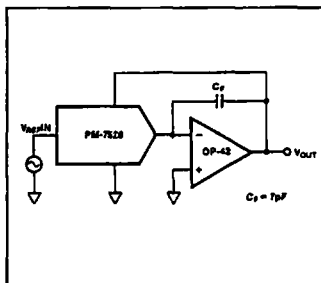
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $OUT A = OUT B = 0V$; $T_A = 25^\circ C$, unless otherwise noted. (Note 13)

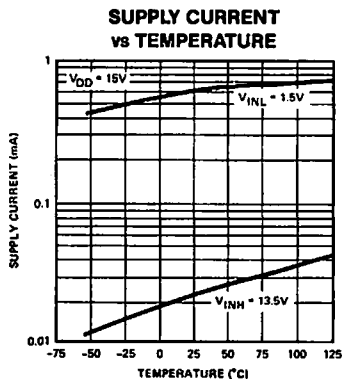
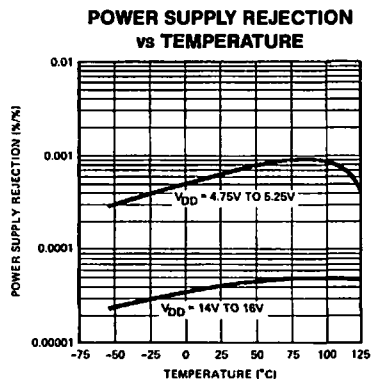
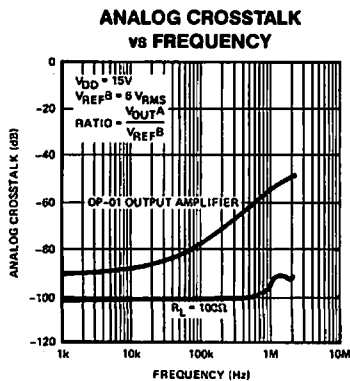
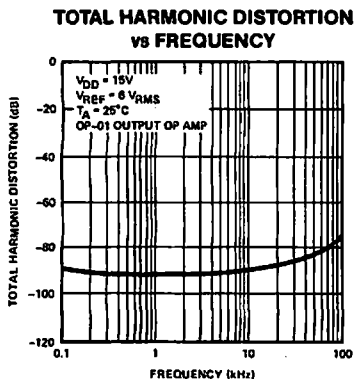
PARAMETER	SYMBOL	CONDITIONS	PM-7528G	UNITS
			TYPICAL	
Digital Input Capacitance	C_{IN}		6	pF
Output Capacitance	$C_{OUT A}$	DAC Latches Loaded with 00000000	22	pF
	$C_{OUT B}$		22	
	$C_{OUT A}$	DAC Latches Loaded with 11111111	40	pF
	$C_{OUT B}$		40	
Propagation Delay (Notes 15, 16, 17)	t_{PD}	$V_{DD} = 15V$	70	ns
		$V_{DD} = 5V$	150	



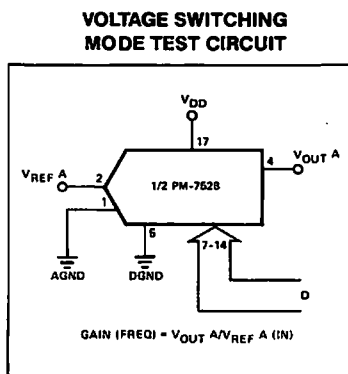
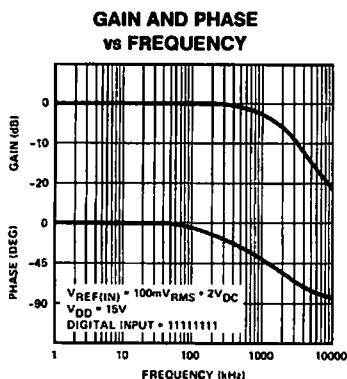
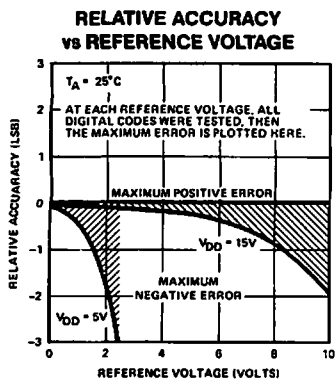
TYPICAL PERFORMANCE CHARACTERISTICS

TOTAL UNADJUSTED ERROR
vs DIGITAL INPUTRELATIVE ACCURACY
vs REFERENCE VOLTAGEFULL-SCALE GAIN ERROR
vs TEMPERATUREOUTPUT
LEAKAGE CURRENT
vs TEMPERATUREGAIN AND PHASE SHIFT
vs FREQUENCY
WITH RESISTIVE LOAD
AND OP-01 AMPLIFIERFEEDTHROUGH vs
FREQUENCYGAIN (V_{OUT}/V_{REFIN})
vs FREQUENCYTEST CIRCUIT
FOR GAIN vs FREQUENCY

TYPICAL PERFORMANCE CHARACTERISTICS



VOLTAGE SWITCHING MODE CHARACTERISTICS



PARAMETER DEFINITIONS

RELATIVE ACCURACY

Relative accuracy, or endpoint nonlinearity, is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale, and is normally expressed in LSB's or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error, or full-scale error, is a measure of the output error between an ideal DAC and the actual device output. The ideal full-scale output is V_{REF} minus 1 LSB. Gain error of both DAC's in the PM-7528 is adjustable to zero with external resistance.

OUTPUT CAPACITANCE

Capacitance from OUT A or OUT B to AGND.

DIGITAL CHARGE INJECTION

The amount of charge injected from the digital inputs to the analog output when the inputs change states. This is normally specified as the area of the glitch in either pAsecs or nVsecs, depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{REF} A, V_{REF} B = AGND.

PROPAGATION DELAY

This is a measure of the internal delays of the circuit. It is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

CHANNEL-TO-CHANNEL ISOLATION

The portion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

DIGITAL CROSSTALK

The glitch energy transferred to the output of one converter, due to a change in digital input code to the other converter, specified in nVsec.

AC FEEDTHROUGH

AC signal due to capacitive coupling from V_{REF} to output with all switches "off."

INTERFACE LOGIC INFORMATION

DAC SELECTION

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A/DAC B}}$ selects which DAC can accept data from the input port.

MODE SELECTION

The inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

WRITE MODE

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low, the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data on the data bit lines DB0-DB7.

HOLD MODE

The selected DAC latch retains the data which was present on the data lines just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

MODE SELECTION TABLE

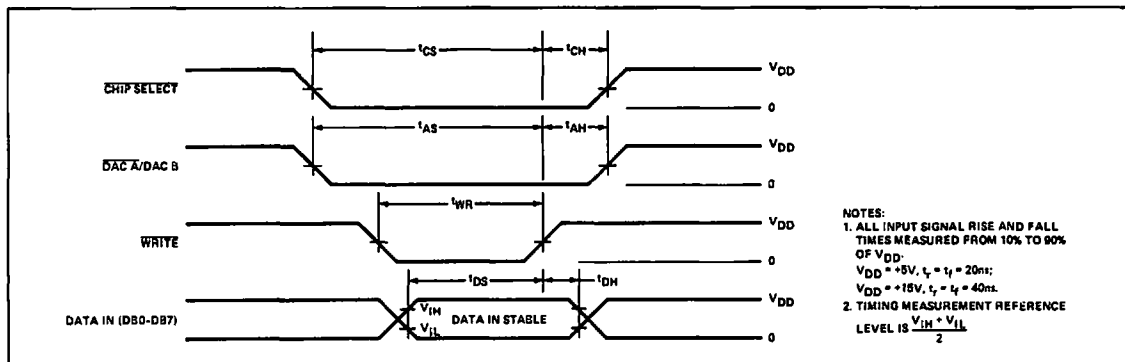
DAC A/DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

CIRCUIT INFORMATION—D/A SECTION

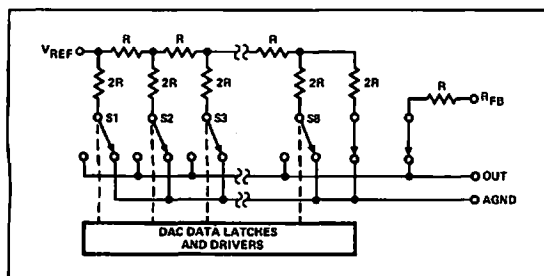
The PM-7528 contains two identical 8-bit multiplying digital-to-analog converters, DAC A and DAC B. Each DAC includes a stable thin-film R-2R resistor ladder and eight NMOS current steering switches. Figure 1 shows a simplified equivalent circuit

WRITE CYCLE TIMING DIAGRAM



of either DAC. The inverted R-2R ladder takes a voltage or current reference and divides it in a binary manner among the eight current steering switches. The number of switches selected to the output (OUT) add their currents together forming an analog output current representation of the switch selection. The DAC OUT and analog ground (AGND) should be maintained at the same voltage for proper operation. The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves linearity performance over temperature and power supply rejection; however when the circuit is not powered up the switch assumes an open state.

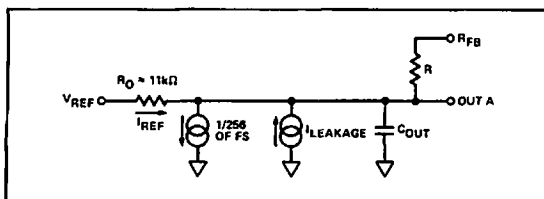
FIGURE 1: Simplified functional circuit for DAC A or DAC B.



EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit of DAC A shown in Figure 2 is similar to DAC B. DAC A and DAC B both share the analog ground pin 1 (AGND). With all digital inputs high, the reference current flows to OUT A. A small leakage current ($I_{LEAKAGE}$) flows across internal junctions, doubling every 10°C . The R-2R ladder termination resistor generates a constant $1/256$ current which is 1 LSB of the reference current (I_{REF}). C_{OUT} is the parallel combination of the NMOS current steering switches. The value of C_{OUT} depends on the number of switches connected to the output. The range of C_{OUT} is 50pF to 120pF maximum. The equivalent output resistance R_O varies with input code from $0.8R$ to $3R$, where R is the nominal ladder resistor of the R-2R ladder.

FIGURE 2: PM-7528 DAC A equivalent circuit. All digital inputs high.

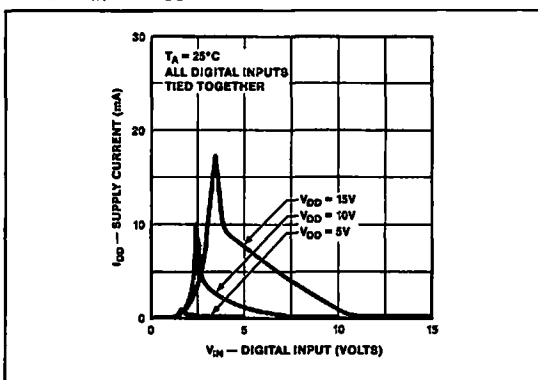


CIRCUIT INFORMATION—DIGITAL SECTION

The digital inputs provide TTL input compatibility ($V_{INH} = 2.4$, $V_{INL} = 0.8\text{V}$) when the PM-7528 operates with V_{DD} of +5V. The digital inputs effect the amount of quiescent supply current as shown in Figure 3. Peak supply current occurs as the digital input (V_{IN}) passes through the transition voltage. Maintaining the digital input voltages as close as possible to the supplies (V_{DD} and DGND) minimizes supply current consumption. When operating the PM-7528 from CMOS logic the digital inputs are driven very close to the supply rails, minimizing power consumption.

Digital input protection from electrostatic discharge and electrostatic buildup occurs in the input network shown in Figure 4.

FIGURE 3: Typical plots of supply current, I_{DD} vs logic input voltage (V_{IN}), for $V_{DD} = +5\text{V}$, $+10\text{V}$, and $+15\text{V}$.



BURN-IN CIRCUIT

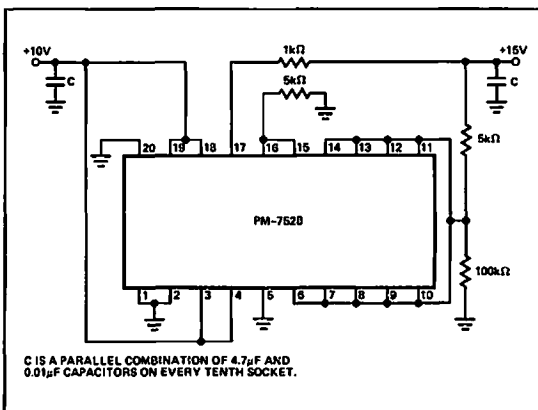
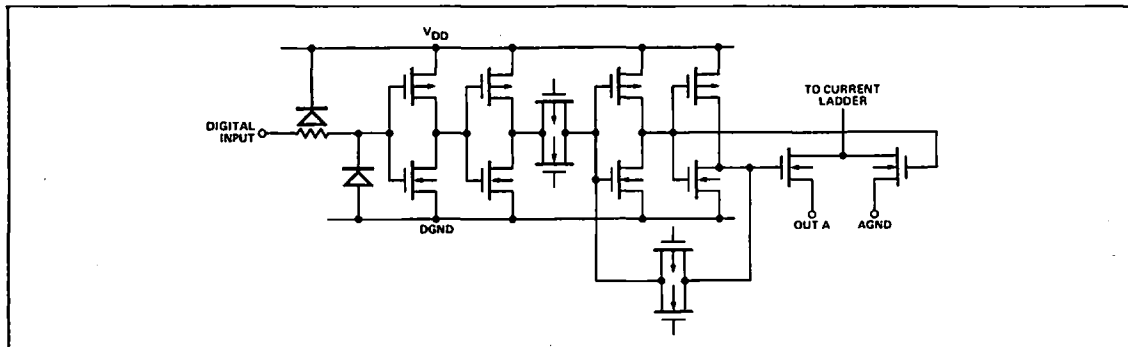


FIGURE 4: Simplified equivalent gate-input protection circuit. One of eight current switches, and its associated internal CMOS-drive-circuitry, is shown.



APPLICATIONS INFORMATION

The most common application of this DAC is voltage output operation. Unipolar output operation provides a 0 to 10 volt output swing when connected, as shown in Figure 5. The maximum output voltage polarity is the inverse of the input reference voltage, since the op amp inverts the input currents. The transfer equation for unipolar operation is $V_{OUT} = -V_{IN} \times D/256$, where D is the decimal value of the data bit inputs DB0 thru DB7 and V_{IN} is the reference input voltage. The transfer equation highlights another popular application of CMOS DAC's, multiplication. The output voltage is the product of the reference voltage and the digital input code. The reference input voltage can be any value in the range of ± 25 volts for both

DC or AC signals. The circuit in Figure 5 performs two-quadrant multiplication. Table 1 provides example analog outputs for the given digital input codes.

For bipolar output operation connect the PM-7528 as shown in Figure 6. This circuit configuration provides an offset current, derived from the reference, to enable the output op amp to swing in both polarities. The digital input coding becomes offset binary. Table 2 provides some example analog outputs for various digital inputs (D). The transfer equation for bipolar operation is $V_{OUT} = V_{IN} \times (D/128 - 1)$, where D is the decimal value of the data bit inputs DB0 thru DB7. This circuit provides full four-quadrant multiplication able to accept both polarities on all inputs as well as the circuit output.

FIGURE 5: Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table 1.

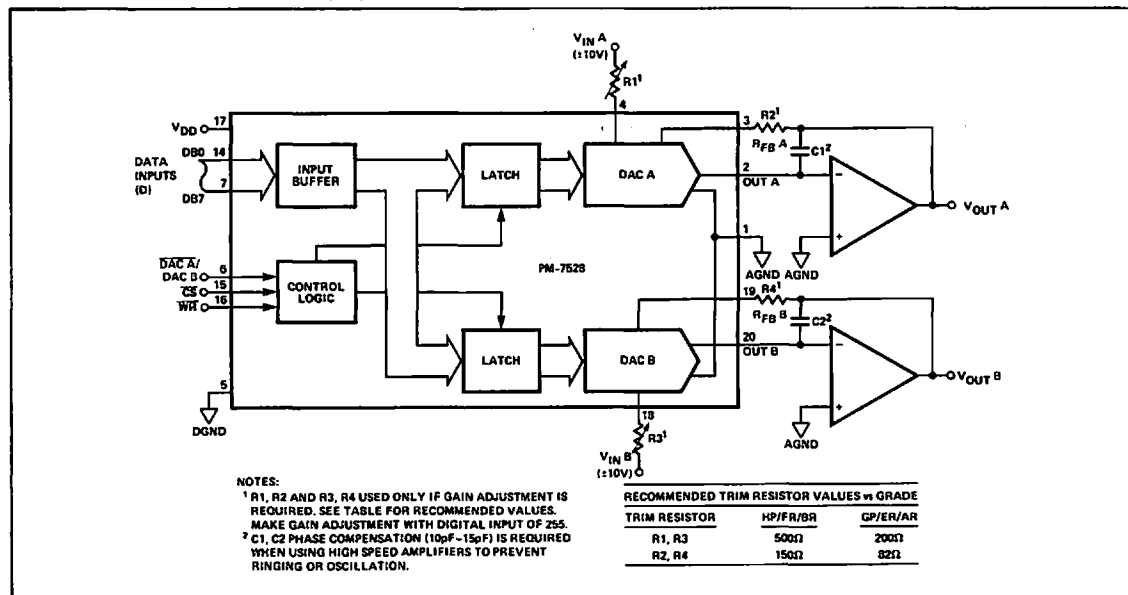


TABLE 1: Unipolar Binary Code Table. See Figure 5.

DAC LATCH CONTENTS		ANALOG OUTPUT (DAC A or DAC B)
MSB	LSB	
1	11111111	$-V_{IN} \left(\frac{255}{256} \right)$
1	00000001	$-V_{IN} \left(\frac{129}{256} \right)$
1	00000000	$-V_{IN} \left(\frac{128}{256} \right) = -\frac{V_{IN}}{2}$
0	11111111	$-V_{IN} \left(\frac{127}{256} \right)$
0	00000001	$-V_{IN} \left(\frac{1}{256} \right)$
0	00000000	$-V_{IN} \left(\frac{0}{256} \right) = 0$

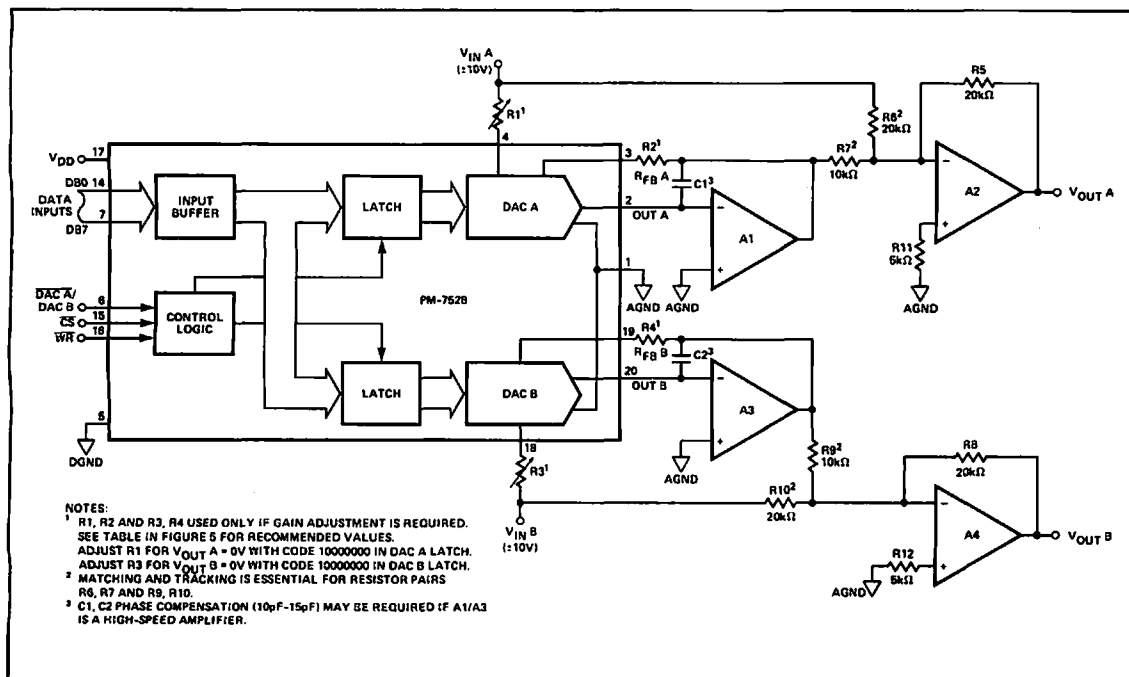
NOTE: $1 \text{ LSB} = (2^{-8})(V_{\text{IN}}) = \frac{1}{256}(V_{\text{IN}})$

TABLE 2: Bipolar (Offset Binary) Code Table. See Figure 6.

DAC LATCH CONTENTS		ANALOG OUTPUT (DAC A or DAC B)
MSB	LSB	
1	11111111	$+V_{IN} \left(\frac{127}{128} \right)$
1	0000001	$+V_{IN} \left(\frac{1}{128} \right)$
1	0000000	0
0	11111111	$-V_{IN} \left(\frac{1}{128} \right)$
0	0000001	$-V_{IN} \left(\frac{127}{128} \right)$
0	0000000	$-V_{IN} \left(\frac{128}{128} \right)$

NOTE: $1 \text{ LSB} = (2^{-7})(V_{\text{IN}}) = \frac{1}{128}(V_{\text{IN}})$

FIGURE 6: Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table 2.



APPLICATION HINTS

To ensure system performance consistent with PM-7528 specifications, careful attention must be given to the following points:

1. **GENERAL GROUND MANAGEMENT:** AC or transient voltages between the PM-7528 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal, is to tie AGND and DGND together at the PM-7528. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that diodes (1N914 or equivalent) be connected in inverse parallel between the PM-7528 AGND and DGND pins.
2. **OUTPUT AMPLIFIER OFFSET:** CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output with a maximum magnitude of $0.67 V_{OS}$ (V_{OS} is amplifier input-offset voltage). This differential nonlinearity term adds to the $R/2R$ differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1 LSB over the temperature range of interest.
3. **HIGH-FREQUENCY CONSIDERATIONS:** The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open-loop response; this can cause ringing or oscillation. Stability can be restored by adding a phase-compensation capacitor in parallel with the feedback resistor.
4. **DYNAMIC PERFORMANCE:** The dynamic performance of the two DACs in the PM-7528 will depend upon the gain and phase characteristics of the output amplifiers, together with the optimum choice of the PC board layout and decoupling components.
5. **CIRCUIT LAYOUT SUGGESTIONS:** Analog and digital ground traces should be routed between package pins to isolate the digital inputs from the analog circuitry. Analog ground traces should also be placed between pins 17-18, 18-19, 3-4, 4-5 to minimize reference feedthrough to the output in multiplying applications. A power supply bypass capacitor (0.1 μ F) is recommended across V_{DD} to DGND.

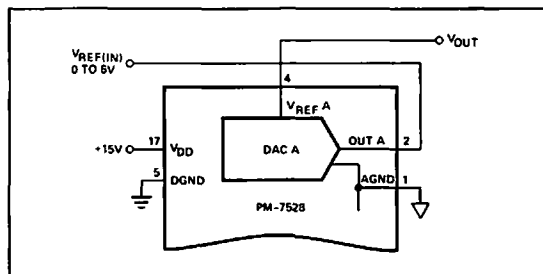
SINGLE SUPPLY OPERATION, VOLTAGE SWITCHING

With the PM-7528 connected in the voltage switching mode of operation, Figure 7, only one power supply is necessary. There is no voltage inversion between the reference input polarity and the output in the voltage switching mode.

Two characteristic curves in the typical performance characteristics section were generated using this voltage switching mode of operation. The first graph, linearity error versus input reference voltage, shows that to maintain a $\pm 1/2$ LSB maximum linearity error, V_{REF} should be less than 1.5 volts for $V_{DD} = 5$ volts or less than 6 volts for $V_{DD} = 15$ volts. The gain-phase response graph shows a dominant pole response for single supply applications where the reference input is an AC signal. In this application the reference input should remain between 1.5 volts and ground when $V_{DD} = 5$ volts. Additionally settling time measures 400 to 500 nano seconds for a digital input change of 255 to 0 when $V_{DD} = 5V$.

The output terminal in the voltage switching mode has a constant output resistance ($\approx 11K \Omega$) independent of the digital input code. The output should be buffered with a voltage follower when driving low impedance loads.

FIGURE 7: PM-7528 in Single Supply, Voltage Switching Mode



SINGLE SUPPLY, CURRENT SWITCHING

An alternate single-supply operating mode of the PM-7528 results when offsetting the analog ground. Figure 8 shows the method of connection. The advantage of this connection method is the ability to set the output voltage swing in the center of the supply voltage. This allows use of lower cost op amps that would not work in single-supply voltage-switching applications.

The transfer equation in this mode of operation is;

$$V_{OUT}(D) = D/256 (AGND - V_{REF}) + AGND$$

where D is the whole number binary input

A popular connection in the current-steering single-supply mode consists of a 2.5 volt reference connected to AGND, the V_{REF} input grounded, V_{DD} connected to 5 volts and the external ($V+$) op amp tied to 12 volts. This hookup results in the following transfer equation;

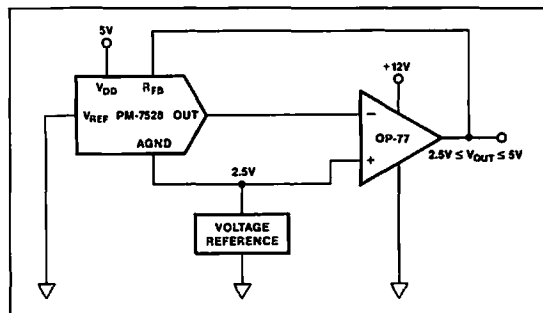
$$V_{OUT}(D) = 2.5 (1 + D/256)$$

$$\text{where } V_{OUT}(255) = 2.5 (1 + 255/256) = 5V$$

$$V_{OUT}(0) = 2.5V$$

To maintain best linearity keep AGND equal to or less than 2.5 volts when V_{DD} is 5 volts.

FIGURE 8: PM-7528 in Single Supply, Current-Steering Mode

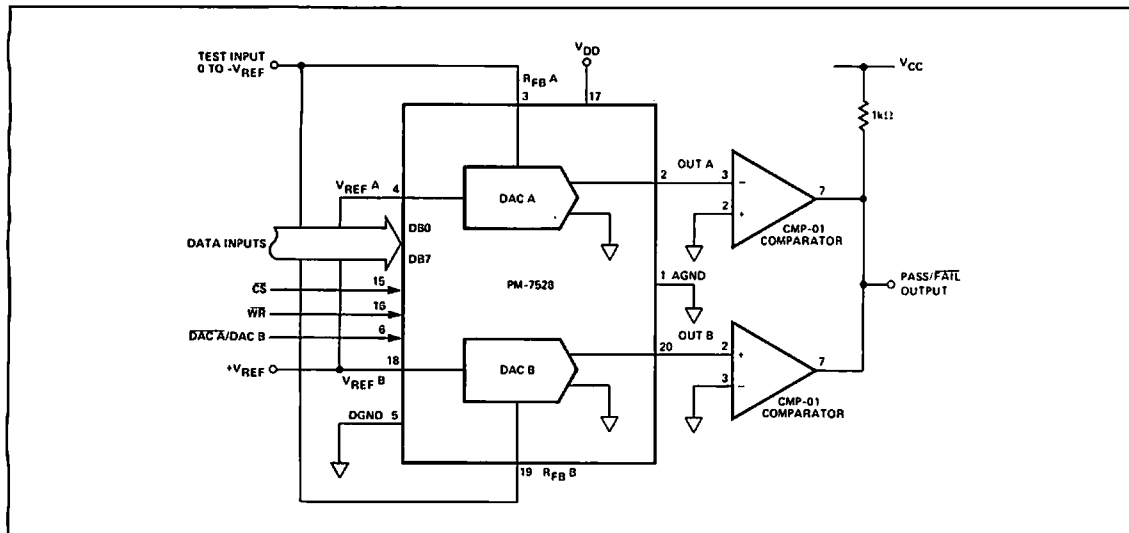


PROGRAMMABLE WINDOW COMPARATOR

A programmable window-comparator in Figure 9 will determine if voltage inputs applied to the DAC feedback resistors are within limits programmed into the PM-7528 data latches. The

input signal range depends on the reference and polarity, that is the test input range is 0 to minus V_{REF} . The A and B data latches are programmed with the upper and lower test limits. A signal within the programmed limits will drive the output to logic high.

FIGURE 9: Digitally Programmable Window Comparator (Upper and Lower Limit Detector).



MICROPROCESSOR INTERFACE

FIGURE 10: PM-7528 Dual DAC to 6800 CPU Interface.

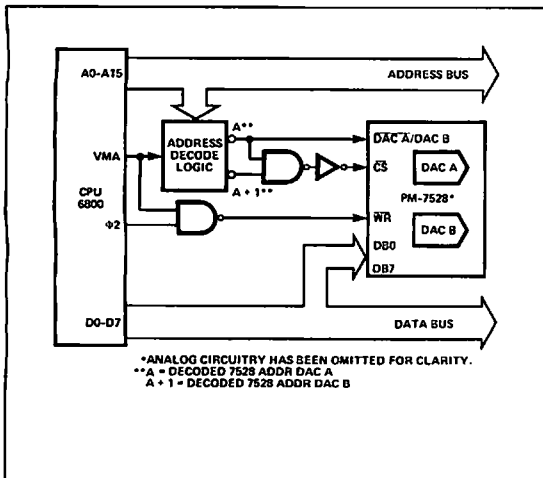
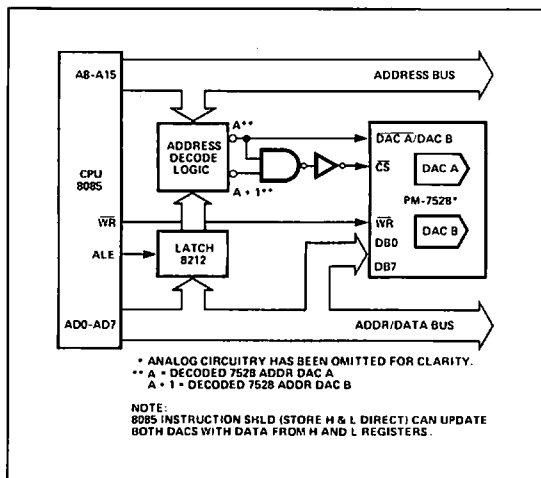


FIGURE 11: PM-7528 Dual DAC to 8085 CPU Interface.



DIGITALLY CONTROLLED SIGNAL ATTENUATOR

Figure 12 shows the PM-7528 configured as a two-channel programmable attenuator. Applications include stereo, audio, and telephone signal-level control applications. In order to

generate logarithmic attenuation, Table 4 was generated based on the equation:

$$\text{Digital Input} = 256 \times \exp \left(\frac{-\text{Attenuation (dB)}}{20} \right)$$

FIGURE 12: Digitally-Controlled Dual Telephone Attenuator.

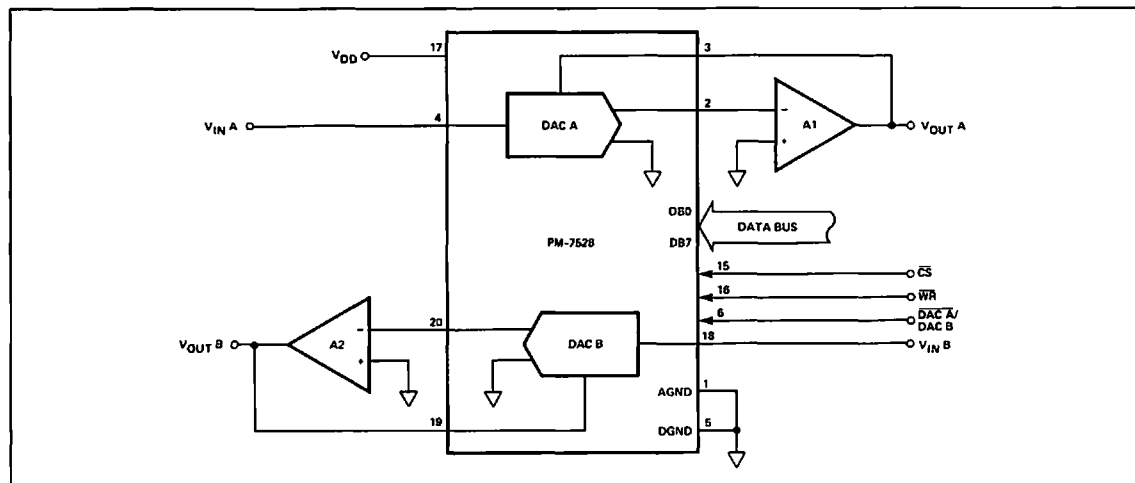


TABLE 4: Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 12

ATTN. dB	DAC INPUT CODE	CODE IN DECIMAL	ATTN. dB	DAC INPUT CODE	CODE IN DECIMAL
0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43



Precision Monolithics Inc.

PM-7533

CMOS LOW COST 10-BIT MULTIPLYING
D/A CONVERTER

FEATURES

- 10-Bit Resolution
- Full Four-Quadrant Multiplication
- Nonlinearity: 1/2 or 1 LSB
- TTL/CMOS Compatible
- Improved Gain Error and Linearity Error from +5V to +15V
- Low Power Consumption
- Low Feedthrough Error
- Low Cost
- AD7520 and AD7533 Replacement
- Full Temperature Operation
- Improved ESD Protection

APPLICATIONS

- Digital/Synchro Conversion
- Programmable Gain Amplifiers
- Ratimetric A/D Conversion
- Function Generator
- CRT Graphics Generator
- Digitally-Controlled Attenuator
- Digitally-Controlled Power Supplies
- Digital Filters
- Linear Automatic Gain Control

ORDERING INFORMATION†

PACKAGE: 16-PIN

	MILITARY* TEMPERATURE -55°C to +125°C	INDUSTRIAL TEMPERATURE -25°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
NONLINEARITY			
±0.1% (±1 LSB)	PM7533BQ	PM7533FQ	PM7533HP
±0.05% (±1/2 LSB)	PM7533AQ	PM7533EQ	PM7533GP

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7533AQ	AD7533UD	MILITARY
PM7533BQ	AD7533TD	
PM7533BQ	AD7533SD	
PM7533EQ	AD7533CD	INDUSTRIAL
PM7533FQ	AD7533BD	
PM7533FQ	AD7533AD	
PM7533GP	AD7533LN	COMMERCIAL
PM7533HP	AD7533KN	
PM7533HP	AD7533JN	

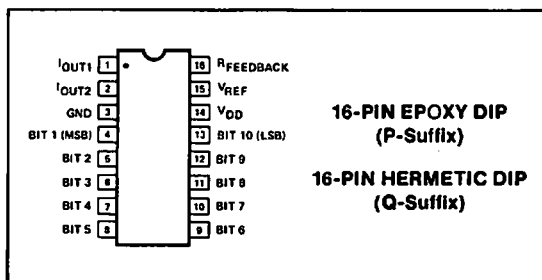
GENERAL DESCRIPTION

The PM-7533 is a 10-bit 4-quadrant multiplying DAC. It is manufactured using thin film on an oxide-isolated, silicon-gate, monolithic CMOS wafer fabrication process. PMI's advanced thin-film resistor processing provides true 10-bit linearity and excellent long-term stability without laser trimming.

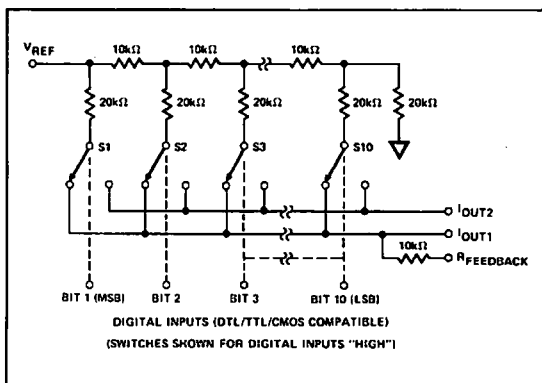
The PM-7533 is pin and function equivalent to the AD7520 and AD7533.

The PMI PM-7533 applications flexibility allows direct interface to TTL or CMOS circuitry and operation from +5V to +15V power supplies. Output scaling is provided by the internal feedback resistor and an external op amp; both positive and negative reference voltages can be accommodated.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



DIGITAL-TO-ANALOG CONVERTERS

11

**ABSOLUTE MAXIMUM RATINGS** ($T_A = +25^\circ\text{C}$, unless otherwise noted)

V_{DD} (to GND)	-0.3V, +17V
V_{REF} (to GND)	$\pm 25\text{V}$
R_{FB} (to GND)	$\pm 25\text{V}$
Digital Input Voltage Range	-0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2)	-0.3V to V_{DD}
Power Dissipation (Package)	
Ceramic (Suffix Q)	
To $+70^\circ\text{C}$	450mW
Derates Above $+75^\circ\text{C}$ By	6mW/ $^\circ\text{C}$
Plastic (Suffix P)	
To $+70^\circ\text{C}$	670mW
Derates Above $+70^\circ\text{C}$ By	8.3mW/ $^\circ\text{C}$
Operating Temperature Range	
Military (AQ, BQ Versions)	-55°C to $+125^\circ\text{C}$
Industrial (EQ, FQ Versions)	-25°C to $+85^\circ\text{C}$
Commercial (GP, HP Versions)	0°C to $+70^\circ\text{C}$

Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$+300^\circ\text{C}$

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener protected, however, permanent damage may occur on unconnected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +15\text{V}$, $V_{REF} = +10\text{V}$, $AGND = DGND = 0\text{V}$, $V_{OUT1} = V_{OUT2} = 0\text{V}$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ apply for PM-7533AQ/BQ, $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ apply for PM-7533EQ/FQ, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ apply for PM-7533GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7533A/E/G			PM-7533B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY									
Resolution	N		10	—	—	10	—	—	Bits
Relative Accuracy (Note 1)	INL		—	—	±0.05 (±1/2)	—	—	±0.1 (±1)	% FSR (LSB)
Differential Nonlinearity (Note 12)	DNL		—	—	±0.1 (±1)	—	—	±0.1 (±1)	% FSR LSB
Gain Error (Notes 2, 3)	G _{FSE}	T _A = +25°C	—	—	±1.4 (±14)	—	—	±1.4 (±14)	% FS (LSB)
		T _A = Full Temp. Range	—	—	±1.5 (±15)	—	—	±1.5 (±15)	% FS (LSB)
Power Supply Rejection ΔGain/ΔV _{DD} (Note 4)	PSRR	T _A = +25°C T _A = Full Temp. Range	—	—	0.005 0.008	—	—	0.005 0.008	%/%
Output Leakage Current I _{OUT1} (Pin 1) (Note 6)	I _{LKG1}	T _A = +25°C T _A = Full Temp. Range	—	—	±50 ±200	—	—	±50 ±200	nA
Output Leakage Current I _{OUT2} (Pin 2) (Note 7)	I _{LKG2}	T _A = +25°C T _A = Full Temp. Range	—	—	±50 ±200	—	—	±50 ±200	nA
DYNAMIC ACCURACY									
Output Current Settling Time (Notes 5, 8)	t _s	T _A = +25°C (Note 10) T _A = Full Temp. Range	—	—	600 800	—	—	600 800	ns
Feedthrough Error (Notes 5, 10)	FT	T _A = +25°C T _A = Full Temp. Range	—	—	±0.05 ±0.1	—	—	±0.05 ±0.1	% FSR
REFERENCE INPUT									
Reference Input Resistance (Pin 15) (Note 11)	R _{IN}		5	—	20	5	—	20	kΩ
ANALOG OUTPUTS									
Output Capacitance (Note 5)	C _{OUT1} C _{OUT2}	Digital Inputs = V _{INH}	—	—	100 35	—	—	220 60	pF
Output Capacitance (Note 5)	C _{OUT1} C _{OUT2}	Digital Inputs = V _{INL}	—	—	60 100	—	—	120 165	pF



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7533AQ/BQ, $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7533EQ/FQ, $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7533GP/HP, unless otherwise noted. (Continued)

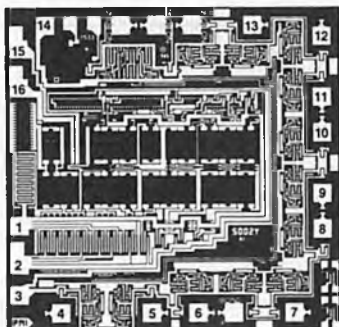
PARAMETER	SYMBOL	CONDITIONS	PM-7533A/E/G			PM-7533B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS									
Digital Input High	V _{INH}		2.4	—	—	2.4	—	—	V
Digital Input Low	V _{INL}		—	—	0.8	—	—	0.8	V
Input Leakage Current	I _{IN}	V _{IN} = 0V and V _{DD}	—	—	±1	—	—	±1	μA
Input Capacitance (Note 5)	C _{IN}		—	—	10	—	—	10	pF
POWER REQUIREMENTS									
Power Supply Voltage	V _{DD}		—	—	+15 ±10%	—	—	+15 ±10%	V
Power Supply Voltage Range	PSR	Accuracy is not guaranteed over this range	+5	—	+16	+5	—	+16	V
Supply Current	I _{DD}	Digital Inputs = V _{INL} or V _{INH}	—	—	2	—	—	2	mA

NOTES:

- "FSR" is full-scale range.
- Full-scale (FS) = $-(V_{REF}) \left(\frac{1023}{1024} \right)$; Digital Inputs = V_{INH} .
- Maximum gain change from $T_A = +25^\circ C$ to T_{MIN} or T_{MAX} is $\pm 0.1\%$ FSR.
- Digital inputs = V_{INH} , $V_{DD} = +14V$ to $+17V$.
- Guaranteed and not tested.
- Digital inputs = V_{INL} .
- Digital inputs = V_{INH} .
- Settles to 0.05% FSR; $R_{LOAD} = 100\Omega$; digital inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH} .
- AC parameters sample tested to ensure spec compliance.
- Digital input = V_{INL} ; $V_{REF} = 20V_{p-p}$, $f = 100kHz$ Sinewave.
- Absolute temperature coefficient is approximately $+50ppm/^\circ C$.
- All grades guaranteed monotonic.



DICE CHARACTERISTICS



DIE SIZE 0.102×0.100 inch, 10,200 sq. mils
(2.591×2.540 mm, 6.58 sq. mm)

1. CURRENT OUTPUT 1
2. CURRENT OUTPUT 2
3. GROUND
4. DIGITAL INPUT BIT 1 (MOST SIGNIFICANT BIT)
5. DIGITAL INPUT BIT 2
6. DIGITAL INPUT BIT 3
7. DIGITAL INPUT BIT 4
8. DIGITAL INPUT BIT 5
9. DIGITAL INPUT BIT 6
10. DIGITAL INPUT BIT 7
11. DIGITAL INPUT BIT 8
12. DIGITAL INPUT BIT 9
13. DIGITAL INPUT BIT 10 (LEAST SIGNIFICANT BIT)
14. POSITIVE POWER SUPPLY
15. REFERENCE INPUT VOLTAGE
16. INTERNAL FEEDBACK RESISTOR

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +15V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7533G LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		10	Bits MIN
Relative Accuracy (Notes 1, 2)	INL		± 0.1 (± 1)	% FSR (LSB) MAX
Differential Nonlinearity (Note 10)	DNL		± 0.1 (± 1)	%FSR (LSB) MAX
Gain Error (Notes 2, 3, 4)	G_{FSE}		± 1.4 (± 14)	% FS (LSB) MAX
Power Supply Rejection $\Delta \text{Gain} / \Delta V_{DD}$ (Notes 2, 5, 6)	PSR		0.005	% / % MAX
Output Leakage Current I_{OUT1} (Notes 2, 7)	I_{LKG1}		± 50	nA MAX
Output Leakage Current I_{OUT2} (Notes 2, 8)	I_{LKG2}		± 50	nA MAX
REFERENCE INPUT				
Reference Input Resistance (Notes 2, 9)	R_{IN}		5/20	k Ω MIN/MAX



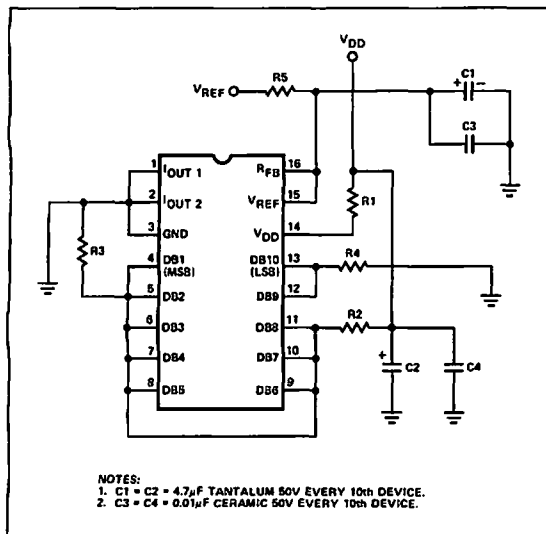
WAFER TEST LIMITS at $V_{DD} = +15V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = +25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7533G LIMIT	UNITS
DIGITAL INPUTS				
Digital Input High (Note 2)	V_{INH}		2.4	V MIN
Digital Input Low (Note 2)	V_{INL}		0.8	V MAX
Input Leakage Current (Note 2)	I_{IN}	$V_{IN} = 0V$ and V_{DD}	± 1	μA MAX
POWER REQUIREMENTS				
Power Supply Voltage	V_{DD}		$+15 \pm 10\%$	V MAX
Supply Current (Note 2)	I_{DD}	Digital Inputs = V_{INL} or V_{INH}	2	mA MAX

NOTES:

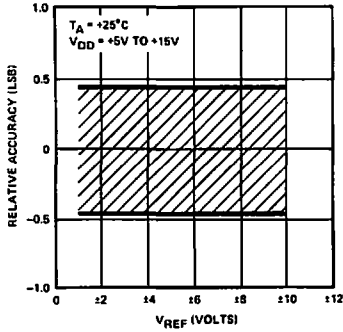
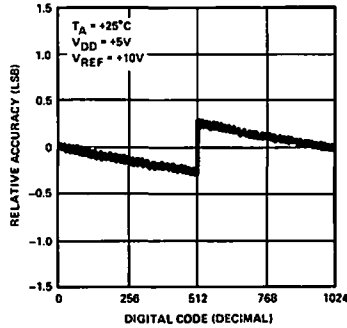
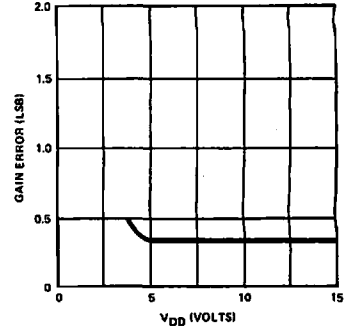
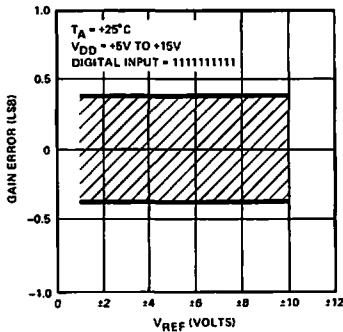
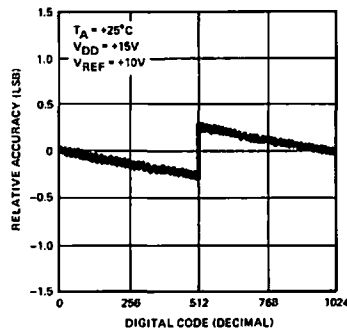
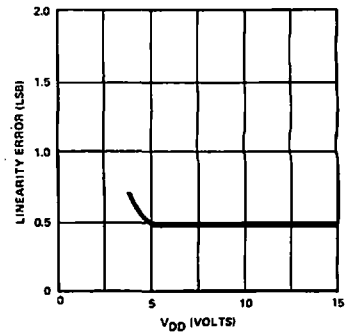
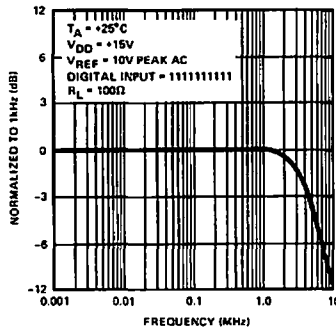
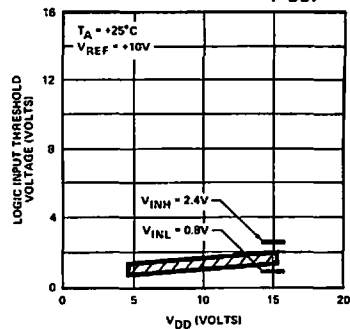
- "FSR" is full-scale range.
- DICE final electrical tests are: relative accuracy, gain error, output leakage current, V_{INH} , V_{INL} , PSR, R_{IN} , I_{IN} and I_{DD} at $+25^\circ C$.
- Full-scale (FS) = $-(V_{REF}) \left(\frac{1023}{1024} \right)$; Digital inputs = V_{INH} .
- Maximum gain change from $T_A = +25^\circ C$ to T_{MIN} or T_{MAX} is $\pm 0.1\%$ FSR.
- Digital inputs = V_{INH} , $V_{DD} = +14V$ to $+17V$.
- Guaranteed and not tested.
- Digital inputs = V_{INL} .
- Digital inputs = V_{INH} .
- Absolute temperature coefficient is approximately $+300ppm/^\circ C$.
- Guaranteed monotonic.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

BURN-IN CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTICS

RELATIVE ACCURACY
(NONLINEARITY) vs V_{REF} RELATIVE ACCURACY
(NONLINEARITY) vs
DIGITAL CODEGAIN ERROR vs
SUPPLY VOLTAGEGAIN ERROR vs V_{REF} RELATIVE ACCURACY
(NONLINEARITY) vs
DIGITAL CODELINEARITY ERROR vs
SUPPLY VOLTAGE V_{REF} FREQUENCY
RESPONSELOGIC INPUT THRESHOLD
VOLTAGE vs
SUPPLY VOLTAGE (V_{DD})

DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where n is equal to the number of bits. Resolution in no way implies linearity.

RELATIVE ACCURACY

Relative accuracy or end-point (nonlinearity) is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full-scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1 LSB.

SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when using the DAC's internal feedback resistor.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches off.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

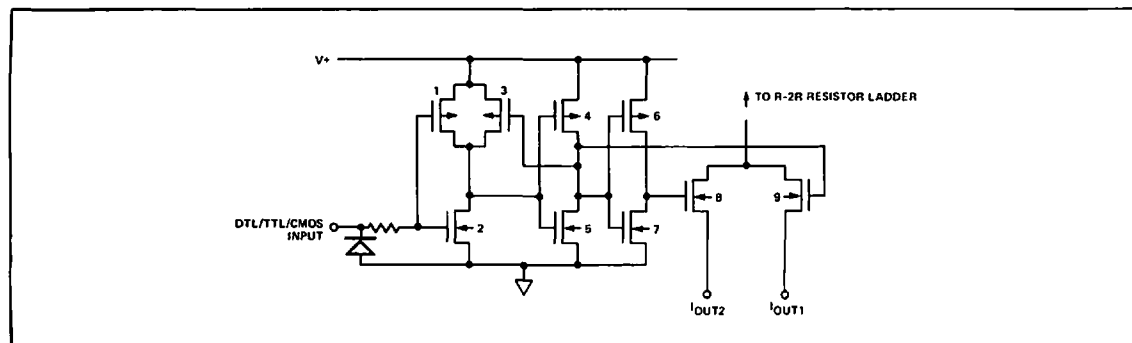
OUTPUT LEAKAGE CURRENT

Current which appears on I_{OUT1} terminal with all digital inputs low or on I_{OUT2} terminal when all inputs are high.

CIRCUIT DESCRIPTION

The PM-7533 is a 10-bit multiplying D/A converter. It consists of a silicon-chrome thin-film R-2R resistor ladder network and ten pairs of NMOS current steering switches, all on a monolithic chip. The NMOS current steering switches are controlled by CMOS inverters. Most applications require the addition of only an operational amplifier and a current or voltage reference.

FIGURE 2: CMOS Switch



An inverted R-2R ladder network in a simplified D/A converter circuit is shown in Figure 1. The current through each ladder leg is switched between I_{OUT1} and I_{OUT2} under the control of the digital inputs. This allows a constant current to be maintained in each ladder leg regardless of the digital input switch states.

The design incorporates a matching MOS transistor in series with the feedback and terminating resistors. These MOS transistors, shown as switches in Figure 1, provide improved gain and linearity performance over the operating temperature range. The resulting typical gain temperature coefficient is 2ppm/°C.

FIGURE 1: Simplified DAC Circuit

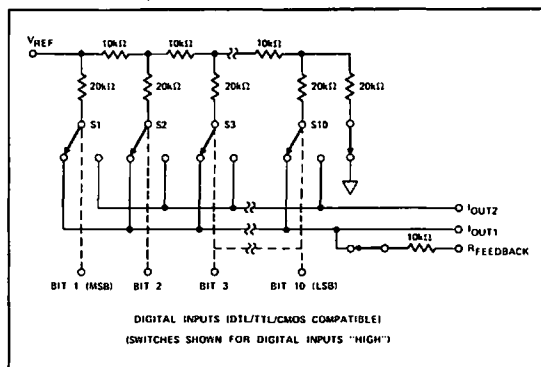


Figure 2 shows one of ten digital input CMOS inverters driving an NMOS switch. The size of devices 1, 2, and 3 are optimized to make the digital inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives the two inverters (4, 5) and (6, 7), which drives the two NMOS switches (8 and 9). The switch "ON" resistances are binarily-scaled so that the voltage drop across each switch is the same; that is, switch S1 in Figure 1 (8 and 9 of Figure 2) was designed for an "ON" resistance of 20 ohms, switch S2 for 40 ohms, etc. With a 10V reference input, switch S1 current is 0.5mA, switch S2 is 0.25mA, etc. This will maintain a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal so that the D/A converter accuracy is maintained.

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits of the DAC with all digital inputs high and low respectively. With all digital inputs in the high state as shown in Figure 3, the reference current is switched to the I_{OUT1} terminal, and the I_{OUT2} terminal is open-circuited. Only the output capacitance, surface, leakages, and junction leakages appear at the I_{OUT2} terminal. The $1/1024$ current source is a constant 1-bit current drain through the termination resistor of the R-2R ladder network. The $I_{LEAKAGE}$ current source represents a combination of surface and junction leakages to the substrate. The "ON" capacitance of the output NMOS switch is higher on the I_{OUT1} terminal when all digital inputs are high (MOS transistor gate capacitance increases with applied gate voltage).

FIGURE 3: Equivalent DAC Circuit
(All digital inputs HIGH).

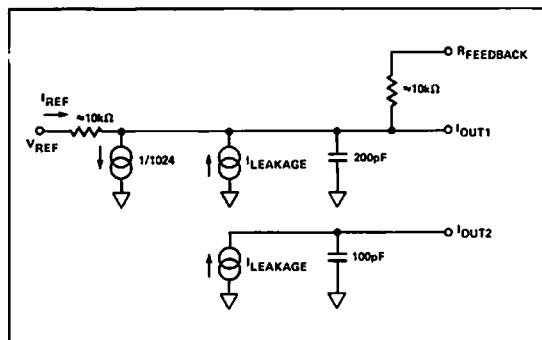
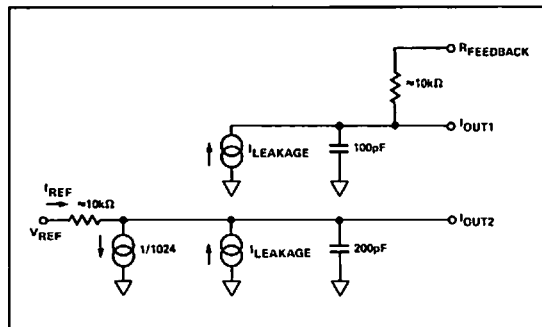


FIGURE 4: Equivalent DAC Circuit
(All digital inputs LOW).



When the conditions are reversed with all digital inputs low as shown in Figure 4, the I_{OUT1} terminal is open-circuited and the current is directed towards the I_{OUT2} terminal.

APPLICATIONS INFORMATION

Figure 5 shows a simple unipolar circuit using the PM-7533. Resistors R1 and R2 are used to trim for full scale. Full-scale output voltage = $-V_{REF} \times (1023/1024)$ with all digital inputs high. Full scale can also be adjusted using V_{REF} thereby eliminating resistors R1 and R2. In many applications, R1 and R2 are not required. Zero-scale output voltage (with all digital inputs low) should be adjusted to less than 10% of 1 LSB using the op amp offset adjust. This will help to keep the nonlinearity errors to a minimum. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high-speed op amps.

The circuit of Figure 5 can be used either as a fixed reference digital-to-analog converter, or can be used with an AC signal at the V_{REF} terminal. Used with a fixed reference voltage, the output voltage range will be from zero to $-V_{REF}$, (the op amp inverts the voltage). The circuit behaves as an attenuator when used with an AC V_{REF} signal. The input voltage range is $\pm 20V$, but this voltage will be limited by the op amp voltage range. The digital-input-code versus analog-output-voltage is shown in Table 1. The transfer function is:

$$V_O = -V_{IN} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \dots + \frac{A_{10}}{2^{10}} \right)$$

where $A_1 \dots A_{10}$ assumes a value of 1 for an ON bit and 0 for an OFF bit.

FIGURE 5: Unipolar Binary Operation
(2-Quadrant Multiplication)

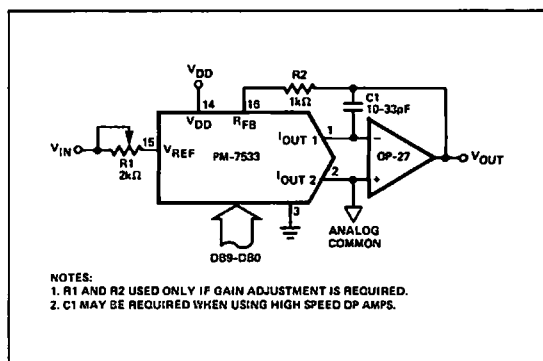




TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT MSB	LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1 1 1 1 1 1 1 1 1 1		$-V_{REF} \left(\frac{1023}{1024} \right)$
1 0 0 0 0 0 0 0 0 1		$-V_{REF} \left(\frac{513}{1024} \right)$
1 0 0 0 0 0 0 0 0 0		$-V_{REF} \left(\frac{512}{1024} \right) = \frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1		$-V_{REF} \left(\frac{511}{1024} \right)$
0 0 0 0 0 0 0 0 0 1		$-V_{REF} \left(\frac{1}{1024} \right)$
0 0 0 0 0 0 0 0 0 0		$-V_{REF} \left(\frac{0}{1024} \right) = 0$

NOTES:

1. Nominal full scale for the circuit of Figure 5 is given by

$$FS = -V_{REF} \left(\frac{1023}{1024} \right)$$

2. Nominal LSB magnitude for the circuit of Figure 5 is given by

$$LSB = V_{REF} \left(\frac{1}{1024} \right) \text{ or } V_{REF} (2^{-10})$$

Figure 6 shows a simple bipolar output circuit using the PM-7533 and a PMI OP-215 dual op amp. The circuit uses offset binary coding and a fixed DC voltage for V_{REF} . Digitally-controlled attenuation of an AC signal occurs when the signal is used as the signal source at V_{REF} . Negative output full-scale is adjusted by setting the digital inputs to all zeros and adjusting the value of the V_{REF} voltage or $R5$. The zero-scale output voltage is adjusted while the digital inputs

are set to 1000000000 and adjusting $R1$ for a zero output voltage (less than 10% of 1 LSB). Resistors $R3$, $R4$ and $R5$ must be selected for matching and tracking in order to keep offset and full scale errors to a minimum. Resistors $R1$ and $R2$ temperature coefficients must be taken into account if they are used. $C1$ phase compensation capacitor may not be needed and should be selected empirically. The digital input code versus analog output voltage is shown in Table 2.

TABLE 2: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB	LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1 1 1 1 1 1 1 1 1 1		$+V_{REF} \left(\frac{511}{512} \right)$
1 0 0 0 0 0 0 0 0 1		$+V_{REF} \left(\frac{1}{512} \right)$
1 0 0 0 0 0 0 0 0 0		0
0 1 1 1 1 1 1 1 1 1		$-V_{REF} \left(\frac{1}{512} \right)$
0 0 0 0 0 0 0 0 0 1		$-V_{REF} \left(\frac{511}{512} \right)$
0 0 0 0 0 0 0 0 0 0		$-V_{REF} \left(\frac{512}{512} \right)$

NOTES:

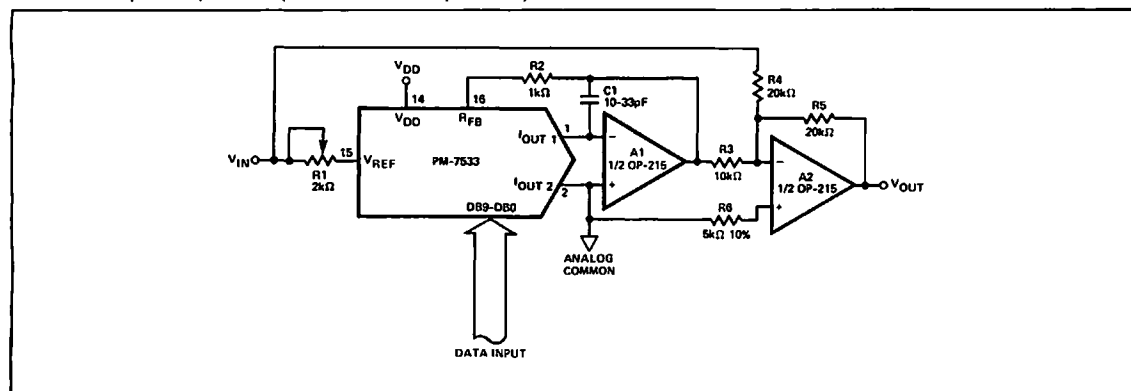
1. Nominal full scale for the circuit of Figure 6 is given by

$$FSR = V_{REF} \left(\frac{512}{512} \right)$$

2. Nominal LSB magnitude for the circuit of Figure 6 is given by

$$LSB = V_{REF} \left(\frac{1}{512} \right)$$

FIGURE 6: Bipolar Operation (4-Quadrant Multiplication)



The PM-7533 may be used in the voltage output operation as shown in Figure 7. This circuit configuration will lend itself to single-supply operation because signal inversion does not occur. The output should be buffered due to its high output resistance (10k Ω) to prevent loading errors. The reference voltage should be kept to +1.5 volts maximum to keep nonlinearity errors to less than 1 LSB as shown in Figure 8.

By connecting the DAC in the feedback of an op amp as shown in Figure 9, the circuit behaves as a programmable gain amplifier (analog/digital divider). The transfer function is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \dots + \frac{A_{10}}{2^{10}}} \right)$$

where $A_1 \dots A_{10}$ assumes a value of 1 or 0.

FIGURE 7: Voltage Output Operation

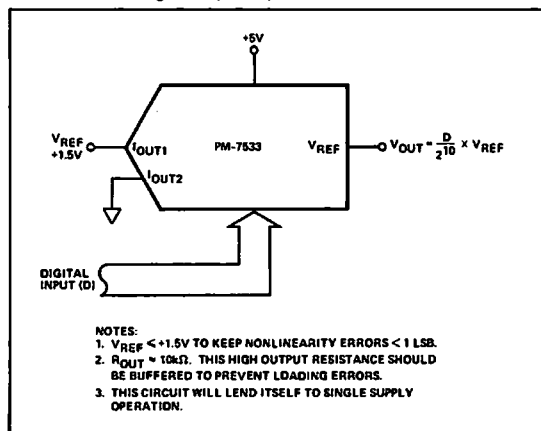


FIGURE 8: Voltage Mode

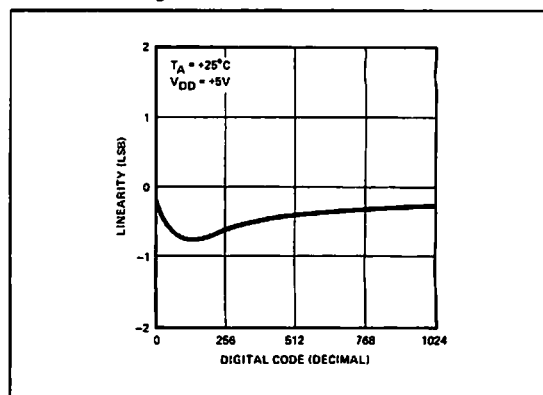
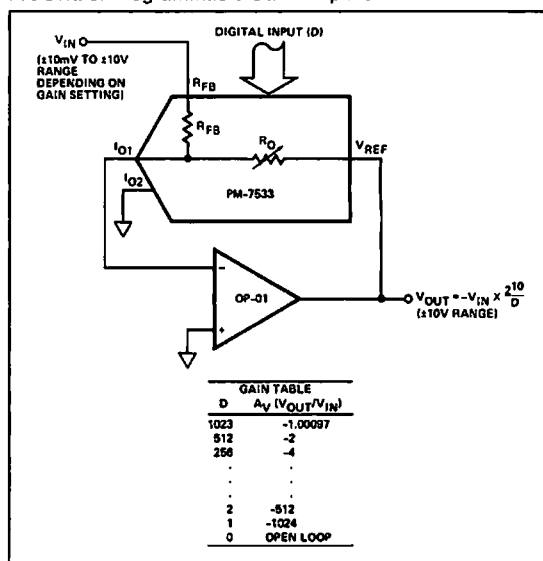


FIGURE 9: Programmable Gain Amplifier





Precision Monolithics Inc.

PM-7541

CMOS 12-BIT MONOLITHIC MULTIPLYING
D/A CONVERTER

FEATURES

- Full Four-Quadrant Multiplication
- 12-Bit Endpoint Linearity ($\pm 1/2$ LSB)
- Pretrimmed Gain
- TTL/CMOS Compatible
- Low Power Consumption
- Low Feedthrough Error
- Direct Replacement for AD7521 and AD7541
- Superior Power Supply Rejection from +5V to +15V
- Low Gain and Linearity Tempcos (TYP 2ppm of FSR/ $^{\circ}$ C)
- Latch-Up Resistant

APPLICATIONS

- Digital/Synchro Conversion
- Programmable Amplifiers
- Ratimetric A/D Conversion
- Function Generator
- CRT Graphics Generator
- Digitally-Controlled Attenuator
- Digitally-Controlled Power Supplies
- Digital Filters

ORDERING INFORMATION†

PACKAGE: 18-PIN

	MILITARY*	INDUSTRIAL	COMMERCIAL
	TEMPERATURE	TEMPERATURE	TEMPERATURE
	-55 $^{\circ}$ C TO +125 $^{\circ}$ C	-25 $^{\circ}$ C TO +85 $^{\circ}$ C	0 $^{\circ}$ C TO +70 $^{\circ}$ C
NONLINEARITY			
1 LSB	PM7541BX	PM7541FX	PM7541HP
1/2 LSB	PM7541AX	PM7541EX	PM7541GP

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

CROSS REFERENCE

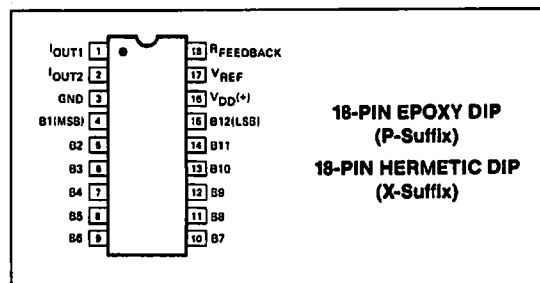
PMI	ADI	TEMPERATURE RANGE
PM7541AX	AD7541TD	MILITARY
PM7541BX	AD7541SD	
PM7541EX	AD7541BD	INDUSTRIAL
PM7541FX	AD7541AD	
PM7541GP	AD7541KN	COMMERCIAL
PM7541HP	AD7541JN	

GENERAL DESCRIPTION

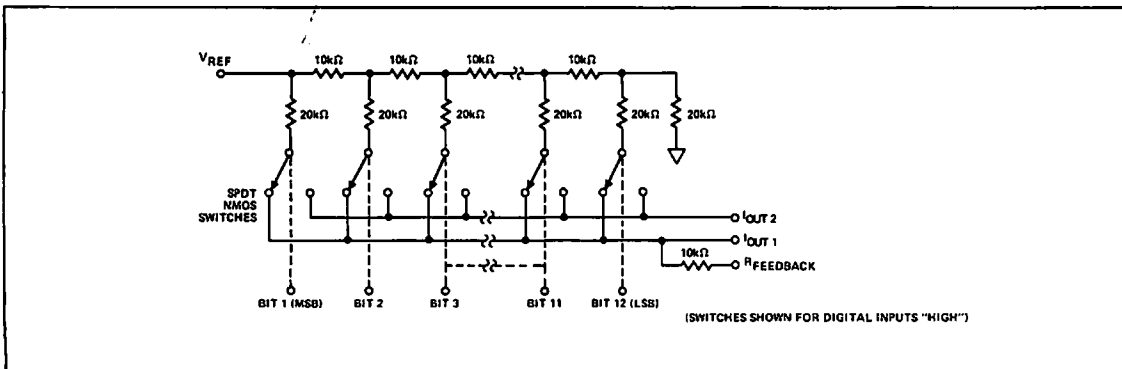
The PMI PM-7541 is a 12-bit, 4-quadrant multiplying digital-to-analog converter. It is manufactured using an advanced oxide-isolated, silicon-gate, monolithic CMOS technology.

Laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity and excellent absolute accuracy. The low power dissipation, together with NMOS temperature-compensating switches, assures the performance over the full temperature range. It is a pin-compatible replacement for Analog Devices AD7521 and AD7541 with equal or better performance.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**(T_A = +25°C, unless otherwise noted.)

V _{DD} (to GND)		+17V
V _{REF} (to GND)		±25V
V _{RFB} (to GND)		±25V
Digital Input Voltage Range		V _{DD} to GND
Output Voltage (Pin 1, Pin 2)		-0.3V to V _{DD}
Power Dissipation (Package)		450mW
Derate Above +75°C		6mW/°C
Operating Temperature Range		
AX/BX Versions		-55°C to +125°C
EX/FX Versions		-25°C to +85°C
GP/HP Versions		0°C to +70°C

Dice Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
Lead Temperature (Soldering, 60 sec)		300°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 17) and R_{FEB} (Pin 18).
2. The digital control inputs are zener protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, GND = 0V, V_{OUT1} = V_{OUT2} = 0V; and T_A = -55°C to +125°C apply for PM-7541AX/BX; T_A = -25°C to +85°C apply for PM-7541EX/FX; and T_A = 0°C to +70°C apply for PM-7541GP/HP, unless otherwise noted.

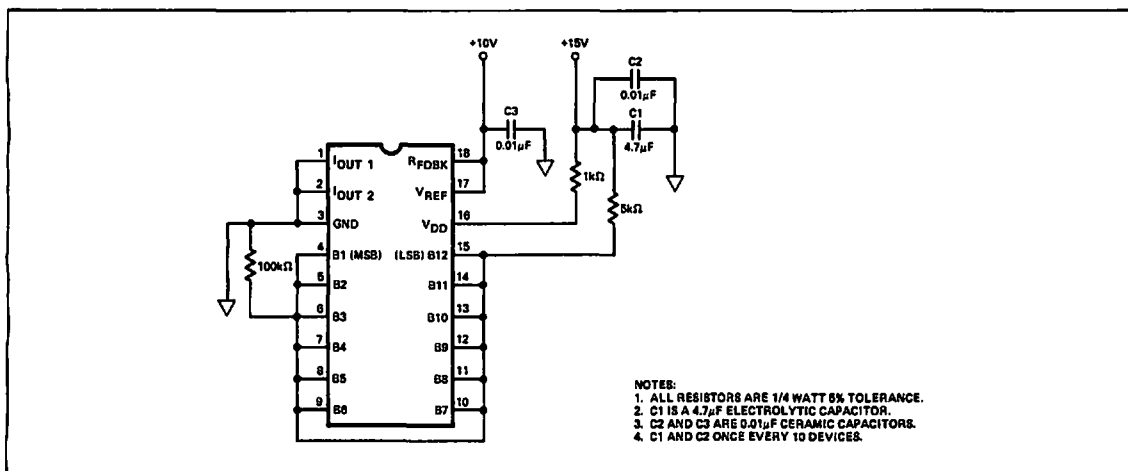
PARAMETER	SYMBOL	CONDITIONS	PM-7541A/E/G			PM-7541B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Nonlinearity (Notes 1, 2)	INL		—	—	±1/2	—	—	±1	LSB
Gain Error (Notes 3, 4)	G _{FSE}	T _A = +25°C T _A = Full Temp. Range	—	—	±12.5 ±16.7	—	—	±12.5 ±16.7	LSB
Power Supply Rejection ΔGain/ΔV _{DD}	PSRR	V _{DD} = +14.5V to +15.5V T _A = +25°C T _A = Full Temp. Range	—	—	±0.01 ±0.02	—	—	±0.01 ±0.02	%/%
Output Leakage Current (I _{OUT1}) (Notes 5, 6)	I _{LKG}	T _A = +25°C T _A = Full Temp. Range	—	—	±50 ±200	—	—	±50 ±200	nA
DYNAMIC PERFORMANCE									
Output Current Settling Time (Note 7)	t _S	To ±1/2 LSB of FSR	—	—	1.0	—	—	1.0	μs
Feedthrough Error (Note 7)	FT	V _{REF} = 20V _{p-p} @ f = 10kHz All digital inputs low	—	—	2.0	—	—	2.0	mV _{p-p}
REFERENCE INPUT									
Input Resistance (Note 8)	R _{REF}		5	—	20	5	—	20	kΩ
DIGITAL INPUTS									
Digital Input High	V _{IH}		2.4	—	—	2.4	—	—	V
Digital Input Low	V _{IL}		—	—	0.8	—	—	0.8	V
Input Leakage Current	I _{IL}	V _{IN} = 0 to 15V	—	—	±1	—	—	±1	μA
Input Capacitance (Note 7)	C _{IN}		—	—	8	—	—	8	pF
Input Coding		(Tables 1, 2)	Binary or Offset			Binary or Offset			

ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $GND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$; and $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7541AX/BX; $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7541EX/FX; and $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7541GP/HP, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7541A/E/G			PM-7541B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG OUTPUTS									
Output Capacitance (Note 7)	C _{OUT 1}	Digital Inputs = V _{IH}	—	85	200	—	85	200	pF
	C _{OUT 2}		—	30	60	—	30	60	
Output Capacitance (Note 7)	C _{OUT 1}	Digital Inputs = V _{IL}	—	30	60	—	30	60	pF
	C _{OUT 2}		—	85	200	—	85	200	
POWER SUPPLY									
V _{DD} Range	V _{DD}	Accuracy is not guaranteed over this range.	+5	—	+16	+5	—	+16	V
Supply Current	I _{DD}	Digital Inputs = V _{IH} or V _{IL}	—	—	2	—	—	2	mA

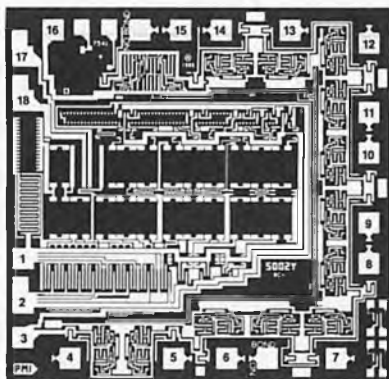
NOTES:

1. A/E/G versions are monotonic to 12-bits.
2. B/F/H versions are monotonic to 11-bits.
3. Using internal feedback resistor.
4. Maximum gain change from $+25^\circ C$ to T_{MAX} or T_{MIN} is ± 4.2 LSB maximum.
5. Digital Inputs = V_{IL} .
6. Specification also applies for I_{OUT2} with all digital inputs = V_{IH} .
7. Guaranteed and not tested.
8. Absolute temperature coefficient is approximately ± 300 ppm/ $^\circ C$.

BURN-IN CIRCUIT




DICE CHARACTERISTICS



DIE SIZE 0.102 × 0.100 inch, 10,200 sq. mils
(2.590 × 2.540 mm, 6.58 sq. mm)

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

1. CURRENT OUTPUT 1
2. CURRENT OUTPUT 2
3. GROUND
4. DIGITAL INPUT (BIT 1) (MOST SIGNIFICANT BIT)
5. DIGITAL INPUT (BIT 2)
6. DIGITAL INPUT (BIT 3)
7. DIGITAL INPUT (BIT 4)
8. DIGITAL INPUT (BIT 5)
9. DIGITAL INPUT (BIT 6)
10. DIGITAL INPUT (BIT 7)
11. DIGITAL INPUT (BIT 8)
12. DIGITAL INPUT (BIT 9)
13. DIGITAL INPUT (BIT 10)
14. DIGITAL INPUT (BIT 11)
15. DIGITAL INPUT (BIT 12) (LEAST SIGNIFICANT BIT)
16. POSITIVE POWER SUPPLY
17. REFERENCE INPUT VOLTAGE
18. INTERNAL FEEDBACK RESISTOR

WAFER TEST LIMITS at $V_{DD} = +15V$, $V_{REF} = +10V$, $GND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = +25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	PM-7541G LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Nonlinearity	INL		±1	LSB MAX
Gain Error (Note 1)	G_{FSE}		±12.5	LSB MAX
Power Supply Rejection	PSRR	$V_{DD} = +14.5V$ to $+15.5V$	±0.01	%/% MAX
Output Leakage Current (I_{OUT1}) (Note 2)	I_{LKG}	Digital Inputs = V_{IL}	±50	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		5/20	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	$V_{IH} = 0$ to $15V$	±1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	2	mA MAX

NOTES:

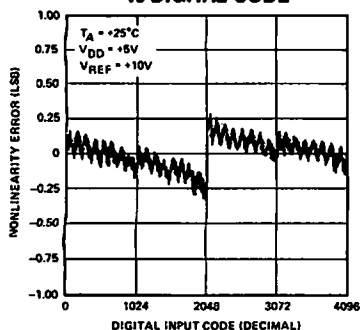
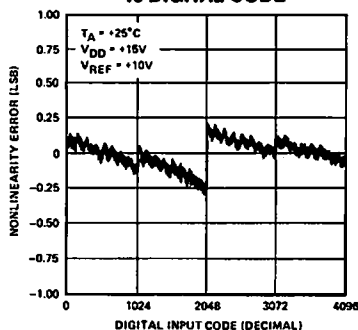
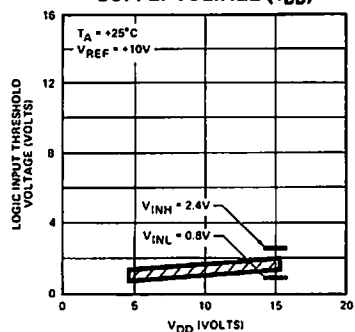
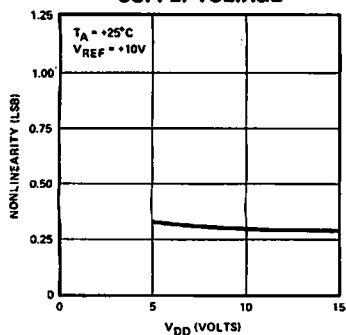
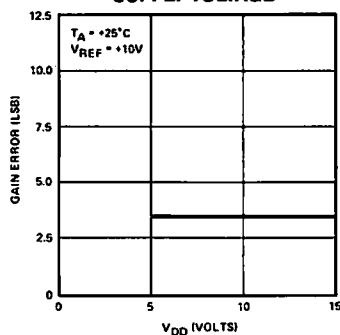
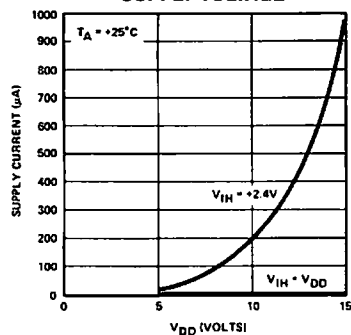
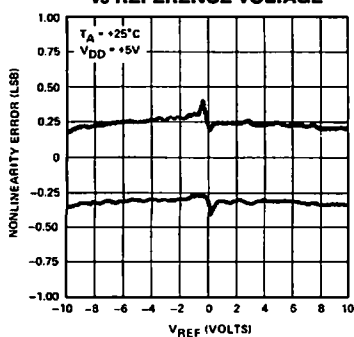
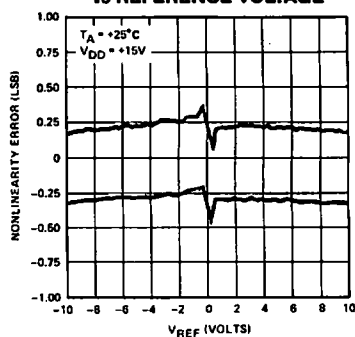
1. Using internal feedback resistor.

2. Specification also applies for I_{OUT2} but all Digital Inputs = V_{IH} .

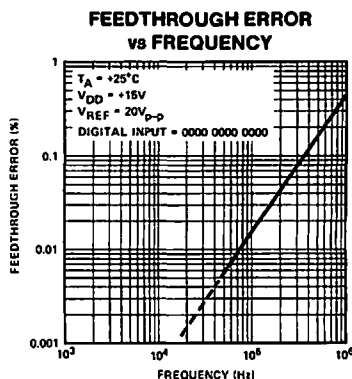
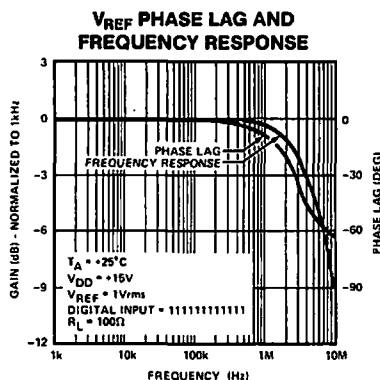
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



TYPICAL PERFORMANCE CHARACTERISTICS

NONLINEARITY ERROR
vs DIGITAL CODENONLINEARITY ERROR
vs DIGITAL CODELOGIC INPUT THRESHOLD
VOLTAGE vs
SUPPLY VOLTAGE (V_{DD})NONLINEARITY vs
SUPPLY VOLTAGEGAIN ERROR vs
SUPPLY VOLTAGESUPPLY CURRENT vs
SUPPLY VOLTAGENONLINEARITY ERROR
vs REFERENCE VOLTAGENONLINEARITY ERROR
vs REFERENCE VOLTAGE

TYPICAL PERFORMANCE CHARACTERISTICS



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus; i.e., zero to full scale.

GAIN

Ratio of the DAC's external-operational-amplifier output voltage to the V_{REF} input voltage.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} or I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT

Current which appears on I_{OUT1} terminal with all digital inputs LOW, or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The PM-7541 is a 12-bit multiplying D/A converter consisting of a highly-stable, silicon-chrome thin film R-2R ladder network

and twelve pairs of NMOS current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier.

A simplified circuit of the PM-7541 is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between I_{OUT1} and I_{OUT2} BUS lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The design includes a matching switch in series with the feedback (R_{FB}) and terminating resistors. These switches (Figure 1) provide improved gain and linearity performance over the operating temperature range.

FIGURE 1: Simplified DAC Circuit

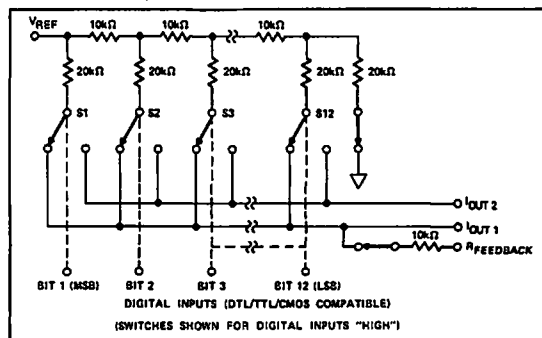
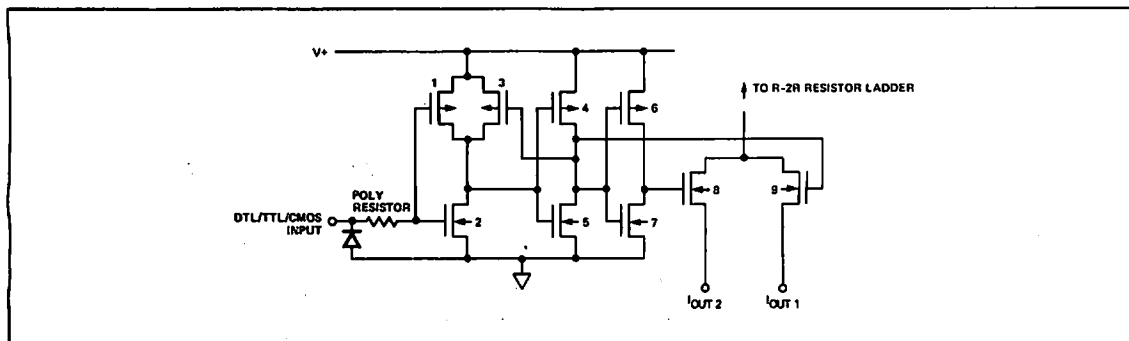
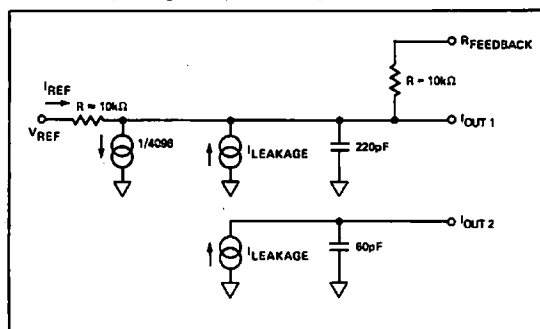


FIGURE 2: CMOS Switch



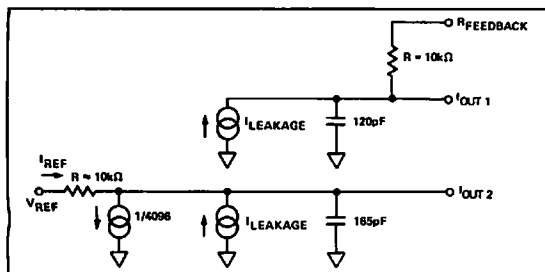
One of the twelve CMOS switches is shown in Figure 2. The digital input stage, devices 1, 2, and 3, drives the two inverters, devices 4, 5, 6, and 7; these inverters in turn drive the two output current steering switches, devices 8 and 9. Devices 1, 2, and 3 are designed such that the digital control inputs are DTL, TTL, and CMOS compatible over the full military temperature range.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., then with a 10 volt reference input, the current through switch 1 is 0.5mA, switch 2 is 0.25mA, etc., a constant 5mV drop will then be maintained across each switch.

FIGURE 4: PM-7541 Equivalent Circuit
(All Digital Inputs HIGH)

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show the equivalent circuits for all digital inputs LOW and HIGH respectively. The reference current is switched to $I_{OUT 2}$ when all inputs are LOW and $I_{OUT 1}$ when inputs are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate; the $1/4096$ current source represents the constant 1-bit current drain through the ladder terminating resistor. The output capacitance is dependent upon the digital input code, and is therefore modulated between the low and high values.

FIGURE 3: PM-7541 Equivalent Circuit
(All Inputs LOW)

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, is also modulated by the digital input code. The resistance looking back into the $I_{OUT 1}$ terminal, may be anywhere between $10k\Omega$ (the feedback resistor alone when all digital inputs are low) and $7.5k\Omega$ (the feedback resistor in parallel with approximately $30k\Omega$ of the R-2R ladder network resistance when any single bit logic is high). The static accuracy and dynamic performance will be affected by this modulation. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7541. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase Compensation (See Figures 5 and 6).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

APPLICATIONS INFORMATION

APPLICATION TIPS

Linearity depends upon the potential of I_{OUT1} and I_{OUT2} (pins 1 and 2) being exactly equal to GND (pin 3). In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground, see Figures 5 and 6. The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than $\pm 200\mu V$ (less than 10% of 1 LSB).

The operational amplifiers usual bias current compensation resistor in the noninverting input should not be used; the input should be connected directly to ground with a low-resistance wire. This resistor can cause a variable offset voltage contributing an error. All pins going to ground should be taken to a common point to avoid ground loops. The V_{DD} power supply should have a low noise level and not have transients greater than $\pm 17V$.

Unused digital inputs must always be grounded or taken to V_{DD} ; this will prevent noise from triggering the high impedance digital input resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value ($1M\Omega$) resistor; this will prevent the accumulation of static charge whenever the PC card is disconnected from the system.

OUTPUT AMPLIFIER CONSIDERATIONS

For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been pointed out that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input-terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

FIGURE 5: Unipolar Binary Operation (2-Quadrant)

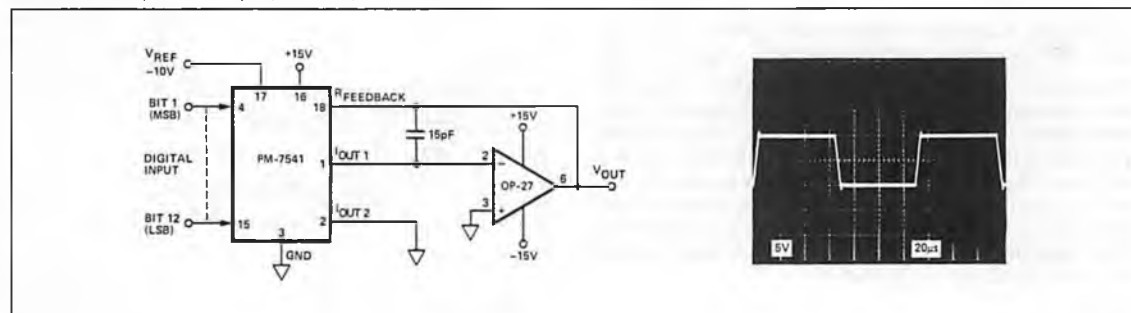
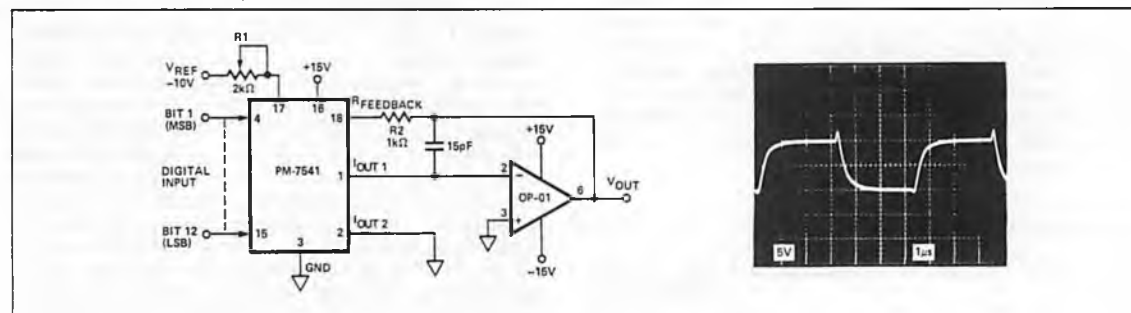


FIGURE 6: Unipolar Binary Operation (2-Quadrant)



The static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 8 and the equation:

$$\text{Error Voltage} = V_{OS} \left(1 + \frac{R_{FB}}{R_O} \right)$$

where R_O = function of digital code.

$$R_O \cong 10k\Omega \text{ for more than 4-bits of logic 1.}$$

$$R_O \cong 30k\Omega \text{ for any single bit logic 1.}$$

Therefore, the offset gain varies as follows:

$$\text{At code } 001111111111: V_{ERROR1} = V_{OS} \left(1 + \frac{10k\Omega}{10k\Omega} \right) = 2 V_{OS}$$

$$\text{At code } 010000000000: V_{ERROR2} = V_{OS} \left(1 + \frac{10k\Omega}{30k\Omega} \right) = \frac{4}{3} V_{OS}$$

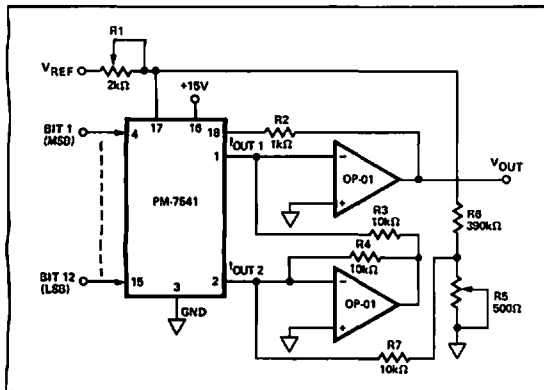
The error difference is $2/3 V_{OS}$.

Since one LSB has a weight (for $V_{REF} = +10V$) of 2.5mV for the PM-7541 DAC, it is clearly important that V_{OS} be nulled, either using the amplifier's nulling pins or an external network.

APPLICATIONS

Figures 5, 6, and 7 show simple unipolar and bipolar circuits with their associated waveforms using the PM-7541 and two PMI types of output amplifiers. A small feedback capacitor should be used across the amplifier to help prevent overshoot and ringing when using high-speed op amps. Resistor R1 is used to trim for full scale, low tempco (approximately 50ppm/°C) resistors or trimpots should be selected when gain adjustments are required.

FIGURE 7: Bipolar Operation (4-Quadrant)



UNIPOLAR BINARY OPERATION (2-QUADRANT)

The circuits of Figures 5 and 6 can either be used as a fixed reference D/A converter, or as an attenuator with an AC input voltage. In the fixed reference mode, the DAC provides an analog output voltage in the range of zero to plus or minus V_{REF} , depending on V_{REF} polarity. The reference input voltage can range between $-20V$ to $+20V$; this is due to the ability of V_{REF} being able to exceed V_{DD} , the limiting factor being the op amp voltage range. Table 1 shows the code relationship for the circuit of Figure 6. R1 can be omitted with a resulting maximum gain error of 0.3% of full scale.

TABLE 1: Code Table for Circuit of Figure 6

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-0.99975 V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 0	$-0.50000 V_{REF}$
0 1 1 1 1 1 1 1 1 1 1 1	$-0.49975 V_{REF}$
0 0 0 0 0 0 0 0 0 0 0 0	0

BIPOLAR BINARY OPERATION (FOUR-QUADRANT)

The recommended circuit and code relationship is shown in Figure 7 and Table 2. The digital input is offset binary coded and multiplies V_{REF} per Table 2. Resistors R3 and R4 should be equal within 0.1% at all temperatures, but need not track the resistors within the PM-7541. The network comprised of R5, R6, and R7 sums $1/2$ LSB of current into I_{OUT2} to ensure correct coding at zero. R1 can be adjusted to produce the outputs shown in Table 2. However, when the application permits it, R1 and R2 should be omitted. The maximum gain error in this condition is 0.3% of full scale. R5 may be replaced by a 100 Ω fixed resistor; the maximum zero error is then 0.015% of full scale. The input offset voltage of both amplifiers should be adjusted to less than 0.1mV and be better than 0.5mV over the temperature range of interest. With V_{REF} set to 10V, R5 is adjusted so that with code 100000000000, $V_{OUT} = 0V \pm 0.2mV$. R1 is adjusted so that code 000000000000 causes V_{OUT} to equal V_{REF} .

TABLE 2: Code Table for Circuit of Figure 7

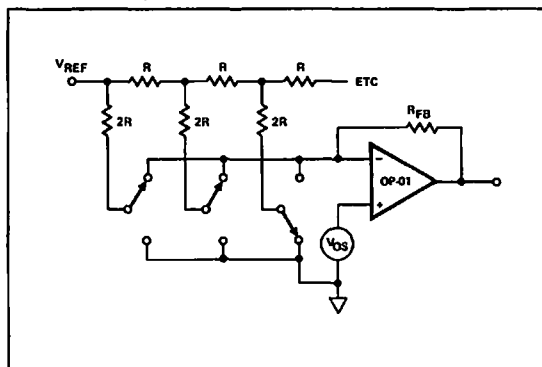
DIGITAL INPUT	NOMINAL ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-0.99951 V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 1	$-0.00049 V_{REF}$
1 0 0 0 0 0 0 0 0 0 0 0	0
0 1 0 0 0 0 0 0 0 0 0 0	$+0.50000 V_{REF}$
0 0 0 0 0 0 0 0 0 0 0 0	$+1.00000 V_{REF}$

OFFSET ADJUSTMENT

1. Adjust V_{REF} to approximately +10V.
2. Set R_5 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT2} amplifier offset trimpot for $0V \pm 0.1mV$ at I_{OUT2} amplifier output.
5. Connect a short circuit across R_4 .
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset trimpot for $0V \pm 0.1mV$ at I_{OUT1} amplifier output.
8. Remove short circuit across R_4 .
9. Connect MSB (Bit-1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R_5 for $0V \pm 0.2mV$ at V_{OUT} .

GAIN ADJUSTMENT

1. Connect all digital inputs to V_{DD} .
2. Monitor V_{OUT} for $-V_{REF} \left(1 - \frac{1}{2^{11}}\right)$ volts reading while adjusting R_1 .

FIGURE 8: Simplified Circuit**ANALOG/DIGITAL DIVISION**

The transfer function for the PM-7541 connected in the multiplying mode as shown in Figure 6 is:

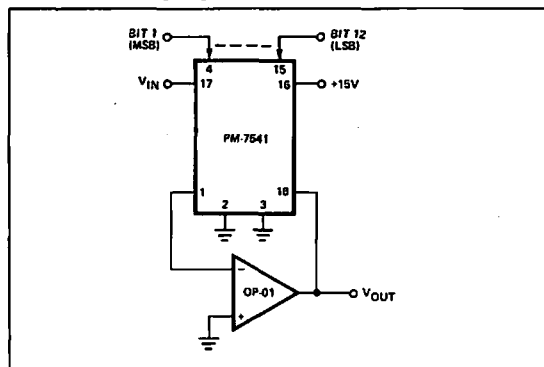
$$V_O = -V_{IN} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}} \right)$$

where A_x assume a value of 1 for an "ON" bit and 0 for an "OFF" bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 9, it now is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}}} \right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (± 1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

FIGURE 9: Analog/Digital Divider



PM-7541A

CMOS 12-BIT MONOLITHIC MULTIPLYING
D/A CONVERTER

Precision Monolithics Inc.

FEATURES

- 7541 With Improved Accuracy And Ruggedness
- $\pm 1/2$ LSB Max Nonlinearity Over Full Temp. Range (12-Bit Linearity)
- ± 1 LSB Max Gain Error—No User Adjustment Required
- Less Than 0.03 LSB Max Zero Scale Error (5nA)
- Low Gain Tempo 5ppm/ $^{\circ}$ C Max
- All Data Input Pins Designed With ESD Protective Circuitry
- Full Four Quadrant Multiplication
- Low Power Consumption
- Low Feedthrough Error And Digital Charge Injection
- Superior Power Supply Rejection
- From +5V to +15V001%/V Max
- Direct Replacement For AD7541 And AD7541A
- Both DIP Packages Suitable For Auto-Insertion, Surface Mount Packaging Available

APPLICATIONS

- Digital/Synchro Conversion
- Programmable Amplifiers
- Ratimetric A/D Conversion
- Function Generators
- Digitally-Controlled Attenuators
- Digitally-Controlled Power Supplies
- Digitally-Controlled Filters

ORDERING INFORMATION†

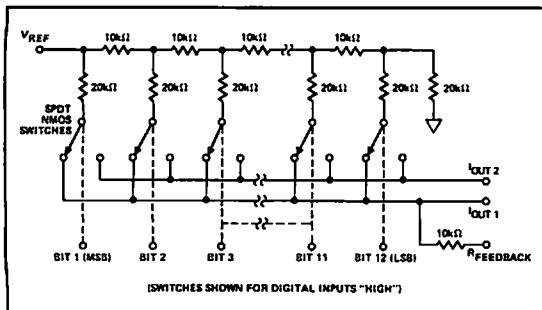
PACKAGES				
GAIN ERROR	NON-LIN- EARITY	MILITARY* TEMPERATURE -55°C to +125°C	INDUSTRIAL TEMPERATURE -25°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
± 1 LSB	$\pm 1/2$ LSB	PM7541AAX	PM7541AEX	PM7541AGP
± 1 LSB	$\pm 1/2$ LSB	PM7541AARC/883	—	—
± 2 LSB	$\pm 1/2$ LSB	PM7541ABX	PM7541AFX	PM7541AHP
± 2 LSB	$\pm 1/2$ LSB	PM7541ABRC/883	—	PM7541AHPCT†

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

FUNCTIONAL DIAGRAM



CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7541AAX	AD7541ATD	MILITARY
PM7541ABX	AD7541ASD	MILITARY
PM7541AEX	AD7541ABQ	INDUSTRIAL
PM7541AFX	AD7541AAQ	INDUSTRIAL
PM7541AGP	AD7541AKN	COMMERCIAL
PM7541AHP	AD7541AJN	COMMERCIAL

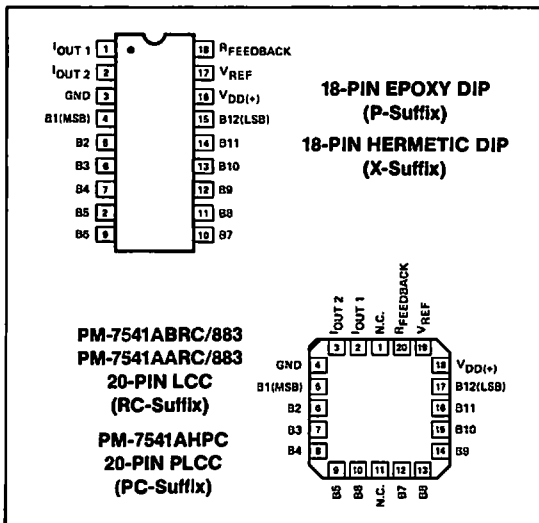
GENERAL DESCRIPTION

PMI's PM-7541A is a 12-bit resolution, current output, 4-quadrant multiplying digital-to-analog converter. Manufactured with advanced oxide-isolated, silicon-gate, monolithic CMOS technology, the PM-7541A features circuitry designed to protect data inputs against damage from electrostatic discharges.

Laser-trimmed thin-film resistors provide true 12-bit linearity with excellent absolute accuracy. The PM-7541A's low power dissipation, along with NMOS temperature compensating switches, insures high performance across the full temperature range.

The PM-7541A is a superior pin-compatible replacement for the industry standard 7541 and the AD7541A. Available in standard plastic and cerdip packages, the PM-7541A is compatible with automatic insertion equipment. The improved performance of the PM-7541A permits upgrading existing designs with greater ruggedness and accuracy. Tighter linearity and gain error specifications may permit reduced system parts count by eliminating trimming circuitry.

PIN CONNECTIONS



DIGITAL-TO-ANALOG CONVERTERS

11

**ABSOLUTE MAXIMUM RATINGS**(T_A = +25°C, unless otherwise noted.)

V _{DD} (to GND)	+17V
V _{REF} (to GND)	±25V
V _{RFB} (to GND)	±25V
Digital Input Voltage Range	V _{DD} to GND
Output Voltage (Pin 1, Pin 2)	-0.3V to V _{DD}
Power Dissipation (Any Package)	450mW
Derate Above +75°C	6mW/°C
Operating Temperature Range	
AX/BX/ARC/BRC Versions	-55°C to +125°C
EX/FX Versions	-25°C to +85°C
GP/HP/HPC Versions	0°C to +70°C

Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 17) and R_{FB} (Pin 18).
2. The digital control inputs are zener protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, V_{OUT 1} = V_{OUT 2} = 0V; T_A = -55°C to +125°C apply for PM-7541AAX/BX/ARC/BRC; T_A = -25°C to +85°C apply for PM-7541AEX/FX; and T_A = 0°C to +70°C apply for PM-7541AGP/HP/HPC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	LSB
Nonlinearity (Note 1)	INL		—	—	±1/2	LSB
Differential Nonlinearity (Note 2)	DNL	PM-7541AA/E/G PM-7541AB/F/H	— —	— —	±1/2 ±1	LSB
Gain Error (Note 3)	G _{FSE}	T _A = +25°C	—	—	1	LSB
		PM-7541AA/E/G	—	—	2	
		PM-7541AB/F/H	—	—	2	
		T _A = Full Temp. Range	—	—	2	
		PM-7541AA/E/G	—	—	3	
PM-7541AB/F/H	—	—	3			
Gain Tempco (ΔGain/ΔTemp.) (Note 6)	TC _{QFS}		—	±2	±5	ppm/°C
Power Supply Rejection Ratio (ΔGain/ΔV _{DD})	PSRR	ΔV _{DD} = ±5%	—	—	±0.001	%/%
		T _A = +25°C	—	—	±0.002	
		T _A = Full Temp. Range	—	—	±0.002	
Output Leakage Current (Notes 4, 5)	I _{LKG}	T _A = +25°C	—	—	5	nA
		PM-7541AA/B/E/F/G/H	—	—	100	
		T _A = Full Temp. Range	—	—	100	
		PM-7541AA/B	—	—	10	
		PM-7541AE/F/G/H	—	—	10	
Zero Scale Error (Notes 12, 13)	I _{ZSE}	T _A = +25°C	—	0.002	—	LSB
		PM-7541AA/B/E/G/H	—	0.002	—	
		T _A = Full Temp. Range	—	0.05	—	
		PM-7541AA/B	—	0.01	—	
		PM-7541AE/F/G/H	—	0.01	—	
REFERENCE INPUTS						
Input Resistance (Note 9)	R _{REF}		7	11	15	kΩ



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = 0V$; $T_A = -55^{\circ}C$ to $+125^{\circ}C$ apply for PM-7541AAX/BX/ARC/BRC; $T_A = -25^{\circ}C$ to $+85^{\circ}C$ apply for PM-7541AEX/FX; and $T_A = 0^{\circ}C$ to $+70^{\circ}C$ apply for PM-7541AGP/HP/HPC, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{DD} Range	V_{DD}	Accuracy is not guaranteed over this range	+5	15	+17	V
		Digital Inputs = V_{IH} or V_{IL}	—	—	2	mA
Supply Current	I_{DD}	Digital Inputs = 0V or V_{DD} $T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	— —	— —	100 100	μA
DIGITAL INPUTS						
Digital Input High	V_{IH}		2.4	—	—	V
Digital Input Low	V_{IL}		—	—	0.8	V
Input Leakage Current (Note 10)	I_{IL}	$V_{IN} = 0$ to $+15V$	—	—	± 1	μA
Input Capacitance (Note 6)	C_{IN}	$V_{IN} = 0V$	—	—	8	pF
DYNAMIC PERFORMANCE						
Propagation Delay (Notes 6, 7)	t_{PD}	From Digital Input Change to 90% of Final Analog Output $T_A = +25^{\circ}C$	—	100	150	ns
Output Current Settling Time (Notes 6, 7, 8)	t_s	To $\pm 1/2$ LSB ($\pm 0.01\%$ of Full Scale Range) $T_A = +25^{\circ}C$	—	0.6	1	μs
Feedthrough Error (V_{REF} to I_{OUT}) (Note 6)	FT	$V_{REF} = 20V_{P-P}$ @ $f = 10kHz$ All Digital Inputs Low $T_A = +25^{\circ}C$	—	2	5	mV _{P-P}
Digital to Analog Glitch Energy (Notes 6, 11)	Q	$T_A = +25^{\circ}C$	—	700	1000	nVs
ANALOG OUTPUTS						
Output Capacitance (Note 6)	C_{OUT1}	Digital Inputs = V_{IH}	—	85	120	pF
	C_{OUT2}		—	30	50	
	C_{OUT1}	Digital Inputs = V_{IL}	—	30	50	
	C_{OUT2}		—	85	120	

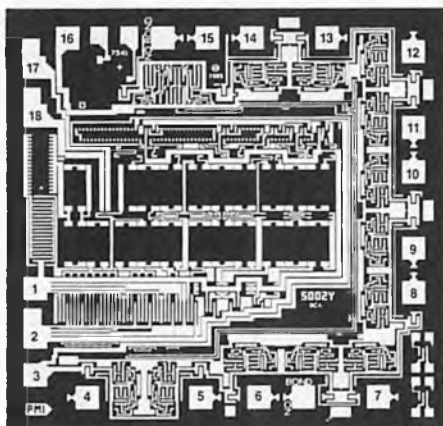
NOTES:

- $\pm 1/2$ LSB = $\pm 0.012\%$ of Full Scale.
- All grades are monotonic to 12-bits over temperature.
- Using internal feedback resistor.
- Applies to I_{OUT1} ; digital inputs = V_{IL} .
- Specification also applies for I_{OUT2} with all digital inputs = V_{IH} .
- Guaranteed by design and not tested.
- I_{OUT} Load = 100 Ω , C_{EXT} = 13pF, digital inputs = 0V to V_{DD} or V_{DD} to 0V.

- Extrapolated to $1/2$ LSB: t_s = Propagation Delay (t_{PD}) + 9τ , where τ = measured first time constant of the final RC decay.
- Absolute temperature coefficient is approximately $+50$ ppm/ $^{\circ}C$.
- Digital inputs are CMOS gates; I_{IN} is typically 1nA at $+25^{\circ}C$.
- $V_{REF} = 0V$, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
- $V_{REF} = +10V$, all digital inputs = 0V.
- Calculated from: $I_{ZSE}(\text{in LSBs}) = \frac{R_{REF}(4096)I_{LKG}}{V_{REF}}$



DICE CHARACTERISTICS



DIE SIZE 0.102 × 0.100 Inch, 10,200 sq. mils
(2.59 × 2.54 mm, 6.58 sq. mm)

1. CURRENT OUTPUT 1
2. CURRENT OUTPUT 2
3. GROUND
4. DIGITAL INPUT (BIT 1) (MOST SIGNIFICANT BIT)
5. DIGITAL INPUT (BIT 2)
6. DIGITAL INPUT (BIT 3)
7. DIGITAL INPUT (BIT 4)
8. DIGITAL INPUT (BIT 5)
9. DIGITAL INPUT (BIT 6)
10. DIGITAL INPUT (BIT 7)
11. DIGITAL INPUT (BIT 8)
12. DIGITAL INPUT (BIT 9)
13. DIGITAL INPUT (BIT 10)
14. DIGITAL INPUT (BIT 11)
15. DIGITAL INPUT (BIT 12) (LEAST SIGNIFICANT BIT)
16. POSITIVE POWER SUPPLY
17. REFERENCE INPUT VOLTAGE
18. INTERNAL FEEDBACK RESISTOR

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +15V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = +25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	PM-7541AG LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Nonlinearity	INL		$\pm 1/2$	LSB MAX
Differential Nonlinearity	DNL		± 1	LSB MAX
Gain Error (Note 1)	G_{FSE}		± 1	LSB MAX
Power Supply Rejection	PSRR	$\Delta V_{DD} = \pm 5\%$	± 0.001	%/% MAX
Output Leakage Current (I_{OUT1}) (Note 2)	I_{LKG}	Digital Inputs = V_{IL}	± 5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		7/15	k Ω MIN/MAX
DIGITAL INPUTS				
Digital Input High	V_{IH}		2.4	V MIN
Digital Input Low	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	$V_{IN} = 0$ to $15V$	± 1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	2	mA MAX
		Digital Inputs = $0V$ or V_{DD}	100	μA MAX

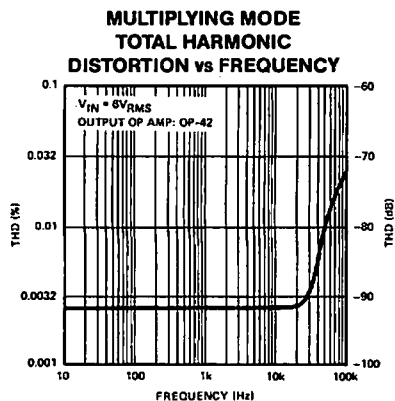
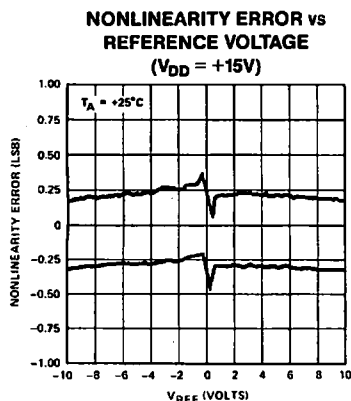
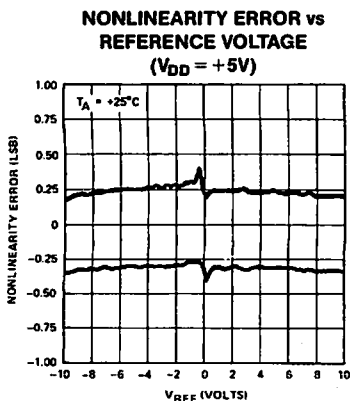
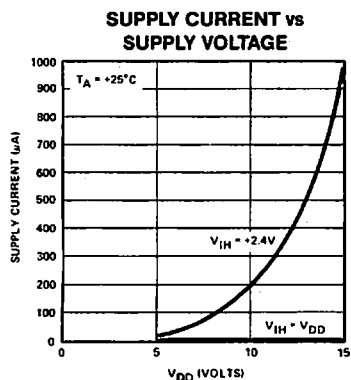
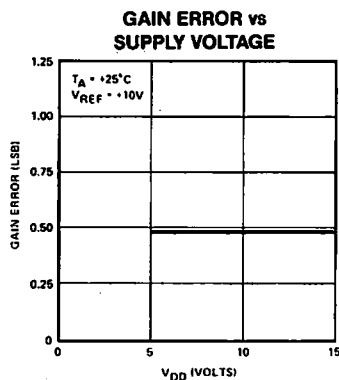
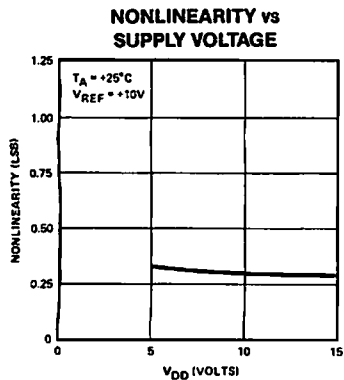
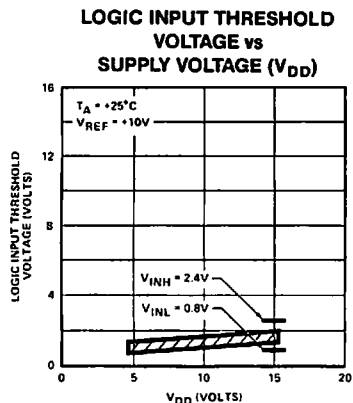
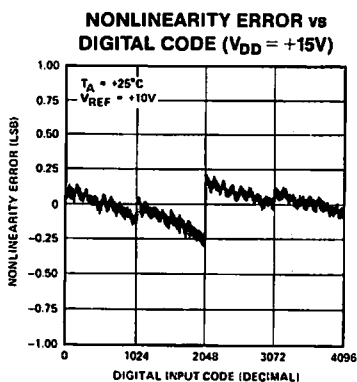
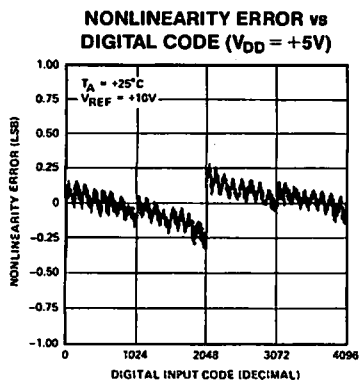
NOTES:

1. Using internal feedback resistor.
2. Specification also applies for I_{OUT2} but all Digital Inputs = V_{IH} .

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

APPLICATION TIPS

Linearity depends upon the potential of I_{OUT1} and I_{OUT2} (pins 1 and 2) being exactly equal to GND (pin 3). In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground, see Figures 5 and 6. The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be null'd to less than $\pm 200\mu\text{V}$ (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than +17V.

Unused digital inputs must always be grounded or taken to V_{DD} ; this will prevent noise from triggering the high impedance digital input resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value (1M Ω) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition voltage. The supply current decreases as the input voltage approaches the supply rails (V_{DD} or $DGND$), i.e., rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input-terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

The static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 7 and the equation:

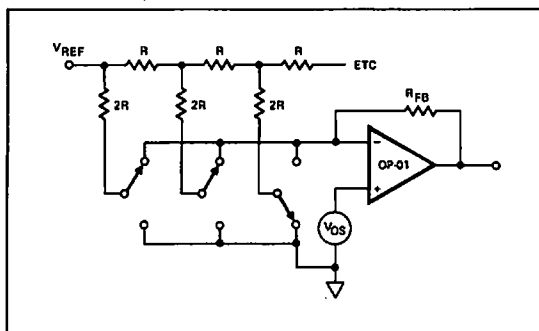
$$\text{Error Voltage} = V_{OS} \left(1 + \frac{R_{FB}}{R_O} \right)$$

where R_0 is a function of the digital code, and:

$R_0 \cong 10k\Omega$ for more than 4-bits of logic 1

$R_O \cong 30k\Omega$ for any single bit logic 1

FIGURE 7: Simplified Circuit



Therefore, the offset gain varies as follows:

At code 0011 1111 1111: $V_{\text{ERROR}1} = V_{\text{OS}} \left(1 + \frac{10\text{k}\Omega}{10\text{k}\Omega} \right) = 2 V_{\text{OS}}$

At code 0100 0000 0000: $V_{\text{ERROR } 2} = V_{\text{OS}} \left(1 + \frac{10\text{k}\Omega}{30\text{k}\Omega} \right) = \frac{4}{3} V_{\text{OS}}$

The error difference is $\frac{2}{3} V_{OS}$.

Since one LSB has a weight (for $V_{REF} = +10V$) of 2.5mV for the PM-7541A DAC, it is clearly important that V_{OS} be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS} . Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, and OP-27.

APPLICATIONS

Figures 5, 6, and 8 show simple unipolar and bipolar circuits with their associated waveforms using the PM-7541A and two types of PMI output amplifiers. A small feedback capacitor should be used across the amplifier to help prevent overshoot and ringing when using high-speed op amps. Resistor R1 is used to trim for full scale. Low tempco (approximately 50ppm/°C) resistors or trimpots should be selected when gain adjustments are required.

UNIPOLAR BINARY OPERATION (2-QUADRANT)

The circuits of Figures 5 and 6 can either be used as a fixed reference D/A converter, or as an attenuator with an AC input voltage. In the fixed reference mode, the DAC provides an analog output voltage in the range of zero to plus or minus V_{REF} , depending on V_{REF} polarity. The reference input voltage can range between $-20V$ to $+20V$; this is due to the ability of V_{REF} being able to exceed V_{DD} , the limiting factor being the op amp's voltage range. Table 1 shows the code relationship for the circuit of Figures 5 and 6. R1 can be omitted with a resulting maximum gain error of 0.02% of full scale.

TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT MSB	NOMINAL ANALOG OUTPUT LSB (V_{OUT} as shown in Figures 5 and 6)
1111 1111 1111	$-V_{REF} \left(\frac{4095}{4096} \right)$
1000 0000 0001	$-V_{REF} \left(\frac{2049}{4096} \right)$
1000 0000 0000	$-V_{REF} \left(\frac{2048}{4096} \right) = -\frac{V_{REF}}{2}$
0111 1111 1111	$-V_{REF} \left(\frac{2047}{4096} \right)$
0000 0000 0001	$-V_{REF} \left(\frac{1}{4096} \right)$
0000 0000 0000	$-V_{REF} \left(\frac{0}{4096} \right) = 0$

NOTES:

1. Nominal full scale for the circuits of Figures 5 and 6 is given by
 $FS = -V_{REF} \left(\frac{4095}{4096} \right)$.
2. Nominal LSB magnitude for the circuits of Figures 5 and 6 is given by
 $LSB = V_{REF} \left(\frac{1}{4096} \right)$ or $V_{REF} (2^{-10})$.

BIPOLAR BINARY OPERATION (4-QUADRANT)

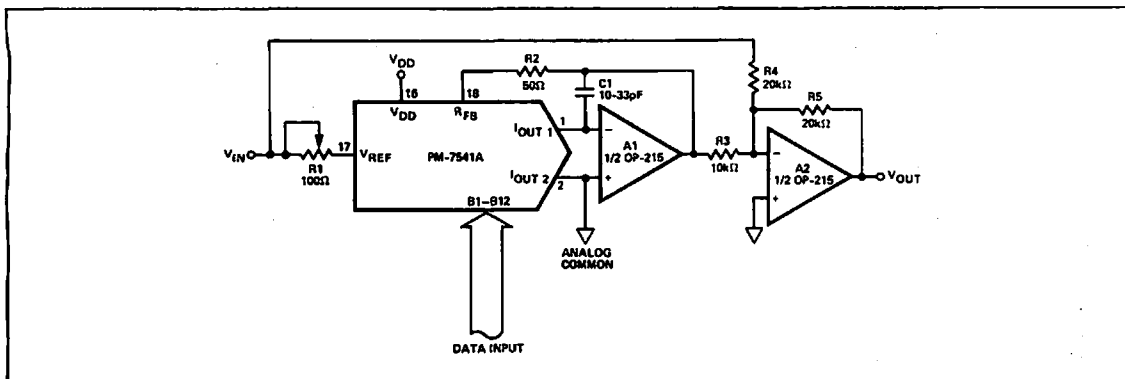
Figure 8 shows a simple bipolar output circuit using the PM-7541A and a PMI OP-215 dual op amp. The circuit uses offset binary coding and a fixed DC voltage for V_{REF} . Digitally-controlled attenuation of an AC signal occurs when the signal is used as the signal source at V_{REF} . Negative output full-scale is adjusted by setting the digital inputs to all zeros and adjusting the value of the V_{IN} voltage or R5. The zero-scale output voltage is adjusted while the digital inputs are set to 1000 0000 0000 by adjusting R1 for a zero output voltage (less than 10% of 1 LSB). Resistors R3, R4, and R5 must be selected for matching and tracking in order to keep offset and full scale errors to a minimum. Resistors R1 and R2 temperature coefficients must be taken into account if they are used. C1 phase compensation capacitor may not be needed and should be selected empirically. The digital input code versus analog output voltage is shown in Table 2.

TABLE 2: Bipolar (Offset Binary) Code Table

DIGITAL INPUT MSB	NOMINAL ANALOG OUTPUT LSB (V_{OUT} as shown in Figure 8)
1111 1111 1111	$+V_{REF} \left(\frac{2047}{2048} \right)$
1000 0000 0001	$+V_{REF} \left(\frac{1}{2048} \right)$
1000 0000 0000	0
1111 1111 1111	$-V_{REF} \left(\frac{1}{2048} \right)$
0000 0000 0001	$-V_{REF} \left(\frac{2047}{2048} \right)$
0000 0000 0000	$-V_{REF} \left(\frac{2048}{2048} \right)$

NOTES:

1. Nominal full scale for the circuit of Figure 8 is given by
 $FS = V_{REF} \left(\frac{2047}{2048} \right)$.
2. Nominal LSB magnitude for the circuit of Figure 8 is given by
 $LSB = V_{REF} \left(\frac{1}{2048} \right)$.

FIGURE 8: Bipolar Operation (4-Quadrant Multiplication)

ANALOG/DIGITAL DIVISION

The transfer function for the PM-7541A connected in the multiplying mode as shown in Figures 5 and 6 is:

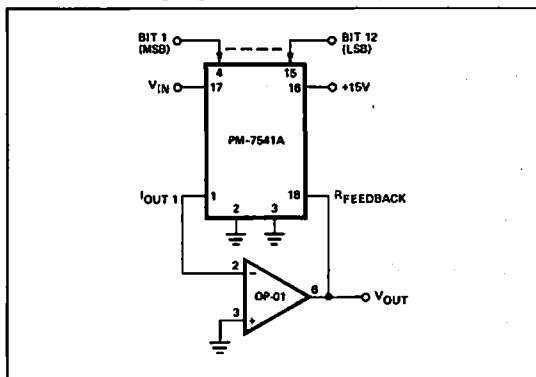
$$V_O = -V_{IN} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}} \right)$$

where A_x assume a value of 1 for an "ON" bit and 0 for an "OFF" bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 9, it now is:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}}} \right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (± 1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

FIGURE 9: Analog/Digital Divider




PM-7542

12-BIT (4-BIT NYBBLE INPUT)
MULTIPLYING CMOS D/A CONVERTER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- 4-Bit Bus Compatible 12-Bit Multiplying DAC
- Complete Microprocessor Interface with On-Chip Address Decoding and Asynchronous CLEAR Input
- Fast Interface Timing
- Superior Accuracy: $\pm 1/2$ LSB INL Error Over Temperature and ± 1 LSB Gain Error
- Excellent Power Supply Rejection 0.002%/°C Max
- Reduced Digital Charge Injection
- Reduced Output Capacitance
- Small (16-Pin), Narrow (0.3") DIP Packages Suitable for Auto-Insertion and SO Surface Mount Package
- Improved ESD Resistance
- Superior Direct Replacement for AD7542

APPLICATIONS

- Process Control and Industrial Automation
- Programmable Amplifiers
- Digitally-Controlled Power Supplies
- Digitally-Controlled Attenuators
- Digitally-Controlled Filters
- Instrumentation
- Avionics

ORDERING INFORMATION†

GAIN ERROR	NON-LINEARITY	MILITARY* TEMPERATURE	INDUSTRIAL TEMPERATURE	COMMERCIAL TEMPERATURE
± 1 LSB	$\pm 1/2$ LSB	PM7542AQ	PM7542EQ	PM7542GP
± 2 LSB	$\pm 1/2$ LSB	PM7542BQ	PM7542FQ	PM7542HP
± 2 LSB	$\pm 1/2$ LSB	PM7542BRC/883††	—	PM7542HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

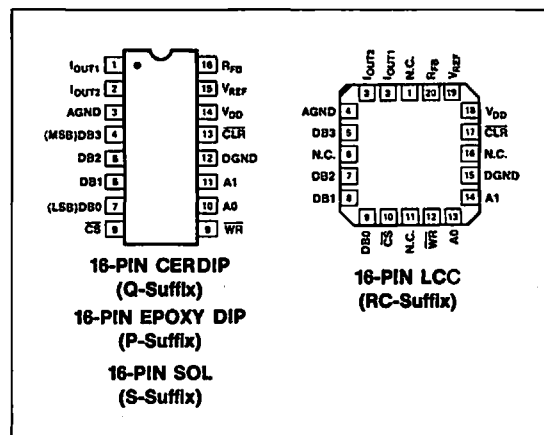
CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7542AQ PM7542BQ PM7542BQ	AD7542GTD AD7542TD AD7542SD	MIL
PM7542EQ PM7542FQ PM7542FQ	AD7542GBO AD7542BD AD7542AD	IND
PM7542GP PM7542HP PM7542HP	AD7542GKN AD7542KN AD7542JN	COM

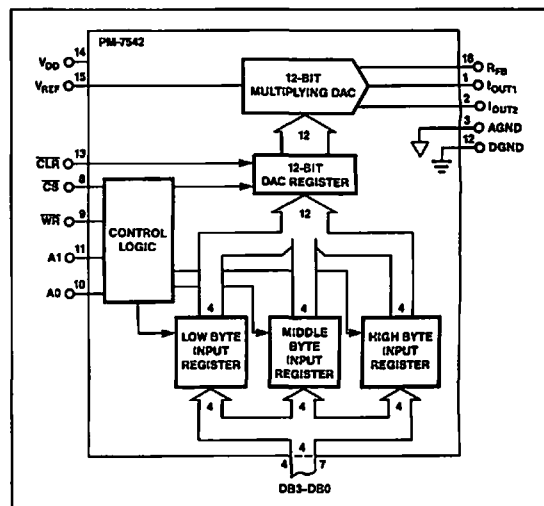
GENERAL DESCRIPTION

The PM-7542 is a 12-bit resolution, current output, multiplying CMOS DAC with a microprocessor interface to 4-bit busses. Improved analog accuracy, a fast digital interface, and input ESD protective circuitry make this a superior second-source to the industry standard 7542. This improved performance permits the easy upgrading of accuracy and ruggedness in existing designs.

PIN CONNECTIONS



FUNCTIONAL BLOCK DIAGRAM



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



Under microprocessor control, 4-bit data bytes are loaded from a data bus into three 4-bit input registers. The resulting 12-bit data word can then be transferred to a DAC register, updating the analog output. Data input and transfer operations resemble the WRITE cycle of a static RAM. An asynchronous CLEAR input permits the immediate resetting of the DAC register to all zeros, without affecting the data resident in the input registers.

Improved linearity and gain error performance may permit a reduced circuit parts count through the elimination of trimming components. Fast interface timing reduces design considerations while minimizing microprocessor wait states. The PM-7542 is available in standard plastic and cerdip packages that are compatible with auto-insertion equipment.

ABSOLUTE MAXIMUM RATINGS

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

V_{DD} (to DGND)	+17V
V_{REF} (to DGND)	$\pm 25\text{V}$
V_{RFB} (to DGND)	$\pm 25\text{V}$

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5\text{V}$; $V_{REF} = +10\text{V}$; $V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0\text{V}$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for PM-7542AQ/BQ; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for PM-7542EQ/FQ; and $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for PM-7542GP/HP, unless otherwise noted.

			PM-7542			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Nonlinearity (Note 1)	INL		—	—	±1/2	LSB
Differential Nonlinearity (Note 2)	DNL	PM-7542A/E/G PM-7542B/F/H	— —	— —	±1/2 ±1	LSB
Gain Error (Note 3)	G _{FSE}	T _A = +25°C				
		PM-7542A/E/G	—	—	1	
		PM-7542B/F/H	—	—	2	
		T _A = Full Temp. Range				
		PM-7542A/E/G	—	—	2	
PM-7542B/F/H	—	—	3			
Gain Tempco (ΔGain/ΔTemp) (Note 6)	TC _{GFS}		—	—	±5	ppm/°C
Power Supply Rejection Ratio (ΔGain/ΔTemp)	PSRR	ΔV _{DD} = ±5%	—	—	±0.002	%/%
Output Leakage Current (Notes 4, 5)	I _{LKG}	T _A = +25°C	—	—	±5	
		T _A = Full Temp. Range				
		PM-7542A/B	—	—	±100	nA
		PM-7542E/F/G/H	—	—	±25	
Zero Scale Error (Notes 8, 13)	I _{ZSE}	T _A = +25°C	—	0.002	—	
		T _A = Full Temp. Range				
		PM-7542A/B	—	0.05	—	LSB
		PM-7542E/F/G/H	—	0.01	—	

AGND to DGND	-0.3V to V_{DD}
Digital Input Voltage Range	-0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2)	-0.3V to V_{DD}
Power Dissipation (Any Package)	450mW
Derate Above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	
A/B/BRC Versions	-55°C to $+125^\circ\text{C}$
E/F Versions	-40°C to $+85^\circ\text{C}$
GP/HP/HS Versions	0°C to $+70^\circ\text{C}$
Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than AGND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = +10V$; $V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ for PM-7542AQ/BQ; $T_A = -40^\circ C$ to $+85^\circ C$ for PM-7542EQ/FQ; and $T_A = 0^\circ C$ to $+70^\circ C$ for PM-7542GP/HP, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	PM-7542 TYP	MAX	UNITS
Input Resistance (Note 9)	R_{IN}		7	11	15	k Ω
AC PERFORMANCE						
Output Current Settling Time (Notes 6, 7)	t_s	$T_A = +25^\circ C$	—	—	1	μs
Digital to Analog Glitch Energy (Note 6)	Q	$V_{REF} = 0V$ I_{OUT} Load = 100 Ω $C_{EXT} = 13pF$ DAC register loaded alternately with all 0s and all 1s	—	—	200	nVs
Total Harmonic Distortion (Note 6)	THD	$V_{REF} = 6V$ RMS @ 1kHz DAC register loaded with all 1s	—	—	—90	dB
Output Noise Voltage Density (Notes 6, 14)	e_n	10Hz to 100kHz measured between R_{FB} and I_{OUT}	—	—	13	nV/ $\sqrt{Hz}$
POWER SUPPLY						
Supply Voltage Range	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	All digital inputs = V_{IH} or V_{IL} All digital inputs = 0V or V_{DD}	— —	— —	2.5 0.1	mA
DIGITAL INPUTS						
Digital Input HIGH	V_{IH}		2.4	—	—	V
Digital Input LOW	V_{IL}		—	—	0.8	V
Input Leakage Current (Note 10)	I_{IL}	$V_{IN} = 0V$ to $+5V$	—	—	± 1	μA
Input Capacitance (Note 6)	C_{IN}	$V_{IN} = 0V$	—	—	8	pF
ANALOG OUTPUTS						
Output Capacitance (Note 6)	C_{OUT}	Digital Inputs = V_{IH}	—	—	140	pF
Output Capacitance (Note 6)	C_{OUT}	Digital Inputs = V_{IL}	—	—	70	pF
TIMING CHARACTERISTICS (Note 6)						
WRITE Pulse Width	t_{WR}	$T_A = +25^\circ C$	120	—	—	ns
		$T_A =$ Full Temp. Range	220	—	—	ns
CLEAR Pulse Width	t_{CLR}	$T_A = +25^\circ C$	200	—	—	ns
		$T_A =$ Full Temp. Range	300	—	—	ns
Address Valid to WRITE Hold Time	t_{AWH}	$T_A = +25^\circ C$	50	—	—	ns
		$T_A =$ Full Temp. Range	65	—	—	ns
Chip Select to WRITE Hold Time	t_{CWH}	$T_A = +25^\circ C$	50	—	—	ns
		$T_A =$ Full Temp. Range	100	—	—	ns
Input Register Loading Chip Select to WRITE Set-up Time	t_{CWS}	$T_A = +25^\circ C$	60	—	—	ns
		$T_A =$ Full Temp. Range	130	—	—	ns



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = +10V$; $V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ for PM-7542AQ/BQ; $T_A = -40^\circ C$ to $+85^\circ C$ for PM-7542EQ/FQ; and $T_A = 0^\circ C$ to $+70^\circ C$ for PM-7542GP/HP, unless otherwise noted. (Continued)

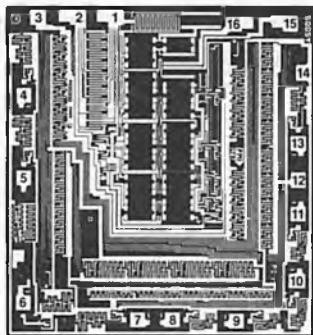
PARAMETER	SYMBOL	CONDITIONS	MIN	PM-7542	MAX	UNITS
				TYP		
Input Register Loading Address Valid to WRITE Set-up Time	t_{AWS}	$T_A = +25^\circ C$	80	—	—	ns
		$T_A = \text{Full Temp. Range}$	180	—	—	
Data Set-up Time	t_{DS}	$T_A = +25^\circ C$	50	—	—	ns
		$T_A = \text{Full Temp. Range}$	65	—	—	
Data Hold Time	t_{DH}	$T_A = +25^\circ C$	50	—	—	ns
		$T_A = \text{Full Temp. Range}$	65	—	—	
DAC Register Loading Chip Select to WRITE Set-up Time	t_{CWS}	$T_A = +25^\circ C$	60	—	—	ns
		$T_A = \text{Full Temp. Range}$	150	—	—	
DAC Loading Address Valid to WRITE Set-up Time	t_{AWS}	$T_A = +25^\circ C$	120	—	—	ns
		$T_A = \text{Full Temp. Range}$	240	—	—	

NOTES:

- $\pm 1/2$ LSB = $\pm 0.012\%$ of Full Scale.
- All grades are monotonic to 12-bits over temperature.
- Using internal feedback resistor.
- Applies to I_{OUT1} ; all digital inputs = V_{IL} .
- Specification also applies for I_{OUT2} when all digital inputs = V_{IH} .
- Guaranteed by design and not tested.
- I_{OUT1} Load = 100Ω , $C_{EXT} = 13pF$, digital input = $0V$ to V_{DD} or V_{DD} to $0V$.
- $V_{REF} = +10V$, all digital inputs = $0V$.
- Absolute temperature coefficient is less than $+50$ ppm/ $^\circ C$.
- Digital inputs are CMOS gates; I_{IN} is typically $1nA$ at $+25^\circ C$.
- $V_{REF} = 0V$, all digital inputs = $0V$ to V_{DD} or V_{DD} to $0V$.
- All digital inputs = $0V$.
- Calculated from worst case R_{REF} :
 I_{ZSE} (in LSBs) = $(R_{REF} \times I_{LKG} \times 4096) / V_{REF}$.
- Calculations from $e_n = \sqrt{4KTRB}$ where:
 K = Boltzmann constant, $J/^\circ K$ R = resistance Ω
 T = resistor temperature, $^\circ K$ B = bandwidth, Hz



DICE CHARACTERISTICS



DIE SIZE 0.116 × 0.109 inch, 12,644 sq. mils
(2.95 × 2.77 mm, 8.17 sq. mm)

- | | |
|--------------------|--------------------------|
| 1. I_{OUT1} | 9. $\overline{WR}$ |
| 2. I_{OUT2} | 10. A0 |
| 3. AGND | 11. A1 |
| 4. DB3 (MSB) | 12. DGND |
| 5. DB2 | 13. CLR |
| 6. DB1 | 14. V_{DD} (Substrate) |
| 7. DBO (LSB) | 15. V_{REF} |
| 8. $\overline{CS}$ | 16. R_{FB} |

For additional DICE ordering information, refer to
1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +5V$, $V_{REF} = +10V$; $V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

PM-7542GBC				
PARAMETER	SYMBOL	CONDITIONS	LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Integral Nonlinearity	INL		$\pm 1/2$	LSB MAX
Differential Nonlinearity	DNL		$\pm 1/2$	LSB MAX
Gain Error	G_{FSE}	Using internal feedback resistor	± 1	LSB MAX
Power Supply Rejection Ratio	PSRR	$\Delta V_{DD} = \pm 5\%$	± 0.002	%/% MAX
Output Leakage Current (I_{OUT1})	I_{LKG}	Digital Inputs = V_{IL}	± 5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		7/15	k Ω MIN/MAX
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V MIN
Digital Input LOW	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	$V_{IN} = 0V$ to V_{DD}	± 1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}	2.5	mA MAX
		Digital Inputs = $0V$ or V_{DD}	0.1	

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e. zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output. Feedthrough error limits are specified with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} terminal to ground.

OUTPUT LEAKAGE CURRENT

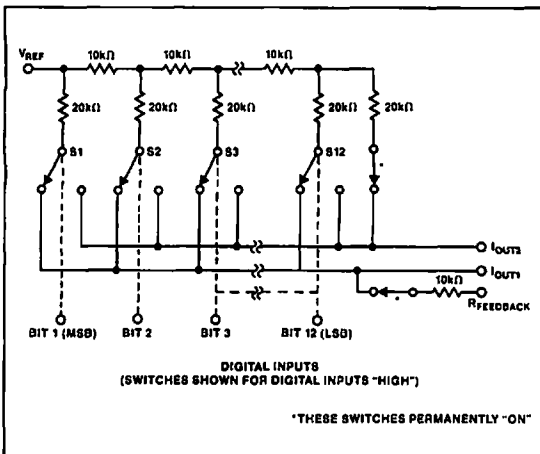
Current appearing at I_{OUT1} when all digital inputs are LOW, or at I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The PM-7542 is a 12-bit multiplying D/A converter with a very low temperature coefficient, R-2R resistor ladder network, data input and control logic, and four data registers. The digital circuitry forms an interface between the 12-bit DAC and a four-bit data bus.

An asynchronous CLEAR function allows resetting the DAC register to a zero code (0000 0000 0000) without altering data stored in the registers.

FIGURE 1: Simplified DAC Circuit



A simplified circuit of the PM-7542 DAC is shown in Figure 1. An inverted R-2R ladder network consisting of silicon-chrome, thin-film resistor, and twelve pairs of NMOS current-steering switches steer binarily weighted currents into either I_{OUT1} or I_{OUT2} . Switching current to I_{OUT1} or I_{OUT2} yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R (typically 11kΩ). The V_{REF} input may be driven by any reference voltage or current, AC or DC, that is within the limits stated in the Absolute Maximum Ratings chart.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., a constant 5mV drop will then be maintained across each switch.

To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R-2R ladder's terminating resistor. The "Simplified DAC Circuit", Figure 1, shows the location of the series switches. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

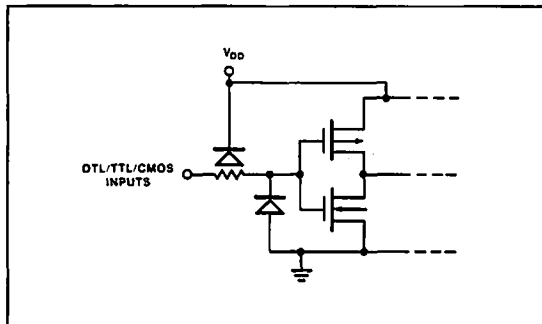
ESD PROTECTION

The PM-7542 data inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes.

These protection diodes are designed to clamp the inputs well below dangerous levels during static discharge conditions.

FIGURE 2: Digital Input Protection



EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits for the DAC with all bits LOW and HIGH, respectively. The reference current is switched to I_{OUT2} when all data bits are LOW and to I_{OUT1} when all bits are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate. The $1/4096$ current source represents the constant 1-bit current drain through the ladder's terminating resistor.

Output capacitance is dependent upon the digital input code. This is because the gate capacitance of MOS transistors increases with applied gate voltage. This output capacitance varies between the low and high values.

FIGURE 3: PM-7542 Equivalent Circuit (All Inputs LOW)

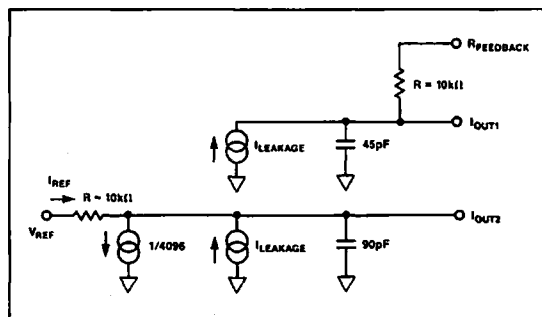
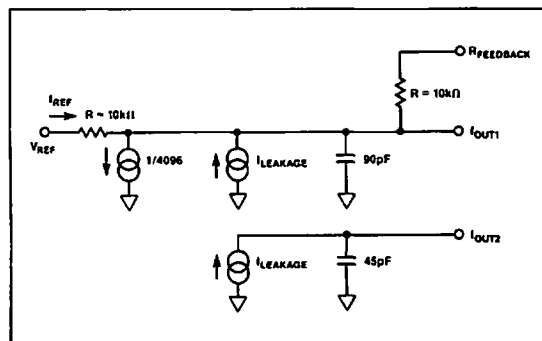


FIGURE 4: PM-7542 Equivalent Circuits (All Digital Inputs HIGH)



DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT} terminal, may be between $11k\Omega$ (the feedback resistor alone when all digital inputs are LOW) and $7.5k\Omega$ (the feedback resistor in parallel with approximately $30k\Omega$ of the R-2R ladder network resistance when any single bit logic is HIGH). Static accuracy and dynamic performance will be affected by these variations. The gain and phase stability of the output amplifier, board layout, and power

supply decoupling will all affect the dynamic performance of the PM-7542. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 8 and 9).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

APPLICATIONS INFORMATION

APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT1} , I_{OUT2} , and AGND (pins 1, 2, and 3) being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground (see Figures 8 and 9). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than $\pm 200\mu V$ (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a single common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than $+17V$.

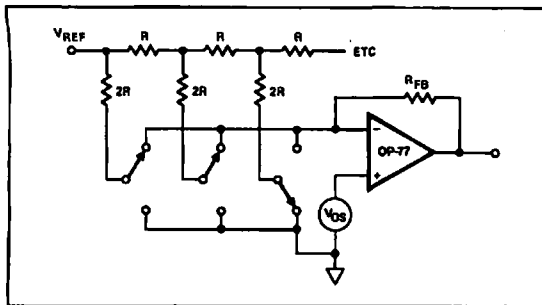
Unused digital inputs must always be grounded or taken to V_{DD} ; this will prevent noise from triggering the high impedance digital inputs resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value ($1M\Omega$) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition voltage. The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e. rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

When using high speed op amps, a small feedback capacitor (typically $15pF$) should be used across the amplifier to minimize overshoot and ringing. For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

FIGURE 5: Simplified Circuit



Static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 5 and the equation:

$$V_{\text{ERROR}} = V_{\text{OS}} \left(1 + \frac{R_{\text{FB}}}{R_{\text{O}}} \right)$$

where R_{O} is a function of the digital code, and:
 $R_{\text{O}} = 10\text{k}\Omega$ for more than four bits of logic 1,
 $R_{\text{O}} = 30\text{k}\Omega$ for any single bit of logic 1.

Therefore, the offset gain varies as follows:
 at code 0011 1111 1111,

$$V_{\text{ERROR}} = V_{\text{OS}} \left(1 + \frac{10\text{k}\Omega}{10\text{k}\Omega} \right) = 2V_{\text{OS}}$$

at code 0100 0000 0000,

$$V_{\text{ERROR}} = V_{\text{OS}} \left(1 + \frac{10\text{k}\Omega}{30\text{k}\Omega} \right) = 4/3V_{\text{OS}}$$

The error difference is $2/3 V_{\text{OS}}$.

Since one LSB has a weight (for $V_{\text{REF}} = +10\text{V}$) of 2.4 mV for the PM-7542, it is clearly important that V_{OS} be minimized,

either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS} . Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, OP-27, and OP-42.

INTERFACE LOGIC OPERATION

The PM-7542 has been designed to be interfaced as a memory mapped output device as shown in Figure 6.

As shown in the device truth table, Table 1, $\overline{\text{CS}}$ is an externally decoded device address, selecting the device when needed.

A0 and A1 are internally decoded operation addresses. Each of these four available operations requires a memory location. Data operations are performed by executing a memory WRITE to the address for that operation. This WRITE cycle is identical to that of a RAM. Updating the entire 12-bit data word requires four WRITE cycles (three data nybble loads and one data word transfer). Timing for a WRITE cycle is shown in Figure 7.

The $\overline{\text{CLR}}$ input allows the asynchronous reset of the DAC register to 0000 0000 0000. This reset does not affect data held in the input registers. While in unipolar mode, a CLEAR will result in the analog output going to 0V. In bipolar mode, the output will go to $-V_{\text{REF}}$.

INTERFACE INPUT DESCRIPTION

$\overline{\text{CS}}$ (Pin 8)—Chip Select. Active Low.

Selected, with $\overline{\text{WR}}$ data into an input register or transfer data from input to DAC registers.

$\overline{\text{WR}}$ (Pin 9)—Write Input. Active Low.

Selected, with $\overline{\text{CS}}$ and appropriate address inputs, to load data into an input register or transfer data from input to DAC registers.

A0 (Pin 10), A1 (Pin 11)—Address Inputs.

Addressed, with $\overline{\text{CS}}$ and $\overline{\text{WR}}$ selected, to perform data load or data transfer operations. See Table 1 for truth table.

$\overline{\text{CLR}}$ (Pin 13)—Clear Input. Active Low. Asynchronous.

When LOW, 12-bit DAC register is forced to a zero code (0000 0000 0000) regardless of other interface inputs.

FIGURE 6: Simplified Input Control Structure

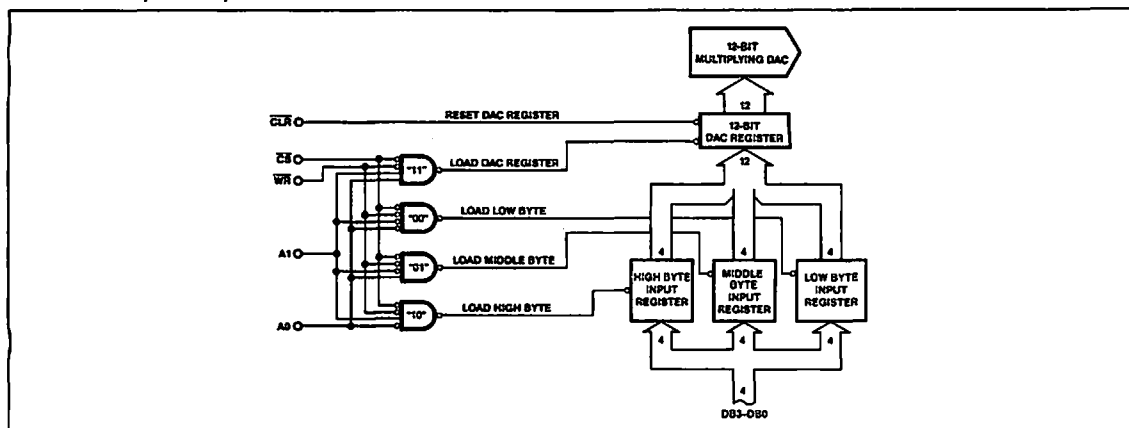


TABLE 1: PM-7542 Truth Table

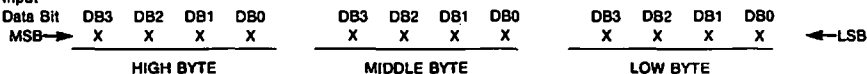
CONTROL INPUTS					OPERATION
A1	A0	CS	WR	CLR	
X	X	X	X	0	Reset 12-bit DAC Register to Zero Code (Code = 0000 0000 0000). Does not affect Input Registers.
X	X	1	X	1	No operation. Device not selected.
0	0	0		1	Load LOW Byte (Note 5) Data Register on Rising Edge.
0	1	0		1	Load MIDDLE Byte (Note 5) Data Register on Rising Edge.
1	0	0		1	Load HIGH Byte (Note 5) Data Register on Rising Edge.
1	1	0		1	Load DAC Register with 12-Bit Data in LOW, MIDDLE, and HIGH Byte Data Registers (Note 6).

Load Addressed Data Register With Data at DB0-DB3.

NOTES:

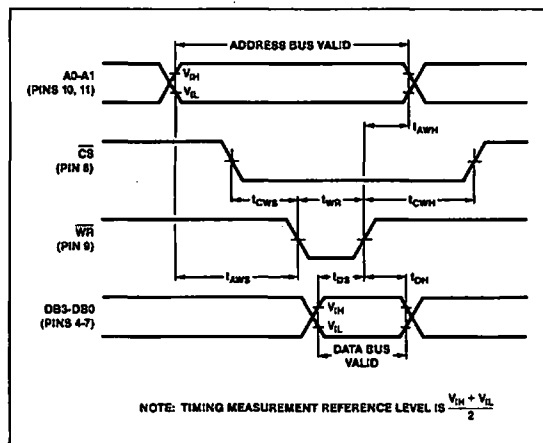
1. 1 indicates logic HIGH
2. 0 indicates logic LOW
3. X indicates don't care
4. $\downarrow$ indicates LOW to HIGH transition
5. Input

5. Input



6. These control signals are level triggered.

FIGURE 7: PM-7542 Timing Diagram



UNIPOLAR OPERATION (2-QUADRANT)

The circuits shown in Figures 8 and 9 may be used with an AC or DC reference voltage. The circuits output will range between 0V and approximately $-V_{REF}$ (4095/4096) depending upon the digital input code. The relationship between the digital input and the analog output is shown in Table 2. The limiting parameters for the V_{REF} range are the maximum input voltage range of the op amp or $\pm 25V$, whichever is lowest.

FIGURE 8: Unipolar Operation with High Accuracy Op Amp (2-Quadrant)

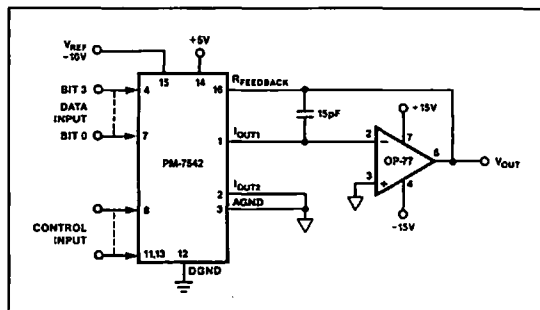
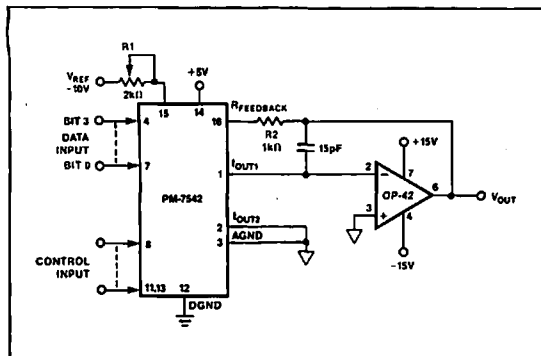


FIGURE 9: Unipolar Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)


Gain error may be trimmed by adjusting R1 as shown in Figure 9. The DAC register must first be loaded with all 1s. R1 may then be adjusted until $V_{OUT} = -V_{REF}$ (4095/4096). In the case of an adjustable V_{REF} , R1 and $R_{FEEDBACK}$ may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

In many applications the PM-7542's negligible zero scale error and very low gain error permit the elimination of the trimming components (R1 and the external $R_{FEEDBACK}$) without adverse effects on circuit performance.

TABLE 2: Unipolar Code Table

DIGITAL INPUT		NOMINAL ANALOG OUTPUT
MSB	LSB	(V_{OUT} as shown in Figures 8 and 9)
1 1 1 1	1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{4095}{4096} \right)$
1 0 0 0	0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{2049}{4096} \right)$
1 0 0 0	0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{2048}{4096} \right) = -\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{2047}{4096} \right)$
0 0 0 0	0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{1}{4096} \right)$
0 0 0 0	0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{0}{4096} \right) = 0$

NOTES:

- Nominal full scale for the circuits of Figures 8 and 9 is given by $FS = V_{REF} \left(\frac{4095}{4096} \right)$.
- Nominal LSB magnitude for the circuits of Figures 8 and 9 is given by $LSB = V_{REF} \left(\frac{1}{4096} \right)$ or $V_{REF} (2^{-n})$.

TABLE 3: Bipolar (Offset Binary) Code Table

DIGITAL INPUT		NOMINAL ANALOG OUTPUT
MSB	LSB	(V_{OUT} as shown in Figure 10)
1 1 1 1	1 1 1 1 1 1 1 1	$+V_{REF} \left(\frac{2047}{2048} \right)$
1 0 0 0	0 0 0 0 0 0 0 1	$+V_{REF} \left(\frac{1}{2048} \right)$
1 0 0 0	0 0 0 0 0 0 0 0	0
1 1 1 1	1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{1}{2048} \right)$
0 0 0 0	0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{2047}{2048} \right)$
0 0 0 0	0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{2048}{2048} \right)$

NOTES:

- Nominal full scale for the circuit of Figure 10 is given by $FS = V_{REF} \left(\frac{2047}{2048} \right)$.
- Nominal LSB magnitude for the circuit of Figure 10 is given by $LSB = V_{REF} \left(\frac{1}{2048} \right)$.

BIPOLAR OPERATION (4-QUADRANT)

Figure 10 details a suggested circuit for bipolar, or offset binary operation. Table 3 shows the digital input to analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

Resistors R3, R4, and R5 must be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R3 and R4 causes offset and full scale errors while an R5 to R4 and R3 mismatch will result in full-scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R1 until $V_{OUT} = 0V$. R1 and R2 may be omitted, adjusting the ratio of R3 to R4 to yield $V_{OUT} = 0V$. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and either adjusting the amplitude of V_{REF} or the value of R5 until the desired V_{OUT} is achieved.

ANALOG/DIGITAL DIVISION

The transfer function for the PM-7542 connected in the multiplying mode as shown in Figures 8 and 9 is:

$$V_O = -V_{IN} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}} \right)$$

where A_X assumes a value of 1 for an "ON" bit and 0 for an "OFF" bit.

FIGURE 10: Bipolar Operation (4-Quadrant, Offset Binary)

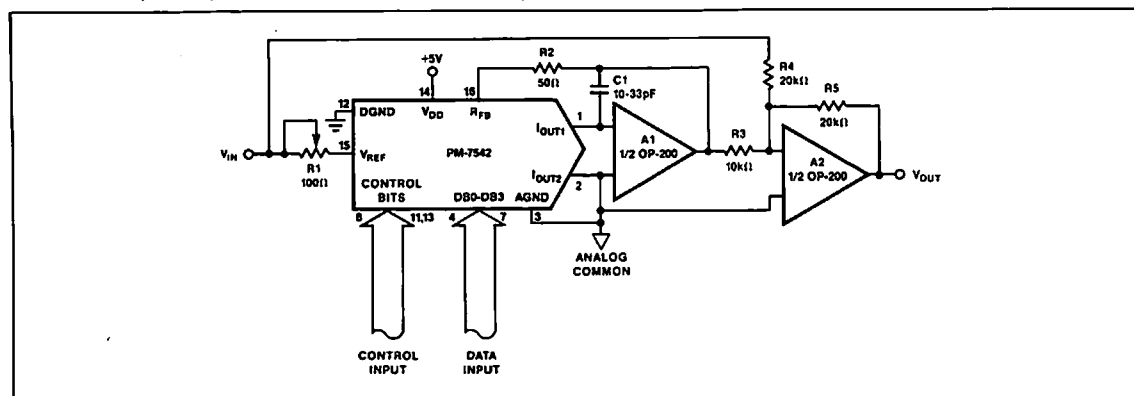
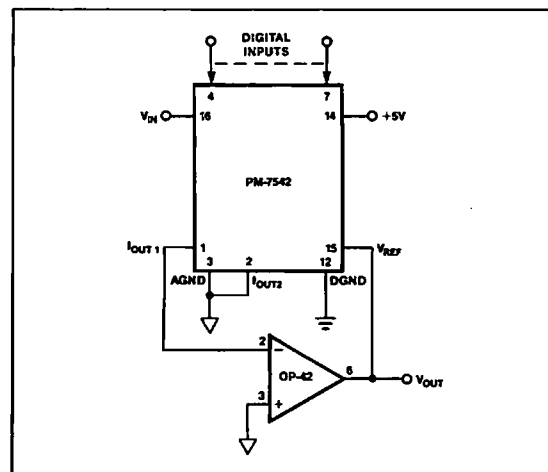


FIGURE 11: Analog/Digital Divider



The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 11. It is now:

$$V_O = \frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}}}$$

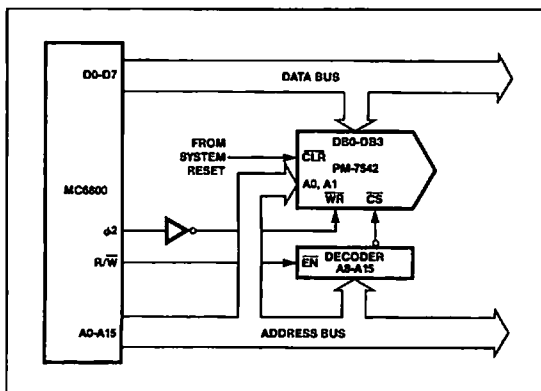
The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (± 1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

INTERFACING TO THE MC6800

A typical interface configuration is shown in Figure 12. Data loading and transfer is performed by executing memory WRITE operations to the four operational addresses specified by A1 and A0.

Addresses ABBB, ABBB+1, and ABBB+2 are assigned to load data into the low, middle, and high byte registers, respectively. Data transfer from input to DAC registers is assigned to address ABBB+3. Eight bits of the full 12-bit data word are stored in memory location XXY. The most significant data bits occupy the lower four bits of memory location XXY+1.

FIGURE 12: Interfacing the PM-7542 to the MC6800





DATA OPERATIONS SUBROUTINE

	JSR	WWZZ	Jump to Data Op Routine at WWZZ
WWZZ	PSH A		Push Acc. A Onto Stack
	TPA		
	PSH A		Push CCR Onto Stack
	LDA A	XXYY	Load Data to Acc.
	STA A	AABB	Load Low Byte
	ROR A		Rotate Right
	ROR A		
	ROR A		
	ROR A		
	STA A	AABB+1	Load Middle Byte
	LDA A	XXYY+1	Load Most Significant Byte to Acc.
	STA A	AABB+2	Load High Byte
	STA A	AABB+3	Transfer Data Word to DAC Register
	PUL A		
	TAP		Pop CCR From Stack
	PUL A		Pop Acc. A From Stack
	RTS		Return to Main Program



Precision Monolithics Inc.

PM-7543

12-BIT SERIAL INPUT
MULTIPLYING CMOS D/A CONVERTER

PRELIMINARY

FEATURES

- Fast, Flexible Microprocessor Interface with Serial Data Input
- Superior Accuracy
 - $\pm 1/2$ LSB INL Max
 - ± 1 LSB Gain Error Max
 - Low 5ppm/ $^{\circ}$ C Max Tempco
- Improved ESD Resistance
- Auto-Insertable DIP Package
- Surface Mount SOL Package
- Superior Direct Replacement for AD7543

APPLICATIONS

- Process Control and Industrial Automation
- Programmable Amplifiers
- Digitally-Controlled Power Supplies
- Digitally-Controlled Attenuators
- Digitally-Controlled Filters
- Instrumentation
- Avionics
- Auto-Calibration Systems

ORDERING INFORMATION†

GAIN ERROR	NON- LINEARITY	TEMPERATURE RANGE		
		MILITARY*	INDUSTRIAL	COMMERCIAL
± 1 LSB	$\pm 1/2$ LSB	PM7543AQ	PM7543EQ	PM7543GP
± 2 LSB	$\pm 1/2$ LSB	PM7543BQ	PM7543FQ	PM7543HP
± 2 LSB	$\pm 1/2$ LSB	PM7543BRC/883††	—	PM7543HS††

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for /883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, and plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

CROSS REFERENCE

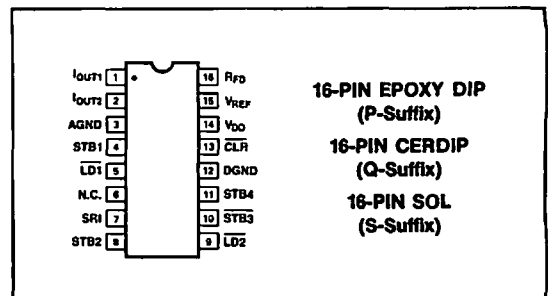
PMI	ADI	TEMPERATURE RANGE
PM7543AQ	AD7543GTD	MIL
PM7543BQ	AD7543TD	
PM7543BQ	AD7543SD	
PM7543EQ	AD7543GBD	IND
PM7543FQ	AD7543BO	
PM7543FQ	AD7543AD	
PM7543GP	AD7543GKN	COM
PM7543HP	AD7543KN	
PM7543HP	AD7543JN	

GENERAL DESCRIPTION

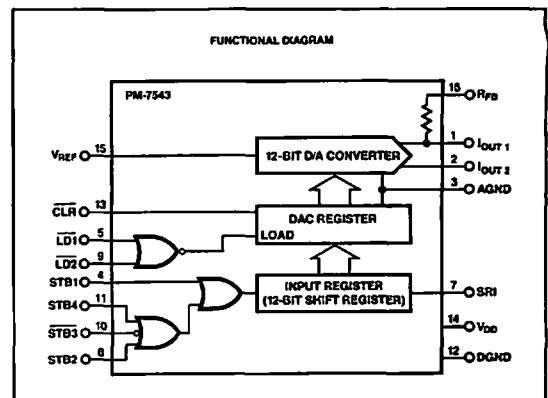
The PM-7543 is a 12-bit resolution, current output, multiplying CMOS DAC with a serial data input. Serial data input allows a reduced pin count and conserves PC board space. Improved analog performance, a fast microprocessor interface, and improved ESD protective circuitry make the PM-7543 a superior pin-compatible second-source to the industry standard 7543. Improved analog parameters such as digital charge injection, power supply rejection, output capacitance, and feedthrough, result in greater ease of application. This improved performance permits the easy upgrading of accuracy and ruggedness in existing designs.

The PM-7543 consists of a serial-in, parallel-out 12-bit wide shift register, a 12-bit wide DAC register, and a 12-bit DAC. Serial data is clocked from the SRI pin into a 12-bit input shift register. The strobe inputs are used to clock in data on (user selected) rising or falling strobe edges. When the shift reg-

PIN CONNECTIONS



FUNCTIONAL BLOCK DIAGRAM



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



ister's data has been updated, the new data word is transferred to the DAC register with use of the LOAD inputs.

Separate LOAD control inputs allow simultaneous output updating of multiple DACs. An asynchronous CLEAR input permits resetting of the DAC register without altering the data resident in the input register.

Improved linearity and gain error performance may permit reduced circuit parts count through the elimination of trimming components. Fast interface timing may reduce timing design considerations while minimizing microprocessor wait states. The PM-7543 is available in standard plastic and cerdip packages that are compatible with auto-insertion equipment. For an even smaller package, consider the DAC-8043, available in an 8-pin mini-DIP.

ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$, unless otherwise noted.)

V_{DD} (to DGND)	+17V
V_{REF} (to DGND)	$\pm 25\text{V}$
V_{RFB} (to DGND)	$\pm 25\text{V}$

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5\text{V}$; $V_{REF} = +10\text{V}$; $V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0\text{V}$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for PM-7543AR/BR; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for PM-7543ER/FR; and $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for PM-7543GP/HP/HS, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	PM-7543 TYP	MAX	UNITS
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Nonlinearity (Note 1)	INL		—	—	$\pm 1/2$	LSB
Differential Nonlinearity (Note 2)	DNL	PM-7543A/E/G PM-7543B/F/H	— —	— —	$\pm 1/2$ ± 1	LSB
Gain Error (Note 3)	G_{FSE}	$T_A = +25^\circ\text{C}$	—	—	1	LSB
		PM-7543A/E/G	—	—	2	
		PM-7543B/F/H	—	—	2	
		$T_A = \text{Full Temp. Range}$	—	—	2	
		PM-7543A/E/G PM-7543B/F/H	— —	— —	3 3	
Gain Tempco ($\Delta\text{Gain}/\Delta\text{Temp}$) (Note 6)	TC_{GFS}		—	—	± 5	ppm/ $^\circ\text{C}$
Power Supply Rejection Ratio ($\Delta\text{Gain}/\Delta\text{Temp}$)	PSRR	$\Delta V_{DD} = \pm 5\%$	—	—	± 0.002	%/%
Output Leakage Current (Notes 4, 5)	I_{LKG}	$T_A = +25^\circ\text{C}$	—	—	± 5	nA
		$T_A = \text{Full Temp. Range}$	—	—	± 100	
		PM-7543A/B PM-7543E/F/G/H	— —	— —	± 25 ± 25	
Zero Scale Error (Notes 8, 13)	I_{ZSE}	$T_A = +25^\circ\text{C}$	—	0.002	—	LSB
		$T_A = \text{Full Temp. Range}$	—	0.05	—	
		PM-7543A/B PM-7543E/F/G/H	— —	0.01 0.01	— —	
Input Resistance (Note 9)	R_{IN}		7	11	15	k Ω

AGND to DGND	-0.3V to V_{DD}
Digital Input Voltage Range	-0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2)	-0.3V to V_{DD}
Power Dissipation (Any Package)	450mW
Derate Above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	
AX/BX Versions	-55°C to $+125^\circ\text{C}$
EX/FX Versions	-40°C to $+85^\circ\text{C}$
GP/HP Versions	0°C to $+70^\circ\text{C}$
Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than AGND potential on any terminal except V_{REF} (Pin 15) and R_{FB} (Pin 16).
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = +10V$; $V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V$; $T_A = -55^{\circ}C$ to $+125^{\circ}C$ for PM-7543AR/BR; $T_A = -40^{\circ}C$ to $+85^{\circ}C$ for PM-7543ER/FR; and $T_A = 0^{\circ}C$ to $+70^{\circ}C$ for PM-7543GP/HP/HS, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	PM-7543 TYP	MAX	UNITS
AC PERFORMANCE						
Output Current Settling Time (Notes 6, 7)	t_s	$T_A = +25^{\circ}C$	—	—	1	μs
Digital to Analog Glitch Energy (Note 6)	Q	$V_{REF} = 0V$ I_{OUT} Load = 100Ω $C_{EXT} = 13pF$ DAC register loaded alternately with all 0s and all 1s	—	—	200	nVs
Total Harmonic Distortion (Note 6)	THD	$V_{REF} = 6V$ RMS @ 1kHz DAC register loaded with all 1s	—	—	-90	dB
Output Noise Voltage Density (Notes 6, 14)	e_n	10Hz to 100kHz measured between R_{FB} and I_{OUT}	—	—	13	$nV/\sqrt{Hz}$
DIGITAL INPUTS						
Digital Input HIGH	V_{IH}		2.4	—	—	V
Digital Input LOW	V_{IL}		—	—	0.8	V
Input Leakage Current (Note 10)	I_{IL}	$V_{IN} = 0V$ to $+5V$	—	—	± 1	μA
Input Capacitance (Note 6)	C_{IN}	$V_{IN} = 0V$	—	—	8	pF
ANALOG OUTPUTS						
Output Capacitance (Note 6)	C_{OUT}	Digital Inputs = V_{IH}	—	—	140	pF
Output Capacitance (Note 6)	C_{OUT}	Digital Inputs = V_{IL}	—	—	70	pF
TIMING CHARACTERISTICS (Note 6)						
Serial Input to Strobe Setup Times	t_{DS1}	STB1 used as the strobe	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	50 100	— —	— —
	t_{DS2}	STB2 used as the strobe	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	20 40	— —	— —
	t_{DS3}	STB3 used as the strobe	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	0 0	— —	— —
	t_{DS4}	STB4 used as the strobe	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	0 0	— —	— —
Serial Input to Strobe Hold Times	t_{DH1}	STB1 used as the strobe	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	30 60	— —	— —
	t_{DH2}	STB2 used as the strobe	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	60 120	— —	— —
	t_{DH3}	STB3 used as the strobe	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	80 160	— —	— —
	t_{DH4}	STB4 used as the strobe	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp. Range}$	80 160	— —	— —



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = +10V$; $V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ for PM-7543AR/BR; $T_A = -40^\circ C$ to $+85^\circ C$ for PM-7543ER/FR; and $T_A = 0^\circ C$ to $+70^\circ C$ for PM-7543GP/HP/HS, unless otherwise noted. (Continued)

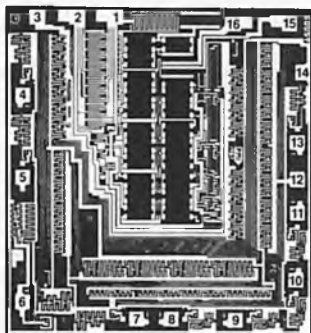
PARAMETER	SYMBOL	CONDITIONS	PM-7543			UNITS
			MIN	TYP	MAX	
SRI Data Pulse Width	t_{SRI}	$T_A = +25^{\circ}\text{C}$	80	—	—	ns
		$T_A = \text{Full Temp. Range}$	160	—	—	
STB1 Pulse Width	t_{STB1}	$T_A = +25^{\circ}\text{C}$	80	—	—	ns
		$T_A = \text{Full Temp. Range}$	160	—	—	
STB2 Pulse Width	t_{STB2}	$T_A = +25^{\circ}\text{C}$	80	—	—	ns
		$T_A = \text{Full Temp. Range}$	160	—	—	
STB3 Pulse Width	t_{STB3}	$T_A = +25^{\circ}\text{C}$	100	—	—	ns
		$T_A = \text{Full Temp. Range}$	200	—	—	
STB4 Pulse Width	t_{STB4}	$T_A = +25^{\circ}\text{C}$	100	—	—	ns
		$T_A = \text{Full Temp. Range}$	200	—	—	
Load Pulse Width	t_{LD1}, t_{LD2}	$T_A = +25^{\circ}\text{C}$	150	—	—	ns
		$T_A = \text{Full Temp. Range}$	300	—	—	
LSB Strobe into Input Register to Load DAC Register Time	t_{ASB}	$T_A = +25^{\circ}\text{C}$	0	—	—	ns
		$T_A = \text{Full Temp. Range}$	0	—	—	
CLR Pulse Width	t_{CLR}	$T_A = +25^{\circ}\text{C}$	200	—	—	ns
		$T_A = \text{Full Temp. Range}$	400	—	—	
POWER SUPPLY						
Supply Voltage	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	All digital inputs = V_{IH} or V_{IL}	—	—	2.5	mA
		All digital inputs = 0V or V_{DD}	—	—	0.1	

NOTES:

- $\pm 1/2$ LSB = $\pm 0.012\%$ of Full Scale.
- All grades are monotonic to 12-bits over temperature.
- Using internal feedback resistor.
- Applies to I_{OUT1} ; all digital inputs = V_{IL} .
- Specification also applies for I_{OUT2} when all digital inputs = V_{IH} .
- Guaranteed by design and not tested.
- I_{OUT1} Load = 100Ω , $C_{EXT} = 13pF$, digital input = 0V to V_{DD} or V_{DD} to 0V.
- $V_{REF} = +10V$, all digital inputs = 0V.
- Absolute temperature coefficient is less than $+50ppm/^\circ C$.
- Digital inputs are CMOS gates; I_{IH} is typically 1nA at $+25^\circ C$.
- $V_{REF} = 0V$, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
- All digital inputs = 0V.
- Calculated from worst case R_{REF} :
 I_{ZSE} (in LSBs) = $(R_{REF} \times I_{LKG} \times 4096)/V_{REF}$.
- Calculations from $e_n = \sqrt{4K TRB}$ where:
 K = Boltzmann constant, $J/^\circ K$ R = resistance Ω
 T = resistor temperature, $^\circ K$ B = bandwidth, Hz



DICE CHARACTERISTICS



- | | |
|---------------|--------------------------|
| 1. I_{OUT1} | 9. $\overline{WR}$ |
| 2. I_{OUT2} | 10. A0 |
| 3. AGND | 11. A1 |
| 4. STB1 | 12. DGND |
| 5. LD1 | 13. CLR |
| 6. N.C. | 14. V_{DD} (Substrate) |
| 7. SRI | 15. V_{REF} |
| 8. STB2 | 16. R_{FB} |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

DIE SIZE 0.116 × 0.109 inch, 12,644 sq. mils
(2.95 × 2.77 mm, 8.17 sq. mm)

WAFER TEST LIMITS at $V_{DD} = +5V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = V_{AGND} = V_{DGND} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

			PM-7543G	
PARAMETER	SYMBOL	CONDITIONS	LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Integral Nonlinearity	INL		±1/2	LSB MAX
Differential Nonlinearity	DNL		±1/2	LSB MAX
Gain Error	G _{FSE}	Using internal feedback resistor	±1	LSB MAX
Power Supply Rejection Ratio	PSRR	ΔV _{DD} = ±5%	±0.002	%/% MAX
Output Leakage Current (I _{OUT1})	I _{LKG}	Digital Inputs = V _{IL}	±5	nA MAX
REFERENCE INPUT				
Input Resistance	R _{REF}		7/15	kΩ MIN/MAX
DIGITAL INPUTS				
Digital Input HIGH	V _{IH}		2.4	V MIN
Digital Input LOW	V _{IL}		0.8	V MAX
Input Leakage Current	I _{IL}	V _{IN} = 0V to V _{DD}	±1	μA MAX
POWER SUPPLY				
Supply Current	I _{DD}	Digital Inputs = V _{IH} or V _{IL} Digital Inputs = 0V or V _{DD}	2.5 0.1	mA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e. zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output. Feedthrough error limits are specified with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from I_{OUT1} to ground.

OUTPUT LEAKAGE CURRENT

Current appearing at I_{OUT1} when all digital inputs are LOW, or at I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The PM-7543 is a 12-bit multiplying D/A converter with a very low temperature coefficient, R-2R resistor ladder network, data input and control logic, and two data registers. The digital circuitry forms an interface in which serial data can be loaded, under microprocessor control, into a 12-bit shift register and then transferred, in parallel, to the 12-bit DAC register.

An asynchronous CLEAR function allows resetting the DAC register to a zero code (0000 0000 0000) without altering data stored in the registers.

A simplified circuit of the PM-7543 DAC is shown in Figure 1. An inverted R-2R ladder network consisting of silicon-chrome, thin-film resistor, and twelve pairs of NMOS current-steering switches steer binarily weighted currents into either I_{OUT1} or I_{OUT2} . Switching current to I_{OUT1} or I_{OUT2} yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R (typically 11k Ω). The V_{REF} input may be driven by any reference voltage or current, AC or DC, that is within the limits stated in the Absolute Maximum Ratings chart.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., a constant 5mV drop will then be maintained across each switch.

To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R-2R ladder's terminating resistor. The "Simplified DAC Circuit", Figure 1, shows the location of the series switches. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

ESD PROTECTION

The PM-7543 data inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes.

These protection diodes are designed to clamp the inputs well below dangerous levels during static discharge conditions.

FIGURE 1: Simplified DAC Circuit

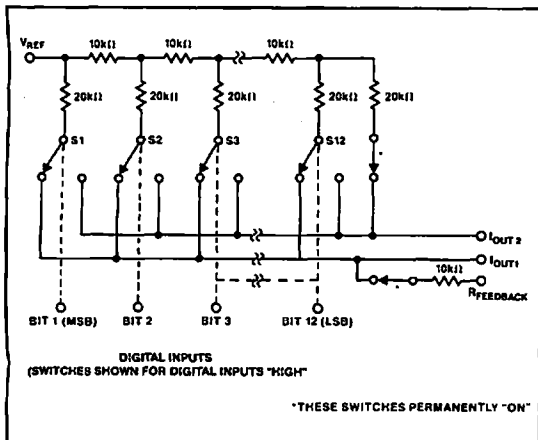
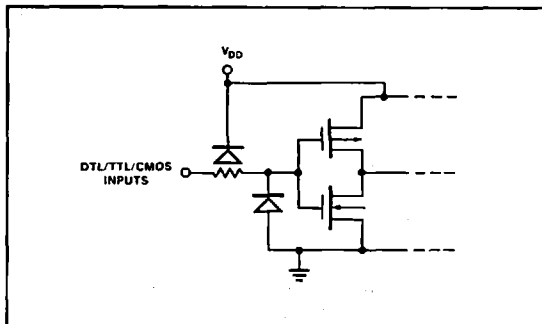


FIGURE 2: Digital Input Protection



EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits for the DAC with all bits LOW and HIGH, respectively. The reference current is switched to I_{OUT2} when all data bits are LOW, and to I_{OUT1} when all bits are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate. The $1/4096$ current source represents the constant 1-bit current drain through the ladder's terminating resistor.

Output capacitance is dependent upon the digital input code. This is because the gate capacitance of MOS transistors increases with applied gate voltage. This output capacitance varies between the low and high values.

FIGURE 3: PM-7543 Equivalent Circuit (All Inputs LOW)

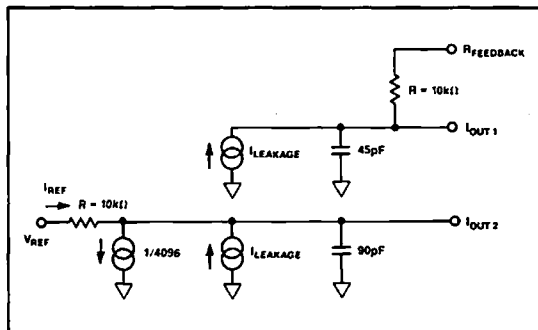
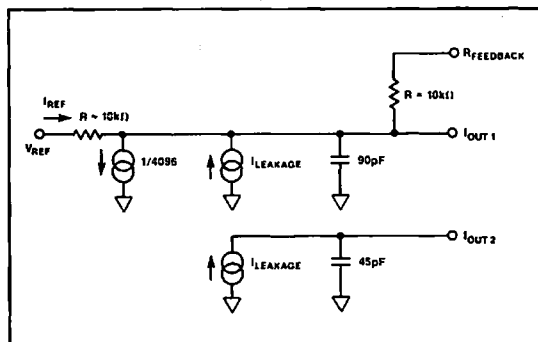


FIGURE 4: PM-7543 Equivalent Circuit (All Digital Inputs HIGH)



DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT1} terminal, may be between $11k\Omega$ (the feedback resistor alone when all digital inputs are LOW) and $7.5k\Omega$ (the feedback resistor in parallel with approximately $30k\Omega$ of the R-2R ladder network resistance when any single bit logic is HIGH). Static accuracy and dynamic performance will be affected by these variations. The gain and phase stability of the output amplifier, board layout, and power

supply decoupling will all affect the dynamic performance of the PM-7543. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 7 and 8).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

APPLICATIONS INFORMATION

APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT1} , I_{OUT2} , and AGND (pins 1, 2, and 3) being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground (see Figures 7 and 8). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than $\pm 200\mu V$ (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a single common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than $\pm 17V$.

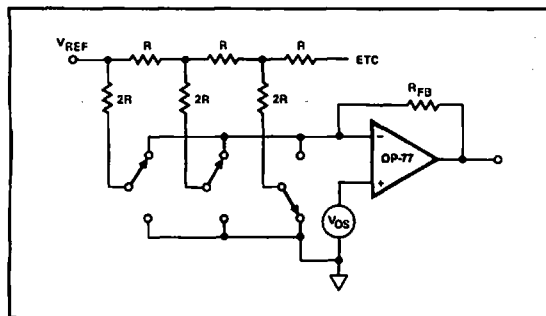
Unused digital inputs must always be grounded or taken to V_{DD} ; this will prevent noise from triggering the high impedance digital inputs resulting in output errors. It is also recommended that the used digital inputs be taken to ground or V_{DD} via a high value ($1M\Omega$) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition voltage. The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e. rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

When using high speed op amps, a small feedback capacitor (typically $15pF$) should be used across the amplifier to minimize overshoot and ringing. For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

FIGURE 5: Simplified Circuit



Static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 5 and the equation:

$$V_{\text{ERROR}} = V_{\text{OS}} \left(1 + \frac{R_{\text{FB}}}{R_{\text{O}}} \right)$$

where R_{O} is a function of the digital code, and:

$R_{\text{O}} = 10\text{k}\Omega$ for more than four bits of logic 1,

$R_{\text{O}} = 30\text{k}\Omega$ for any single bit of logic 1.

Therefore, the offset gain varies as follows:

at code 0011 1111 1111,

$$V_{\text{ERROR1}} = V_{\text{OS}} \left(1 + \frac{10\text{k}\Omega}{10\text{k}\Omega} \right) = 2V_{\text{OS}}$$

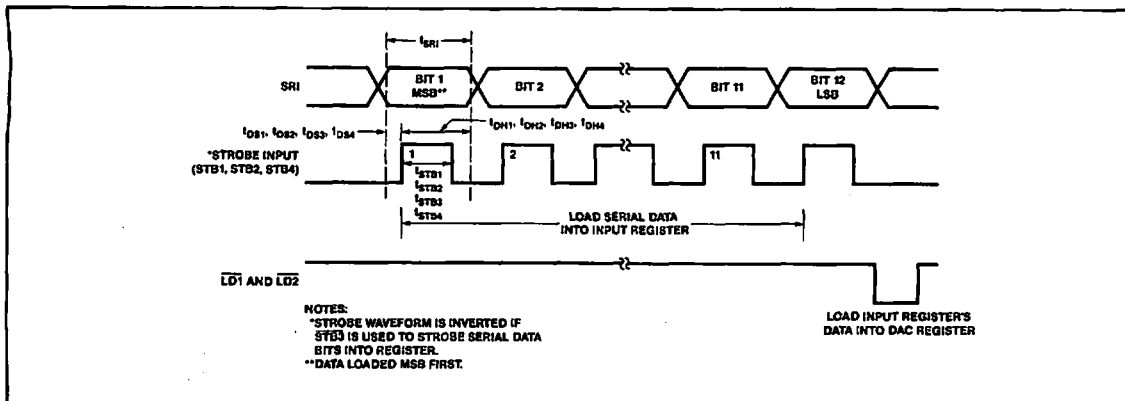
at code 0100 0000 0000,

$$V_{\text{ERROR2}} = V_{\text{OS}} \left(1 + \frac{10\text{k}\Omega}{30\text{k}\Omega} \right) = 4/3V_{\text{OS}}$$

The error difference is $2/3 V_{\text{OS}}$.

Since one LSB has a weight (for $V_{\text{REF}} = +10\text{V}$) of 2.4mV for the PM-7543, it is clearly important that V_{OS} be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS} . Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, OP-27, and OP-42.

FIGURE 6: Timing Diagram



INTERFACE LOGIC OPERATION

The microprocessor interface of the PM-7543 has been designed with multiple STROBE and LOAD inputs to maximize interfacing options. Decoding of control signals may be done on-chip or with the use of external decoding circuitry (see Figure 11).

Serial data can be clocked into the input register with the use of STB1, STB2, or STB4. The strobe inputs are active on rising edge. STB3 may be used with a falling edge to clock in data.

Holding any STROBE input at its selected state (i.e. STB1, 2 or 4 at logic HIGH or STB3 at logic LOW) will act to prevent any further data input.

When a new data word has been entered into the input register, it is transferred to the DAC register by asserting both LOAD inputs.

The CLR input allows the asynchronous reset of the DAC register to 0000 0000 0000. This reset does not affect data held in the input registers. While in unipolar mode, a CLEAR will result in the analog output going to 0V. In bipolar mode, the output will go to $-V_{\text{REF}}$.

INTERFACE INPUT DESCRIPTION

STB1 (Pin 4), STB2 (Pin 8), STB4 (Pin 11)—Input Register Strobe. Inputs Active on Rising Edge.

Selected to load serial data into input register. See Table 1 for details.

STB3 (Pin 10)—Input Register Strobe Input. Active on Falling Edge.

Selected to load serial data into input register. See Table 1 for details.

LD1 (Pin 5), LD2 (Pin 9)—Load DAC Register Inputs. Active Low.

Selected together to load contents of Input Register into DAC register.

CLR (Pin 13)—Clear Input. Active Low. Asynchronous.

When LOW, 12-bit DAC register is forced to a zero code (0000 0000 0000) regardless of other interface inputs.

TABLE 1: PM-7543 Truth Table

PM-7543 Logic Inputs							PM-7543 Operation	Notes
Input Register		Control Inputs		DAC Register		Control Inputs		
STB4	STB3	STB2	STB1	CLR	LD2	LD1		
0	1	0	$\overline{f}$	X	X	X	Serial Data Bit Loaded from SRI into Input Register	2,3
0	1	$\overline{f}$	0	X	X	X		
0	$\overline{f}$	0	0	X	X	X		
$\overline{f}$	1	0	0	X	X	X		
1	X	X	X				No Operation (Input Register)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Reset DAC Register to Zero Code (Code: 0000 0000 0000) (Asynchronous Operation)	1,3
				1	1	X	No Operation (DAC Register)	3
				1	X	1		
				1	0	0	Load DAC Register with the Contents of Input Register	3

NOTES:

1. CLR = 0 Asynchronously resets DAC Register to 0000 0000 0000, but has no effect on Input Register.
2. Serial data is loaded into Input Register MSB first, on edges shown $\overline{f}$ is positive edge, $\overline{f}$ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

UNIPOLAR OPERATION (2-QUADRANT)

The circuit shown in Figures 7 and 8 may be used with an AC or DC reference voltage. The circuit's output will range between 0V and approximately $-V_{REF}$ (4095/4096) depending upon the digital input code. The relationship between the digital input and the analog output is shown in Table 2. The limiting parameters for the V_{REF} range are the maximum input voltage range of the op amp or $\pm 25V$, whichever is lowest.

FIGURE 7: Unipolar Operation with High Accuracy Op Amp (2-Quadrant)

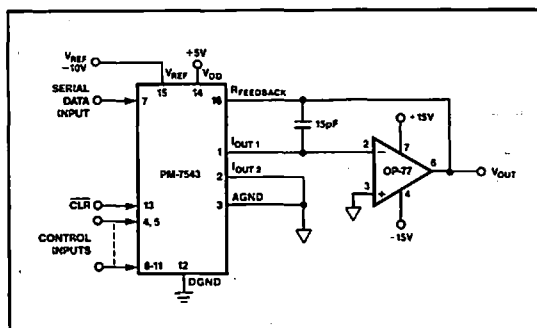
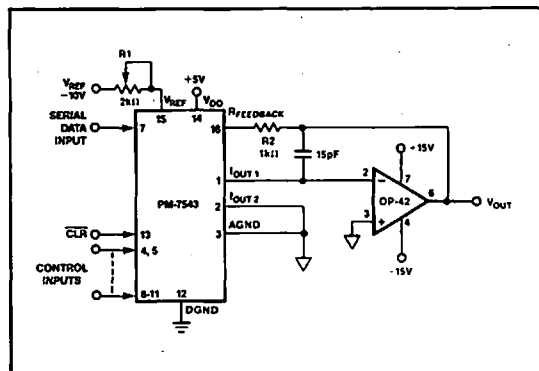


FIGURE 8: Unipolar Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)



Gain error may be trimmed by adjusting R1 as shown in Figure 8. The DAC register must first be loaded with all 1s. R1 may then be adjusted until $V_{OUT} = -V_{REF}$ (4095/4096). In the case of an adjustable V_{REF} , R1 and RFEEDBACK may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

In many applications the PM-7543's negligible zero scale error and very low gain error permit the elimination of the trimming components (R1 and the external RFEEDBACK) without adverse effects on circuit performance.

TABLE 2: Unipolar Code Table

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
MSB	LSB
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{4095}{4096} \right)$
1 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{2049}{4096} \right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{2048}{4096} \right) = -\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{2047}{4096} \right)$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{1}{4096} \right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{0}{4096} \right) = 0$

NOTES:

- Nominal full scale for the circuits of Figures 7 and 8 is given by
 $FS = -V_{REF} \left(\frac{4095}{4096} \right)$.
- Nominal LSB magnitude for the circuits of Figures 7 and 8 is given by
 $LSB = V_{REF} \left(\frac{1}{4096} \right)$ or $V_{REF} (2^{-12})$.

BIPOLAR OPERATION (4-QUADRANT)

Figure 9 details a suggested circuit for bipolar, or offset binary operation. Table 2 shows the digital input to analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

Resistors R3, R4, and R5 must be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R3 and R4 causes offset and full scale errors while an R5 to R4 and R3 mismatch will result in full-scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R1 until $V_{OUT} = 0V$. R1 and R2 may be omitted, adjusting the ratio of R3 to R4 to yield $V_{OUT} = 0V$. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and either adjusting the amplitude of V_{REF} or the value of R5 until the desired V_{OUT} is achieved.

TABLE 3: Bipolar (Offset Binary) Code Table

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
MSB	LSB
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF} \left(\frac{2047}{2048} \right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF} \left(\frac{1}{2048} \right)$
1 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF} \left(\frac{1}{2048} \right)$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF} \left(\frac{2047}{2048} \right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF} \left(\frac{2048}{2048} \right)$

NOTES:

- Nominal full scale for the circuit of Figure 9 is given by
 $FS = V_{REF} \left(\frac{2047}{2048} \right)$.
- Nominal LSB magnitude for the circuit of Figure 9 is given by
 $LSB = V_{REF} \left(\frac{1}{2048} \right)$.

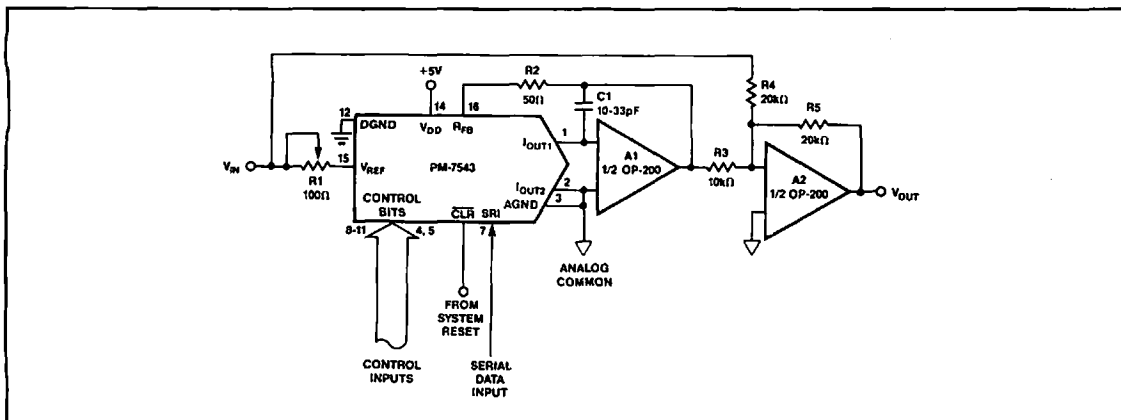
ANALOG/DIGITAL DIVISION

The transfer function for the PM-7543 connected in the multiplying mode as shown in Figures 7 and 8 is:

$$V_O = -V_{IN} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}} \right)$$

where A_X assume a value of 1 for an "ON" bit and 0 for an "OFF" bit.

FIGURE 9: Bipolar Operation (4-Quadrant, Offset Binary)



The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 10. It is now:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}}} \right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (± 1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

INTERFACING TO THE MC6800

As shown in Figure 11 and listed in Table 4, the PM-7543 may be interfaced to the 6800 by successively executing memory WRITE instructions while manipulating the data between WRITES, so that each WRITE presents the next bit.

In this example the most significant bits are found in memory locations 0000 and 0001. The four MSBs are found in the lower half of 0000, the eight LSBs in 0001. The data is taken from the D7 line.

The serial data loading is triggered by STB4 which is asserted by a decoded memory WRITE to memory location 2000, $R/\overline{W}$, and $\phi 2$. A WRITE to address 4000 transfers data from input register to DAC register.

FIGURE 10: Analog/Digital Divider

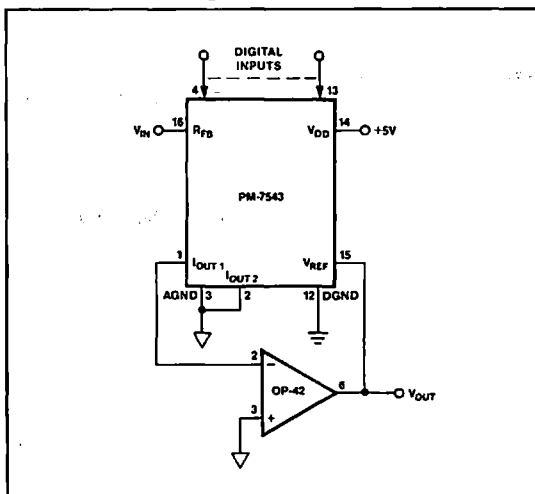
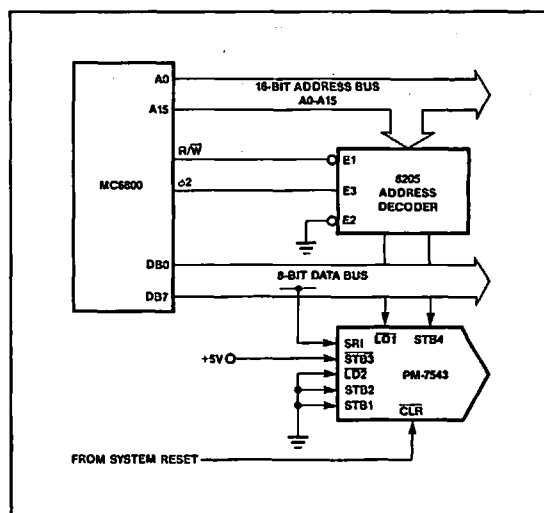


FIGURE 11: PM-7543-MC6800 Interface

**TABLE 4: Example Program for PM-7543/MC6800 Interface**

LABEL	MNEMONIC	OPERAND	COMMENT
	LDA	B, 04	
	LDA	A, 0000	Load 4 Most Significant Bits
LOOP	ROL	A	Reposition the Data in ACC A
	DEC	B	
	BNE	LOOP	
	LDA	B, 04	
	BSR	SHIFT	Output Data
	LDA	B, 08	
	LDA	A, 0001	Load 8 Least Significant Bits
	BSR	SHIFT	Output Data
	STA	A, 4000	Load DAC Register From Input Register
	RTS		Return to Main Program
Shift	STA	A, 2000	Strobe Data into PM-7543
	ROL	A	
	DEC	B	
	BNE	SHIFT	
	RTS		



PM-7545/PM-7645

12-BIT BUFFERED MULTIPLYING CMOS D/A CONVERTERS

Precision Monolithics Inc.

FEATURES

- Preadjusted Full Scale ± 1 LSB Maximum Gain Error
- Low Gain Temperature Coefficient 2ppm/ $^{\circ}$ C
- Small 20-Pin 0.3" Wide DIP
- PM-7545 TTL Compatible for $V_{DD} = 5V$
- PM-7645 TTL and 5V CMOS Compatible for $V_{DD} = 15V$
- High ESD Resistance

ORDERING INFORMATION†

PACKAGE: 20-PIN

MAXIMUM GAIN ERROR $T_A = +25^{\circ}\text{C}$	MILITARY* TEMPERATURE -55 $^{\circ}$ C to +125 $^{\circ}$ C	INDUSTRIAL TEMPERATURE -25 $^{\circ}$ C to +85 $^{\circ}$ C	COMMERCIAL TEMPERATURE 0 $^{\circ}$ C to +70 $^{\circ}$ C
± 1 LSB	PM7545AR	PM7545ER	PM7545GP
± 3 LSB	PM7545BR	PM7545FR	PM7545HP
± 3 LSB	—	—	PM7545HPC††
± 1 LSB	PM7645AR	PM7645ER	PM7645GP
± 3 LSB	PM7645BR	PM7645FR	PM7645HP

* For devices processed in total compliance to MIL-STD-883, add /B83 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

CROSS REFERENCE

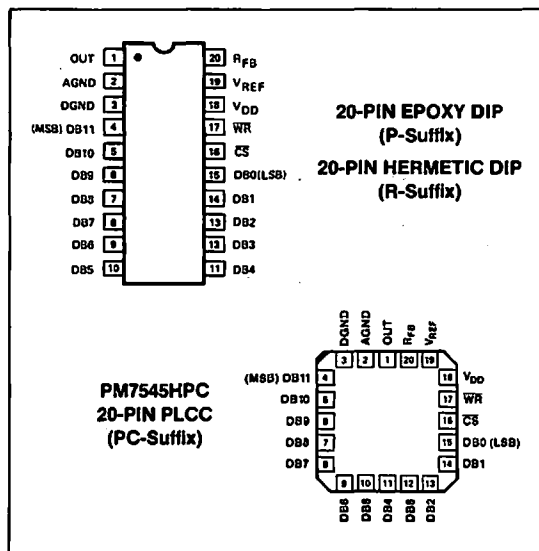
PMI	ADI	TEMPERATURE RANGE
PM7545AR PM7545BR PM7545FR PM7545HP	AD7545GUD AD7545UD AD7545TD AD7545SD	MILITARY
PM7545ER PM7545FR PM7545FR PM7545FR	AD7545GCQ AD7545CCQ AD7545BQ AD7545AQ	INDUSTRIAL
PM7545GP PM7545HP PM7545HP PM7545HP	AD7545GLN AD7545LN AD7545KN AD7545JN	COMMERCIAL

GENERAL DESCRIPTION

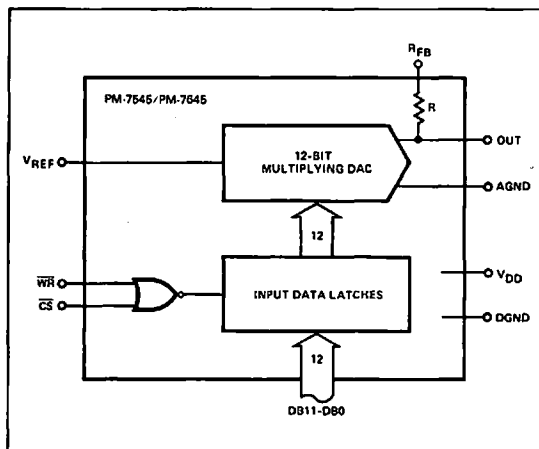
The PM-7545/PM-7645 are 12-bit CMOS multiplying DACs with internal data latches. Digital data is input in a 12-bit wide data format, while $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control inputs are active low. During this time the latches are transparent allowing digital inputs direct connection to the DAC. When $\overline{\text{WR}}$ is returned to logic high, the current data word in the latch is saved.

The PM-7545 operates from 5 to 15 volt power supplies, offering TTL logic compatibility at V_{DD} of 5V and CMOS logic compatibility at V_{DD} of 15V. The PM-7645 is specified for operation at V_{DD} of 15V, offering TTL logic input compatibility.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



DIGITAL-TO-ANALOG CONVERTERS

11

**ABSOLUTE MAXIMUM RATINGS**(T_A = 25°C unless otherwise noted.)

V _{DD} to DGND	−0.3V, +17V
Digital Input Voltage to DGND	−0.3V, V _{DD}
AGND to DGND	−0.3V, V _{DD}
V _{RFB} , V _{REF} to DGND	±25V
V _{PI1} to DGND	−0.3V, V _{DD}
Power Dissipation (Any Package) to +75°C	450mW
Derates Above +75°C by	6mW/°C
Operating Temperature Range	
Military (AR, BR) Grades	−55°C to +125°C
Industrial (ER, FR) Grades	−25°C to +85°C
Commercial (GP, HP, HPC) Grades	0°C to +70°C
Die Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

CAUTION:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
3. The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper anti-static handling procedures.
4. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V; T_A = −55°C to +125°C apply for PM-7545AR/BR, T_A = −25°C to +85°C apply for PM-7545ER/FR, T_A = 0°C to +70°C apply for PM-7545GP/HP/HPC, unless otherwise noted. 15V operating characteristics are shown on the following pages.

PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G			PM-7545B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Relative Accuracy	INL	T _A = Full Temp. Range	—	—	±1/2	—	—	±1/2	LSB
Differential Nonlinearity	DNL	T _A = Full Temp. Range (Note 1)	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G _{FSE}	T _A = +25°C	—	—	±1	—	—	±3	LSB
		T _A = Full Temp. Range	—	—	±2	—	—	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG _{FS}	(Note 4)	—	±2	±5	—	±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV _{DD}	PSS	T _A = +25°C	—	—	0.002	—	—	0.002	%/%
		T _A = Full Temp. Range (ΔV _{DD} = ±5%)	—	—	0.004	—	—	0.004	
Output Leakage Current at OUT	I _{LKG}	T _A = +25°C, WR = CS = 0V, All Digital Inputs = 0V	—	—	10	—	—	10	nA
		T _A = Full Temp. Range	—	—	200	—	—	200	
		A/B Versions	—	—	50	—	—	50	
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 5, 6, 7)	t _{PD}	T _A = +25°C	—	—	300	—	—	300	ns
		(OUT Load = 100f, C _{EXT} = 13pF)	—	—	—	—	—	—	
Current Settling Time	t _s	T _A = Full Temp. Range (To 1/2 LSB) (Note 4) I _{OUT} Load = 100Ω	—	—	1	—	—	1	μs
Digital Charge Injection	Q	T _A = +25°C	—	—	300	—	—	300	nC
		T _A = Full Temp. Range V _{REF} = AGND (Note 4)	—	—	400	—	—	400	
AC Feedthrough at I _{OUT}	FT	T _A = Full Temp. Range V _{REF} = ±10V, f = 10kHz All Digital Inputs = 0V	—	5	—	—	5	—	mV _{p-p}



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{REF} = +10V$, $V_{OUT} = 0V$, $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7545AR/BR, $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7545ER/FR, $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7545GP/HP/HPC, unless otherwise noted. 15V operating characteristics are shown on the following pages. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G			PM-7545B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R _{REF}	T _A = Full Temp. Range Input Resistance	7	11	15	7	11	15	kΩ
ANALOG OUTPUTS									
Output Capacitance (Note 4)	C _{OUT}	T _A = Full Temp. Range DB0-DB11 = 0V, WR = CS = 0V	—	—	70	—	—	70	pF
C _{OUT}		DB0-DB11 = V _{DD} , WR = CS = 0V	—	—	150	—	—	150	
DIGITAL INPUTS									
Input High Voltage	V _{INH}	T _A = Full Temp. Range	2.4	—	—	2.4	—	—	V
Input Low Voltage	V _{INL}		—	—	0.8	—	—	0.8	
Input Current	I _{IN}	T _A = +25°C	—	—	1	—	—	1	μA
		T _A = Full Temp. Range	—	—	10	—	—	10	
Input Capacitance DB0-DB11, WR, CS	C _{IN}	T _A = Full Temp. Range V _{IN} = 0 (Note 4)	—	—	8	—	—	8	pF
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)		See Timing Diagram							
Chip Select to Write Setup Time	t _{CS}	T _A = +25°C	280	200	—	280	200	—	ns
		T _A = Full Temp. Range	380	270	—	380	270	—	
Chip Select to Write Hold Time	t _{CH}	T _A = Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t _{WR}	T _A = +25°C	250	175	—	250	175	—	ns
		T _A = Full Temp. Range	380	270	—	380	270	—	
Data Setup Time	t _{DS}	T _A = +25°C	140	100	—	140	100	—	ns
		T _A = Full Temp. Range	210	150	—	210	150	—	
Data Hold Time	t _{DH}	T _A = Full Temp. Range	10	—	—	10	—	—	ns
POWER SUPPLY									
Supply Current	I _{DD}	T _A = Full Temp. Range (All Digital Inputs V _{INL} or V _{INH})	—	—	2	—	—	2	mA
		T _A = +25°C	—	2	100	—	2	100	
		I _{DD}	T _A = Full Temp. Range (All Digital Inputs 0V or V _{DD})	—	5	100	—	5	100

NOTES:

- 12-bit monotonic over full temperature range.
- Includes the effects of 5ppm max. gain T.C.
- Using Internal R_{FB} . DAC register loaded with 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
- GUARANTEED and NOT TESTED.
- From digital input change to 90% of final analog output.
- All digital inputs = 0V to V_{DD} ; or V_{DD} to 0V.
- Logic inputs are MOS gates, typical input current (at $+25^\circ C$) is less than 1nA.
- Sample tested at $+25^\circ C$ to ensure compliance.
- Chip select $\overline{CS}$ must be coincident or present before and/or after write $\overline{WR}$; that is, $t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$.



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $V_{OUT} = 0V$, $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7545/PM-7645AR/BR, $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7545/PM-7645ER/FR, $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7545/PM-7645GP/HP and PM-7545HPC, unless otherwise noted.

			PM-7545A/E/G PM-7645A/E/G			PM-7545B/F/H PM-7645B/F/H			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Relative Accuracy	INL	T _A = Full Temp. Range	—	—	±1/2	—	—	±1/2	LSB
Differential Nonlinearity	DNL	T _A = Full Temp. Range (Note 1)	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G _{FSE}	T _A = +25°C	—	—	±1	—	—	±3	LSB
		T _A = Full Temp. Range	—	—	±2	—	—	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG _{FS}	(Note 4)	—	±2	±5	—	±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV _{DD}	PSS	T _A = +25°C	—	—	0.002	—	—	0.002	%/%
		T _A = Full Temp. Range (ΔV _{DD} = ±5%)	—	—	0.004	—	—	0.004	
Output Leakage Current at OUT	I _{LKG}	T _A = +25°C, $\overline{WR} = \overline{CS} = 0V$, All Digital Inputs = 0V	—	—	10	—	—	10	nA
		T _A = Full Temp. Range	—	—	200	—	—	200	
		A/B Versions	—	—	200	—	—	200	
		E/F/G/H Versions	—	—	50	—	—	50	
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 5, 6, 7)	t _{pD}	T _A = +25°C (OUT Load = 100f, C _{EXT} = 13pF)	—	—	250	—	—	250	ns
Current Settling Time	t _s	T _A = Full Temp. Range (To 1/2 LSB) (Note 4) I _{OUT} Load = 100f	—	—	1	—	—	1	μs
Digital Charge Injection	Q	T _A = +25°C	—	—	250	—	—	250	nVs
		T _A = Full Temp. Range V _{REF} = AGND (Note 4)	—	—	300	—	—	300	
AC Feedthrough at I _{OUT}	FT	T _A = Full Temp. Range V _{REF} = ±10V, f = 10kHz All Digital Inputs = 0V	—	5	—	—	5	—	mV _{p-p}
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R _{REF}	T _A = Full Temp. Range Input Resistance	7	11	15	7	11	15	kΩ
ANALOG OUTPUTS									
Output Capacitance (Note 4) C _{OUT}	C _{OUT}	T _A = Full Temp. Range DB0-DB11 = 0V, $\overline{WR} = \overline{CS} = 0V$	—	—	60	—	—	60	pF
		DB0-DB11 = V _{DD} , $\overline{WR} = \overline{CS} = 0V$	—	—	120	—	—	120	
DIGITAL INPUTS									
Input High Voltage	V _{INH}	T _A = Full Temp. Range, PM-7545	13.5	—	—	13.5	—	—	V
Input Low Voltage	V _{INL}		—	—	1.5	—	—	1.5	
Input High Voltage	V _{INH}	T _A = Full Temp. Range, PM-7645	2.4	—	—	2.4	—	—	V
Input Low Voltage	V _{INL}		—	—	0.8	—	—	0.8	
Input Current	I _{IN}	T _A = +25°C	—	—	1	—	—	1	μA
		T _A = Full Temp. Range	—	—	10	—	—	10	
Input Capacitance DB0—DB11, $\overline{WR}$, $\overline{CS}$	C _{IN}	T _A = Full Temp. Range V _{IN} = 0 (Note 4)	—	—	8	—	—	8	pF



ELECTRICAL CHARACTERISTICS at $V_{DD} = +15V$, $V_{REF} = +10V$, $V_{OUT} = 0V$, $AGND = DGND = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ apply for PM-7545/PM-7645AR/BR, $T_A = -25^\circ C$ to $+85^\circ C$ apply for PM-7545/PM-7645ER/FR, $T_A = 0^\circ C$ to $+70^\circ C$ apply for PM-7545/PM-7645GP/HP and PM-7545HPC, unless otherwise noted. (Continued)

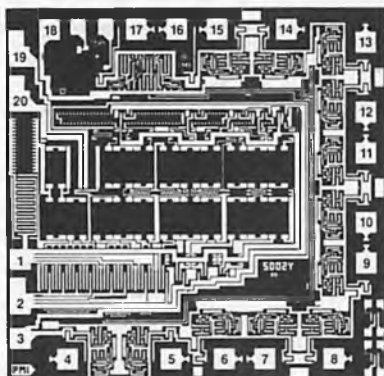
PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G PM-7645A/E/G			PM-7545B/F/H PM-7645B/F/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY									
Supply Current	I_{DD}	T_A = Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DO}	T_A = +25°C T_A = Full Temp. Range (All Digital Inputs 0V or V_{DD})	—	2 5	100 100	—	2 5	100 100	μA
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)		See Timing Diagram	PM-7545 A/E/G			PM-7545 B/F/H			
Chip Select to Write Setup Time	t_{CS}	T_A = +25°C T_A = Full Temp. Range	180 200	120 150	— —	180 200	120 150	— —	ns
Chip Select to Write Hold Time	t_{CH}	T_A = Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C T_A = Full Temp. Range	160 240	100 170	— —	160 240	100 170	— —	ns
Data Setup Time	t_{DS}	T_A = +25°C T_A = Full Temp. Range	90 120	60 80	— —	90 120	60 80	— —	ns
Data Hold Time	t_{DH}	T_A = Full Temp. Range	10	—	—	10	—	—	ns
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)		See Timing Diagram	PM-7645 A/E/G			PM-7645 B/F/H			
Chip Select to Write Setup Time	t_{CS}	T_A = +25°C T_A = Full Temp. Range	150 210	— —	— —	150 210	— —	— —	ns
Chip Select to Write Hold Time	t_{CH}	T_A = Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C T_A = Full Temp. Range	150 210	— —	— —	150 210	— —	— —	ns
Data Setup Time	t_{DS}	T_A = +25°C T_A = Full Temp. Range	225 300	— —	— —	225 300	— —	— —	ns
Data Hold Time	t_{DH}	T_A = Full Temp. Range	10	—	—	10	—	—	ns

NOTES:

- 12-bit monotonic over full temperature range.
- Includes the effects of 5ppm max. gain T.C.
- Using internal R_{FB} , DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
- GUARANTEED and NOT TESTED.
- From digital input change to 90% of final analog output.
- All digital inputs = 0V to V_{DD} , or V_{DD} to 0V.
- Logic inputs are MOS gates, typical input current (at $+25^\circ C$) is less than 1nA.
- Sample tested at $+25^\circ C$ to ensure compliance.
- Chip select $\overline{CS}$ must be coincident or present before and/or after write $\overline{WR}$; that is, $t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$.



DICE CHARACTERISTICS



DIE SIZE 0.102×0.100 inch, 10,200 sq. mils
(2.59×2.54 mm, 6.58 sq. mm)

- | | |
|---------------|---------------|
| 1. OUT | 11. DB4 |
| 2. AGND | 12. DB3 |
| 3. DGND | 13. DB2 |
| 4. DB11 (MSB) | 14. DB1 |
| 5. DB10 | 15. DB0 (LSB) |
| 6. DB9 | 16. CS |
| 7. DB8 | 17. WR |
| 8. DB7 | 18. V_{DD} |
| 9. DB6 | 19. V_{REF} |
| 10. DB5 | 20. R_{FB} |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $T_A = 25^\circ\text{C}$, $V_{DD} = +5$ or $+15\text{V}$, $V_{REF} = +10\text{V}$, $V_{OUT} = 0\text{V}$, AGND = DGND = 0V.

PARAMETER	SYMBOL	CONDITIONS	PM-7545G/PM-7645G	
			LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	$\pm 1/2$	LSB MAX
Differential Nonlinearity	DNL		$\pm 1/2$	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111 1111	± 5	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 0000 0000 0000 Pad 1	± 10	nA MAX
Input Resistance	R_{REF}	Pad 19	7/15	k Ω MIN/k Ω MAX
Digital Input High	V_{INH}	$V_{DD} = 5\text{V}$ PM-7545 only $V_{DD} = 15\text{V}$	2.4 13.5	V MIN
Digital Input Low	V_{INL}	$V_{DD} = 5\text{V}$ PM-7545 only $V_{DD} = 15\text{V}$	0.8 1.5	V MAX
Digital Input High	V_{INH}	$V_{DD} = 15\text{V}$ PM-7645 only	2.4	V MIN
Digital Input Low	V_{INL}	$V_{DD} = 15\text{V}$ PM-7645 only	0.8	V MAX
Input Current	I_{IN}	$V_{IN} = 0\text{V}$ or V_{DD}	± 1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	2 0.1	mA MAX
DC Supply Rejection ($\Delta\text{Gain}/\Delta V_{DD}$)	PSS	$\Delta V_{DD} = \pm 5\%$	0.002	%/% MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

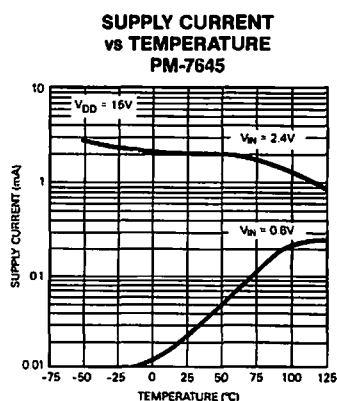
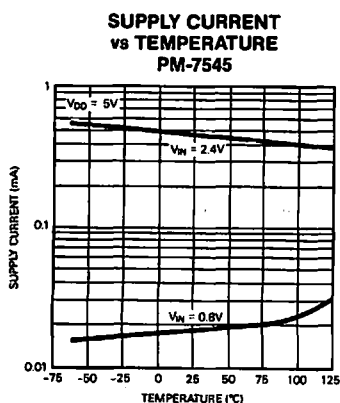
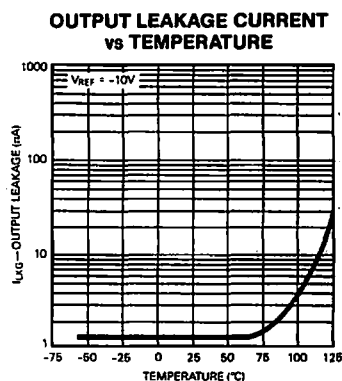
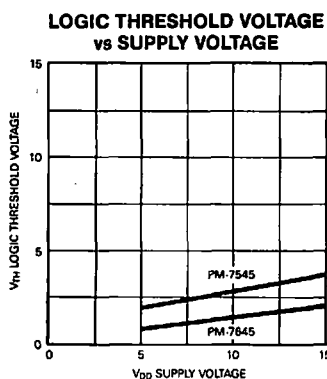
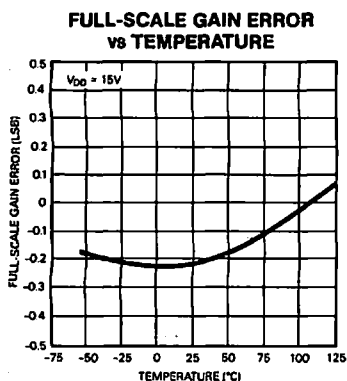


TYPICAL ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $AGND = DGND = 0V$, $V_{REF} = +10V$, $OUT = 0V$; $T_A = 25^\circ C$, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	PM-7545G/PM-7645G	UNITS
			TYPICAL	
Digital Input Capacitance	C_{IN}		7	pF
Output Capacitance	C_{OUT}	DAC Latches Loaded with 0000 0000 0000	50	pF
		DAC Latches Loaded with 1111 1111 1111	110	
Propagation Delay (Notes 2, 3, 4)	t_{pD}	$V_{DD} = 15V$	140	ns
		$V_{DD} = 5V$ PM-7545 only	230	

NOTES:

- These characteristics are for design guidance only and are not subject to test.
- From digital input change to 90% of final analog output.
- OUT load = 100Ω , $C_{EXT} = 13pF$.
- $\overline{CS} = \overline{WR} = 0$, $DB0$ to $DB11 = 0V$ to V_{DD} or V_{DD} to $0V$.

TYPICAL PERFORMANCE CHARACTERISTICS

PARAMETER DEFINITIONS

RELATIVE ACCURACY

Sometimes referred to as endpoint nonlinearity, and is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Relative Accuracy is measured after the zero and full-scale points have been adjusted, and is normally expressed in LSB or as a percentage of full scale.

DIFFERENTIAL NONLINEARITY

This is the difference between the measured change and the ideal change between any two adjacent codes. A differential nonlinearity of ± 1 LSB maximum over the full operating temperature range will ensure that a device is monotonic (the output will increase for an increase in digital code applied).

GAIN ERROR

Gain or full scale error is the amount of output error between the ideal output and the actual output. The ideal output is V_{REF} minus 1 LSB. The gain error is adjustable to zero using external resistance.

OUTPUT CAPACITANCE

The capacitance from OUT to AGND.

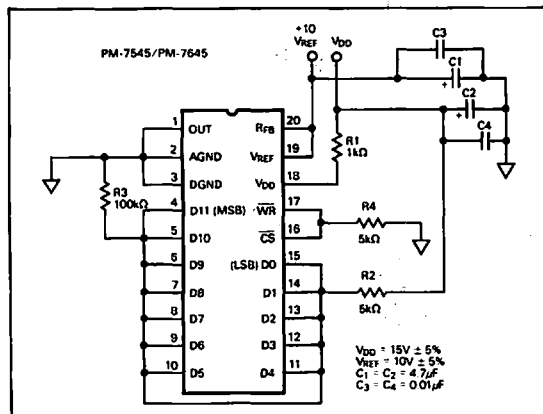
PROPAGATION DELAY

This is measured from the digital input change to the analog output current reaching 90% of its final value.

DIGITAL CHARGE INJECTION

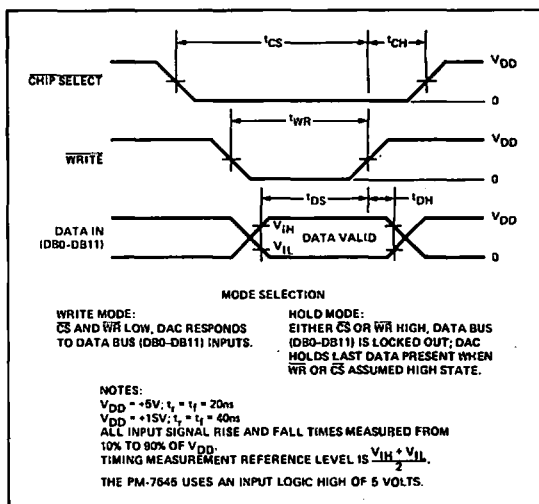
This is a measure of the amount of charge injected to the analog output from the digital inputs, when the digital inputs change states. It is the area of the glitch and is specified in nVsec; it is measured with $V_{REF} = AGND$.

BURN-IN CIRCUIT



LOGIC INFORMATION

WRITE CYCLE TIMING DIAGRAM



D/A CONVERTER SECTION

FIGURE 1: Simplified D/A Circuit of PM-7545

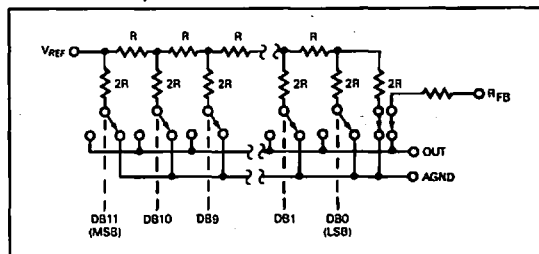


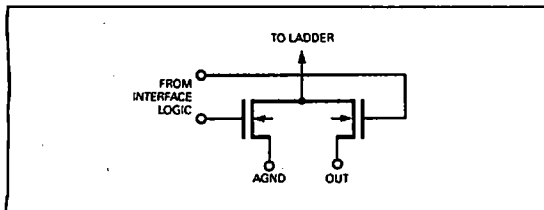
Figure 1 shows a simplified circuit of the D/A Converter section and Figure 2 gives an approximate equivalent switch circuit. R is typically 11kΩ.

The binary-weighted currents are switched between OUT and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT terminal, C_{OUT} , is code dependent and varies from 70pF (all switches to AGND) to 150pF (all switches to OUT). One of the current switches is shown in Figure 2.

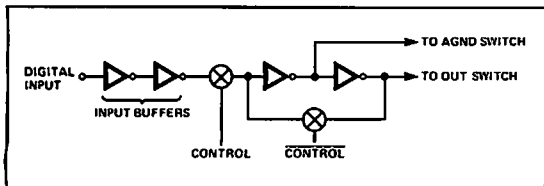
The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the $R/2R$ ladder characteristics resistance and is equal to value "R"). Since the input resistance at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} is recommended to define scale factor.)

The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves performance over temperature and power supply rejection; however when the circuit is not powered up the switch assumes an open state.

FIGURE 2: N-Channel Current Steering Switch


DIGITAL SECTION

Figure 3 shows the digital structure for one bit. The digital signals **CONTROL** and **CONTROL** are generated from **CS** and **WR**.

FIGURE 3: Digital Input Structure


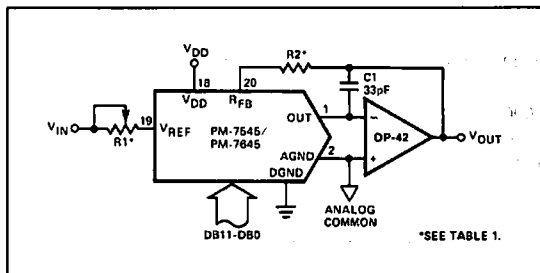
The input buffers are simple CMOS inverters designed such that when the PM-7545 is operated with $V_{DD} = 5V$, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0 volts to 6.0 volts, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and $DGND$) as is practically possible. The PM-7545 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With $V_{DD} = +15V$, the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V. The PM-7645 operates with $V_{DD} = 15V$ only; the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the PM-7545/PM-7645. Resistor R_1 is used to trim for full scale. The following versions (PM-7545AR, PM-7545ER, PM-7545GP) have a guaranteed maximum gain error of ± 1 LSB at $+25^\circ C$ and $V_{DD} = +5V$, and in many applications the gain trim resistors are

not required. Capacitor C_1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuits of Figures 4 and 5 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (the inversion is introduced by the op amp); or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD} . Table 2 shows the code relationship for the circuit of Figure 4.

FIGURE 4: Unipolar Binary Operation

TABLE I: Recommended Trim Resistor Value vs. Grades

TRIM RESISTOR	CR	HP/FR/BR	GP/ER/AR
R1	200Ω	100Ω	20Ω
R2	68Ω	33Ω	6.8Ω

TABLE II: Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT
1111	1111	1111	$-V_{IN} \cdot \left\{ \frac{4095}{4096} \right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{ \frac{2048}{4096} \right\} = -1/2 V_{IN}$
0000	0000	0001	$-V_{IN} \cdot \left\{ \frac{1}{4096} \right\}$
0000	0000	0000	0 Volts

Figure 5 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter U₁ on the MSB line, converts 2's-complement input code to offset binary code. The inverter U₁ may be omitted if the inversion is done in software.

R₃, R₄ and R₅ must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R₃ value to R₄ causes both offset and full scale error. Mismatch of R₅ to R₄ and R₃ causes full scale error.

TABLE III: 2's Complement Code Table for Circuit of Figure 5

DATA INPUT			ANALOG OUTPUT
0111	1111	1111	$+V_{IN} \cdot \left\{ \frac{2047}{2048} \right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{ \frac{1}{2048} \right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{ \frac{1}{2048} \right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{ \frac{2048}{2048} \right\}$

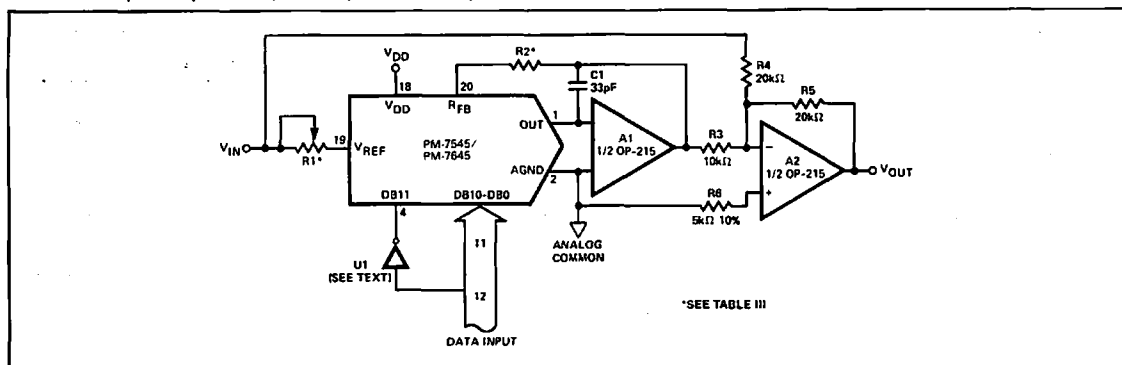
APPLICATION HINTS

Output Offset: CMOS D/A converters exhibit a code-dependent output resistance that causes a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input-offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than 10% of 1 LSB over the temperature range of operation.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the PM-7545/PM-7645. It is recommended that two diodes (1N914 or equivalent) be connected in inverse parallel between AGND and DGND pins in complex systems where AGND and DGND tie on the backplane.

Digital Glitches: When $\overline{WR}$ and $\overline{CS}$ are both low, the latches are transparent and the D/A converter inputs follow the data inputs. Some bus systems do not always have data valid for the whole period during which $\overline{WR}$ is low. This will allow invalid data to briefly appear at the DAC inputs during the write cycle. This can cause unwanted glitches at the DAC output. Retiming the write pulse $\overline{WR}$, so that it only occurs when data is valid, will eliminate the problem.

FIGURE 5: Bipolar Operation (2's Complement Code)

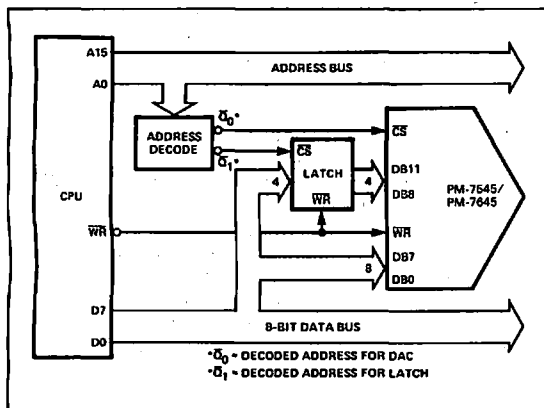


INTERFACING THE PM-7545/PM-7645 TO MICROPROCESSORS

The PM-7545 can be directly interfaced to either an 8 or 16-bit microprocessor via its 12-bit wide data latch using the $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control signals.

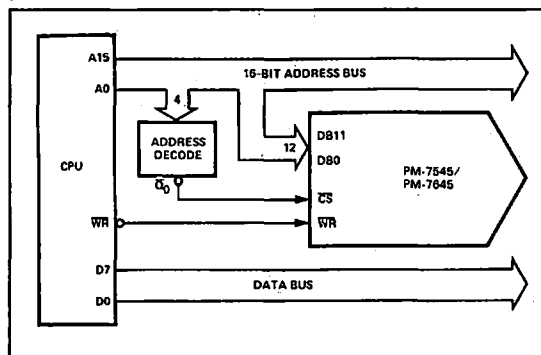
An 8-bit processor interface configuration is shown in Figure 6. It uses two memory addresses, one for the lower 8-bits and one for the upper 4-bits of data into the DAC via the latch.

FIGURE 6: 8-Bit Processor to PM-7545/7645 Interface



Connection to an 8-bit processor with a full 16-bit wide address bus (such as the 6800, 8080, Z80) is shown in Figure 7. The 12 lower address lines are fed directly to the PM-7545; this allows the PM-7545 to use 4k bytes for its address location. The address field of the instruction is organized so that the lower 12-bits contain the DAC data. Data is written into the DAC using a single write instruction.

FIGURE 7: Connecting the PM-7545/7645 to an 8-Bit Microprocessor via the Address Bus



FEATURES

- **8-Bit Bus Compatible 12-Bit DAC**
- **Versatile Microprocessor Interface with Selectable Data Input Format and Data Override**
- **Faster Interface Timing**
- **High Accuracy: Low $\pm 1/2$ LSB INL Error Over Temperature and ± 1 LSB Gain Error**
- **Superior Power Supply Rejection**
from +5V to +15V **0.001%/ % Max**
- **Low Feedthrough Error and Digital Charge Injection**
- **Data Inputs Designed with ESD Protective Circuitry**
- **Narrow (0.3") DIP Packages Suitable for Auto-Insertion**
- **Superior Direct Replacement for AD7548**
- **Full Four Quadrant Multiplication**

APPLICATIONS

- **Process Control**
- **Programmable Amplifiers**
- **Digitally Controlled Power Supplies**
- **Digitally Controlled Attenuators**
- **Digitally Controlled Filters**

ORDERING INFORMATION†

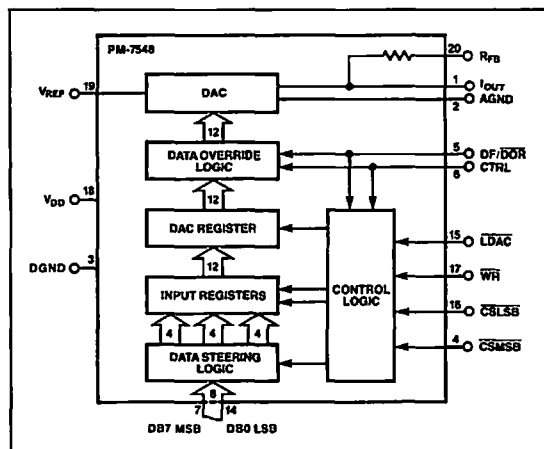
PACKAGE: 20-PIN				
GAIN ERROR	NON- LINEARITY	MILITARY*	INDUSTRIAL	COMMERCIAL
		TEMPERATURE -55°C TO +125°C	TEMPERATURE -25°C TO +85°C	TEMPERATURE 0°C TO +70°C
±1LSB	±1/2LSB	PM7548AR	PM7548ER	PM7548QP
±2LSB	±1/2LSB	PM7548BR	PM7548FR	PM7548HP
±2LSB	±1/2LSB	PM7548BRC/883	—	PM7548HPC†

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

FUNCTIONAL BLOCK DIAGRAM



CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7548AR PM7548BR	AD7548TD AD7548SD	MILITARY
PM7548ER PM7548FR	AD7548BQ AD7548AQ	INDUSTRIAL
PM7548GP PM7548HP	AD7548KN AD7548JN	COMMERCIAL

GENERAL DESCRIPTION

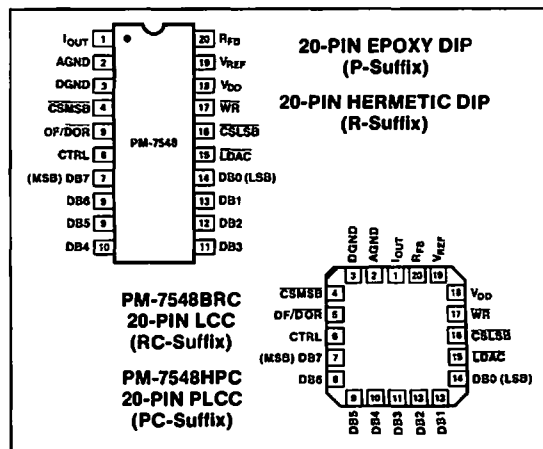
The PM-7548 is a 12-bit resolution, current output, CMOS D/A converter with a microprocessor interface for 8-bit busses. Its improved accuracy and inputs designed with ESD protection circuitry make it a superior pin-compatible replacement to the industry standard 7548. These performance improvements permit the upgrading of existing designs with greater accuracy and ruggedness. Tighter linearity and gain error specifications may permit a reduced circuit parts count through the elimination of trimming components. The PM-7548 is available in standard plastic and Cerdip packages that are compatible with auto-insertion equipment.

The PM-7548's versatile interface allows data to be loaded into an output register in two bytes. The PM-7548 can accept data right or left justified, least or most significant byte first, under microprocessor control. Faster interface timing minimizes microprocessor wait states.

Analog output updating and the loading of new data into the input registers may be coincident or separated in time by use of the $\overline{\text{LDAC}}$ control input. This allows user control of data update and analog output update timing.

Data override control allows full-scale or zero-scale analog outputs without altering the contents of the DAC registers. This permits the user to perform circuit calibration without the need to load calibration data into the DAC registers.

PIN CONNECTIONS



**ABSOLUTE MAXIMUM RATINGS** ($T_A = +25^\circ\text{C}$, unless otherwise noted.)

V_{DD} (to GND)	+17V
V_{REF} (to GND)	$\pm 25\text{V}$
V_{RFB} (to GND)	$\pm 25\text{V}$
Digital Input Voltage Range	-0.3V to V_{DD}
Output Voltage (Pin 1, Pin 2)	-0.3V to V_{DD}
Power Dissipation (Any Package)	450mW
Derate Above $+75^\circ\text{C}$	6mW/ $^\circ\text{C}$
Operating Temperature Range	
AR/BR/BRC Versions	-55°C to $+125^\circ\text{C}$
ER/FR Versions	-25°C to $+85^\circ\text{C}$
GP/HP/HPC Versions	0°C to $+70^\circ\text{C}$

Dice Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C

CAUTION:

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 17) and R_{FB} (Pin 18).
2. The digital control inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper anti-static handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and dice. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5\text{V}$, $+12\text{V}$, or $+15\text{V}$; $V_{REF} = +10\text{V}$; $V_{OUT} = V_{AGND} = V_{DGND} = 0\text{V}$; $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for PM-7548AR/BR/BRC, $T_A = -25^\circ\text{C}$ to $+85^\circ\text{C}$ for PM-7548ER/FR, and $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for PM-7548GP/HP/HPC, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7548			UNITS
			MIN	TYP	MAX	
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Integral Nonlinearity (Note 1)	INL		—	—	1/2	LSB
Differential Nonlinearity (Note 2)	DNL	PM-7548A/E/G PM-7548B/F/H	— —	— —	1/2 1	LSB
Gain Error (Note 3)	G _{FSE}	T _A = +25°C	—	—	—	LSB
		PM-7548A/E/G	—	—	1	
		PM-7548B/F/H	—	—	2	
		T _A = Full Temperature Range	—	—	—	
		PM-7548A/E/G	—	—	2	
		PM-7548B/F/H	—	—	3	
Gain Temperature Coefficient (Note 6)	TCG _{FS}		—	±1	±5	ppm/°C
Power Supply Rejection Ratio	PSRR	T _A = +25°C	—	—	±0.001	%/%
		T _A = Full Temperature Range	—	—	±0.002	
Output Leakage Current (Notes 4, 5)	I _{LKG}	T _A = +25°C	—	±0.5	±5	nA
		T _A = Full Temperature Range	—	—	—	
		PM-7548A/B	—	±12	±100	
		PM-7548E/F/G/H	—	—	±25	
Feedthrough Error (Note 6)	FT	V _{REF} = 20V _{p-p} at f = 10kHz All digital inputs LOW	—	—	5	mV _{p-p}
Zero Scale Error (Notes 12, 13)	I _{ZSE}	T _A = +25°C	—	0.002	—	LSB
		T _A = Full Temperature Range	—	0.07	—	
		PM-7548A/B	—	0.01	—	
		PM-7548E/F/G/H	—	—	—	
Input Resistance (Note 9)	R _{IN}		7	11	15	kΩ
AC PERFORMANCE						
Output Current Settling-Time (Notes 6, 7, 8)	t _s	T _A = +25°C	—	—	1	μs
Digital to Analog Glitch Energy (Notes 6, 11)	Q	V _{REF} = 0V I _{OUT} Load = 100Ω C _{EXT} = 13pF DAC register loaded alternately with all 0s and all 1s	—	—	200	nVs



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V, +12V, \text{ or } +15V$; $V_{REF} = +10V$; $V_{OUT} = V_{AGND} = V_{DGND} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ for PM-7548AR/BR/BRC, $T_A = -25^\circ C$ to $+85^\circ C$ for PM-7548ER/FR, and $T_A = 0^\circ C$ to $+70^\circ C$ for PM-7548GP/HP/HPC, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7548			UNITS
			MIN	TYP	MAX	
Total Harmonic Distortion (Note 6)	THD	$V_{REF} = 6V_{rms}$ @ 1kHz DAC register loaded with all 1s	—	—	-90	dB
Output Noise Voltage Density (Notes 6, 14)	e_n	10Hz to 100kHz, measured between R_{FB} and I_{OUT}	—	—	13	$nV/\sqrt{Hz}$
DIGITAL INPUTS						
Digital Input HIGH	V_{IH}		2.4	—	—	V
Digital Input LOW	V_{IL}		—	—	0.8	V
Input Leakage Current (Note 10)	I_{IL}	$V_{IN} = 0V$ to $+15V$	—	—	± 1	μA
Input Capacitance (Note 6)	C_{IN}	$V_{IN} = 0V$	—	—	6	pF
ANALOG OUTPUTS						
Output Capacitance (Note 6)	C_{OUT}	Digital Inputs = V_{IH}	—	—	140	pF
Output Capacitance (Note 6)	C_{OUT}	Digital Inputs = V_{IL}	—	—	70	pF
TIMING CHARACTERISTICS (Note 6)						
Data Valid Setup Time	t_{DS}	$T_A = 25^\circ C$ $T_A = \text{Full Temperature Range}$	160 210	— —	— —	ns
Data Valid Hold Time	t_{DH}	$T_A = 25^\circ C$ $T_A = \text{Full Temperature Range}$	10 10	— —	— —	ns
CSMSB or CSLSB to WR Setup Time	t_{CWS}	$T_A = 25^\circ C$ $T_A = \text{Full Temperature Range}$	0 0	— —	— —	ns
CSMSB or CSLSB to WR Hold Time	t_{CWH}	$T_A = 25^\circ C$ $T_A = \text{Full Temperature Range}$	0 0	— —	— —	ns
LDAC to WR Setup Time	t_{LWS}	$T_A = 25^\circ C$ $T_A = \text{Full Temperature Range}$	0 0	— —	— —	ns
LDAC to WR Hold Time	t_{LWH}	$T_A = 25^\circ C$ $T_A = \text{Full Temperature Range}$	0 0	— —	— —	ns
Write Pulse Width	t_{WR}	$T_A = 25^\circ C$ $T_A = \text{Full Temperature Range}$	120 120	— —	— —	ns

NOTES:

- $\pm 1/2$ LSB = $\pm 0.012\%$ of Full Scale.
- All grades are monotonic to 12-bits over temperature.
- Using internal feedback resistor.
- Applies to I_{OUT} ; digital inputs = V_{IL} .
- Specification also applies for AGND with all digital inputs = V_{IH} .
- Guaranteed by design and not subject to test.
- I_{OUT} Load = 100 Ω , $C_{EXT} = 13pF$, digital inputs = 0V to V_{DD} or V_{DD} to 0V.
- Extrapolated to 1/2 LSB: t_S = Propagation Delay (t_{PD}) + 9 τ , where τ = measured first time constant of the final RC decay.
- Absolute temperature coefficient is approximately +50ppm/ $^\circ C$.
- Digital inputs are CMOS gates; I_{IH} is typically 1nA at $+25^\circ C$.
- $V_{REF} = 0V$, all digital inputs = 0V to V_{DD} or V_{DD} to 0V.
- $V_{REF} = +10V$, all digital inputs = 0V.
- Calculated from worst case R_{REF} : I_{ZSE} (in LSBs) = $(R_{REF} \times I_{LKG} \times 4096)/V_{REF}$.
- Calculated from $e_n = \sqrt{4KTRB}$
where: K = Boltzmann constant, $J/^\circ K$
T = resistor temperature, $^\circ K$
R = resistance, Ω
B = bandwidth, Hz.



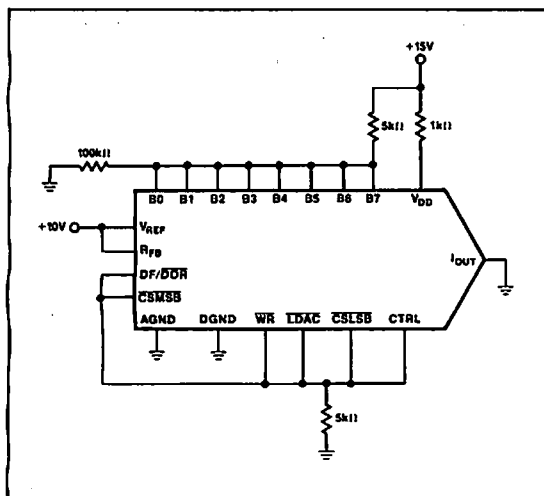
ELECTRICAL CHARACTERISTICS at $V_{DD} = +12V$, or $+15V$; $V_{REF} = +10V$; $V_{OUT} = V_{AGND} = V_{DGND} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ for PM-7548AR/BR/BRC, $T_A = -25^\circ C$ to $+85^\circ C$ for PM-7548ER/FR, and $T_A = 0^\circ C$ to $+70^\circ C$ for PM-7548GP/HP/HPC, unless otherwise noted.

		PM-7548				
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V _{DD} Range	V _{DD}		11.4	—	15.75	V
Supply Current	I _{DD}	All digital inputs = V _{INH} or V _{INL}	—	—	3	mA
		All digital input = 0V or V _{DD}	—	—	1	

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$; $V_{REF} = +10V$; $V_{OUT} = V_{AGND} = V_{DGND} = 0V$; $T_A = -55^\circ C$ to $+125^\circ C$ for PM-7548AR/BR/BRC, $T_A = -25^\circ C$ to $+85^\circ C$ for PM-7548ER/FR, and $T_A = 0^\circ C$ to $+70^\circ C$ for PM-7548GP/HP/HPC, unless otherwise noted.

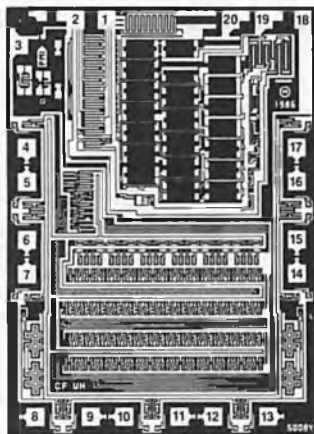
			PM-7548			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V _{DD} Range	V _{DD}		4.75	5	5.25	V
Supply Current	I _{DD}	All digital inputs = V _{INH} or V _{INL}	—	—	2	mA
		All digital input = 0V or V _{DD}	—	120	300	

BURN-IN CIRCUIT





DICE CHARACTERISTICS



DIE SIZE 0.096×0.130 inch, 12,480 sq. mils
(2.46×3.33 mm, 8.20 sq. mm)

- | | |
|--------------|------------------------|
| 1. I_{OUT} | 11. DB3 |
| 2. AGND | 12. DB2 |
| 3. DGND | 13. DB1 |
| 4. CSMSB | 14. DB0 (LSB) |
| 5. DF/DOR | 15. LDAC |
| 6. CTRL | 16. $\overline{CSLSB}$ |
| 7. DB7 (MSB) | 17. WR |
| 8. DB6 | 18. V_{DD} |
| 9. DB5 | 19. V_{REF} |
| 10. DB4 | 20. RFB |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +5V$, $V_{REF} = +10V$, $AGND = DGND = 0V$, $V_{OUT} = AGND = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7548GBC LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		12	Bits MIN
Nonlinearity	INL		$\pm 1/2$	LSB MAX
Differential Nonlinearity	DNL		$\pm 1/2$	LSB MAX
Gain Error (Note 1)	G_{FSE}		± 1	LSB MAX
Power Supply Rejection	PSRR	$\Delta V_{DD} = \pm 5\%$	± 0.001	%/% MAX
Output Leakage Current (I_{OUT})	I_{LKG}	$V_{DD} = +15V$ Digital Inputs = V_{IL}	± 5	nA MAX
REFERENCE INPUT				
Input Resistance	R_{REF}		7/15	k Ω MIN/MAX
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V MIN
Digital Input LOW	V_{IL}		0.8	V MAX
Input Leakage Current	I_{IL}	$V_{DD} = +15V$ $V_{IN} = 0$ to 15V	± 1	μA MAX
POWER SUPPLY				
Supply Current	I_{DD}	$V_{DD} = +15V$ Digital Inputs = V_{IH} or V_{IL}	3	mA MAX
		Digital Inputs = 0V or V_{DD}	1	

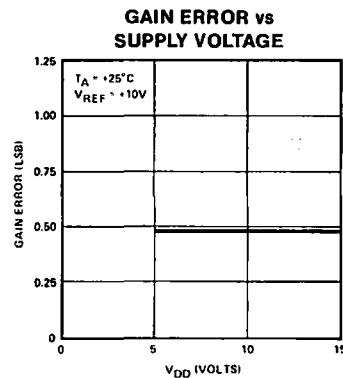
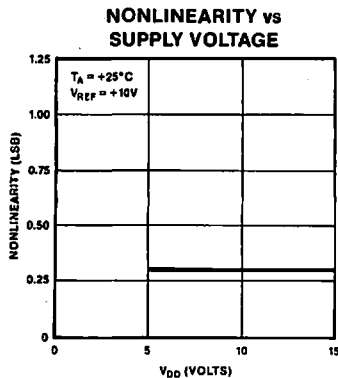
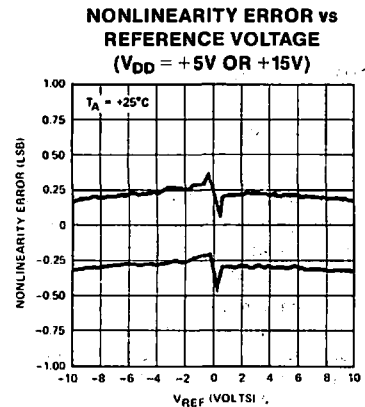
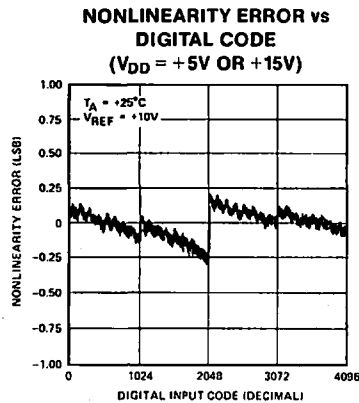
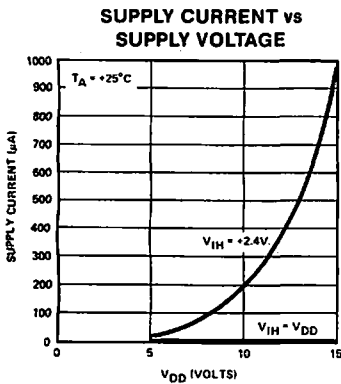
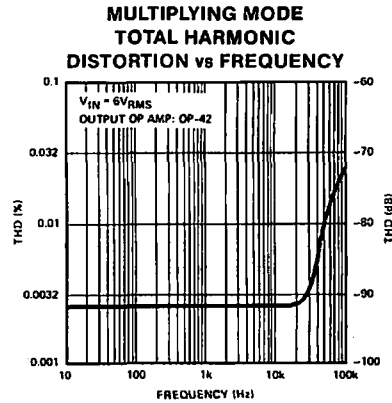
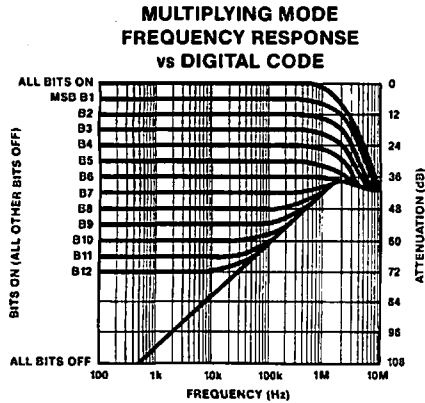
NOTES:

1. Using internal feedback resistor.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.



TYPICAL PERFORMANCE CHARACTERISTICS



SPECIFICATION DEFINITIONS

RESOLUTION

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into, where "n" is equal to the number of bits.

SETTLING TIME

Time required for the analog output of the DAC to settle to within 1/2 LSB of its final value for a given digital input stimulus; i.e. zero to full scale.

GAIN

Ratio of the DAC's external operational amplifier output voltage to the V_{REF} input voltage when all digital inputs are HIGH.

FEEDTHROUGH ERROR

Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE

Capacitance from I_{OUT} terminal with all digital inputs LOW, or on AGND terminal when all inputs are HIGH.

OUTPUT LEAKAGE CURRENT

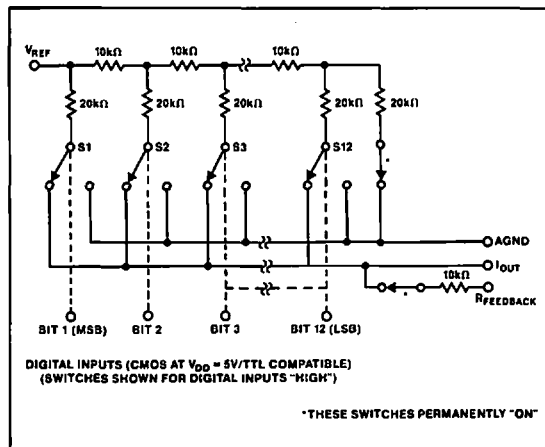
Current appearing at I_{OUT} when all digital inputs are LOW, or at AGND when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The PM-7548 is a 12-bit multiplying D/A converter with a very low temperature coefficient, R-2R resistor ladder network, data-steering and control logic, and two data registers.

The digital circuitry forms a versatile interface between the 12-bit DAC and an 8-bit data bus. Several data formats can be accommodated, single or double buffering is available, and a data override function allows calibration data to be loaded into the DAC without altering data stored in the buffer registers.

FIGURE 1: Simplified DAC Circuit



A simplified circuit of the PM-7548 is shown in Figure 1. An inverted R-2R ladder network consisting of silicon-chrome, thin-film resistors, and twelve pairs of NMOS current-steering switches steer binarily weighted currents into either I_{OUT} or AGND. Switching current to ground or I_{OUT} yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R (typically 11k Ω). The V_{REF} input may be driven by any reference voltage or current, ac or dc, that is within the limits stated in the Absolute Maximum Ratings chart.

The PM-7548 design incorporates a regulator circuit which assures TTL compatibility at any V_{DD} from +5V to +15V across the full military temperature range. This regulator also contributes to the DAC's exceptional PSRR performance, and maintains timing performance independent of supply voltage.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., a constant 5mV drop will then be maintained across each switch.

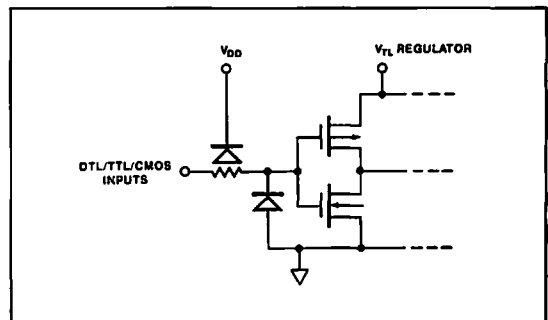
To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R-2R ladder's terminating resistor. The "Simplified DAC Circuit", Figure 1, shows the location of the series switches. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn "ON" these series switches.

ESD PROTECTION

The PM-7548 data inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry.

Figure 2 shows the input protection diodes. High voltage static charges applied to the digital inputs are shunted to the supply and ground rails through forward biased diodes.

FIGURE 2: Digital Input Protection



These protection diodes are designed to clamp the inputs well below dangerous levels during static discharge conditions.

EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show equivalent circuits for the DAC with all bits LOW and HIGH, respectively. The reference current is switched to AGND when all data bits are LOW and to I_{OUT} when all bits are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate. The $1/4096$ current source represents the constant 1-bit current drain through the ladder's terminating resistor.

Output capacitance is dependent upon the digital input code. This is because the gate capacitance of MOS transistors increases with applied gate voltage. This output capacitance varies between the low and high values.

FIGURE 3: PM-7548 Equivalent Circuit (All Inputs LOW)

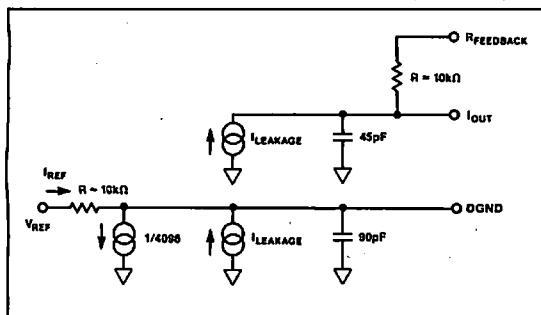
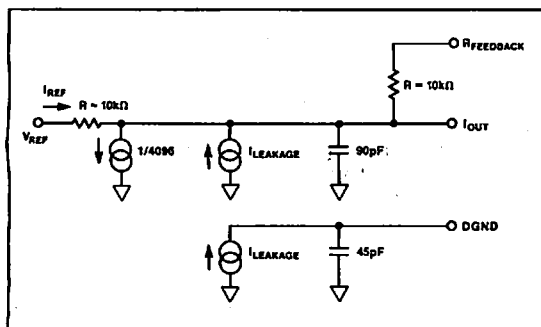


FIGURE 4: PM-7548 Equivalent Circuit (All Digital Inputs HIGH)



INPUT CONTROL INFORMATION

FIGURE 5: PM-7548 Data Input and Control Timing Diagram

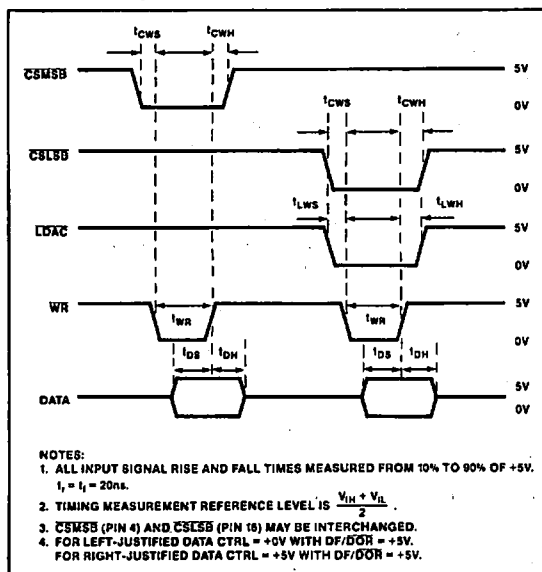
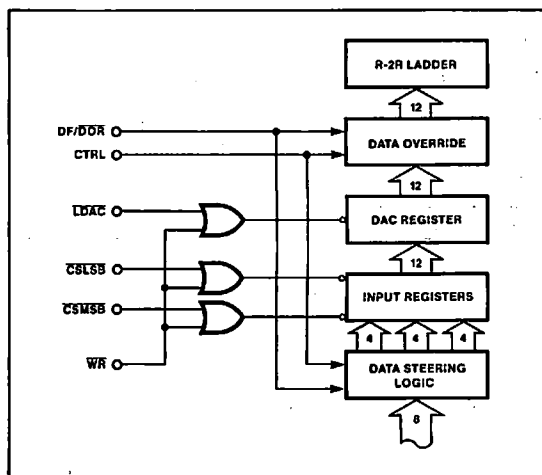


FIGURE 6: Simplified PM-7548 Input Control Structure



**DYNAMIC PERFORMANCE****OUTPUT IMPEDANCE**

The output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT} terminal, may be between $11k\Omega$ (the feedback resistor alone when all digital inputs are low) and $7.5k\Omega$ (the feedback resistor in parallel with approximately $30k\Omega$ of the R-2R ladder network resistance when any single bit logic is high). Static accuracy and dynamic performance will be affected by these variations. The gain and phase stability of the output amplifier, board layout, and power supply decoupling will all affect the dynamic performance of the PM-7548. The use of a compensation capacitor may be required when high-speed operational amplifiers are used. It may be connected across the amplifiers' feedback resistor to provide the necessary phase compensation to critically damp the output.

The considerations when using high-speed amplifiers are:

1. Phase compensation (see Figures 9 and 10).
2. Power supply decoupling at the device socket and use of proper grounding techniques.

INTERFACE INPUT DESCRIPTION

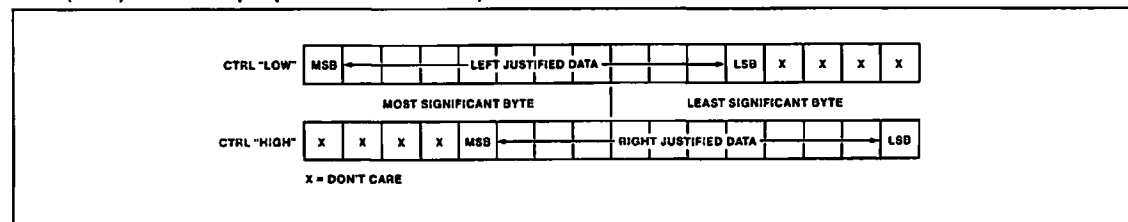
CSMSB (Pin 4) - Chip Select Most Significant Byte. Active Low. Selected either with $\overline{WR}$, to load most significant byte data into the input register, or with $\overline{WR}$ and $\overline{LDAC}$ to load data into both input and DAC registers.

CSLSB (Pin 16) - Chip Select Least Significant Byte. Active Low. Selected either with $\overline{WR}$ to load least significant byte data into the input register, or with $\overline{WR}$ and $\overline{LDAC}$ to load data into both input and DAC registers.

DF/ $\overline{DOR}$ (Pin 5) - Data Format/Data Override. When LOW, DAC is forced to full-scale or zero-scale output as selected by CTRL. Use of Data Override does not affect data held in DAC register. When DF/ $\overline{DOR}$ is HIGH, CTRL selects either right or left data input format. DF/ $\overline{DOR}$ is normally held HIGH.

DF/ $\overline{DOR}$	CTRL	Function
0	0	DAC forced to zero-scale (all zeros)
0	1	DAC forced to full-scale (all ones)
1	0	Left-justified data format selected
1	1	Right-justified data format selected

CTRL (Pin 6) - Control Input (Refer also to DF/ $\overline{DOR}$)



$\overline{LDAC}$ (Pin 15) - Load DAC Input. Active Low. Selected, with other interface inputs, to load DAC register from input register or external data bus.

$\overline{WR}$ (Pin 17) - Write Input. Active Low. Selected, with other interface input, to load data into input register and to transfer data from input register to DAC register.

Selected, with other interface input, to load data into input register and to transfer data from input register to DAC register.

$\overline{WR}$	CSMSB	CSLSB	$\overline{LDAC}$	Function
0	1	0	1	Load LSByte to Input Register
0	1	0	0	Load LSByte to Input and DAC Registers
0	0	1	1	Load MSByte to Input Register
0	0	1	0	Load MSByte to Input and DAC Registers
0	1	1	0	Load Input Register to DAC Register
1	X	X	X	No Data Transfer

DATA LOADING AND TRANSFER**DATA INPUT AND TRANSFER**

Data may be loaded into the input register in either a left- or right-justified format. The data format is selected through the DF/ $\overline{DOR}$ and CTRL inputs (refer to Interface Input Description).

Data transfer, from the input register to the DAC register, can be automatic upon loading of the second data byte into the input register or can occur at a later time through a strobed transfer.

STROBED DATA TRANSFER MODE

Strobed data transfer allows the full 12-bit digital word to be loaded into the input register and transferred to the DAC register at some later time. This transfer mode requires three write cycles: two to load the new digital word, and a third to

FIGURE 7: Strobed Data Transfer Mode

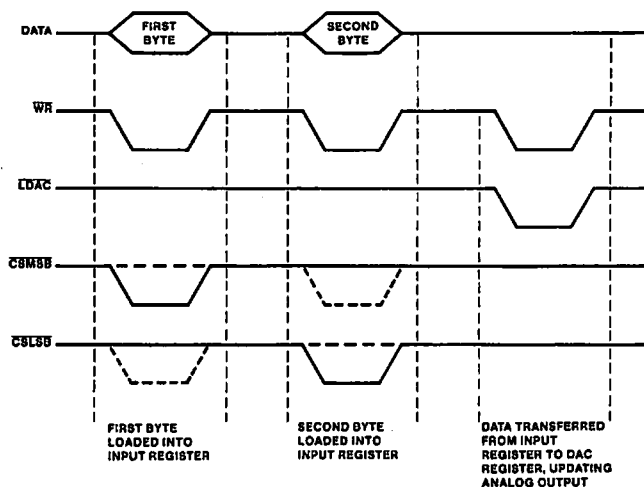
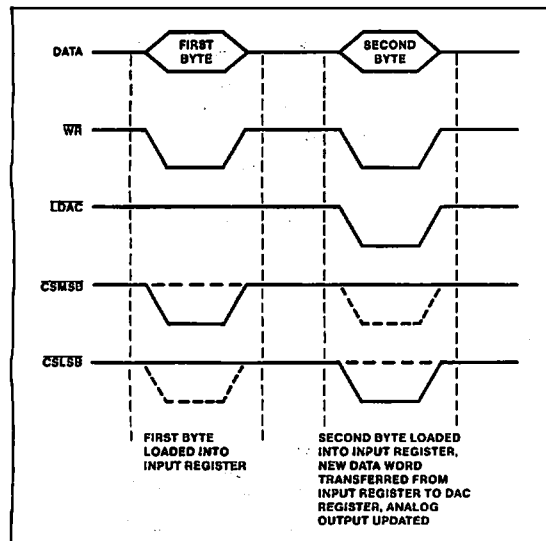


FIGURE 8: Automatic Data Transfer Mode



transfer data to the DAC register. The timing diagram for strobed data transfer is shown in Figure 7.

Strobed data transfer has two primary uses. By separating data loading and transfer operations, the timing of DAC output updating may be more precisely controlled. Simultaneous updating of multiple PM-7548s can also be accomplished by the use of a master strobe signal applied to the LDAC pins of the DACs.

A single data byte can be updated in two write cycles with the strobed transfer mode.

DATA OVERRIDE

System calibration typically requires full-scale and zero-scale DAC outputs (digital words all 1s and 0s respectively). The PM-7548's data override ability allows full-scale and zero-scale outputs without altering the contents of the DAC and input registers, or requiring the controlling microprocessor to load calibration data.

Data override is accessed by setting the DF/ $\overline{DOR}$ pin LOW. The CTRL pin then selects the override code: CTRL LOW yields all 0s, CTRL HIGH yields all 1s.

AUTOMATIC DATA TRANSFER MODE

Data may be transferred automatically from the input register to the DAC register while loading the second (High or Low) byte. This is the simplest and fastest transfer mode, requiring only two write cycles to load and transfer a complete new digital word. This operation can be simplified by connecting LDAC directly to either CSM5B or CSL5B so that the write cycle which loads the second data byte also initiates data word transfer.

The timing diagram for automatic transfer is shown in Figure 8. The first write cycle loads the first data byte into the input register. The second write cycle loads the second data byte and simultaneously transfers the full data word to the DAC register.

Automatic transfer allows updating of a single byte in one write cycle.

APPLICATIONS INFORMATION

APPLICATION TIPS

In most applications, linearity depends upon the potential of I_{OUT} and AGND (pins 1 and 2) being exactly equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground, (see Figures 9 and 10). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than $\pm 200\mu V$ (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than $\pm 17V$.

Unused digital inputs must always be grounded or taken to V_{DD} ; this will prevent noise from triggering the high impedance digital input resulting in output errors. It is also recommended that the used digital inputs be taken to ground

or V_{DD} via a high value ($1M\Omega$) resistor; this will prevent the accumulation of static charge if the PC card is disconnected from the system.

Peak supply current flows as the digital inputs pass through the transition voltage. The supply current decreases as the input voltage approaches the supply rails (V_{DD} or DGND), i.e. rapidly slewing logic signals that settle very near the supply rails will minimize supply current.

OUTPUT AMPLIFIER CONSIDERATIONS

When using high speed op amps, a small feedback capacitor (typically 15pF) should be used across the amplifier to minimize overshoot and ringing. For low speed or static applications, AC specifications of the amplifier are not very critical. In high-speed applications, slew rate, settling time, open-loop gain, and gain/phase margin specifications of the amplifier should be selected for the desired performance. It has already been noted that an offset can be caused by including the usual bias current compensation resistor in the amplifier's noninverting input-terminal. This resistor should not be used. Instead, the amplifier should have a bias current which is low over the temperature range of interest.

FIGURE 9: Unipolar Binary Operation with High Accuracy Op Amp (2-Quadrant)

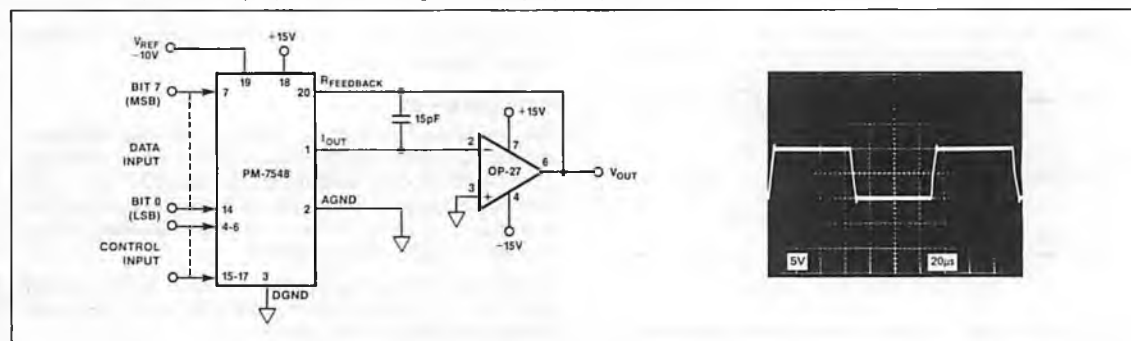
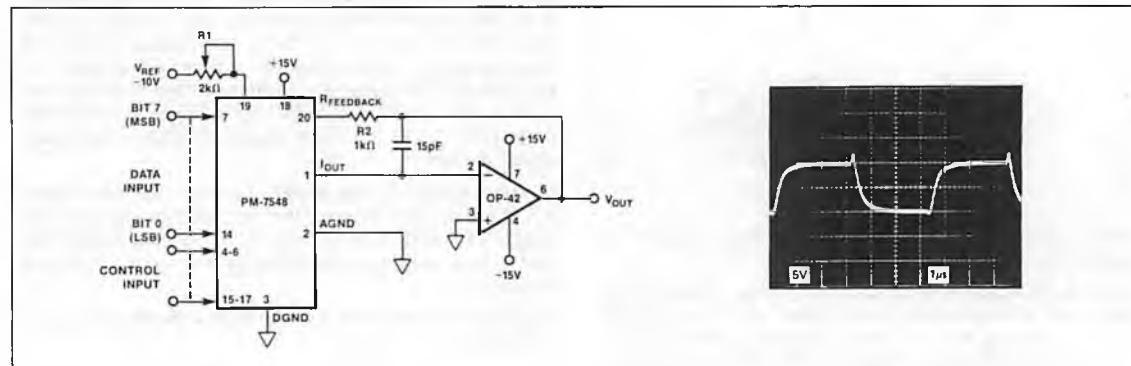


FIGURE 10: Unipolar Binary Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)



Static accuracy is affected by the variation in the DAC's output resistance. This variation is best illustrated by using the circuit of Figure 11 and the equation:

$$V_{\text{ERROR}} = V_{\text{OS}} \left(1 + \frac{R_{\text{FB}}}{R_{\text{O}}} \right)$$

where R_{O} is a function of the digital code, and:

$R_{\text{O}} = 10\text{k}\Omega$ for more than 4-bits of logic 1

$R_{\text{O}} = 30\text{k}\Omega$ for any single bit logic 1

Therefore, the offset gain varies as follows:

At code 0011 1111 1111,

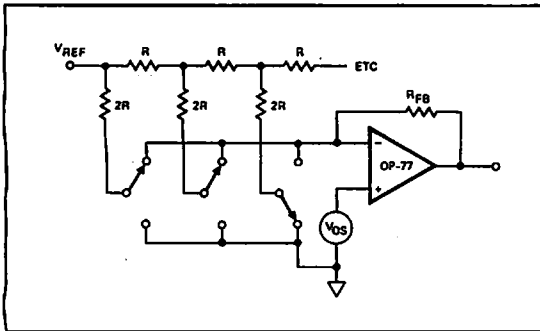
$$V_{\text{ERROR}} = V_{\text{OS}} \left(1 + \frac{10\text{k}\Omega}{10\text{k}\Omega} \right) = 2V_{\text{OS}}$$

At code 0100 0000 0000,

$$V_{\text{ERROR}} = V_{\text{OS}} \left(1 + \frac{10\text{k}\Omega}{30\text{k}\Omega} \right) = 4/3V_{\text{OS}}$$

The error difference is $2/3 V_{\text{OS}}$.

FIGURE 11: Simplified Circuit



Since one LSB has a weight (for $V_{\text{REF}} = +10\text{V}$) of 2.4mV for the PM-7548, it is clearly important that V_{OS} be minimized, either using the amplifier's nulling pins, an external nulling network, or by selection of an amplifier with inherently low V_{OS} . Amplifiers with sufficiently low V_{OS} include PMI's OP-77, OP-07, OP-27, and OP-42.

UNIPOLAR BINARY OPERATION (2-QUADRANT)

The circuit shown in Figures 9 and 10 may be used with an AC or DC reference voltage. The circuit's output will range between 0V and approximately $-V_{\text{REF}} (4095/4096)$ depending upon the digital input code. The relationship between the

digital input code. The relationship between the digital input and the analog output is shown in Table 1. The limiting parameters for the V_{REF} range are the maximum input voltage range for the op amp or $\pm 25\text{V}$, whichever is lowest.

Gain error may be trimmed by adjusting $R1$ as shown in Figure 10. The DAC register must first be loaded with all 1s. This is most easily accomplished by asserting Data Override HIGH ($\overline{\text{DF/DOR}}$ LOW and CTRL HIGH). $R1$ may then be adjusted until $V_{\text{OUT}} = -V_{\text{REF}} (4095/4096)$. In the case of an adjustable V_{REF} , $R1$ and R_{FEEDBACK} may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

In many applications the PM-7548's negligible zero scale error and very low gain error permit the elimination of the trimming components ($R1$ and the external R_{FEEDBACK}) without adverse effects on circuit performance.

TABLE 1: Unipolar Binary Code Table

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
MSB	LSB (V_{OUT} as shown in Figures 9 and 10)
1111 1111 1111	$-V_{\text{REF}} \left(\frac{4095}{4096} \right)$
1000 0000 0001	$-V_{\text{REF}} \left(\frac{2049}{4096} \right)$
1000 0000 0000	$-V_{\text{REF}} \left(\frac{2048}{4096} \right) = -\frac{V_{\text{REF}}}{2}$
0111 1111 1111	$-V_{\text{REF}} \left(\frac{2047}{4096} \right)$
0000 0000 0001	$-V_{\text{REF}} \left(\frac{1}{4096} \right)$
0000 0000 0000	$-V_{\text{REF}} \left(\frac{0}{4096} \right) = 0$

NOTES:

- Nominal full scale for the circuits of Figures 9 and 10 is given by $\text{FS} = V_{\text{REF}} \left(\frac{4095}{4096} \right)$.
- Nominal LSB magnitude for the circuits of Figures 9 and 10 is given by $\text{LSB} = V_{\text{REF}} \left(\frac{1}{4096} \right)$ or $V_{\text{REF}} (2^{-n})$.

BIPOLAR BINARY OPERATION (4-QUADRANT)

Figure 12 details a suggested circuit for bipolar, or offset binary operation. Table 2 shows the digital input to analog output relationship. The circuit uses offset binary coding. Two's complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

TABLE 2: Bipolar (Offset Binary) Code Table

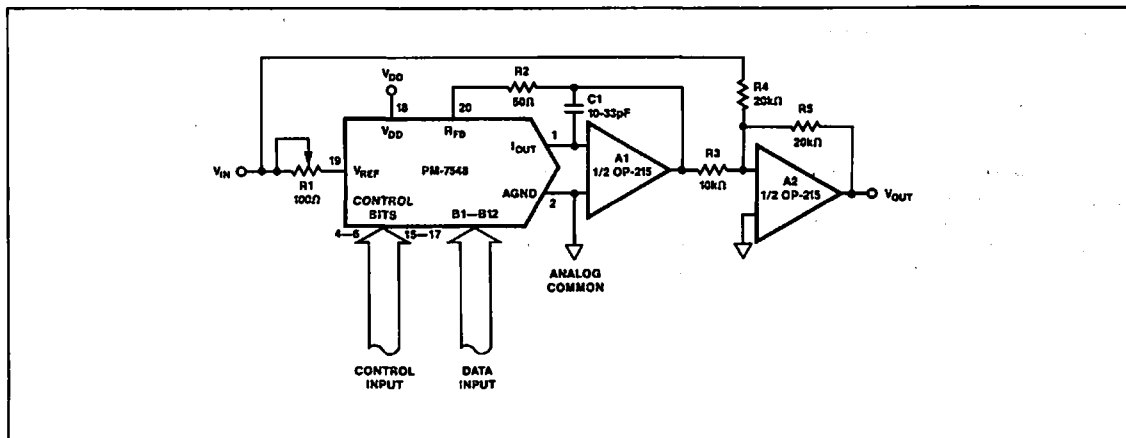
DIGITAL INPUT			NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 12)
MSB		LSB	
1111	1111	1111	$+V_{REF} \left(\frac{2047}{2048} \right)$
1000	0000	0001	$+V_{REF} \left(\frac{1}{2048} \right)$
1000	0000	0000	0
1111	1111	1111	$-V_{REF} \left(\frac{1}{2048} \right)$
0000	0000	0001	$-V_{REF} \left(\frac{2047}{2048} \right)$
0000	0000	0000	$-V_{REF} \left(\frac{2048}{2048} \right)$

NOTES:

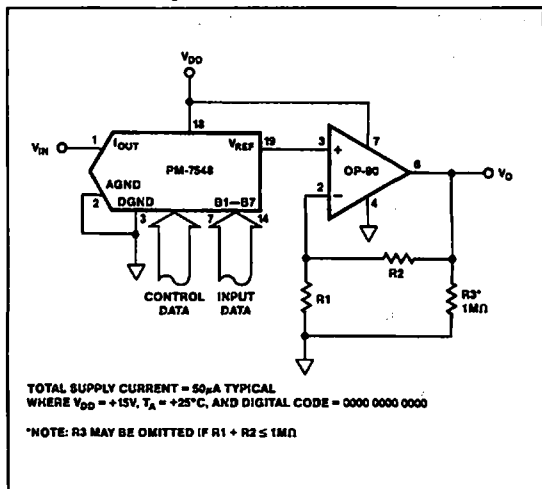
- Nominal full scale for the circuit of Figure 7 is given by
 $FS = V_{REF} \left(\frac{2047}{2048} \right)$.
- Nominal LSB magnitude for the circuit of Figure 7 is given by
 $LSB = V_{REF} \left(\frac{1}{2048} \right)$.

Resistors R3, R4, and R5 must be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R3 and R4 causes offset and full scale errors while an R5 to R4 and R3 mismatch will result in full scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R1 until $V_{OUT} = 0V$. R1 and R2 may be omitted, adjusting the ratio of R3 to R4 to yield $V_{OUT} = 0V$. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and either adjusting the amplitude of V_{REF} or the value of R5 until the desired V_{OUT} is achieved.

FIGURE 12: Bipolar Operation (4-Quadrant)

SINGLE SUPPLY OPERATION

Voltage Switching Mode: Figure 13 shows the PM-7548 in a single supply voltage switching mode. This circuit uses the micropower OP-90 to minimize supply current requirements. This op amp allows the circuit output to swing to ground provided that the op amp sees a resistance to ground of less than 1M Ω .

FIGURE 13: Ultra Low Power Single Supply Operation (Voltage Switching Mode)


As shown, a reference voltage is applied to I_{OUT} and the buffer op amp is tied, in a noninverting orientation, to the V_{REF} pin. The DAC's R-2R ladder acts as a voltage divider, its output voltage at the V_{REF} pin having an impedance of R (typically 11k Ω).

The applied reference voltage must always be positive with respect to AGND. This will avoid the forward biasing of an internal diode found between I_{OUT} and AGND. The reference voltage must also be maintained within $\pm 2.5V$ of AGND (with V_{DD} between $+12V$ and $+15V$) to maintain linearity.

The output voltage of this circuit can be described as:

$$V_{OUT} = V_{REF} \left(\frac{n}{4096} \right) \left(\frac{R1 + R2}{R1} \right)$$

where n is the decimal equivalent of the digital input word. The ratio of $R1$ and $R2$ may be varied to give the desired output range.

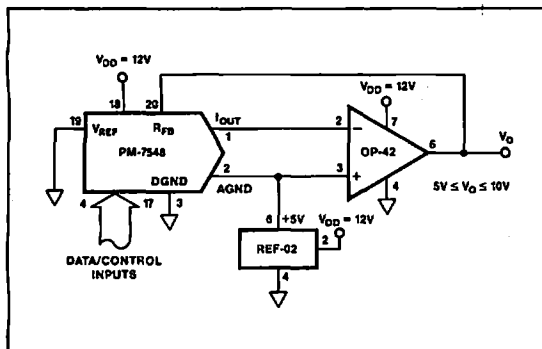
False Ground Mode: Single supply operation can be implemented in a current steering mode as shown in Figure 14. In this circuit, analog ground is offset to a false ground, typically $+5V$. V_{OUT} ranges between $+5V$ and $+10V$ depending on the digital code and the V_{OFFSET} . V_{OUT} is described by:

$$V_{OUT} = V_{OFFSET} + (n/4096) (V_{OFFSET})$$

where n is the decimal equivalent of the digital input word.

This configuration allows the use of an op amp which cannot operate down to $0V$, or "true" ground. For best linearity, V_{DD} should be at least $10V$ above the false ground.

FIGURE 14: Single Supply Operation
(False Ground, Current Steering Mode)



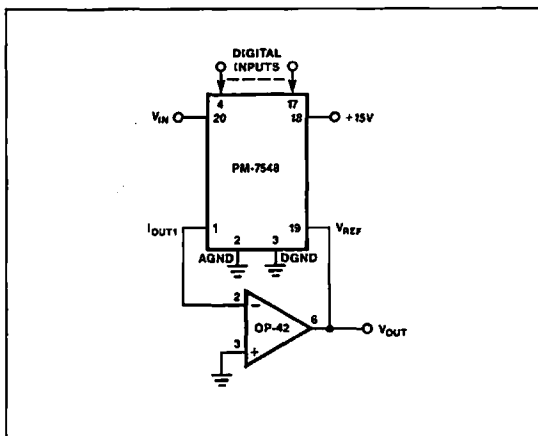
ANALOG/DIGITAL DIVISION

The transfer function for the PM-7548 connected in the multiplying mode as shown in Figure 15 is:

$$V_O = -V_{IN} \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}} \right)$$

where A_X assume a value of 1 for an "ON" bit and 0 for an "OFF" bit.

FIGURE 15: Analog/Digital Divider



The transfer function is modified when the DAC is connected in the feedback of an operational amplifier as shown in Figure 15. It is now:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}}} \right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits "OFF" since division by zero is infinity. With all bits "ON", the gain is 1 (± 1 LSB). The gain becomes 4096 with the LSB, bit 12, "ON".

MICROPROCESSOR INTERFACE

The PM-7548 can be directly interfaced to an 8-bit microprocessor's bus. Two such interfaces are shown in Figures 16 and 17.

Figure 16 shows an automatic transfer interface with an MC6809 microprocessor. The PM-7548 is assigned an address, through use of the decoder, that does not use A_0 . The 8-bit high byte may then be loaded using an even (X) address. Next, the 4-bit low byte is loaded to an odd address (X + 1), A_0 selecting both the low byte data loading and the 12-bit data transfer.

Figure 17 shows a multiple DAC, strobed transfer interface configuration, also using the MC6809. Decoding allows independent loading of data with simultaneous updating of both DACs. This technique can be extended to accommodate an unlimited number of DACs with the use of additional decoding.

FIGURE 16: PM-7548/MC6809 Interface Automatic Transfer Mode

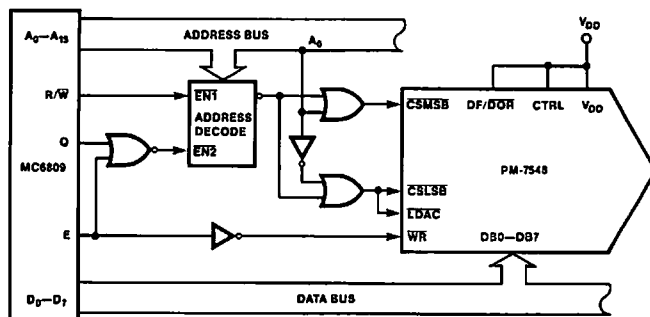
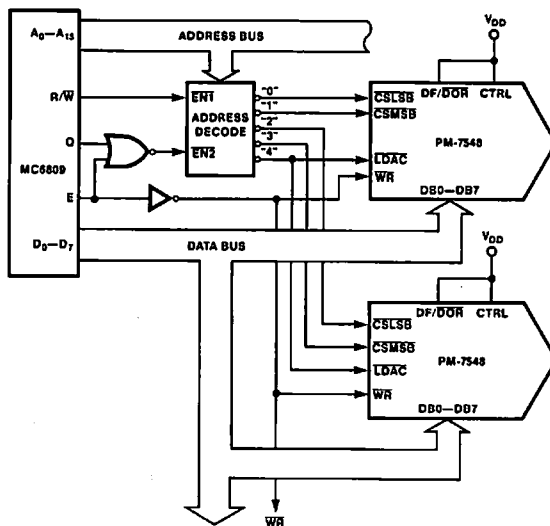


FIGURE 17: PM-7548/MC6809 Interface Multiple DAC, Strobed Transfer Mode



Precision Monolithics Inc.

GENERAL DESCRIPTION

This data sheet covers the electrical requirements of the monolithic 8-bit digital-to-analog converters found in MIL-M-38510/113. Devices supplied to this data sheet are manufactured and tested at PMI's MIL-M-38510 certified facility and are listed in CPL-38510.

Complete device requirements will be found in MIL-M-38510 and MIL-M-38510/113 for Class B processed devices.

Device Types shall be as follows:

- 01 D/A Converter, 8 bit, 0.19% linearity
02 D/A Converter, 8 bit, 0.10% linearity

GENERIC CROSS-REFERENCE INFORMATION

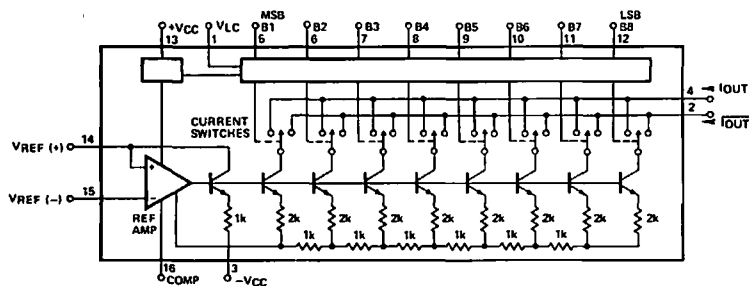
This cross-reference information is presented for the convenience of the user. The Generic-Industry types listed may not have identical operational performance characteristics across the military temperature range or reliability factors equivalent to the MIL-M-38510/113 devices.

Military Device Type	Generic-Industry Type
01	DAC-08
02	DAC-08A

CASE OUTLINE

Per MIL-M-38510, Appendix C, Case Outline D-2 (16-Lead 1/4" × 7/8", dual-in-line). Package type designator "E".

SIMPLIFIED SCHEMATIC



JM38510/11301/11302

JAN 8-BIT MULTIPLYING D/A CONVERTERS

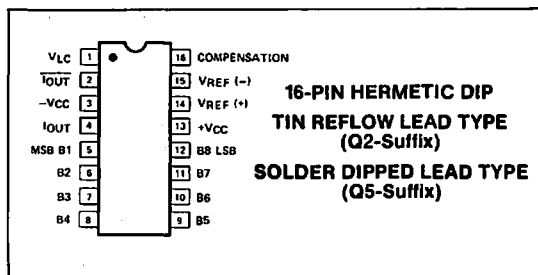
POWER AND THERMAL CHARACTERISTICS

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{J-C}	Maximum θ_{J-A}
Dual-in-line	E	400mW at $T_A = 125^\circ\text{C}$	35°C/W	120°C/W

ORDERING INFORMATION

LINEARITY	JAN SLASH SHEET	PMI DEVICE
0.19%	JM38510/113018EB	DAC08Q2/38510
0.19%	JM38510/113018EA	DAC08Q5/38510
0.10%	JM38510/113022EB	DAC08AQ2/38510
0.10%	JM38510/113022EA	DAC08AQ5/38510

PIN CONNECTIONS



DIGITAL-TO-ANALOG CONVERTERS

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage [+V _{CC} - (-V _{CC})]	36Vdc
Voltage, Digital Input to Negative Supply [V _{logic} - (-V _{CC})]	0 to 36Vdc
Voltage, Logic Control (V _{LC})	-V _{CC} to +V _{CC}
Reference Voltage Input [(V ₁₄ , V ₁₅)]	-V _{CC} to +V _{CC}
Reference Input Current (I ₁₄)	5mA
Reference Input Differential Voltage [(V ₁₄ -V ₁₅)]	±18Vdc
Lead Temperature (Soldering, 60 sec)	300°C

Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	±5Vdc to ±15Vdc*
Ambient Temperature Range	-55°C to +125°C

***NOTE:**

A slight degradation in linearity can occur when the supply voltage is near the ±5V end of the recommended operating range.

ELECTRICAL CHARACTERISTICS at ±V_{CC} = ±15Vdc; Source resistance = 50 ohms; I_{REF} = 2mA; Figure 1; Ambient temperature range = -55°C to +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Monotonicity	Δ(I)	Measure I _O , (I _{ON} - I _{ON-1}) ≥ 0 at each major carry point	0	16	0	16	μA
	Δ(I)	Measure I _O , (I _{ON} - I _{ON-1}) ≥ 0 at each major carry point	0	16	0	16	
Output Symmetry	ΔI _{FS}	I _{FS} - I _{FS}	-8	8	-4	4	μA
Full-Scale Current	T _C (I _{FS})	All input bits high, Measure I _O	-50	50	-50	50	ppm/°C
Temperature Coefficient	T _C (I _{FS})	All input bits low, Measure I _O					
Full-Scale Current	I _{FS}	All input bits high, Measure I _O	1.94	2.04	1.984	2	mA
	I _{FS}	All input bits low, Measure I _O					
Zero-Scale Current	I _{ZS}	All input bits low, Measure I _O	-2	2	-1	1	μA
	I _{ZS}	All input bits high, Measure I _O					
Positive Bit Errors	ΣNL+	Measure I _O (Σ Positive bit errors)/IFS	0	0.19	0	0.10	%
	ΣNL+	Measure I _O (Σ Positive bit errors)/IFS					
Negative Bit Errors	ΣNL-	Measure I _O (Σ Negative bit errors)/IFS	-0.19	0	-0.10	0	%
	ΣNL-	Measure I _O (Σ Negative bit errors)/IFS					
Positive and Negative Bit Error Difference	ΔΣNL	Measure I _O ΣNL+ - ΣNL-	-0.05	0.05	-0.03	0.03	%
	ΔΣNL	Measure I _O ΣNL+ - ΣNL-					
Positive Relative Accuracy	NL+	Measure I _O ΣNL+ + ΔΣNL	0	0.19	0	0.10	%
	NL+	Measure I _O ΣNL+ + ΔΣNL					
Negative Relative Accuracy	NL-	Measure I _O ΣNL- + ΔΣNL	0	0.19	0	0.10	%
	NL-	Measure I _O ΣNL- + ΔΣNL					

Bit Error

Bit error is the deviation of the analog output from its ideal value (after zero-scale and full-scale errors have been calibrated out) when turning on an individual bit. This is measured for all n bits.

$$\text{Bit error (analog value)} = V_n - (\text{FSR}/2^n)$$

Where V_n = analog output with bit n on only.

FSR = full-scale range

n = number of bits

Summation Nonlinearity (ΣNL)

Summation nonlinearity is the sum of all positive bit errors or all negative bit errors, whichever is larger. By summing up all the bit errors in one direction, you obtain the worst possible nonlinearity (i.e. if bit 2 is 1 LSB high and bit 4 is 1/2 LSB high, then bits 2 and 4 together will be 1 1/2 LSBs high. This is essentially the same as integral nonlinearity since the bit errors are superimposed on each other to give the worst case nonlinearity.



ELECTRICAL CHARACTERISTICS at $\pm V_{CC} = \pm 15\text{Vdc}$; Source resistance = 50 ohms; $I_{REF} = 2.0\text{mA}$; Figure 1; Ambient temperature range = -55°C to $+125^{\circ}\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Output Current Range	$I_{FS} R_1$	All input bits high, Measure I_O $-V_{CC} = -10\text{V}$, $V_{REF} = 15\text{V}$	2.1	—	2.1	—	mA
	$\overline{I_{FS} R_1}$	All input bits low, Measure $\overline{I_O}$ $-V_{CC} = -10\text{V}$, $V_{REF} = 15\text{V}$					
	$I_{FS} R_2$	All input bits high, Measure I_O $-V_{CC} = -12\text{V}$, $V_{REF} = 25\text{V}$	4.2	—	4.2	—	
	$\overline{I_{FS} R_2}$	All input bits low, Measure $\overline{I_O}$ $-V_{CC} = -12\text{V}$, $V_{REF} = 25\text{V}$					
Reference Bias Current	I_{REF}	All input bits low	-3	0	-3	0	μA
High Level Input Current	I_{IH}	All input bits $V_{IN} = 18\text{V}$, each input measured separately	-0.05	10	-0.05	10	μA
Low Level Input Current	I_{IL}	All input bits $V_{IN} = 10\text{V}$, each input measured separately	-10	—	-10	—	μA
Full-Scale Current At +18V Compliance	$I_{FS} +$	All input bits high, Measure I_O $V_{IO} = 18\text{V}$	1.90	2.08	1.94	2.04	mA
	$\overline{I_{FS} +}$	All input bits low, Measure $\overline{I_O}$ $V_{IO} = 18\text{V}$					
Full-Scale Current At -10V Compliance	$I_{FS} -$	All input bits high, Measure I_O $V_{IO} = -10\text{V}$	1.90	2.08	1.94	2.04	mA
	$\overline{I_{FS} -}$	All input bits low, Measure $\overline{I_O}$ $V_{IO} = -10\text{V}$					
Change in Full Scale Current Due to Voltage Compliance	ΔI_{FSC}	All input bits high, Measure I_O $25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ $T_A = -55^{\circ}\text{C}$ $V_{IO} = 18\text{V}$ to -10V	-4 -8	4 8	-4 -8	4 8	μA
		All input bits low, Measure $\overline{I_O}$ $25^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ $T_A = -55^{\circ}\text{C}$ $V_{IO} = 18\text{V}$ to -10V	-4 -8	4 8	-4 -8	4 8	
	$\overline{\Delta I_{FSC}}$	All input bits high, Measure I_O $+V_{CC} = 4.5\text{V}$ to $+5.5\text{V}$, $-V_{CC} = -18\text{V}$	-4	4	-4	4	
		All input bits low, Measure $\overline{I_O}$ $+V_{CC} = 4.5\text{V}$ to $+5.5\text{V}$, $-V_{CC} = -18\text{V}$	-8	8	-8	8	
Power Supply Sensitivity From $+V_{CC}$	$P_{SS} I_{FS} +1$	All input bits high, Measure I_O $+V_{CC} = 4.5\text{V}$ to $+5.5\text{V}$, $-V_{CC} = -18\text{V}$	-4	4	-4	4	μA
	$\overline{P_{SS} I_{FS} +1}$	All input bits low, Measure $\overline{I_O}$ $+V_{CC} = 4.5\text{V}$ to $+5.5\text{V}$, $-V_{CC} = -18\text{V}$	-8	8	-8	8	
	$P_{SS} I_{FS} +2$	All input bits high, Measure I_O $+V_{CC} = 12\text{V}$ to 18V , $-V_{CC} = -18\text{V}$	-8	8	-8	8	
	$\overline{P_{SS} I_{FS} +2}$	All input bits low, Measure $\overline{I_O}$ $+V_{CC} = 12\text{V}$ to 18V , $-V_{CC} = -18\text{V}$	-8	8	-8	8	
Power Supply Sensitivity From $-V_{CC}$	$P_{SS} I_{FS} -1$	All input bits high, Measure I_O $+V_{CC} = 18\text{V}$, $-V_{CC} = -12\text{V}$ to -18V	-8	8	-8	8	μA
	$\overline{P_{SS} I_{FS} -1}$	All input bits low, Measure $\overline{I_O}$ $+V_{CC} = 18\text{V}$, $-V_{CC} = -12\text{V}$ to -18V	-8	8	-8	8	
	$P_{SS} I_{FS} -2$	All input bits high, Measure I_O $+V_{CC} = 18\text{V}$, $-V_{CC} = -4.5\text{V}$ to -5.5V $I_{REF} = 1\text{mA}$	-2	2	-2	2	
	$\overline{P_{SS} I_{FS} -2}$	All input bits low, Measure $\overline{I_O}$ $+V_{CC} = 18\text{V}$, $-V_{CC} = -4.5\text{V}$ to -5.5V $I_{REF} = 1\text{mA}$	-2	2	-2	2	

ELECTRICAL CHARACTERISTICS at $\pm V_{CC} = \pm 15\text{Vdc}$; Source resistance = 50 ohms; $I_{REF} = 2.0\text{mA}$; Figure 1; Ambient temperature range = -55°C to $+125^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	01 LIMITS		02 LIMITS		UNITS
			MIN	MAX	MIN	MAX	
Supply Current From $+V_{CC}$	I_{CC+}	All input bits high	0.4	3.8	0.4	3.8	mA
Supply Current From $-V_{CC}$	I_{CC-}	All input bits high	-7.8	-0.8	-7.8	-0.8	mA
Propagation Delay Time, High-to-Low Level	t_{PHL}	Figure 2, Measure V_O	6	60	6	60	ns
Propagation Delay Time, Low-to-High Level	t_{PLH}	Figure 2, Measure V_O	6	60	6	60	ns
Reference Amplifier Input Slew Rate	di_O/dt $T_A = 25^\circ\text{C}$	Figure 3, Measure V_O	1.5	—	1.5	—	mA/ μs
Settling Time, High-to-Low Level	t_{SHL} $T_A = 25^\circ\text{C}$	Figure 2, Output within 1/2 LSB of final value of I_O	10	135	10	135	ns
Settling Time, Low-to-High Level	t_{SLH} $T_A = 25^\circ\text{C}$	Figure 2, Output within 1/2 LSB of final value of I_O	10	135	10	135	ns

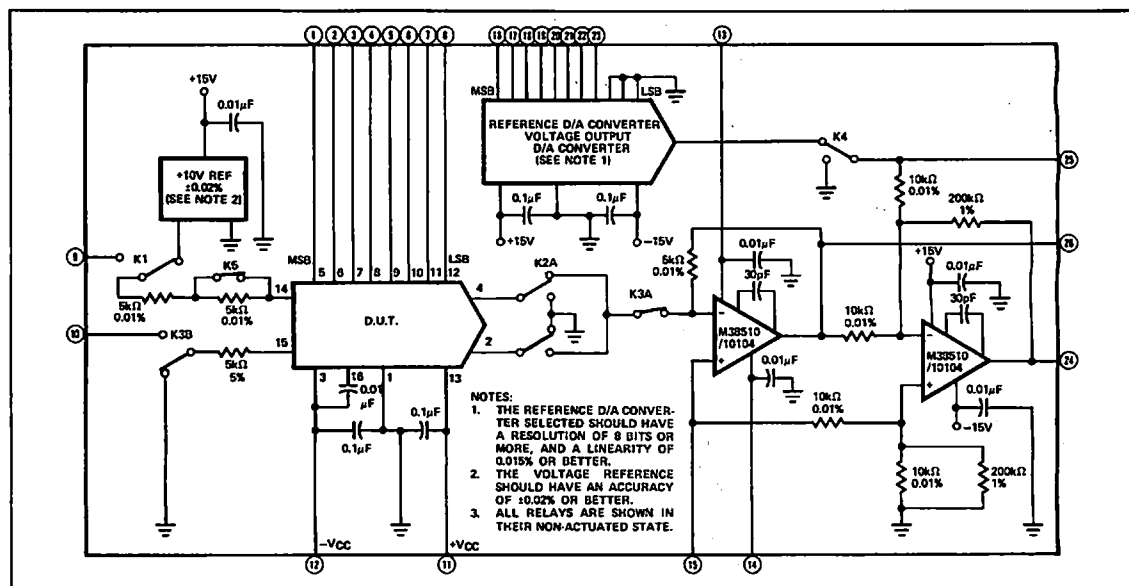


Figure 1. Test Circuit For Static Tests

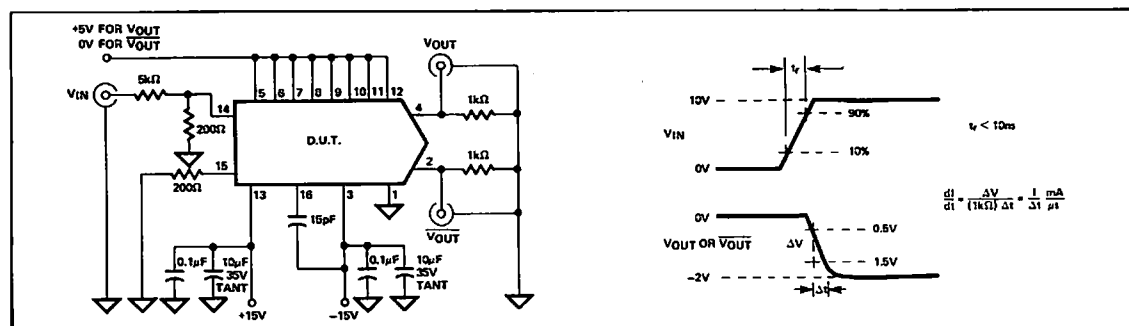


Figure 3. Test Circuit For Slew Rate, Device Types 01, 02

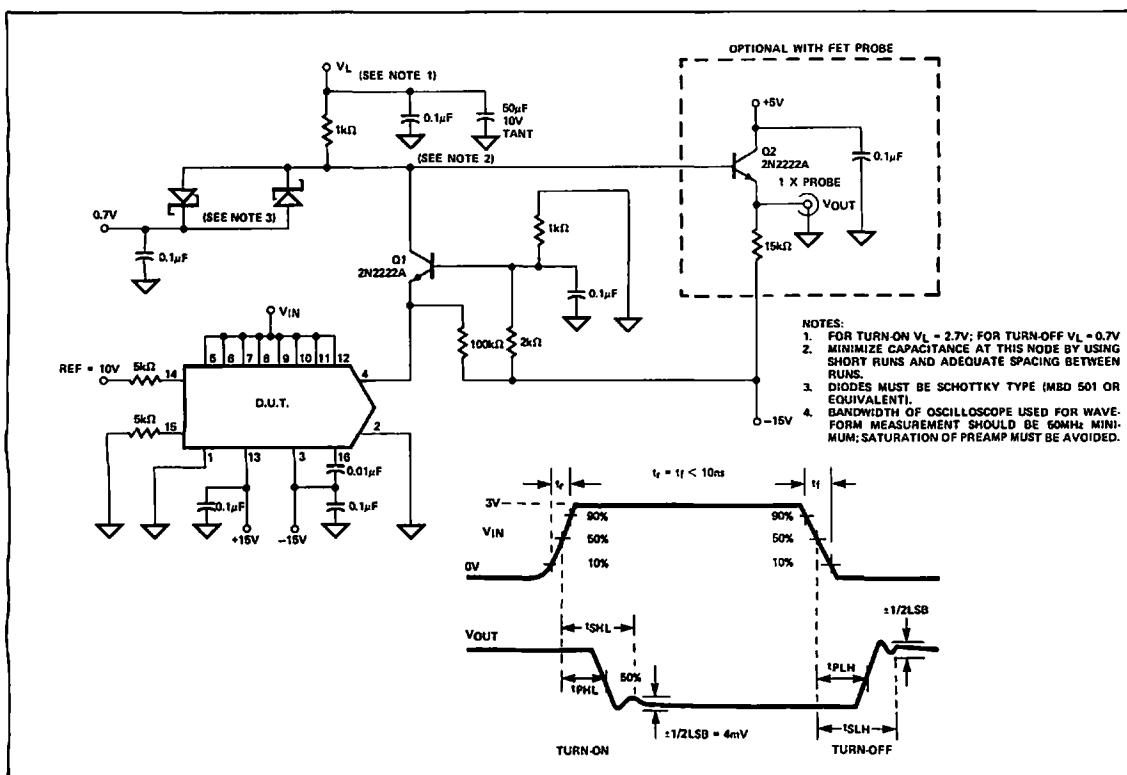


Figure 2. Test Circuit For Propagation Delay and Settling Time, Device Types 01 and 02

BURN-IN

Devices supplied by PMI have been subjected to burn-in per method 1015 of MIL-STD-883 using test condition C or test condition F with the circuit shown in Figure 4.

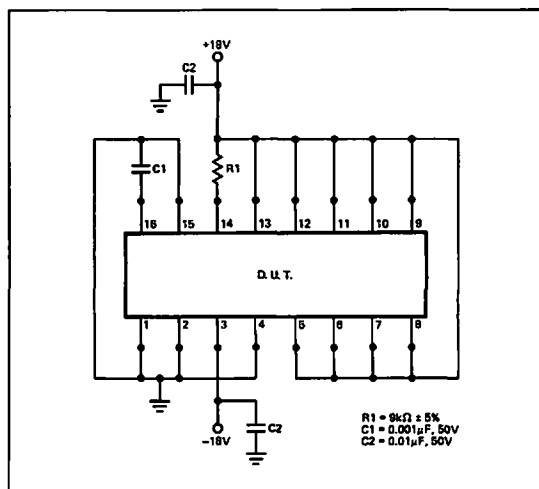


Figure 4. Test Circuit, Burn-In and Operating Life Test

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*Indicates new product or product whose data sheet has been finalized since the 1986 data book.



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A/D CONVERTERS

INTRODUCTION

Analog-to-digital converters (ADC) translate analog input voltages into an equivalent digital value. PMI's ADCs use the general purpose successive approximation conversion (SAC) technique. The basic SAC architecture consists of a DAC, comparator, input scaling resistors, and a successive approximation register. A clock and a voltage reference make a complete ADC system.

PMI uses both bipolar and CMOS technologies to optimize ADC designs. The bipolar technology lends itself to high speed ADC conversion and provides the complete ADC function including an internal reference. The CMOS technology offers ADC designs with very low power consumption and good interface versatility at lower prices. PMI's improved bipolar and oxide-isolated CMOS processes offer the best conversion speeds in the SAC architecture.

A SAC ADC has inherent ratioing capability between the input voltage and the input reference level. The digital output is proportional to V_{IN}/V_{REF} . Important criteria for selection of A/D converters include accuracy, conversion speed and resolution. Other requirements include temperature stability, output coding, output data format, reference stability, clock and power needs.

At the digital output many interface data formats are available to match the wide variety of application needs. The ADC-910 provides a very complete microprocessor-controlled interface which contains data registers, control registers and hand-shaking lines. This architecture provides a complete microprocessor compatible system that allows total software control of all ADC functions. For stand-alone applications the ADC-908 offers direct data output, start conversion and very low power dissipation.

For 12-bit A/D converter applications the new 12 microsecond conversion time ADC-9012 offers a monolithic low-cost solution. This low power CMOS design provides fast 90 nanosec access time and 75 nanosec bus disconnect time for high data transfer rates.

DEFINITIONS—

ANALOG-TO-DIGITAL CONVERTERS

Accuracy—ADC total accuracy consists of the sum of integral nonlinearity (INL) error, zero error, gain error and reference error specifications. The INL is the most critical specification since no additional user calibration can be easily performed. Additional specifications affecting ADC device accuracy includes zero drift, gain drift, power supply sensitivity, and noise. Proper circuit layout and grounding are also important factors in achieving rated performance.

Aperture—The period of time during which an analog input to an ADC should not change more than 1/2 LSB. Determines maximum sampling frequency of the ADC.

ADC—An acronym for Analog-to-Digital Conversion, sometimes written as A/D.

Binary Coding—The digital output of an ADC is considered binary-coded when outputs start at all zeros for a zero-scale analog input counting up to all-ones' output code for a full-scale analog input signal.

Bipolar Mode—An ADC configured to convert both positive and negative input voltages.

Bipolar Offset—The analog displacement of one half of full scale range when the ADC operates in the bipolar mode. The offset is generally derived from the converter reference circuit.

Bus—A parallel path of binary information signals—usually 4, 8, or 16 bits wide.

Byte—A binary digital word often 8 bits long.

Chip Select (CS)—A logic input signal activating data or control information transfer between the ADC and the digital circuitry. This signal is usually active low designated by a bar over the top of (CS). CS is used in conjunction with additional qualifying logic signals to determine the exact activities to take place.

Clock (CK)—The operation of the successive approximation conversion process requires a clock. The clock sets the basic conversion rate.



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Some ADCs have an internal clock, using an external capacitor to set the frequency. Most ADCs have an external clock input.

Code Width—The amount of input voltage change which occurs between output code transitions expressed in LSBs of full scale. The ideal code width is one LSB.

Code Width Uncertainty—The dynamic variation or jitter in the code width due to noise.

Coding—The format of the ADC digital output data. Common formats include binary, offset binary, complementary binary, two's complement, low byte and high byte.

Command Register—An internal register of the ADC that can be programmed by the user to select various modes of operation. For example, unipolar or bipolar conversion selection, range selection, data output format, etc.

Control Lines—Digital input/output pins that activate/monitor and control ADC operation. For example, chip select, write, low byte, high byte, start convert, end of conversion, conversion complete, busy, read, etc.

Conversion Complete (CC)—This digital output signal indicates the end of conversion. When this signal is in the opposite state the ADC is considered to be in the "busy" state.

Conversion Time (t_c)—The amount of time elapsed from the start-conversion control signal until the conversion complete signal occurs.

Differential Nonlinearity (DNL)—The worst-case deviation of distance between transition voltages from the ideal 1 LSB code width. The parameter uses units of LSBs. DNL is one of an ADC's errors which cannot be removed by user adjustments.

Drift—See Gain Drift, Zero Drift, and Offset Drift specifications.

End Of Conversion (EOC)—This digital output signal flags the conversion complete and data ready condition of an ADC.

Full Scale (FS)—Maximum input voltage of an ADC. A full-scale input voltage to a natural binary-coded ADC outputs the all-ones code.

Full-Scale Error—This parameter applied to ADCs is the same as the gain error specification. See Gain Error.

Full-Scale Range (FSR)—The difference between maximum and minimum analog values for an ADC input.

Gain Drift—The change in the full-scale transition voltage measured over the operating temperature range. This parameter has units of % of full scale, ppm of full scale, or LSB. It may also be expressed as % of FS/°C, ppm of FS/°C, etc.

Gain Error—The difference between the actual full-scale transition voltage and the ideal full-scale transition voltage. The units of this parameter are in LSBs or percent of full scale.

Half-Step Offset—The half-step offset is necessary in ADCs to center the analog input voltages half way between the output code transition points. The SAC converter architecture inherently has a 1 LSB transition voltage for the first code change if a half-step offset is not inserted.

High Byte (HB)—In ADCs with resolutions greater than 8 bits, some products are offered in a high byte, low byte format to simplify interface to 8-bit microprocessor systems. The high byte contains the most significant bit and some or all of the upper 8 bits of the ADC output. Generally bits are loaded in a right or left justified format. Individual product data sheets should be consulted.

Input Impedance (R_{IN})—Analog input resistance of the ADC. In SAC converters input impedance is primarily resistive, but should be buffered by an amplifier with a low output impedance at the clock frequency of the SAC ADC to maintain a stiff input voltage to the ADC.

Input Range—The analog voltage input range which results in a zero code to full-scale code digital output in a natural binary-coded ADC. This parameter is identical to full-scale range. Common preset ranges include 0 to 10V, -10 to +10V, -5 to +5V, etc.

Integral Nonlinearity (INL)—This error specification is a measure of the straightness of the ADC transfer function. It is measured as the worst-case deviation in LSBs from a straight line drawn through the center of the first and last code widths. INL is one of the key error specifications of an ADC which cannot be calibrated by the user.

Left Justified Data—In the byte-oriented data-output format, data bit sets shorter than 8 bits are



Precision Monolithics Inc.

A/D CONVERTERS

placed starting in the left side of the data output transfer register. This could apply to the upper or lower byte. For example, a 12-bit ADC will have 4 extra bits which could be left justified.

Least Significant Bit (LSB)—The binary digit with the smallest numerical weighting, normally one LSB equals full-scale range divided by (2^n) , where n is the number of bits of the ADC. This parameter may be expressed in millivolts.

Low Byte (LB)—In ADCs with resolutions greater than 8 bits, some products are offered in a high byte, low byte format to simplify interface to 8-bit microprocessor systems. The low byte contains the least significant bit and some or all of the low 8 bits of the ADC output. Generally bits are loaded in a right or left justified format. Individual product data sheets should be consulted.

Major Transition—The digital output code change between one-and-all-zeros code and zero-and-all-ones code. For example an 8-bit ADC major transition occurs between the codes 1000 0000 and 0111 1111 (half-scale).

Missing Code—As an analog input voltage is swept from zero input to full scale, the output digital codes should change by 1 LSB as each transition voltage is reached. If an output code is skipped, we have a missing code.

Most Significant Bit (MSB)—The binary digit of the resulting ADC conversion with the largest numerical weighting. Normally the MSB has a weighting of one-half full-scale range.

Offset Binary Code—A digital binary code used to represent plus or minus input polarity analog voltages. Negative full-scale voltage is assigned all-zeros code. Zero input voltage has the MSB high (logic one) and the remaining bits at zero. Positive full-scale voltage is assigned all-ones code.

Offset Drift—The change with temperature of analog zero for an ADC operating in the bipolar mode. It is generally expressed in ppm of FSR/ $^{\circ}$ C or LSBs.

Offset Error—The error at analog zero for an ADC operating in the bipolar mode. It has units of % of FSR or LSBs.

Overrange—When analog input voltages exceed

the input range, an overrange condition is in effect. Normally the digital output code stays at all ones for positive overrange and all zeros for negative overrange with standard binary coding.

Power Supply Sensitivity (PSS)—The change in the full-scale transition voltage due to a change in power supply voltage. The units are in LSB, % of FS per % of supply voltage, or ppm of FS per % of supply voltage.

Quantization Error—An ADC of n bits can only identify 2^n output codes; however, there exists an infinite number of analog input values adjacent to the LSB of the ADC which are assigned the same output code. The $\pm 1/2$ LSB limit to resolution is known as the fundamental quantization error of an ADC.

R-2R Ladder—A resistor network providing the basic binary-current-division used in SAC ADCs.

Reference (V_{REF})—Reference voltages determine ADC system's absolute conversion accuracy at full scale. At other voltages the INL and reference determine absolute accuracy. References may be internally or externally supplied.

Relative Accuracy—Relative accuracy error, expressed in LSBs or % of full scale, is the deviation of the analog value at any code from its theoretical value after gain and offset is calibrated. PMI's usage of this specification is identical to the integral nonlinearity specification.

Resolution—The resolution of an ADC is the number of states (2^n) that the analog input voltage is divided (or resolved) into, where n is equal to the number of bits.

Right Justified Data—In the byte-oriented data-output format, data bit sets shorter than 8 bits are placed starting in the right side of the data output transfer register. This could apply to the upper or lower byte. For example, a 12-bit ADC will have 4 extra bits which could be right justified.

Sampling Frequency—The rate at which the ADC can continuously convert analog inputs into digital outputs. In SAC ADCs clock frequency and data transfer overhead determines the sampling frequency.



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A/D CONVERTERS

Short Cycling—Termination of the conversion sequence of an ADC to less than the total number of clock periods required for a full resolution conversion.

Span—Sometimes used to describe the full-scale analog input voltage. Some ADCs have resistor-selectable analog input ranges.

Status Register—A register indicating current status of the analog-to-digital conversion with a busy signal or a conversion complete signal.

Successive Approximation Conversion (SAC)—Successive approximation converters compare an analog input against an accurately-known binary fraction of a reference input. Starting with half the reference value (the MSB) the converter determines whether the input is greater than or less than this value. Next the converter divides the remaining value in half again determining whether the input value is in the upper or lower quarter. This process is continued until all bits have been tried. The digital result of each trial is a numerical representation of the analog input.

Successive Approximation Register (SAR)—A digital circuit that controls the operation of a successive approximation ADC and accumulates the output digital word in its register.

Three-State Output Buffer—A digital output circuit that can be programmed to output a logic low, logic high or a high output impedance state. These devices are generally connected to digital buses.

Transition Noise—Width of the transition voltage region.

Transition Voltage—The transition voltage is the center of a finite band of analog input voltages where the digital output code of the ADC toggles between two adjacent codes.

Unipolar Mode—Operation of an ADC with zero to full-scale voltage inputs of one polarity only.

Word—A set of binary digits that represent the fundamental register size of the digital circuits being used. For example, Z80, 8085, and 6800 microprocessor systems use 8-bit words, while 68000 and 80186 microprocessor systems have 16-bit words.

Zero Drift—The change with temperature of analog zero for an ADC operating in the unipolar mode. It is generally expressed in ppm of FS/°C, or LSBs.

Zero Error—The error at analog zero for an ADC operating in the unipolar mode. This is a user adjustable parameter.



A/D CONVERTERS

Precision Monolithics Inc.

A/D CONVERTER SELECTION GUIDE

8-Bit Resolution

Product	Type	Conversion Time (μ s)	Linearity Error	Supply Voltage	Reference Voltage	Input Voltage Range	Digital Output Coding
PM0820	CMOS Half-Flash	1.5	$\pm 1/2$ LSB	+5	+5	+5 +10	Binary Binary
ADC908	CMOS SAR	6	$\pm 1/2$ LSB	+5	-10	± 10 +10	Offset Binary Binary
PM7574	CMOS SAR	15	$\pm 1/2$ LSB	+5	-10	+10 ± 10	Binary Offset Binary

10-Bit Resolution

Product	Type	Conversion Time (μ s)	Linearity Error	Supply Voltage	Reference Voltage	Input Voltage Range	Digital Output Coding
ADC910	Bipolar SAR	6	$\pm 1/2$ LSB	± 5	2.5 Int	+5, +10 $\pm 5, \pm 10$	Binary Offset Binary

12-Bit Resolution

Product	Type	Conversion Time (μ s)	Linearity Error	Supply Voltage	Reference Voltage	Input Voltage Range	Digital Output Coding
ADC9012	CMOS SAR	12	$\pm 1/2$ LSB	+5, -12	-5	+10	Binary

ANALOG-TO-DIGITAL CONVERTERS



ADC-908

CMOS MICROPROCESSOR-COMPATIBLE
FAST 8-BIT A/D CONVERTER

Precision Monolithics Inc.

FEATURES

- 8-Bit Resolution and Accuracy
- No Missing Codes Over Full Temperature Range
- 6 μ s Conversion Time
- Flexible μ P Interface
- 2.5mA Maximum Standby Current
- Replaces AD7574 With Improved Speed

ORDERING INFORMATION†

PACKAGE: 18-PIN DIP AND SO				
INL (LSB)	DNL (LSB)	MILITARY* TEMPERATURE -55°C TO +125°C	INDUSTRIAL TEMPERATURE -40°C TO +85°C	COMMERCIAL TEMPERATURE 0°C TO 70°C
		ADC908AX	ADC908EX	ADC908GP
$\pm 1/2$	$\pm 3/4$	ADC908BX	ADC908FX	ADC908HP
$\pm 3/4$	$\pm 7/8$	—	—	ADC908GS††
$\pm 1/2$	$\pm 3/4$	—	—	—

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The ADC-908 is a monolithic CMOS successive-approximation analog-to-digital converter. When used with a 1.35MHz clock, a conversion time of 6 μ s is achieved, with full accuracy over the operating temperature range.

The ADC-908 outputs use 3-state logic, allowing direct connection to the data bus or system input port. Active-LOW chip select ($\overline{CS}$) and read/write ($\overline{RD}$) inputs are used to control all

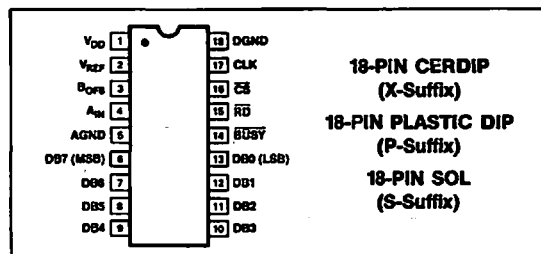
operations. This input structure permits the ADC-908 to be used as a memory-mapped input device. Depending on the control timing waveforms, the ADC-908 is interfaced like static RAM, ROM, or slow memory.

The low power consumption of the ADC-908 is derived from a single +5V supply. A negative reference voltage must also be supplied. Optimum accuracy is achieved when the reference is at -10.00V with a low output resistance. For a low-cost precision -10V/-10.24V reference, ask your PMI sales representative about the REF-08.

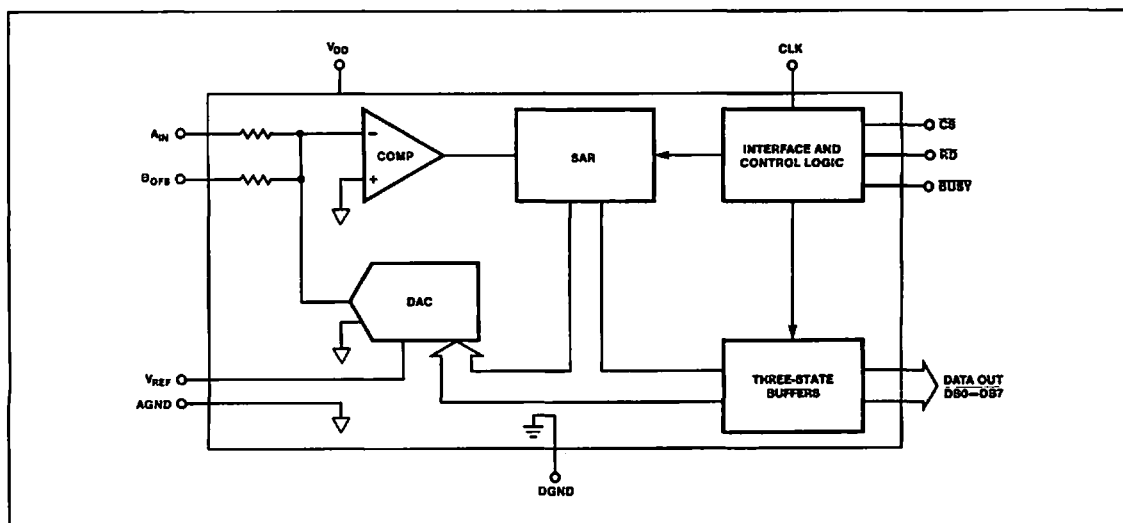
With its on-board comparator, interface logic, optional internal clock, and +5V operation, the ADC-908 is the ideal low-cost solution for microprocessor-based 8-bit A/D systems.

PMI's ADC-908 is pin-and-function compatible with the PM-7574, but offers faster conversion time and faster microprocessor bus interface timing. Conversion time has been reduced by 60% and most key timing specifications, including data access time, START command propagation delay (t_{WBPD}), and reset time, have been improved.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**(T_A = +25°C, unless otherwise noted.)

V _{DD} to AGND	0V, +7.0V
V _{DD} to DGND	0V, +7.0V
AGND to DGND	-0.3V, V _{DD}
CS, RD to DGND	-0.3V, V _{DD} + 0.3V
DB0-DB7 to DGND	-0.3V, V _{DD}
CLK, BUSY to DGND	-0.3V, V _{DD}
B _{OFS} , A _{IN}	±20V
V _{REF}	0V, -20V
Operating Temperature Range	
ADC-908AX, BX	-55°C to +125°C
ADC-908EX, FX	-40°C to +85°C
ADC-908GP, GS, HP	0°C to +70°C
Storage Temperature	-65°C to +150°C

Lead Temperature (Soldering, 10 sec) +300°C

Power Dissipation (Package)

Ceramic (Suffix X) and Plastic (Suffix P)

To +75°C 450mW

Derate Above +75°C by 6mW/°C

Derate Plastic Above +70°C by 8.3mW/°C

Small Outline Wide

To +70°C 400mW

Derate Above 70°C by 10mW/°C

NOTE:

Digital pins are Zener protected. However, proper ESD handling precautions are recommended.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = -10V, Unipolar Configuration, R_{CLK} = 43kΩ, C_{CLK} = 100pF; -40°C ≤ T_A ≤ +85°C for ADC-908E/F, 0°C ≤ T_A ≤ +70°C for ADC-908G/H, -55°C ≤ T_A ≤ +125°C for ADC-908A/B, unless otherwise noted.

			ADC-908			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	N		8	—	—	Bits
Integral Nonlinearity	INL	A/E/G Grades	-1/2	—	+1/2	LSB
		B/F/H Grades	-3/4	—	+3/4	
Differential Nonlinearity	DNL	A/E/G Grades	-3/4	—	+3/4	LSB
		B/F/H Grades	-7/8	—	+7/8	
Gain Error	G _{FSE}	A/E/G Grades T _A = +25°C	-3	—	+3	LSB
		T _A = Full Temp Range	-4.5	—	+4.5	
		B/F/H Grades T _A = +25°C	-5	—	+5	
		T _A = Full Temp Range	-6.5	—	+6.5	
Offset Error	V _{ZSE}	A/E/G Grades T _A = +25°C	-30	—	+30	mV
		T _A = Full Temp Range	-50	—	+50	
		B/F/H Grades T _A = +25°C	-60	—	+60	
		T _A = Full Temp Range	-80	—	+80	
ANALOG INPUTS						
Resistance Mismatch B _{OFS} to A _{IN}	ΔR _{AB}		-1	—	+1	%
Input Resistance at V _{REF} (Note 1)	R _{REF}		5	—	15	kΩ
Input Resistance at B _{OFS} , A _{IN}	R _{B_{OFS}} R _{A_{IN}}		10	—	30	kΩ
Reference Voltage	V _{REF}	Specified Conversion Accuracy	—	-10	—	V
Reference Voltage Range	V _{REF}	Degraded Conversion Accuracy	-5	—	-15	V
Reference Current (Note 8)	I _{REF}	Conversion Complete Prior to Reset.	—	—	2.4	mA
Nominal Analog Input Range						
Unipolar Mode	V _{INU}		—	0 to + V _{REF}	—	V
Bipolar Mode	V _{INB}		—	- V _{REF} to + V _{REF}	—	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{REF} = -10V$, Unipolar Configuration, $R_{CLK} = 43k\Omega$, $C_{CLK} = 100pF$; $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ for ADC-908E/F, $0^{\circ}C \leq T_A \leq +70^{\circ}C$ for ADC-908G/H, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ for ADC-908A/B, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	ADC-908 TYP	MAX	UNITS
LOGIC INPUTS						
Input HIGH Voltage RD, CS Inputs	V_{IH}		2.4	—	—	V
Input LOW Voltage RD, CS Inputs	V_{IL}		—	—	0.8	V
Input Current RD, CS Inputs	I_{IN}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp Range}$	— —	— —	1 10	μA
Input Capacitance RD, CS Inputs (Note 6)	C_{IN}		—	—	5	pF
Input HIGH Voltage, Clock Input	V_{IH}		2.4	—	—	V
Input LOW Voltage, Clock Input	V_{IL}		—	—	0.8	V
Input HIGH Current, Clock Input	I_{IH}		—	—	2	mA
Input LOW Current, Clock Input	I_{IL}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp Range}$	— —	— —	1 10	μA
LOGIC OUTPUTS						
Output HIGH Voltage BUSY, DB0-7	V_{OH}	$I_{SOURCE} = 40\mu A$	4.0	—	—	V
Output LOW Voltage BUSY, DB0-7	V_{OL}	$I_{SINK} = 1.6mA$	—	—	0.4	V
Floating Leakage Current, DB0-7	I_{LKG}	$T_A = +25^{\circ}C$ $T_A = \text{Full Temp Range}$	— —	— —	1 10	μA
Floating State Output Capacitance	C_{OZ}	(Note 6)	—	—	7	pF
POWER REQUIREMENTS						
Standby Current	I_{DD}	$V_{DD} = +4.75V \text{ to } +5.25V$	—	—	2.5	mA
DIGITAL INTERFACE TIMING						
CS Minimum Pulse Width (Note 6)	t_{CS}	$T_A = +25^{\circ}C$	60	—	—	ns
		$T_A = T_{MIN}$	50	—	—	
		$T_A = T_{MAX}$	90	—	—	
RD to CS Setup Time (Note 6)	t_{WCS}		0	—	—	ns
CS to BUSY Propagation Delay (Note 6)	t_{CSPD}	BUSY Load = 20pF				ns
		$T_A = +25^{\circ}C$	—	—	120	
		$T_A = T_{MIN}$	—	—	100	
		$T_A = T_{MAX}$	—	—	150	
		BUSY Load = 100pF				
		$T_A = +25^{\circ}C$	—	—	150	
BUSY to RD Setup Time (Notes 2, 6)	t_{BSR}	$T_A = T_{MIN}$	—	—	120	ns
		$T_A = T_{MAX}$	—	—	200	
			0	—	—	
BUSY to CS Setup Time (Note 6)	t_{BSCS}		0	—	—	ns

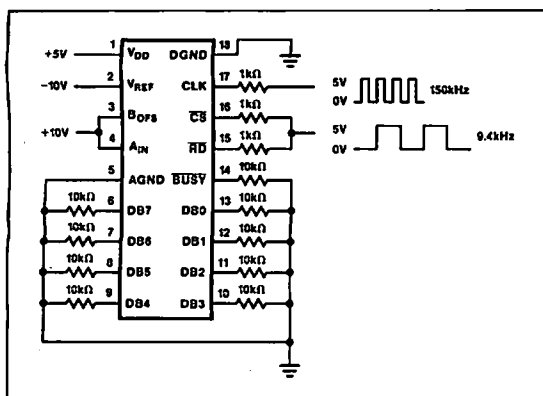


ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{REF} = -10V$, Unipolar Configuration, $R_{CLK} = 43k\Omega$, $C_{CLK} = 100pF$, $-40^\circ C \leq T_A \leq +85^\circ C$ for ADC-908E/F, $0^\circ C \leq T_A \leq +70^\circ C$ for ADC-908G/H, $-55^\circ C \leq T_A \leq +125^\circ C$ for ADC-908A/B, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	ADC-908			UNITS
			MIN	TYP	MAX	
Data Access Time (Note 6)	t_{RAD}	$C_L = 20pF$				
		$T_A = +25^\circ C$	—	—	140	
		$T_A = T_{MIN}$	—	—	100	
		$T_A = T_{MAX}$	—	—	200	
		$C_L = 100pF$				ns
		$T_A = +25^\circ C$	—	—	170	
Data Hold Time (Notes 3, 6)	t_{RHD}	$T_A = +25^\circ C$ (Note 3)	30	—	100	
		$T_A = T_{MIN}$	20	—	70	ns
		$T_A = T_{MAX}$	40	—	140	
$\overline{CS}$ to $\overline{RD}$ Hold Time (Note 6)	t_{RHCS}	$T_A = +25^\circ C$	—	—	200	
		$T_A = T_{MIN}$	—	—	120	ns
		$T_A = T_{MAX}$	—	—	250	
Reset Time Requirement (Note 6)	t_{RESET}	$T_A = +25^\circ C$	450	—	—	ns
		$T_A = \text{Full Temp. Range}$	500	—	—	
Conversion Time (Note 4)	$t_{CONVERT}$	Static RAM Mode				
		External Clock				
		$f = 1.35MHz$	—	—	6	μs
		ROM Mode				
(Notes 4, 5, 6)		Internal Clock	—	—	7	
$\overline{RD}$ HIGH to $\overline{BUSY}$ Propagation Delay, ROM Mode (Notes 4, 5, 6)	t_{WBPD}	$C_L = 20pF$				
		$T_A = +25^\circ C$	—	—	600	ns
		$T_A = T_{MIN}$	—	—	400	
		$T_A = T_{MAX}$	—	—	800	

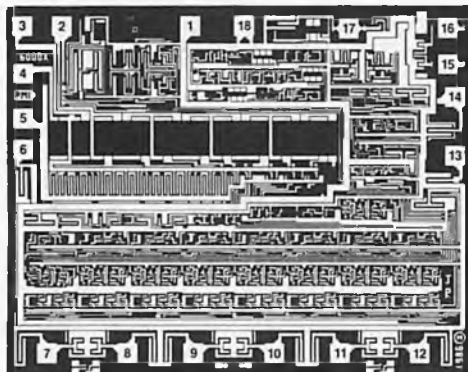
NOTES:

- For optimum gain accuracy over the full temperature range, the source resistance at pin 2 should be kept low.
- In ROM mode, $\overline{RD}$ can go LOW prior to $\overline{BUSY} = \text{HIGH}$, but must not return HIGH until $\overline{BUSY} = \text{HIGH}$.
- Output loading 10pF. A 3k Ω pullup resistor to +5V is used for V_{OL} to High-Z, for V_{OH} to High-Z, a 3k Ω pulldown to GND is used. Measured to 0.5V output change.
- When using the ADC-908 internal oscillator, actual conversion time depends on clock resistor and capacitor as well as temperature.
- ROM interface mode conversion times are typically 1 μs longer than conversion times for other modes, but the ROM interface mode includes an automatic reset in the conversion time.
- Guaranteed but not tested.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.129 × 0.103 inch, 13,287 sq. mils
(3.28 × 2.62 mm, 8.58 sq. mm)

- | | |
|--------------|-----------------------|
| 1. V_{DD} | 10. DB3 |
| 2. V_{REF} | 11. DB2 |
| 3. B_{OFS} | 12. DB1 |
| 4. A_{IN} | 13. DB0(LSB) |
| 5. AGND | 14. $\overline{BUSY}$ |
| 6. DB7(MSB) | 15. RD |
| 7. DB6 | 16. $\overline{CS}$ |
| 8. DB5 | 17. CLK |
| 9. DB4 | 18. DGND |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_{DD} = +5V$, $V_{REF} = -10.000V$, AGND = DGND = 0V, $T_A = +25^\circ C$, unless otherwise noted.

			ADC-908	
PARAMETER	SYMBOL	CONDITIONS	LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits MIN
Integral Nonlinearity	INL		±3/4	LSB MAX
Differential Nonlinearity	DNL		±7/8	LSB MAX
Gain Error	G _{FSE}		±5	LSB MAX
Offset Error	V _{ZSE}		±60	mV MAX
ANALOG INPUTS				
Resistance Mismatch B _{OFS} to A _{IN}	ΔR _{AB}		±1	% MAX
Input Resistance at V _{REF}	R _{REF}		5/15	kΩ MIN/MAX
Input Resistance at B _{OFS} , A _{IN}	R _{BOFS} , R _{IN}		10/30	kΩ MIN/MAX
DIGITAL INPUTS				
Input HIGH Voltage at RD, CS Inputs	V _{IH}		2.4	V MIN
Input LOW Voltage at RD, CS Inputs	V _{IL}		0.8	V MAX
Input Current RD, CS Inputs	I _{IN}		±1	μA MAX
Input HIGH Voltage Clock Input	V _{IH}		2.4	V MIN
Input LOW Voltage Clock Input	V _{IL}		0.8	V MAX
Input HIGH Current Clock Input	I _{IH}		2	mA MAX
Input LOW Current Clock Input	I _{IL}		1	μA MAX



WAFER TEST LIMITS at $V_{DD} = +5V$, $V_{REF} = -10.000V$, $AGND = DGND = 0V$, $T_A = +25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	ADC-908 LIMIT	UNITS
DIGITAL OUTPUTS				
Output HIGH Voltage BUSY, DB0-7	V_{OH}	$I_{SOURCE} = 40\mu A$	4	V MIN
Output LOW Voltage BUSY, DB0-7	V_{OL}	$I_{SINK} = 1.6mA$	0.4	V MAX
Floating Leakage Current	I_{LKG}		1	μA
POWER REQUIREMENTS				
Standby Current	I_{DD}	$V_{DD} = +4.75V$ to $5.25V$	2.5	mA MAX
TIMING				
Conversion Time	$t_{CONVERT}$	Static RAM Mode, External Clock, $f = 1.35MHz$	6	μs MAX

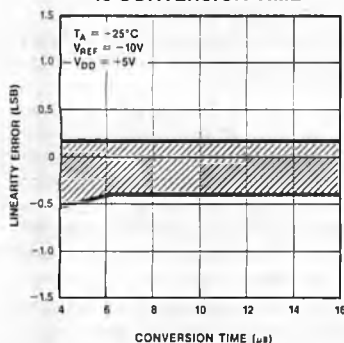
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

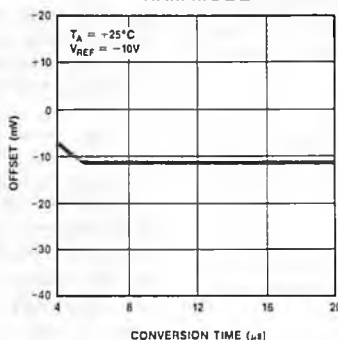
TYPICAL PERFORMANCE CHARACTERISTICS

ANALOG-TO-DIGITAL CONVERTERS

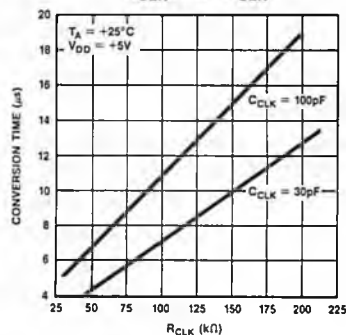
**LINEARITY ERROR
vs CONVERSION TIME**



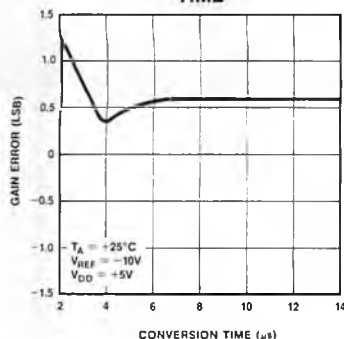
**OFFSET ERROR
vs CONVERSION TIME
RAM MODE**



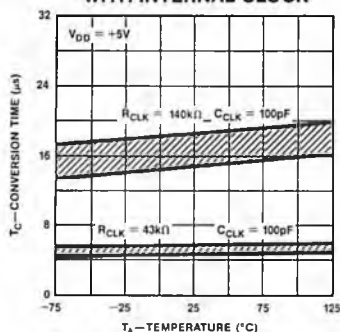
**CONVERSION TIME vs
 R_{CLK} AND C_{CLK}**



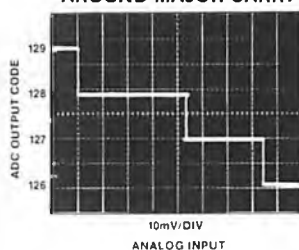
**GAIN ERROR
vs CONVERSION
TIME**



**CONVERSION TIME
vs TEMPERATURE
WITH INTERNAL CLOCK**



**CONVERSION UNCERTAINTY
AROUND MAJOR CARRY**



GENERAL CIRCUIT INFORMATION

The ADC-908 is an 8-bit analog-to-digital converter which uses a successive approximation technique to convert an unknown analog input into a digital code output. The control logic inputs allow easy interface to most microprocessors while three-state outputs allow direct connection to the data bus. Most applications require only passive RC clock components, a -10V reference, and a $+5\text{V}$ power supply. The RC-timed internal clock may be used, or an external clock may be applied to the ADC to maximize performance.

When a Start Conversion command is applied to the $\overline{\text{CS}}$ or $\overline{\text{RD}}$ inputs (see Operating Descriptions for details), $\overline{\text{BUSY}}$ goes LOW indicating a conversion in progress. $\overline{\text{BUSY}}$ may be used as an interrupt to halt the controlling microprocessor during conversion or may be polled to prevent premature data reads.

Starting with the most significant bit (MSB), each successive bit in the DAC is turned on (see Figure 1). The comparator then decides if the DAC output is less than or greater than the signal being converted, and that bit is latched on or off, respectively, before proceeding to the next lower bit and repeating the cycle. When all eight bits have been tested, $\overline{\text{BUSY}}$ goes HIGH, signaling a completed conversion.

Under control of the $\overline{\text{RD}}$ input, the three-state data outputs (D0-D7) change from high-impedance to presenting the new conversion results to the data bus. Following the data read, $\overline{\text{RD}}$ returns HIGH resetting the SAR to 1000 0000 and preparing the ADC for its next conversion.

PIN FUNCTIONS

NOTE: For greater detail on digital input functions, consult Truth Tables and Timing Diagrams.

- Pin 1. V_{DD} Power Supply input, $+5\text{V}$.
- Pin 2. V_{REF} Voltage Reference input, nominal -10V .
- Pin 3. B_{OFS} Bipolar Offset input. $+10\text{V}$ input for bipolar mode operation, tie to V_{IN} for unipolar mode operation.
- Pin 4. A_{IN} Analog Input. 0V to $+10\text{V}$ in unipolar mode, -10V to $+10\text{V}$ in bipolar mode.

- Pin 14. $\overline{\text{BUSY}}$ Conversion status output. $\overline{\text{BUSY}}$ indicates conversion in progress by going LOW at start of conversion and returning HIGH at end of conversion. May be used to interrupt controlling microprocessor or to gate control inputs.
- Pin 15. $\overline{\text{RD}}$ READ input. Used to read data (on falling edge) and to reset converter (on rising edge).
- Pin 16. $\overline{\text{CS}}$ Chip Select input. Asserted to allow ADC operation. Starts conversion when converter is in reset condition. Note: Holding $\overline{\text{CS}}$ HIGH will not prevent a rising edge on $\overline{\text{RD}}$ from resetting the converter.
- Pin 17. CLK External clock input/internal clock RC timing input.

APPLICATIONS INFORMATION

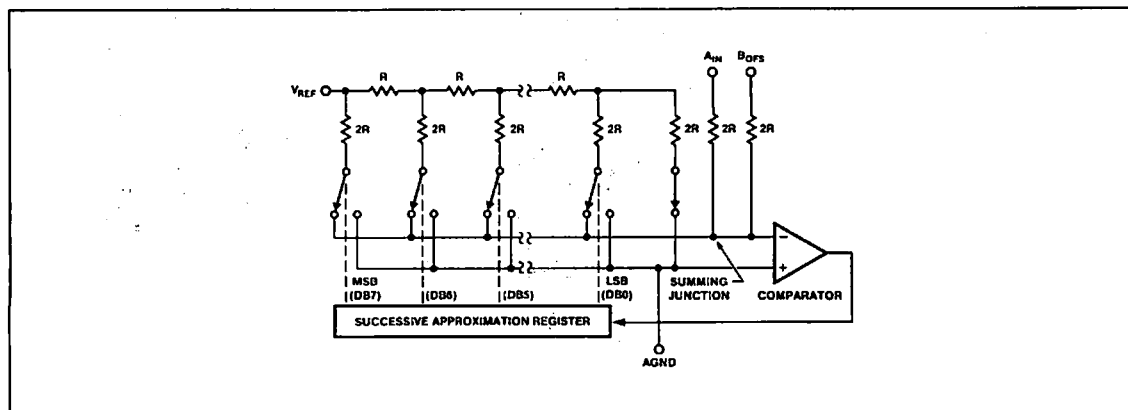
The ADC-908 may be interfaced as if it were a static RAM, a ROM, or a slow-memory device. Each of these interface modes has its own timing and software requirements as described below. These requirements must be rigidly met, as improper timing may cause the ADC-908 to change modes.

HOW TO CHOOSE AN OPERATING MODE

The static-RAM interface mode offers advantages in a tightly controlled hardware and software environment, where the relationship between WRITE and READ instruction pairs is certain. As long as minimum timing is satisfied, converted data may be read at any convenient time after conversion. The use of separate commands to start a conversion, and then read the results, is conceptually easy. However, if the software is subject to uncontrolled modifications, then the paired relationship between WRITE and READ instructions may be lost. Resulting software bugs may result in converted data of unknown age, or altogether invalid data being read.

By contrast, the ROM mode may be more resistant to software bugs. As long as minimum timing is satisfied, each READ instruction obtains new, valid data. However, since the data

FIGURE 1: D/A Converter Used in ADC-908



output at any previous READ instruction is obtained from a conversion performed just after the previous READ instruction, data may be out-of-date. To be sure of obtaining up-to-date data, READ instructions may be coded in pairs (with some NOPs between them); use only the data from the second READ in each pair. The first READ starts the conversion, acting as a substitute for the static-RAM mode WRITE command; the second READ gets the results. The advantage of the ROM mode is the use of a single command, rather than the alternating READ-WRITE required by static-RAM mode.

The slow-memory mode is the simplest mode of all. It is the method of choice where compact coding is essential, or where software bugs are a hazard. In this mode, a single READ instruction will initiate a data conversion, interrupt the microprocessor until completion (WAIT states are introduced), then read the results. If the system throughput tolerates WAIT states, and the hardware is correct, then the slow-memory mode is virtually immune to subsequent software modifications.

OPERATING DESCRIPTION: STATIC-RAM MODE

In this mode, input $\overline{CS}$ is derived from the ADC-908 address decoder, and input $\overline{RD}$ is derived from an active-LOW memory READ signal. (See Figure 2.)

To start a conversion, execute a memory WRITE to the ADC-908. The completed conversion data is obtained by executing a memory READ to the ADC-908. During conversion, output $\overline{BUSY}$ will be LOW. Do not attempt to read data until $\overline{BUSY}$ returns HIGH. The required minimum time between WRITE and READ is usually obtained by including one or more NOP or other program instructions. The use of branch or conditional commands between the WRITE and READ instructions is not recommended due to the possibility of software bugs.

It is important that the WRITE and READ commands be alternately executed. A WRITE instruction has no effect unless the results of the previous WRITE have already been read. Once data has been read, the ADC-908 is internally reset. In other words, two or more READ operations cannot be used in

succession, since only the first READ will produce valid data. A new conversion must be started using WRITE, and the conversion must be completed, before a new READ will produce valid data.

TABLE 1: Truth Table, Static RAM Mode

INPUTS		OUTPUTS		ADC-908 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB7-DB0	
L	H	H	HIGH-Z	Start Convert (Write Cycle)
L	$\downarrow$	H	HIGH-Z to DATA	Read Data (Read Cycle)
L	$\uparrow$	H	DATA to HIGH-Z	Reset Converter
H	X (Note 1)	X	HIGH-Z	No Effect (Not Selected)
L	H	L	HIGH-Z	No Effect (Converter Busy)
L	$\downarrow$	L	HIGH-Z	No Effect (Converter Busy)
L	$\uparrow$ (Note 1)	L	HIGH-Z	Conversion Error Not Allowed

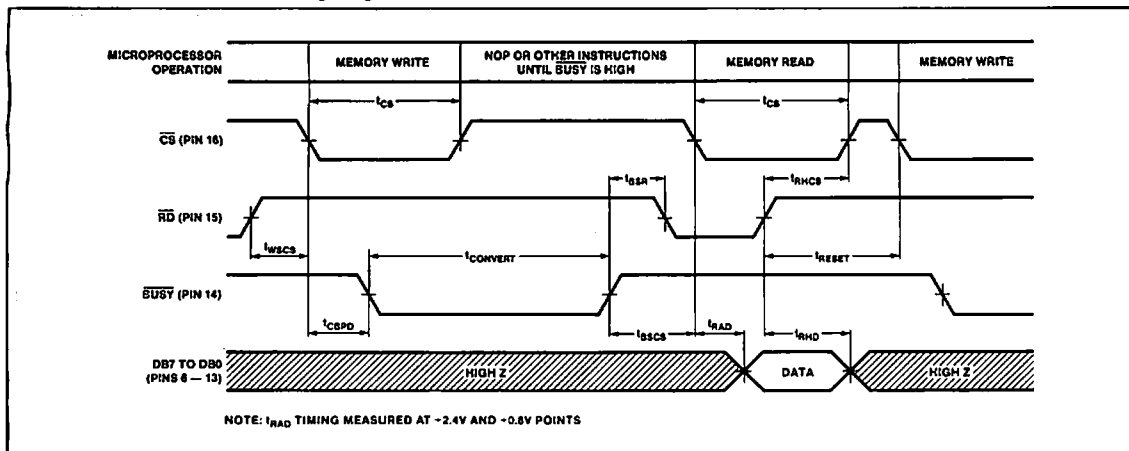
NOTE 1: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

OPERATING DESCRIPTION: ROM MODE

In ROM mode, input $\overline{CS}$ is tied LOW, and input $\overline{RD}$ is derived from the ADC-908 address decoder. To satisfy timing, it is recommended that the decoder be enabled by a system MEMRD (8080), VMA (6800), or similar strobe. (See Figure 3.)

In ROM mode, data is read by executing a READ instruction to the ADC-908 address. At the conclusion of the READ instruction, the ADC-908 automatically resets itself and then proceeds to perform a new data conversion. Output $\overline{BUSY}$ is LOW during conversion. A new READ instruction to the ADC-908 must not be executed until $\overline{BUSY}$ returns HIGH.

FIGURE 2: Static RAM Mode Timing Diagram





This requirement may be met by inserting NOP or other program instructions between consecutive READ operations. Conditional or branch instructions may be used, but keep in mind that data may become out-of-date if excessive time elapses between consecutive READ instructions.

TABLE 2: Truth Table, ROM Mode

INPUTS		OUTPUTS		ADC-908 OPERATION
CS	RD	BUSY	DB7-DB0	
L		H	HIGH-Z to DATA	Read Data
L			DATA to HIGH-Z	Reset and Start New Conversion
L		L	HIGH-Z	No Effect (Converter Busy)
L		L	HIGH-Z	Conversion Error Not Allowed

NOTE 1: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

OPERATING DESCRIPTION: SLOW-MEMORY MODE

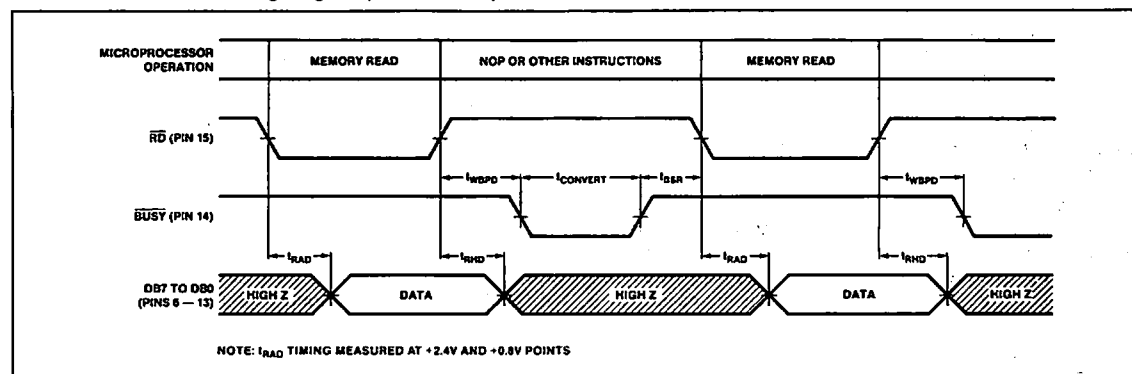
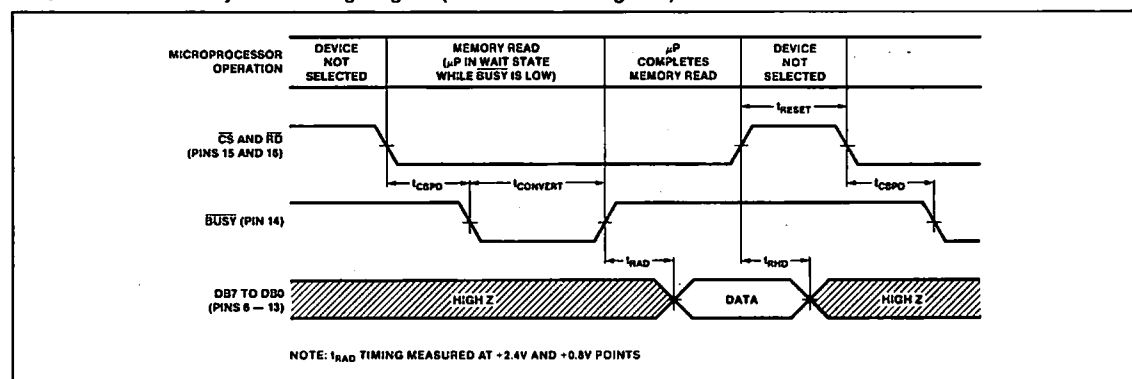
The slow-memory mode is intended for systems in which the ADC-908 $\overline{BUSY}$ output is used as an interrupt to force the

microprocessor into WAIT states during data conversion.

In slow-memory mode, inputs $\overline{CS}$ and $\overline{RD}$ are tied together. The common $\overline{RD}$ and $\overline{CS}$ signal is derived from the ADC-908 address decoder. To satisfy the timing requirements, it is advisable to latch the address using ALE (8085) or SYNC (8080). For 8080 or 8085-based systems, connect the microprocessor $\overline{READY}$ input to the ADC-908 $\overline{BUSY}$ output. (See Figure 4.)

TABLE 3: Truth Table, Slow-Memory Mode

INPUTS		OUTPUTS		ADC-908 OPERATION
CS & RD	BUSY	DB7-DB0		
H	H	HIGH-Z		No Effect (Not Selected)
		HIGH-Z		Start Conversion
L	L	HIGH-Z		Conversion in Progress. μP in WAIT State
L		HIGH-Z to DATA		Conversion Complete. Read Data
	H	DATA to HIGH-Z		Reset and Deselect Converter

FIGURE 3: ROM Mode Timing Diagram ($\overline{CS}$ Held LOW)FIGURE 4: Slow-Memory Mode Timing Diagram ($\overline{CS}$ and $\overline{RD}$ Tied Together)

Do not execute a **WRITE** instruction at the ADC-908 address when in slow-memory mode, since bus conflicts will arise. In some architectures, an accidental **WRITE** instruction may be locked out in hardware, by proper strobing of the ADC-908 address decoder.

INITIALIZATION

In all operating modes, the ADC-908 is initialized by executing a **READ** instruction to the ADC-908 address. The data obtained should be ignored.

CLOCK OSCILLATOR

The ADC-908 may be used with its internal asynchronous clock oscillator. An external resistor and capacitor are required. Typical values are $R = 43k\Omega$ and $C = 100pF$, for conversion times in the $6\mu s$ range. For applications in which the fastest conversion times are required, an external clock is recommended. The external clock must be gated by the use of a 74125-type three-state buffer, with an output pullup resistor. Optimum conversion accuracy is obtained when **CS** goes **LOW** on a positive clock edge. The maximum external clock frequency is 1.35MHz. (See Figure 5 and 6.)

REFERENCE VOLTAGE

A negative reference voltage must be applied to the ADC-908 V_{REF} input. Optimum full-scale accuracy is obtained using $-10.00V$, although V_{REF} may be $-5.00V$, $-10.24V$, or other voltages within its specified range.

Over the full temperature range, optimum gain accuracy is obtained when the input to the V_{REF} pin is from a low-impedance source. A resistor or trimmer may be used in series with the V_{REF} pin, but this trim technique is not as accurate as a low-impedance source. (See Figure 7.)

For a cost-effective $-10.00V$ or $-10.24V$ reference with excellent accuracy and low temperature coefficient, ask for PMI's REF-08. Consult your sales representative for availability.

FIGURE 5: Using the Internal Clock Oscillator

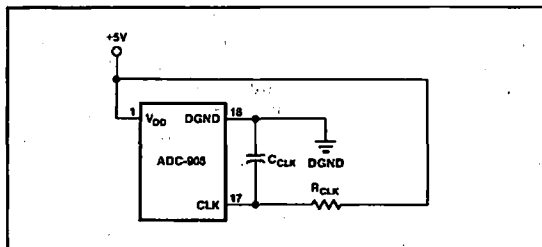


FIGURE 6: Using an External Clock

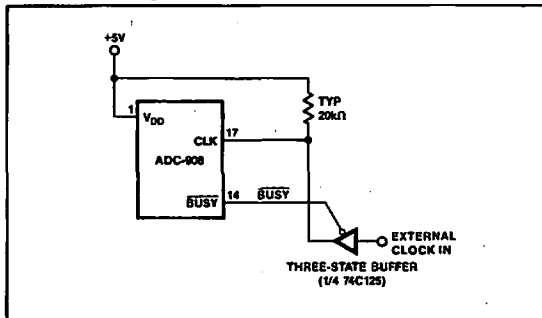
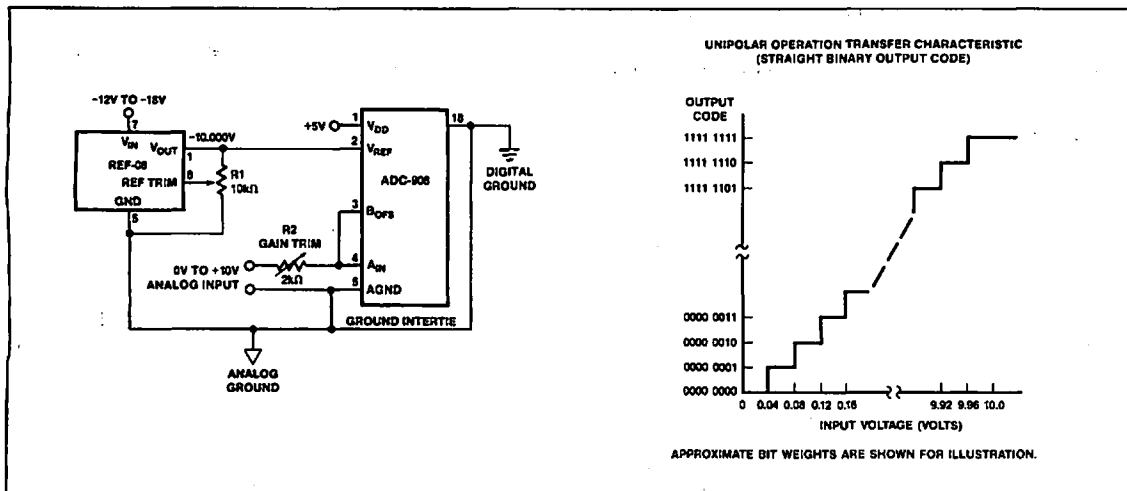


FIGURE 7: Unipolar Operation



ANALOG INPUT VOLTAGE

The ADC-908 unipolar operation is obtained when the analog input voltage is between 0V and $|V_{REF}|$. With the A_{IN} and B_{OFS} pins tied together, input 0V will correspond to code 0000 0000, and input full-scale will correspond to code 1111 1111.

Bipolar operation is obtained by using the B_{OFS} input to offset the A_{IN} input voltage. For example, with $V_{REF} = -10V$, an offset voltage of +10V may be applied to B_{OFS} . The analog signal range will then be $-10V$ to $+10V$ at A_{IN} . Code 0000 0000 will correspond to $-10V$, and positive full scale will be code 1111 1111. Calibration may be performed using trimmers in series with A_{IN} and B_{OFS} . (See Figure 8).

Another method of obtaining bipolar operation is to use an op-amp with gain = $-1/2$, to sum the analog signal with the reference voltage. With a $-10V$ reference and $-10V$ to $+10V$ analog signal, the op amp output will then be 0V to $+10V$. This signal is then treated as an ordinary unipolar input to the ADC-908. With this arrangement, input $+10V$ corresponds to code 0000 0000, and negative full-scale corresponds to code 1111 1111.

UNIPOLAR BINARY OPERATION

Figure 7 shows the analog circuit connections for unipolar operation. The REF-08 supplies the necessary $-10V$ reference input.

Calibration for offset should be made before gain calibration is attempted.

Offset calibration must be performed in the signal conditioning circuitry which drives the A_{IN} input.

To adjust offset:

- 1) Apply $-39.1mV$ (1 LSB) to the input of the buffer amplifier driving A_{IN} .
- 2) While performing continuous conversions, adjust the buffer amplifier's offset adjustment potentiometer until DB7 to DB1 are LOW and DB0 (LSB) flickers.

Following offset calibration, full scale gain can be calibrated:

- 1) Apply $-9.961V$ to the input of the buffer amplifier.

- 2) While performing continuous conversions, adjust the reference trim pot until DB7 to DB1 are HIGH, and DB0 (LSB) flickers.

BIPOLAR OPERATION

Offset Binary—Figure 8 shows a circuit for offset binary bipolar operation. Offset correction should be made at the buffer amplifier driving A_{IN} . Gain error correction should be accomplished by adjusting V_{REF} .

To calibrate this circuit:

- 1) Adjust R1 until $V_{REF} = -10.00V$.
- 2) Adjust R2 and R3 to their mid-points.
- 3) Apply $+10.000V$ to the input buffer amplifier.
- 4) While performing continuous conversions, adjust R2 until DB7 to DB1 are LOW and DB0 (LSB) flickers.
- 5) Ground the input of the input buffer circuit.
- 6) While performing continuous conversions, adjust R3 until the ADC's output code flickers between 0111 1111 and 1000 0000.
- 7) Apply $-10.000V$ to the signal input.
- 8) While performing continuous conversions, adjust R1 until DB7 to DB1 are LOW and the DB0 (LSB) flickers.
- 9) Apply $+9.922V$ to the signal input.
- 10) If the ADC output code is not 1111 1110 ± 1 bit, repeat the calibration procedure, omitting step 1.

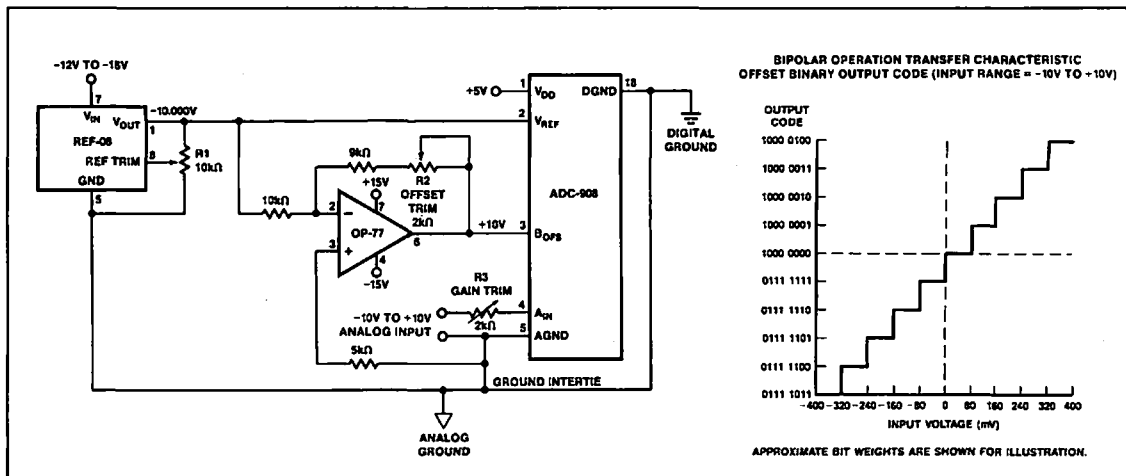
Complementary Offset Binary—Figure 9 shows a complementary offset binary circuit. In this bipolar mode, the $+10V$ to $-10V$ analog input is conditioned to a 0 to $+10V$ signal range for normal unipolar conversion.

In calibrating this circuit, adjust offset before gain.

Offset Adjustment:

- 1) Adjust R1 until $V_{REF} = -10.000V$.
- 2) Adjust R3 to its mid-point.
- 3) Adjust R2 until its tap is at 0V.
- 4) Ground the analog input.
- 5) While performing continuous conversions, adjust R2 until the ADC output flickers between 0111 1111 and 1000 0000.

FIGURE 8: Offset Binary Operation



Gain Adjustment:

- 1) Apply +9.922V across the analog input.
- 2) While performing continuous conversions, adjust R3 until DB7 to DB1 are HIGH and DB0 (LSB) flickers.

DIGITAL CONSIDERATIONS

Control Timing—Fresh data from a recent conversion must be read before beginning a new conversion. Following the data READ, as RD goes HIGH, it resets the SAR and clears the data from the previous conversion.

The timing restrictions detailed in the interface timing diagrams must be observed to prevent the ADC-908 from changing interface modes. For example, if CS is held LOW too long while in RAM mode, the converter will change to ROM mode and initiate a new conversion.

Logic Deglitching—Unrelated activity on the address bus may cause unexpected glitch inputs to the ADC. The glitches may cause unwanted READs, resets, or conversions. In ROM or RAM modes, these may be avoided by gating the address decode logic with RD or WR (8080) or VMA (6800). In slow-memory mode, ALE (8085) or SYNC (8080) may be used to latch the address.

Initialization—Following power-up, the SAR is in an unknown state. Executing a memory READ (disregard the data) will reset the ADC.

ANALOG CONSIDERATIONS

Analog Input Impedances—Low impedance sources must be used to drive the V_{REF} , A_{IN} , and B_{OFS} inputs. Excessive source

impedances may cause errors due to the loading effects of the inputs' finite impedances.

Ground Management—AGND and DGND pins should be connected at or near the ADC to minimize noise effects. If the two grounds cannot be connected near the ADC, the grounds should be clamped with back-to-back Schottky diodes between the AGND and DGND pins.

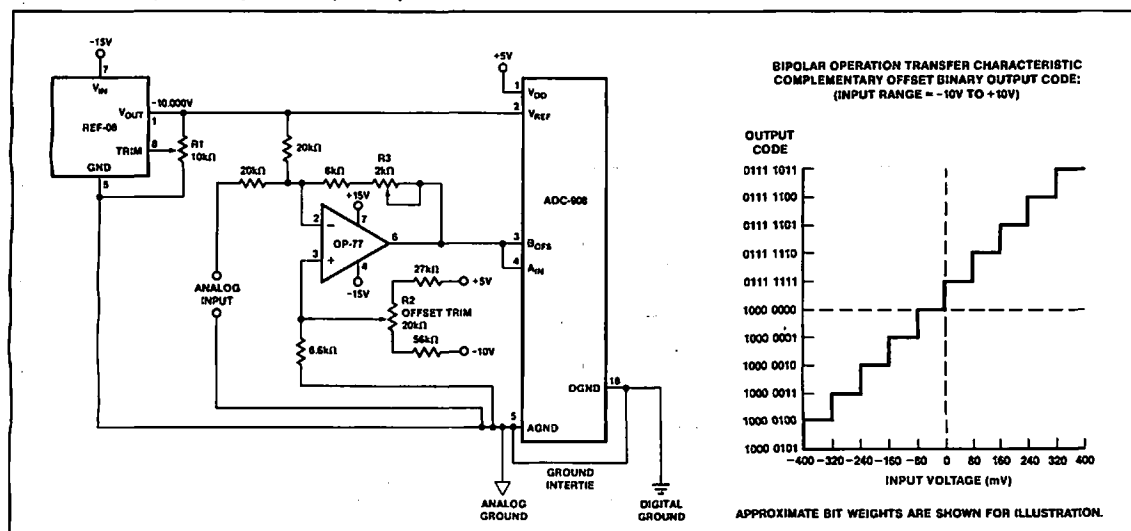
Offset Correction—Conversion offset errors may be corrected by counter-offsetting the buffer amplifier driving A_{IN} . This offset correction may be accomplished by applying a correction current to the buffer's summing junction or by tapping a voltage divider sitting between V_{DD} and V_{REF} , and applying this tap voltage to the noninverting input of the buffer.

Ratiometric Operation—The R-2R type DAC in the ADC-908 permits ratiometric operation of the ADC. Performance degradation may, however, occur as V_{REF} varies from $-10.000V$. This decrease in performance is due to comparator limitations including offset-voltage, gain, and input noise.

The ADC-908 uses the reference as a power supply for the comparator to increase speed and accuracy. Reference voltages of a magnitude less than $-9V$ must be avoided for accurate comparator operation. For best accuracy, the use of a $0.1\mu F$ bypass capacitor from V_{REF} (Pin 2 to AGND) is recommended.

Power Supply Bypassing—For best accuracy, V_{DD} (Pin 1) should be bypassed to AGND with a $0.1\mu F$ capacitor.

FIGURE 9: Complementary Offset Bipolar Operation





ADC-910

MICROPROCESSOR-COMPATIBLE 10-BIT HIGH-SPEED
A/D CONVERTER

Precision Monolithics Inc.

FEATURES

- Includes Clock, Reference, 3-State Buffered Outputs
- Fast Conversion Time 6 μ s
- Four Input Ranges ... +/-2.5V, +/-5.0V, +5.0V and +10.0V
- 1/2 LSB INL
- No Missing Codes Over Temperature
- Low ESD Sensitivity Due to Rugged Bipolar Processing
- Software Programmable Unipolar/Bipolar
- Easily Interfaced to 8 and 16-Bit μ P Bus

ORDERING INFORMATION†

PMI MODEL NO.	TEMPERATURE RANGE
ADC910AT*	
ADC910BT*	-55°C/+125°C
ADC910ET	
ADC910FT	-25°C/+85°C
ADC910GT	
ADC910HT	0°C/+70°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

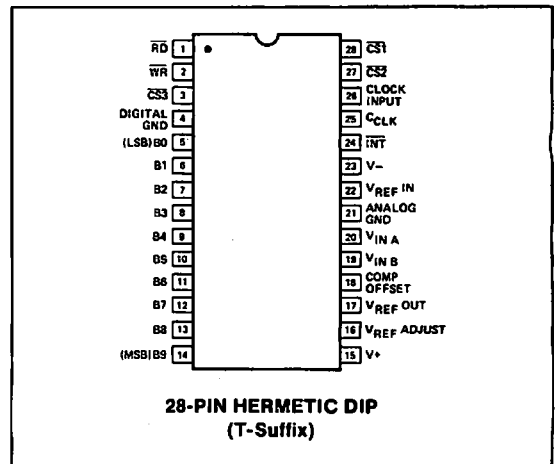
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

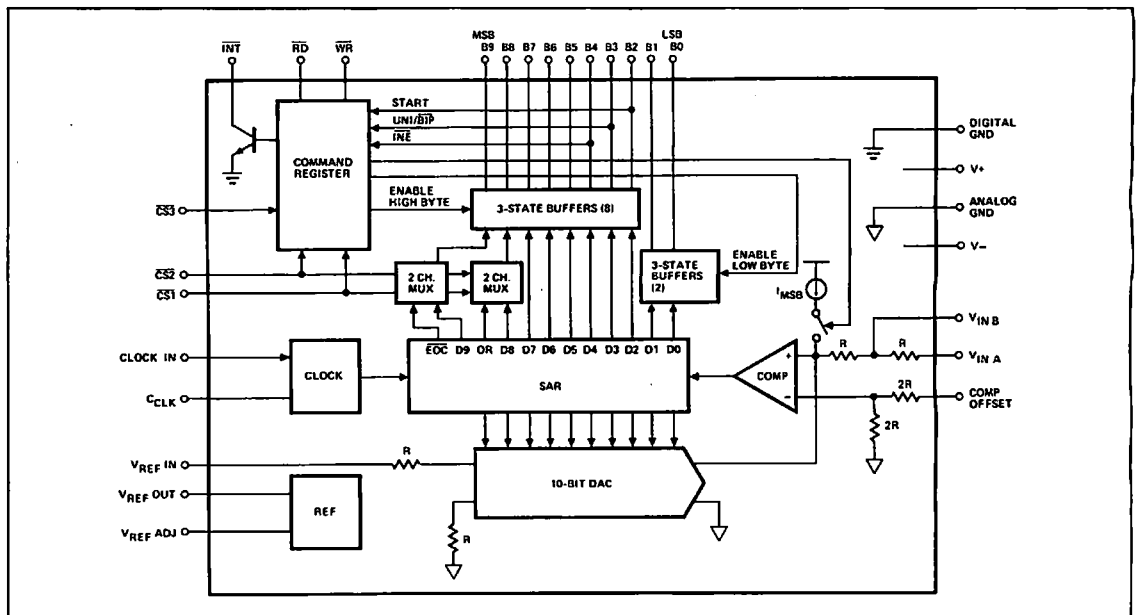
The ADC-910 is a 10-bit A/D converter designed specifically for interfacing with microprocessors. 3-state data outputs allow direct connection to an 8-bit data bus in an MSB byte of

8 bits and an LSB byte of 2 bits. A command register with read/write inputs and 3 Chip Select inputs to control the 10 data lines is included. Interrupt enable, start conversion and bipolar/unipolar mode selection are controlled by the data bus. The use of high-speed Linear Differential Logic results in fast (6 μ s) conversion time and low power dissipation.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC



**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature Range	
ADC-910AT/BT	-55°C to +125°C
ADC-910ET/FT	-25°C to +85°C
ADC-910GT/HT	0°C to +70°C
Maximum Junction Temperature (T _J)	175°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	1000mW
Derate Above 100°C	13.3mW/°C
Lead Temperature (Soldering, 60 sec)	300°C

Supply Voltage (V ₊)	6V
Supply Voltage (V ₋)	6V
V ₊ to V ₋	12V
Logic Inputs	+6V, -0.3V
Logic Outputs (in 3-state)	+6V, -0.3V
V _{INA}	15V
V _{INB}	7.5V
Reference Inputs	3.0V
Digital Ground to Analog Ground Voltage	0.5V

ELECTRICAL CHARACTERISTICS at V₊ = 5V, V₋ = -5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = -55°C to +125°C apply for ADC-910AT/BT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910AT			ADC-910BT			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Integral Nonlinearity (Note 3)	INL	T _A = 25°C	—	—	1/2	—	—	1	LSB
		T _A = Full Temp. Range	—	—	3/4	—	—	1	
Gain Drift (Note 1)	TCG _{FS}	External Reference	—	—	25	—	—	30	ppm FS/°C
		Internal Reference	—	—	40	—	—	50	
Reference Line Regulation		4.75V < V ₊ < 5.25V	—	—	500	—	—	600	μV/V
Positive Supply Current	I ₊		—	30	40	—	30	40	mA
Negative Supply Current	I ₋		—	50	60	—	50	60	mA

ELECTRICAL CHARACTERISTICS at V₊ = 5V, V₋ = -5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = -25°C to +85°C apply for ADC-910ET/FT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910ET			ADC-910FT			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Integral Nonlinearity (Note 3)	INL	T _A = 25°C	—	—	1/2	—	—	1	LSB
		T _A = Full Temp. Range	—	—	1/2	—	—	1	
Gain Drift (Note 1)	TCG _{FS}	External Reference	—	—	20	—	—	25	ppm FS/°C
		Internal Reference	—	—	35	—	—	45	
Reference Line Regulation		4.75V < V ₊ < 5.25V	—	—	500	—	—	600	μV/V
Positive Supply Current	I ₊		—	30	40	—	30	40	mA
Negative Supply Current	I ₋		—	50	60	—	50	60	mA

ELECTRICAL CHARACTERISTICS at V₊ = 5V, V₋ = -5V, V_{REF} = 2.5V, f_{CLK} = 0.5MHz; T_A = 0°C to +70°C apply for ADC-910GT/HT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910GT			ADC-910HT			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Integral Nonlinearity (Note 3)	INL	T _A = 25°C	—	—	1/2	—	—	1	LSB
		T _A = Full Temp. Range	—	—	3/4	—	—	1	
Gain Drift (Note 1)	TCG _{FS}	External Reference	—	10	—	—	10	—	ppm FS/°C
		Internal Reference	—	25	—	—	25	—	
Reference Line Regulation		4.75V < V ₊ < 5.25V	—	300	—	—	300	—	μV/V
Positive Supply Current	I ₊		—	30	—	—	30	—	mA
Negative Supply Current	I ₋		—	50	—	—	50	—	mA

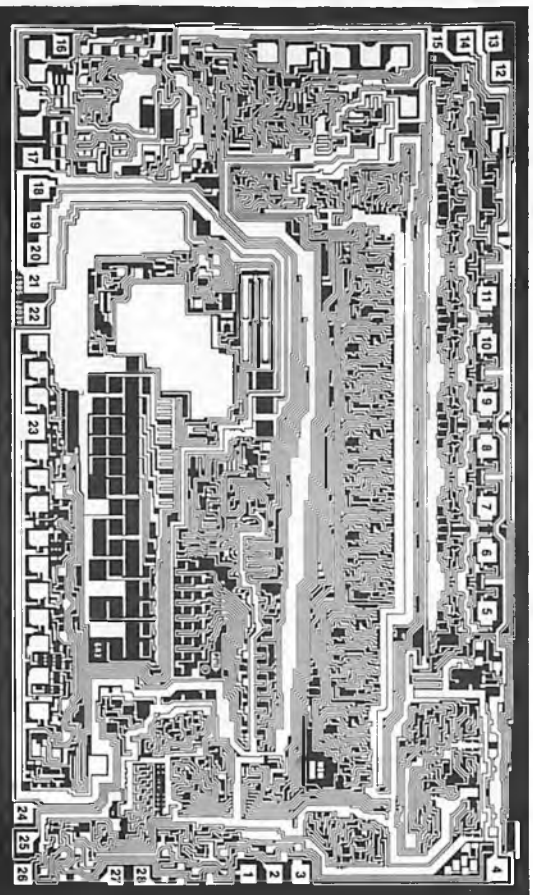
ELECTRICAL CHARACTERISTICS at $V_+ = 5V$, $V_- = -5V$, $V_{REF} = 2.5V$, $f_{CLK} = 0.5MHz$; $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-910AT/ET/GT			ADC-910BT/FT/HT			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution	N	$T_A = \text{Full Temp. Range}$	10	—	—	10	—	—	Bits
Resolution for which No Missing Codes Guaranteed		$T_A = \text{Full Temp. Range (Notes 2, 3)}$	10	—	—	10	—	—	Bits
Gain Error	G_{FSE}	$V_{REF} = 2.500V \text{ (Notes 2, 3)}$	—	—	4	—	—	6	LSB
Unipolar Mode Offset Error	V_{ZSE}	$T_A = \text{Full Temp. Range}$	—	—	1/2	—	—	1	LSB
Bipolar Mode Offset Error	V_{OSE}		—	—	1	—	—	1.5	LSB
Bipolar Mode Zero- Scale Offset Drift	TCV_{ZS}	$T_A = \text{Full Temp. Range (Note 1)}$	—	—	1	—	—	1.5	LSB
Analog Input Impedance	$R_{IN A}$	Pin 20	3.5	5	8	3.5	5	8	k Ω
Analog Input Impedance	$R_{IN B}$	Pin 19	1.75	2.5	4	1.75	2.5	4	k Ω
Reference Input Resistance	R_{REF}	Pin 22	1.75	2.5	3.5	1.75	2.5	3.5	k Ω
Reference Voltage Output	V_{REFOUT}	Pin 17, Untrimmed	2.45	2.50	2.55	2.45	2.50	2.55	V
Reference Voltage Trim Range		$R_T = 10k\Omega$	± 40	—	—	± 40	—	—	mV
Reference Output Load Regulation		$1mA < I < 5mA$, $T_A = \text{Full Temp. Range}$	—	—	1.5	—	—	1.5	mV/mA
Positive Power Supply Sensitivity	$+P_{SS}$	4.75V to 5.25V	—	—	1/2	—	—	1/2	LSB
Negative Power Supply Sensitivity	$-P_{SS}$	-4.75V to -5.25V	—	—	1/2	—	—	1/2	LSB
Conversion Time	T_C	$f_{CLK} = 1MHz \text{ (Note 4)}$	—	—	6	—	6	—	μs
Conversion Time	T_C	$f_{CLK} = 0.5MHz \text{ (Note 5)}$	—	—	12	—	12	—	μs
Digital Input High	V_{INH}	$T_A = \text{Full Temp. Range}$	2.0	—	—	2.0	—	—	V
Digital Input Low	V_{INL}	$T_A = \text{Full Temp. Range}$	—	—	0.8	—	—	0.8	V
Digital Input Current	I_{INH}	$T_A = \text{Full Temp. Range}$	—	0.4	1	—	0.4	1	μA
Digital Input Current	I_{INL}	$T_A = \text{Full Temp. Range}$	—	10	20	—	10	20	μA
Digital Output High	V_{OH}	$I_{OH} = -400\mu A$, $T_A = \text{Full Temp. Range}$	2.4	3.7	—	2.4	3.7	—	V
Digital Output Low	V_{OL}	$I_{OL} = 1.6mA$, $T_A = \text{Full Temp. Range}$	—	0.1	0.4	—	0.1	0.4	V
Digital Output Current	I_{OH}	$V_{OH} = 2.4V$	-400	—	—	-400	—	—	μA
Digital Output Current	I_{OL}	$V_{OL} = 0.4V$	—	—	1.6	—	—	1.6	mA
Three-State Output Leakage	I_{OZ}	$T_A = \text{Full Temp. Range}$	—	5	10	—	5	10	μA

NOTES:

1. Change in $25^\circ C$ value from $25^\circ C$ to T_{Min} or T_{Max} .
2. Tested in the 5V unipolar mode at $6\mu s$ conversion time.
3. Tested in the $\pm 5V$ bipolar mode at $12\mu s$ conversion time.
4. Applies to 5V input unipolar operation; see Figure 1 for connections.
5. Applies to 10V input unipolar operation, and $\pm 5V/\pm 10V$ input bipolar operation; see Figure 1 for connections.

DICE CHARACTERISTICS



DIE SIZE 0.131 × 0.221 inch, 28,951 sq. mils
(3.33 × 5.61 mm, 18.68 sq. mm)

1. RD
2. WR
3. CS₃
4. DIGITAL GND
5. B0 (LSB)
6. B1
7. B2

8. B3
9. B4
10. B5
11. B6
12. B7
13. B8
14. B9 (MSB)
15. V₊
16. V_{REF} ADJUST
17. V_{REF} OUT
18. COMP OFFSET
19. V_{IN} B
20. V_{IN} A
21. ANALOG GND

22. V_{REF} IN
23. V₋
24. INT
25. CLK
26. CLOCK INPUT
27. CS₂
28. CS₁

For additional DICE ordering information, refer to 1988 Data Book, Section 2.



WAFER TEST LIMITS at $V^+ = 5V$, $V^- = -5V$, $V_{REF} = 2.5V$, and $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	ADC-910G LIMIT	UNITS
Integral Nonlinearity	INL		1	LSB MAX
Differential Nonlinearity	DNL		1	LSB MAX
Gain Error	G_{FSE}	$V_{REF} = 2.500V$	6	LSB MAX
Unipolar Mode Offset Error	V_{ZSE}		1	LSB MAX
Analog Input Impedance	$R_{IN A}$	Pin 20	3.5/8	k Ω MIN/MAX
Reference Input Resistance	R_{REF}	Pin 22	1.75/4	k Ω MIN/MAX
Reference Voltage Output	V_{REFOUT}	Pin 17, Untrimmed	2.45/2.55	V MIN/MAX
Positive Power Supply Sensitivity	$+P_{SS}$	4.5V to 5.5V	1/2	LSB MAX
Negative Power Supply Sensitivity	$-P_{SS}$	-4.5V to -5.5V	1/2	LSB MAX
Digital Input High	V_{INH}		2.0	V MIN
Digital Input Low	V_{INL}		0.8	V MAX
Digital Input Current	I_{INH} I_{INL}		1 20	μA MAX
Digital Output High	V_{OH}	$I_{OH} = -400\mu A$	2.4	V MIN
Digital Output Low	V_{OL}	$I_{OL} = 1.6mA$	0.4	V MAX
Digital Output Current	I_{OH} I_{OL}	$V_{OH} = 2.4V$ $V_{OL} = 0.4V$	-400 1.6	μA MIN mA MAX
Three-State Output Leakage	I_{OZ}		10	μA MAX
Positive Supply Current	I^+		40	mA MAX
Negative Supply Current	I^-		60	mA MAX

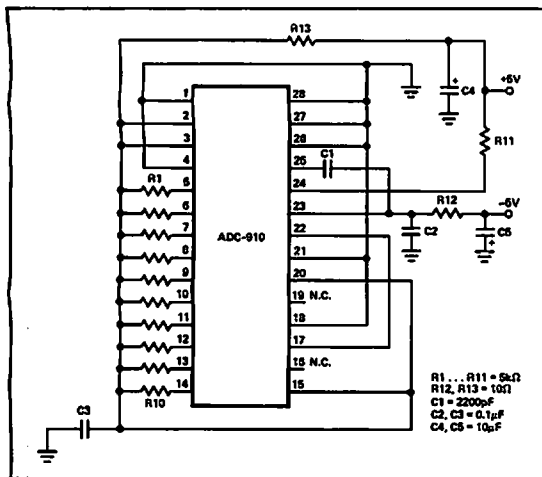
NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V^+ = 5V$, $V^- = -5V$, $V_{REF} = 2.5V$, and $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	ADC-910G TYPICAL	UNITS
Conversion Time	T_C	$f_{CLK} = 1MHz$, 5V Unipolar Mode	6	μs
		$f_{CLK} = 0.5MHz \pm 5V$ Bipolar Mode	12	

BURN-IN CIRCUIT



APPLICATIONS INFORMATION

CIRCUIT OPERATION (Refer to the Simplified Schematic)

The ADC-910 uses a successive approximation type A/D conversion routine. When a start command is received by the command register, the SAR, DAC and comparator begin a bit-by-bit trial against the analog input voltage. When all ten bits have been tried, the ten data outputs of the SAR will contain a 10-bit digital representation of the analog input voltage.

When the conversion is complete, a read command and a chip selection will output the data through the 3-state output buffers. Selecting CS1 will output the eight MSBs (the high byte) and selecting CS2 will output the two LSBs (the low byte). Selecting both CS1 and the CS2 will cause all ten data bits to be output through the 3-state output buffers.

When the conversion is complete, the SAR sends an end of conversion (EOC) signal to the command register, which

turns on the interrupt output open-collector NPN transistor (INT), providing the interrupt disable bit (INE) is set to "0". The EOC signal is also multiplexed into the input of the 3-state buffer for bit 9 (B9). Also, at this time, the overrange signal appears at the SAR output and is multiplexed into the input of the 3-state buffer for bit 8 (B8). These two bits of information comprise the status register, which is multiplexed to the data bus with a read command and a selection of CS3.

Unipolar/bipolar mode selection and the enabling/disabling of the interrupt output is done when the start of conversion command is entered. In the unipolar mode, the I_{MSB} current source is turned off. For bipolar mode operation, the I_{MSB} current source is applied to the summing mode of the comparator. This provides the proper offset of I_{MSB} to do a bipolar conversion.

BASIC CONNECTIONS (Refer to Figure 1)

Power Supply Connections: The ADC-910 is operated on ± 5 volt power supplies. +5 volts is applied to pin 15 and -5 volts is applied to pin 23. These lines should be bypassed near the device with a $0.1\mu\text{F}$ capacitor in parallel with a large value capacitor such as $10\mu\text{F}$.

Analog and Digital Ground: Separate analog and digital grounds are provided to maintain optimum noise rejection. Care should be maintained to insure that digital switching noise is not introduced into the analog ground line. This can be accomplished by making the final ground point as close (physically and electrically) as possible to the analog ground pin of the ADC-910.

Analog Inputs: There are two analog voltage inputs to the ADC-910. $V_{IN\ A}$ (pin 20) accepts input signals between 0 volts and +10 volts in the unipolar mode and between -5 volts and +5 volts in the bipolar mode. $V_{IN\ B}$ (pin 19) accepts input signal levels between 0 volts and +5 volts in the unipolar mode and between -2.5 volts and +2.5 volts in the bipolar mode. The input resistance is nominally $5k\Omega$ for $V_{IN\ A}$ and $2.5k\Omega$ for $V_{IN\ B}$. The comparator offset pin (pin 18) is left open when using $V_{IN\ A}$, and is tied to analog ground when using $V_{IN\ B}$.

FIGURE 1: Basic Connections

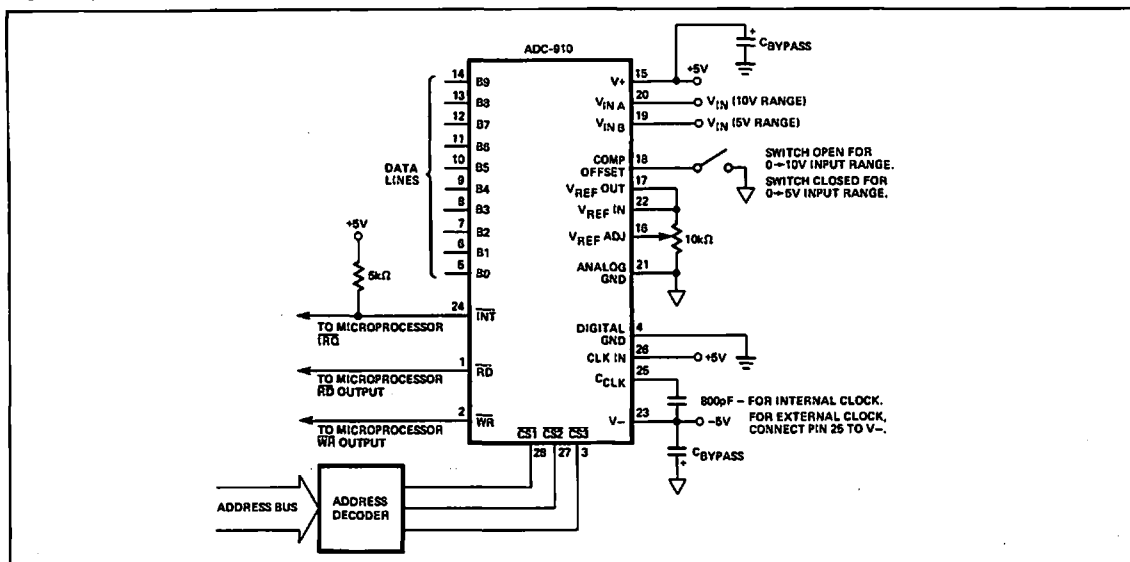


FIGURE 2: Start Conversion and Operating Mode Selection (Write Mode $\overline{WR}$ = "Low", CS3 = "Low")

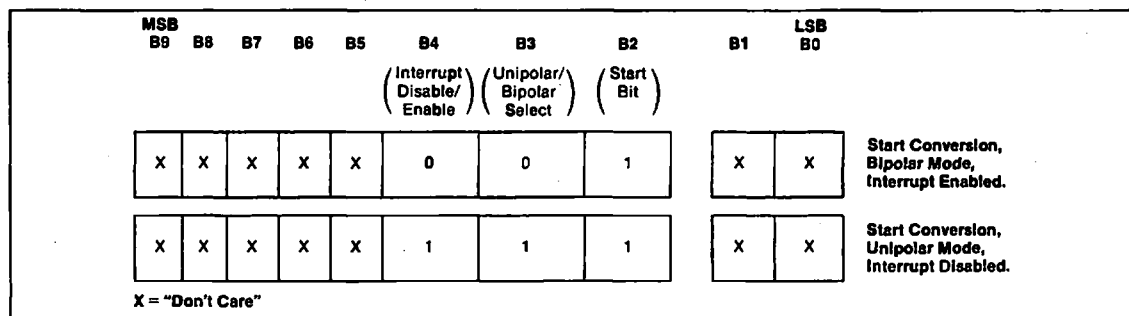


FIGURE 3: Reading Data and Status
(Read Mode $\overline{RD}$ = "Low")

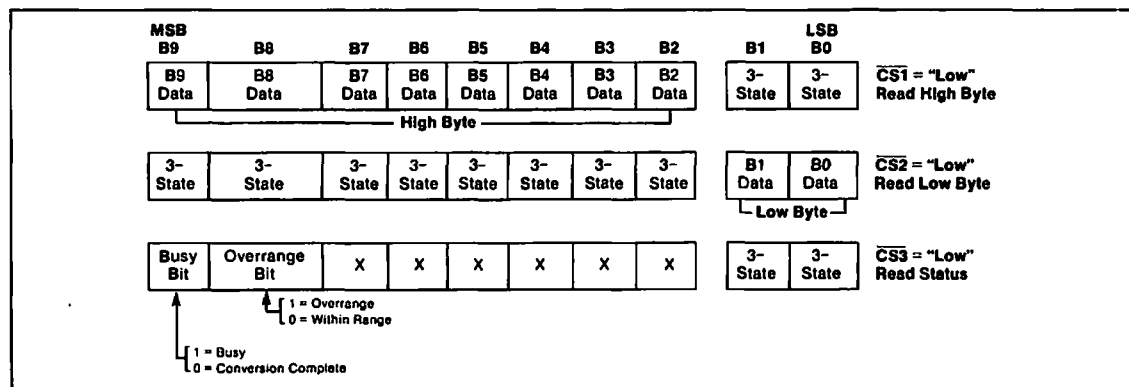
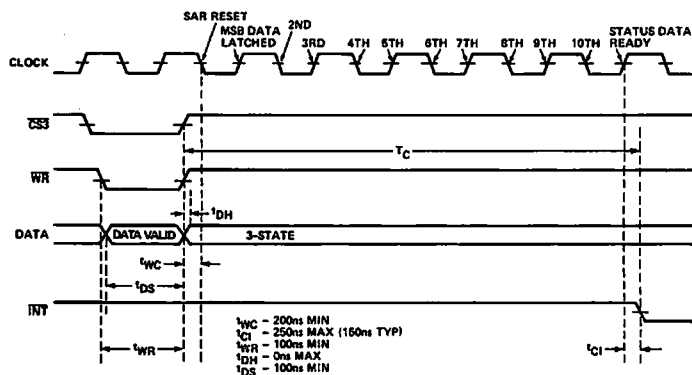
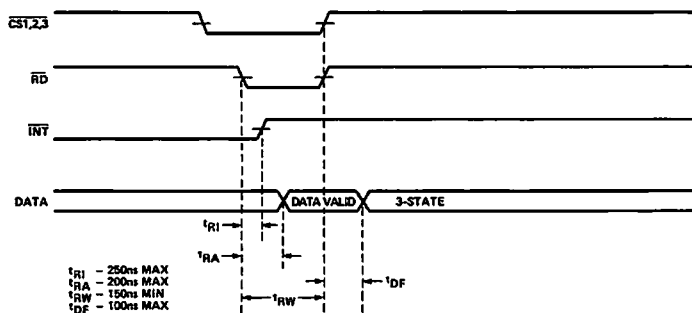


FIGURE 4: ADC-910 Timing Diagrams

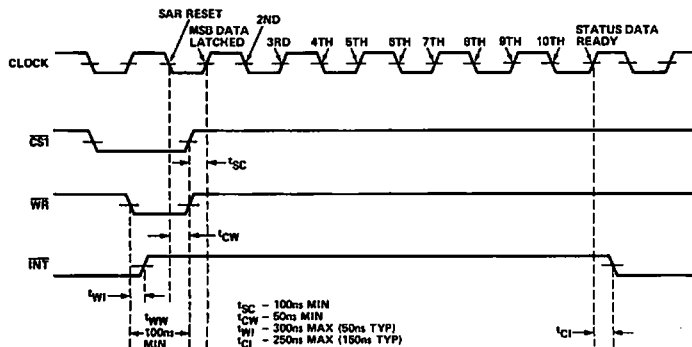
(a) Write Cycle



(b) Read Cycle



(c) Stand-Alone



Voltage Reference: The voltage reference for the ADC-910 is nominally +2.5 volts. To use this internal reference, the reference output pin (pin 17) should be tied to the reference input pin (pin 22). Adjustment of the reference voltage may be done by applying a 10k Ω trimmer between the reference

output and analog ground with the center tap wiper tied to the reference adjust pin (pin 16).

To use an external reference with the ADC-910, simply apply it to the V_{REF} input pin (pin 22). This voltage should be bypassed to analog ground with a 0.01 μ F capacitor.

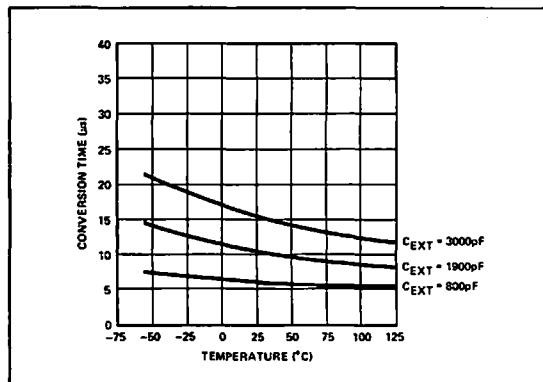


Clock: For internal clock operation, the external capacitor (C_{CLK}) sets the conversion rate. The conversion rate graph provides the relationship of C_{CLK} and temperature to conversion rate. The C_{CLK} capacitor is connected between C_{CLK} (pin 25) and the V^- supply (pin 23), see Figure 1. The clock input (pin 26) is connected to the V^+ supply (pin 15). Internal clock operation exhibits a conversion time variation from device to device for a given C_{CLK} , due to capacitor and internal resistor tolerances of the basic R-C oscillator. For operation at the upper frequencies of 0.5 and 1MHz, an external clock input is recommended.

For external clock operation, no clock capacitor is required. The C_{CLK} pin (pin 25) should be tied to the -5 volt supply and the external clock is applied to the clock input (pin 26). 1.0MHz clock maximum may be used. This will result in a $6\mu s$ conversion time. Slower clock rates will result in slower conversion speeds.

$$\text{Conversion time} \approx 6 \times \frac{1}{f_{CLK}}$$

Conversion time (T_C) also depends on user supplied timing relationship between positive $\overline{WR}$ edge and negative clock edge used to reset the SAR. See Figure 4(a) t_{WC} parameter.



CHIP SELECT, READ AND WRITE INPUTS

(Refer to Figure 2)

Start Commands: To start a conversion the $\overline{WR}$ input (pin 2) must be held "low" while $\overline{CS3}$ (pin 3) is held "low" and a logic "high" is applied to bit 2 (pin 7). Another way to start a conversion is to hold $\overline{CS1}$ (pin 28) and $\overline{WR}$ (pin 2) "low" for a complete clock cycle.

Operating mode selection is done when the start command is applied. As with the start command, $\overline{WR}$ and $\overline{CS3}$ are held "low". A logic "high" applied to bit 4 (pin 9) disables the interrupt and a logic "low" enables the interrupt. A logic "high" applied to bit 3 (pin 8) selects unipolar mode and a logic "low" selects bipolar-mode operation.

READING DATA AND CONVERSION STATUS

(Refer to Figure 3)

Data can be read in two ways: a single 10-bit word or in a 8-bit "high byte" with a 2-bit "low byte". When interfacing to a

16-bit bus, single 10-bit word reading is possible. When using an 8-bit data bus, the "high byte" and "low byte" can be multiplexed onto a single 8-bit bus as indicated in Figure 5.

To read all 10 bits at once, the $\overline{RD}$ (pin 1), $\overline{CS1}$ (pin 28) and $\overline{CS2}$ (pin 27) are all held "low". This turns on 3-state output buffers and all data bits can be read.

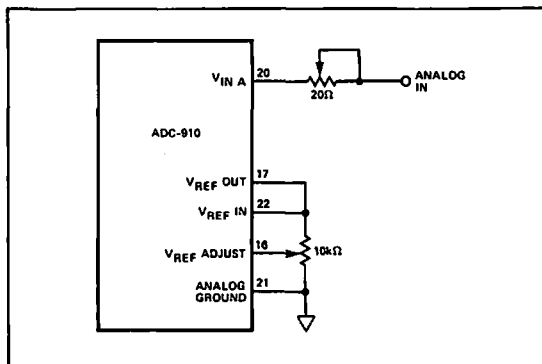
To read the 8-bit "high byte", the $\overline{RD}$ (pin 1) and $\overline{CS1}$ (pin 28) lines are held "low".

To read the 2-bit "low byte", the $\overline{RD}$ and $\overline{CS2}$ lines are held "low".

Included on the ADC-910 is a 2-bit status register which is multiplexed onto the data bus on lines B9 and B8.

To read the status register, $\overline{RD}$ (pin 1) and $\overline{CS3}$ are held "low". End of conversion (EOC) is indicated by a "low" bit 9 (pin 14) and overrange (OR) is indicated by a "high" in bit 8 (pin 13).

FIGURE 5: Calibration Circuit



CALIBRATION (Refer to Figure 5)

Unipolar Mode: To adjust out gain error, a trimmer may be inserted in series with the analog input voltage input. Assuming a 2.500 volt reference is applied at the reference input, gain error trimming is accomplished by adjusting the input trimmer so that the final digital output code transition occurs for an input voltage of $V_A = 9.985$ volts (this is the transition from 1111 1111 10 to 1111 1111 11). When using the internal reference or an adjustable external reference, gain error trimming may be accomplished by adjusting the reference voltage until the final digital output code transition occurs at $V_A = 9.985$ volts.

Bipolar Mode: To trim out offset error, set series trimmer (if used) to 0Ω and tie $V_{IN A}$ to analog ground. Adjust V_{REF} to just beyond the major carry transition (that point where the digital output code changes from 0111 1111 11 to 1000 0000 00).

To trim out gain error, tie $V_{IN A}$ to voltage source. Adjust the series trimmer so that the final digital output code transition (from 1111 1111 10 to 1111 1111 11) occurs at an input voltage of +4.9902V.

DRIVING THE ANALOG INPUT

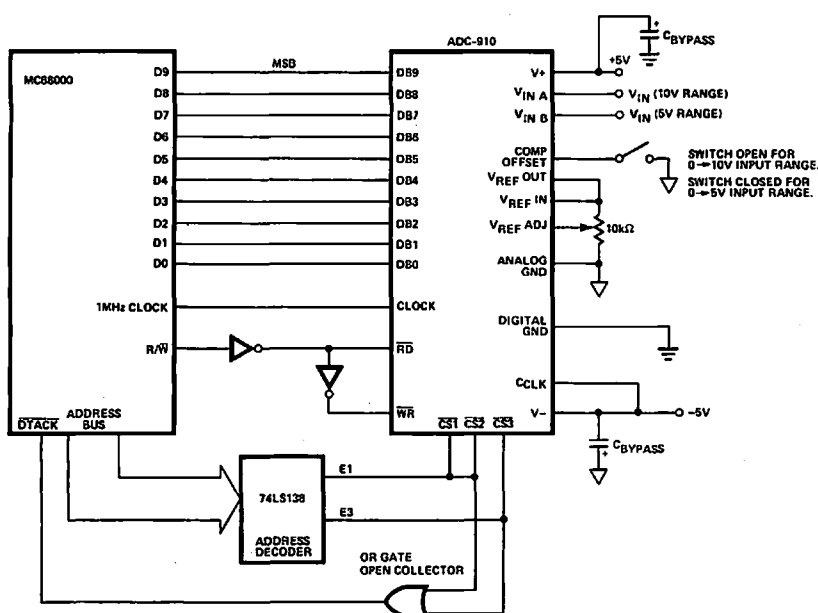
To insure 10-bit accuracy the input to the ADC-910 must be driven by a source which has an output impedance of less than 0.5 ohms at 1MHz.

INTERFACING THE ADC-910 TO THE MC68000

(Refer to Figure 6)

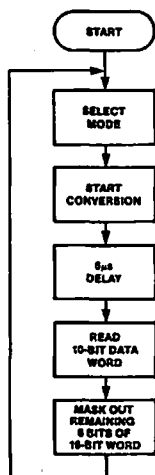
An example of a direct connection to a 16-bit data bus is shown in Figure 6. The 10-bit output of the ADC-910 is connected directly to the 10 least significant bits of the MC68000 data bus. In this example, a Motorola MC68000 Computer Board supports the 68000 μ P. A flow chart and assembly language program is shown below for a simplified 10-bit wide conversion.

FIGURE 6: ADC-910 Interface to MC68000 Computer Board

**INTERFACING THE ADC-910 TO THE 6502 μ P**

(Refer to Figure 7)

An example of direct connection to an 8-bit data bus is shown in Figure 7. Notice that the two least significant bits are connected to data bits B3 and B4. This allows a 10-bit data transfer over an 8-bit bus. In this example, a Synertek Systems SYM-1 Educational Computer Board supports the 6502 μ P. The flow charts and op codes for a variety of conversion exercises are shown below.

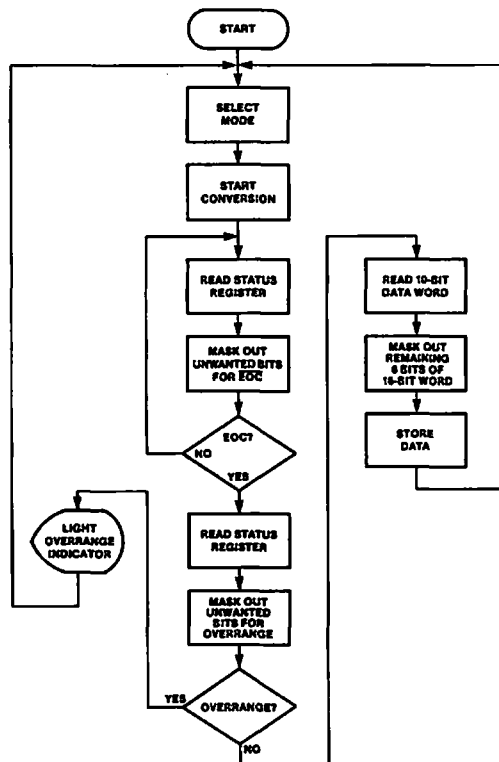
ADC-910 INTERFACE SOFTWARE AND FLOW CHART FOR 16-BIT μ P (MC68000 COMPUTER BOARD)
(a) Minimum Software Using Fixed Delay


PC	MNEMONIC	COMMENT
1000	MOVEQ #12, D0	Select Mode*
1002	MOVE D0, \$50000	Start Conversion
1008	NOP	
100A	NOP	Delay
100C	NOP	
100E	MOVE \$20000, D1	Read Data
1014	ANDI #1023, D1	Mask out B15—B10 leaving B9—B0
1018	JMP \$1000	Jump to 1000

* Loading a decimal 12 into D0 will apply the following binary word to the command register at the start of the conversion:

B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
0 0 0 0 0 0 1 1 0 0

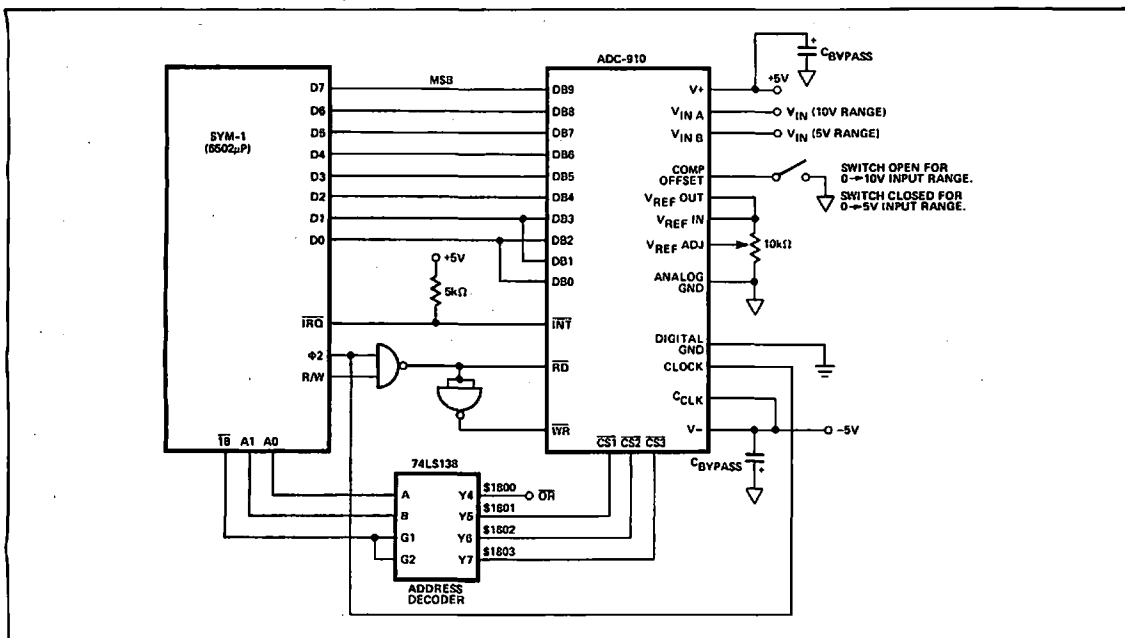
This results in unipolar mode selection with the interrupt disabled.

(b) Polling Status Register for End of Conversion and Overrange


PC	MNEMONIC	COMMENT
1000	MOVEQ #X,D0	Select Mode*
1002	MOVE D0, \$50000	Start Conversion
1008	MOVE \$50000,D1	Read Status Register into D1
100E	AND #512,D1	Mask for EOC Bit (1000000000 = 512 Decimal)
1012	BNE.L \$1008	Loop Until EOC
1016	MOVE \$50000,D2	Read Status Register
101C	AND #256,D2	Mask for OR Bit (0100000000 = 256 Decimal)
1020	BEQ.L \$102E	Branch to \$102E Unless OR
1024	MOVE D3,\$40000	Light OR Indicator
102A	JMP \$1000	Start Over
102E	MOVE \$20000,D4	Read and Store 10-Bit Data
1032	AND #1023,D4	Mask Unwanted 6 LSBs
1036	JMP \$1000	Start Over

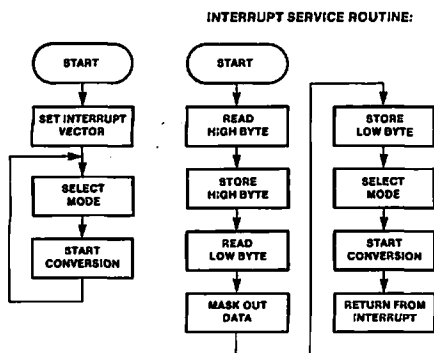
*For Bipolar Mode with Interrupt Enabled: X = 4 Decimal
 For Unipolar Mode with Interrupt Enabled: X = 12 Decimal
 For Bipolar Mode, Interrupt Disabled: X = 20 Decimal
 For Unipolar Mode, Interrupt Disabled: X = 28 Decimal

FIGURE 7: ADC-910 Interface to 6502 μ P on SYM-1 Board



ADC-910 INTERFACE SOFTWARE AND FLOW CHART FOR 6502 μ P (SYM-1)

Interrupt-Driven Conversion



PC	MNEMONIC	OP CODE	COMMENT
0200	LDA#\$02	A9 02	Set Interrupt Vector
0202	STAS\$A679	8D 79 A6	
0205	LDA#\$12	A9 12	
0207	STAS\$A678	8D 78 A6	
020A	LDA#\$03	A9 03	Select Mode (Unipolar, Interrupt Enabled)
020C	STAS\$1803	8D 03 18	Start Conversion
020F	JMP\$20A	4C 0A 02	Jump to 20A (Loop Until Interrupt)
Interrupt Service Routine			
0212	LDA\$1801	AD 01 18	Read High Byte
0215	STA\$024E	8D 4E 02	Store High Byte at 024E
0218	LDA\$1802	AD 02 18	Read Low Byte
021B	AND#\$03	29 03	Mask Out Bits 9—4
021D	STA\$024F	8D 4F 02	Store Low Byte at 024F
0220	LDA#\$03	A9 03	Select Mode
0222	STA\$1803	8D 03 18	Start Conversion
0225	RTI	40	Return from Interrupt



ADC-9012

CMOS MICROPROCESSOR-COMPATIBLE
12-BIT A/D CONVERTER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Low Cost
- 12-Bit Accurate
 - $\pm 1/2$ LSB Nonlinearity Error Over Temperature
 - No Missing Codes at All Temperatures
- 12 Microsecond Conversion Time
- Internal or External Clock
- Fast Bus Access and Disconnect Time
 - $T_{ACC} = 90\text{ns}$ minimum
 - $T_{DIS} = 75\text{ns}$ minimum
- 8 or 16-Bit Data Bus Compatible
- Improved ESD Resistant Design
- Low 85mW Power Consumption
- Space Saving 24-Pin 0.3" DIP, or 24-Lead SOL

APPLICATIONS

- Data Acquisition Systems
- DSP System Front End
- Process Control Systems
- Portable Instrumentation

ORDERING INFORMATION†

GAIN ERROR (LSB)	NON- LINEARITY (LSB)	MILITARY* TEMPERATURE -55°C to +125°C	INDUSTRIAL TEMPERATURE -40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
± 1	$\pm 1/2$	—	ADC9012EP	—
± 4	$\pm 1/2$	ADC9012BW	—	—
± 4	$\pm 1/2$	ADC9012BTC/883	—	—
± 8	± 1	—	ADC9012FW	—
± 8	± 1	—	ADC9012FP	ADC9012HP
± 8	± 1	—	ADC9012FS††	—

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

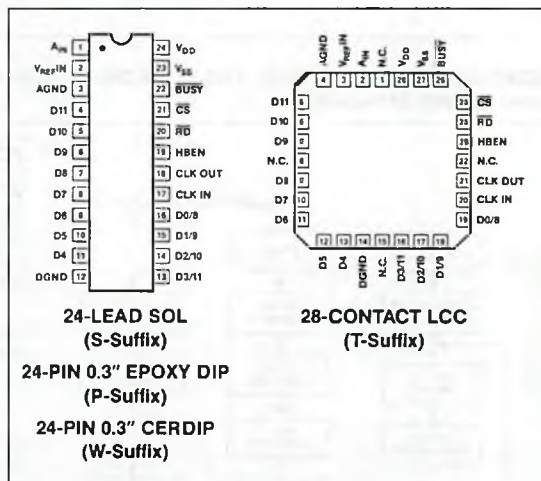
GENERAL DESCRIPTION

The ADC-9012 is a monolithic 12-bit accurate CMOS A/D converter. It contains a complete successive approximation A/D converter built with a high accuracy D/A converter, a precision bipolar transistor high-speed comparator, and successive approximation logic including three-state bus interface for logic compatibility. The accuracy of the ADC-9012 results from the addition of precision bipolar transistors in PMI's advanced-oxide isolated silicon-gate CMOS process. NPN transistors also provide excellent bus interface timing, 90ns access time, and 75ns bus disconnect time which results in faster data transfer without the need for wait states. An external 1MHz clock provides a 12 μ s conversion time.

In stand-alone applications an internal clock can be used with an external crystal.

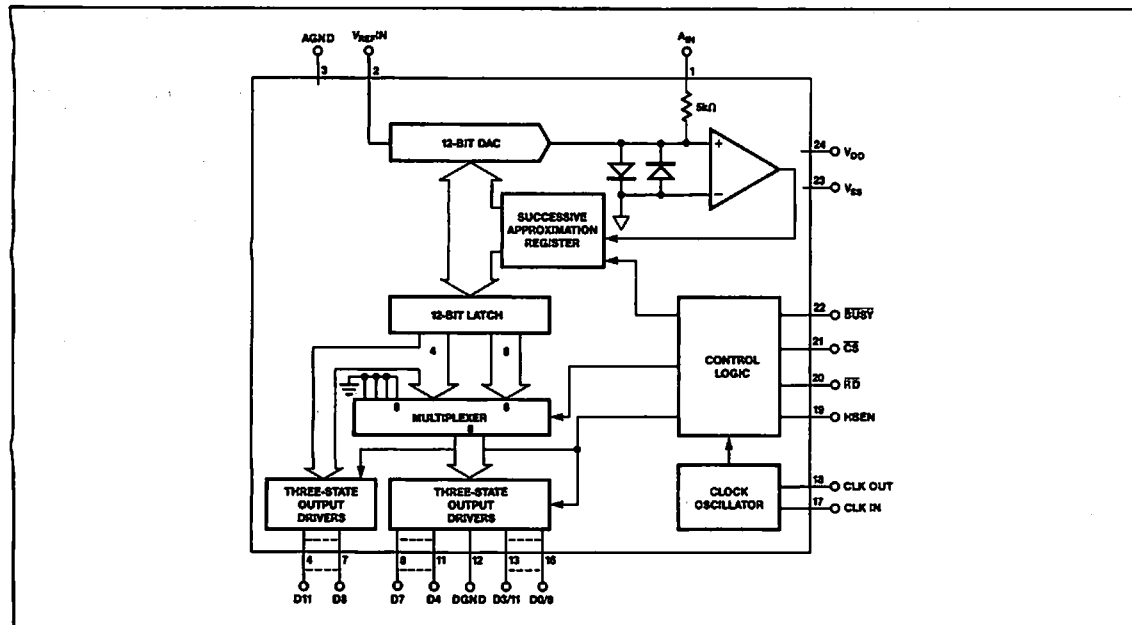
An external negative five-volt reference sets the 0 to +10 volt input range. Plus five and minus 15 volt power supplies result in 85mW of total power consumption.

PIN CONNECTIONS



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DD} to DGND -0.3V to +7V

V_{DD} to DGND -0.3V to +7V

V_{SS} to DGND..... +0.3V to -17V

AGND to DGND $-0.3V, V_{DD} + 0.3V$

A_{IN} to AGND -15V to +15V

Digital Input Voltage to DGND

Plins 17, 19-21 $-0.3V, V_{DD} + 0.3V$

Digital Output Voltage to DGND

Pins 4-11, 13-16, 18, 22 $-0.3V, V_{DD} + 0.3V$

Operating Temperature Range

Operating Temperature Range
 HP 0 to +70°C

EP FP FW FS -40°C to +85°C

BW, BTC..... -55°C to +125°C

Dice Junction Temperature +150°C

Storage Temperature..... -65°C to 150°C

Power Dissipation (Any Package) to +75°C	1,000mW
--	---------

Derates above +75°C by 10mW/°C

CAUTION:

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{SS} = -12$ to $-15V$, $V_{REF} = -5V$, Analog Input 0 to $+10V$; $f_{CLK} = 1MHz$; $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ for ADC-9012E/F, $0^{\circ}C \leq T_A \leq +70^{\circ}C$ for ADC-9012H, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ for ADC-9012B, unless otherwise noted. Specifications apply to Slow-Memory Mode.

PARAMETER	SYMBOL	CONDITIONS	ADC-9012			UNITS
			MIN	TYP	MAX	
Integral Nonlinearity	INL	B/E Grades	-1/2	—	+1/2	LSB
		F/H Grades	-1	—	+1	
Differential Nonlinearity	DNL		-1	—	+1	LSB
Offset Error	V _{ZSE}	E Grade	-1	—	+1	LSB
		B/F/H Grades	-4	—	+4	
Gain Error	G _{FSSE}	E Grade	-1	—	+1	LSB
		B Grade	-4	—	+4	
		F/H Grades	-8	—	+8	



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{SS} = -12$ to $-15V$, $V_{REF} = -5V$, Analog Input 0 to $+10V$; $f_{CLK} = 1MHz$; $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ for ADC-9012E/F, $0^{\circ}C \leq T_A \leq +70^{\circ}C$ for ADC-9012H, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ for ADC-9012B, unless otherwise noted. Specifications apply to Slow-Memory Mode. (Continued)

			ADC-9012			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Full-Scale Tempco (Note 1)	TCG _{FS}	E Grade B/F/H Grades	—	—	+5 +10	ppm/°C
Input Voltage Range	V _{IN}		0	—	+10	V
Input Current Range	I _{IN}		0	—	+3	mA
Power Supply Rejection Ratio	PSRR	ΔV _{DD} = ±10%, ΔV _{SS} = ±10%	—	1/2	1	LSB
Logic Input High Voltage	V _{INH}	$\overline{CS}$, RD, HBEN	2.4	—	—	V
Logic Input Low Voltage	V _{INL}	$\overline{CS}$, RD, HBEN	—	—	0.8	V
Logic Input Current	I _{IN}	$\overline{CS}$, RD, HBEN	—	—	±1	μA
Digital Input Capacitance	C _{IN}	Digital Input, CS, RD, HBEN, CLK IN (Note 1)	—	—	10	pF
Logic Output High Voltage	V _{OH}	I _{SOURCE} = 0.4mA	3.5	—	—	V
Logic Output Low Voltage	V _{OL}	I _{SINK} = 1.6mA	—	—	0.4	V
Three-State Output Leakage	I _{OZ}	D11-D0/8	—	—	10	μA
Digital Output Capacitance	C _{OUT}	D11-D0/8 (Note 1)	—	—	15	pF
Positive Supply Current	I _{DD}	V _{DD} = +5V (Note 2)	—	—	5	mA
Negative Supply Current	I _{SS}	V _{SS} = -12V (Note 2)	—	—	5	mA
Power Consumption	P _{dis}	V _{DD} = +5V, V _{SS} = -12V (Note 2)	—	—	85	mW
Conversion Time	T _c	f _{CLK} = 1MHz (Note 6) Synchronous Clock	—	—	12.5	μs
		Asynchronous Clock	12	—	13.5	
TIMING CHARACTERISTICS (Notes 1, 3)						
CS to RD Set-up Time	t ₁		0	—	—	ns
RD to BUSY Propagation Delay	t ₂	T _A = +25°C	—	—	190	
		T _A = Full Temperature Range	—	—	230	ns
		E/F/H Grades	—	—	270	
		B Grade	—	—	270	
Data Access Time After RD	t ₃	(Note 4) C _L = 20pF	—	—	90	ns
		C _L = 100pF	—	—	125	
Read Pulse Width	t ₄	C _L = 20pF	—	—	90	ns
		C _L = 100pF	—	—	125	
CS to RD Hold Time	t ₅		0	—	—	ns
Data Set-up Time After BUSY	t ₆	(Note 4)	—	—	70	ns
Bus Disconnect Time	t ₇	(Note 5)	20	—	75	ns
HBEN to RD Set-up Time	t ₈		0	—	—	ns
HBEN to RD Hold Time	t ₉		0	—	—	ns
Delay Between Successive Read Operations	t ₁₀		500	—	—	ns

NOTES:

1. Guaranteed by design.
2. Converter inactive; $\overline{CS}$, RD = HIGH, $A_{IN} = +10V$.
3. All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of $+5V$) and timed from a voltage level of 1.8V.
4. t_3 and t_6 are measured with the load circuits of Figure 1 and timed for an output to cross 0.8V or 2.4V.
5. t_7 is the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
6. See Synchronizing Start Conversion Information in Converter Operation Details.

FIGURE 1: Load Circuits for Access Time

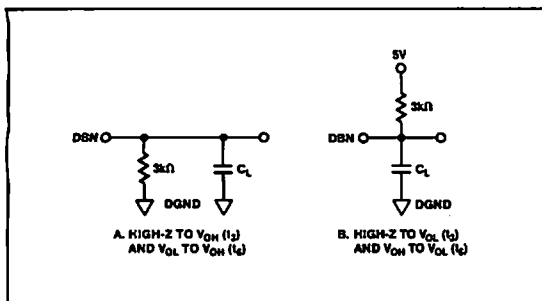


FIGURE 2: Load Circuits for Output Float Delay

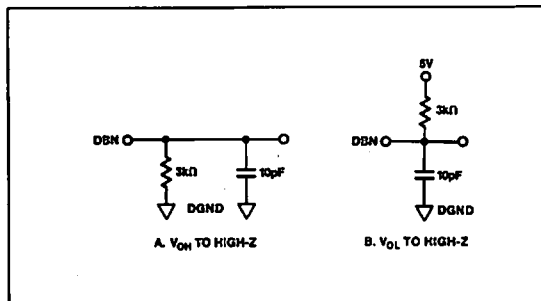


TABLE 1: Pin Function Description

PIN MNEMONIC DESCRIPTION

1	A_{IN}	Analog Input. 0 to +10 volts.
2	V_{REFIN}	Voltage Reference Input. Requires external -5 volt reference.
3	AGND	Analog Ground
4... 11	D11... D4	Three State data outputs become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
13... 16	D3/11... D0/8	Individual pin function is dependent upon High Byte Enable (HBEN) input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

NOTES:

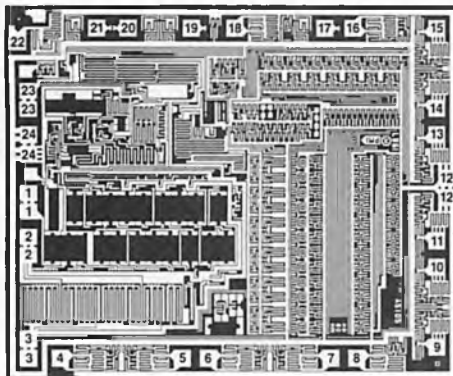
* D11... D0/8 are the ADC data output pins.

DB11... DB0 are the 12-bit conversion results, DB11 is the MSB.

12	DGND	Digital Ground
17	CLK IN	Clock Input pin. An external TTL compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description for crystal (resonator).
19	HBEN	High Byte Enable Input. its primary function is to multiplex the 12 bits of conversion data onto the lower D7... D0/8 outputs (4 MSBs or 8 LSBs). See Pin description 4... 11 and 13... 16. Also disables conversion start when HBEN is high.
20	$\overline{RD}$	READ input. This active LOW signal, in conjunction with $\overline{CS}$ is used to enable the output data three-state drivers and initiates a conversion if $\overline{CS}$ and HBEN are low.
21	$\overline{CS}$	CHIP SELECT input. This active LOW signal, in conjunction with $\overline{RD}$ is used to enable the output data three-state drivers and initiates a conversion if $\overline{RD}$ and HBEN are low.
22	$\overline{BUSY}$	BUSY output indicates converter status. BUSY is LOW during conversion.
23	V_{SS}	Negative Supply, -15V.
24	V_{DD}	Positive Supply, +5V.



DICE CHARACTERISTICS



DIE SIZE 0.122 × 0.148 Inch, 18,056 sq. mils
(3.098 × 3.759 mm, 11.65 sq. mm)

- | | |
|----------------|--------------------------|
| 1. A_{IN} | 13. D3/11 |
| 2. V_{REFIN} | 14. D2/10 |
| 3. AGND | 15. D1/9 |
| 4. D11 | 16. D0/8 |
| 5. D10 | 17. CLK IN |
| 6. D9 | 18. CLK OUT |
| 7. D8 | 19. HBEN |
| 8. D7 | 20. RD |
| 9. D6 | 21. CS |
| 10. D5 | 22. BUSY |
| 11. D4 | 23. V_{SS} |
| 12. DGND | 24. V_{DD} (Substrate) |

For additional DICE ordering information, refer to
1988 Data Book, Section 2.

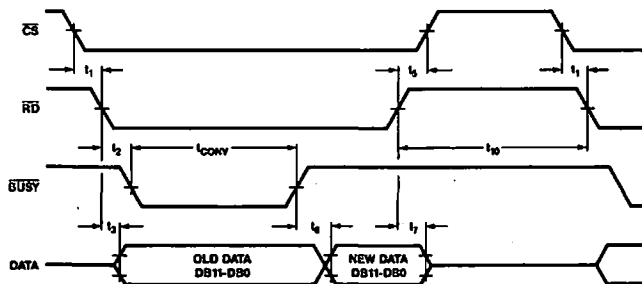
WAFER TEST LIMITS at $V_{DD} = +5V$, $V_{SS} = -12V$ to $-15V$, $V_{REF} = -5V$, $A_{IN} = 0V$ to $+10V$, and $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	ADC-9012G	
			LIMIT	UNITS
Integral Nonlinearity	INL		± 1	LSB MAX
Differential Nonlinearity	DNL		± 1	LSB MAX
Offset Error	V_{ZSE}		± 8	LSB MAX
Gain Error	G_{FSE}		± 8	LSB MAX
Analog Input Resistance	R_{AIN}		4/6	K Ω MIN/MAX
Logic Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{RD}$, HBEN	2.4	V MIN
Logic Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, HBEN	0.8	V MAX
Logic Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN	± 1	μA MAX
Logic Output High Voltage	V_{OH}	$I_{SOURCE} = 0.4mA$	3.5	V MIN
Logic Output Low Voltage	V_{OL}	$I_{SINK} = 1.6mA$	0.4	V MAX
Positive Supply Current	I_{DD}	$V_{DD} = +5V$ (Note 1)	5	mA MAX
Negative Supply Current	I_{SS}	$V_{SS} = -12V$ (Note 1)	5	mA MAX

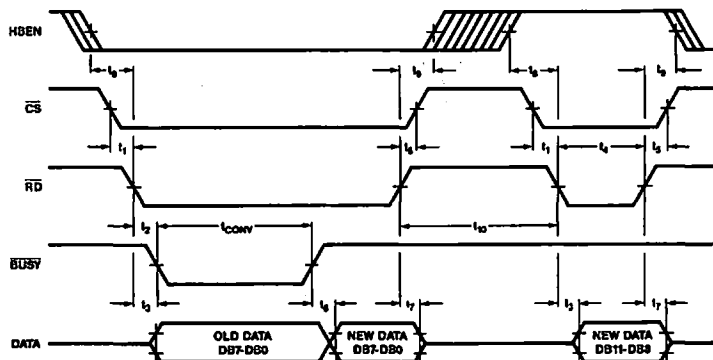
NOTES:

1. Converter inactive $\overline{CS} = \overline{RD} = HBEN =$ Logic HIGH, $A_{IN} = +10V$.

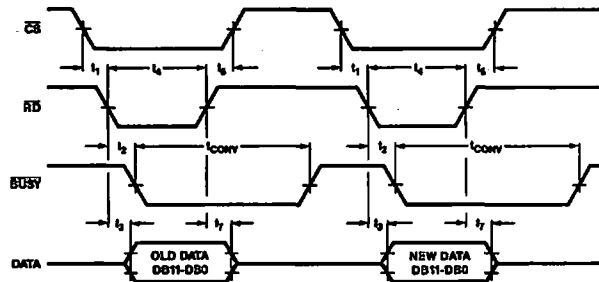
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

FIGURE 3: Parallel Read Timing Diagram, Slow-Memory Mode (HBEN = LOW)

SLOW-MEMORY MODE, PARALLEL READ DATA BUS STATUS

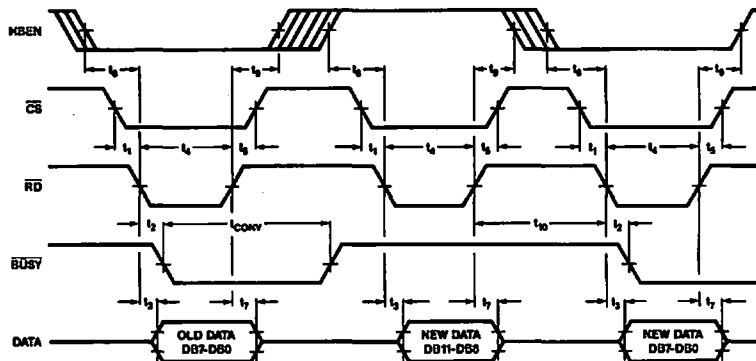
ADC-9012 DATA OUTPUTS	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
READ	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

FIGURE 4: Two-Byte Read Timing Diagram, Slow-Memory Mode

SLOW-MEMORY MODE, TWO-BYTE READ DATA BUS STATUS

ADC-9012 DATA OUTPUTS	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
FIRST READ	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SECOND READ	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

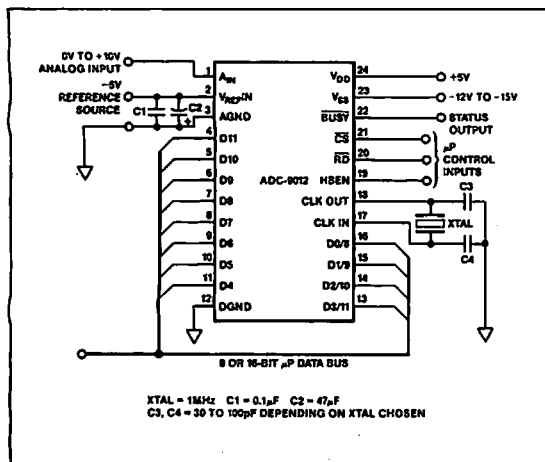
FIGURE 5: Parallel Read Timing Diagram, ROM Mode (HBEN = LOW)

ROM MODE, PARALLEL READ DATA BUS STATUS

ADC-9012 DATA OUTPUTS	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
FIRST READ (OLD DATA)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SECOND READ	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

FIGURE 6: Two-Byte Read Timing Diagram, ROM Mode

ROM MODE, TWO-BYTE READ DATA BUS STATUS

ADC-9012 DATA OUTPUTS	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
FIRST READ (OLD DATA)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
SECOND READ	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
THIRD READ	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

FIGURE 7: Basic Connection Diagram



CONVERTER OPERATION DETAILS

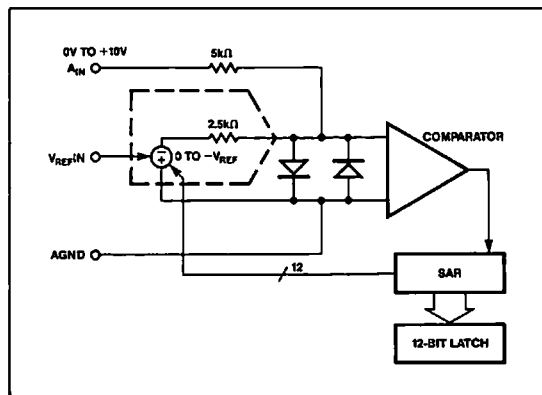
The CS, RD and HSEN digital inputs control the start of conversion. A high-to-low transition on both CS and RD initiate a conversion sequence. The HSEN high-byte-enable input must be low or coincident with the read RD input edge. The start of conversion resets the internal successive approximation register (SAR) and enables the three-state outputs. See Figure 8. The busy line is active low during the conversion process.

During conversion, the SAR sequences the voltage output DAC from the most-significant-bit (MSB) to the least-significant-bit (LSB). The analog input connects to the comparator via a 5k Ω resistor. The DAC which has a 2.5k Ω output resistance connects to the same comparator input. The comparator, performing a zero crossing detection, tests the addition of successively weighted bits from the DAC output versus the analog input signal. The MSB decision occurs after the second negative edge of the CLK IN following conversion initiation. The remaining 11-bit trials occur on the next 11 negative CLK IN edges. Once a conversion cycle is started it cannot be stopped or restarted, without upsetting the remaining bit decisions. Every conversion cycle must have 13 negative CLK IN edges. At the end of conversion the comparator input voltage is zero. The SAR contains the 12-bit data word representing the analog input voltage. The BUSY line returns to logic high, signalling end of conversion. The SAR transfers the new data to the 12-bit latch.

SYNCHRONIZING START CONVERSION

Aligning the negative edge of the RD with the rising edge of CLK IN provides synchronization of the start convert signal to the conversion process for sampling system applications. Without synchronization the conversion time will vary from 12 to 13 clock cycles. See Figure 9.

FIGURE 8: Simplified Analog Input Circuitry of ADC-9012



POWER ON INITIALIZATION

During system power-up the ADC-9012 comes up in a random state. One complete conversion of 13 clock cycles must be performed to reset the A/D conversion process. The results of the first conversion should be disregarded. The second 13 clock cycles will provide a valid A/D conversion. This is important in battery operated systems where power supplies are shut down between measurement times.

DRIVING THE ANALOG INPUT

During conversion, the DAC output current modulates the analog input current at the CLK IN frequency of 1MHz. The analog input to the ADC-9012 must not change during the conversion process. This requires an external buffer with low output impedance at 1MHz. Suitable devices meeting this requirement include the OP-27, OP-42, and the SMP-11.

INTERNAL CLOCK OSCILLATOR

Figure 10 shows the ADC-9012 internal clock circuit. The clock oscillates at the external crystal or ceramic resonator frequency. The 1MHz crystal or ceramic resonator connects between the CLK IN (pin 17) and the CLK OUT (pin 18). Capacitance values (C1, C2) depend on the crystal or ceramic resonator manufacturer. Typical values range from 30pF to 100pF.

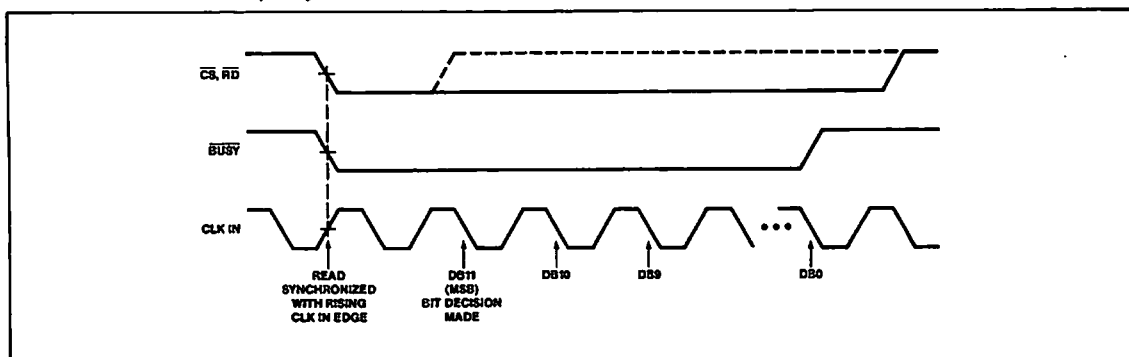
EXTERNAL CLOCK INPUT

A TTL compatible signal connected to CLK IN provides proper converter clock operation. No connection is necessary to the CLK OUT pin. The CLK IN duty cycle is not critical, since all internal circuit timing occurs on the negative CLK IN edge. The duty cycle of the external clock input can range from 20% to 80%. Figure 9 shows the important waveforms.

EXTERNAL REFERENCE

A low-output resistance negative-five volt reference is necessary. The external reference should be able to supply 3mA of reference current. A bypass capacitor is necessary on the

FIGURE 9: External Clock Input Synchronization



reference input lead to minimize system noise. The reference input to the internal DAC is code dependent requiring anywhere from zero to 3mA. The reference voltage tolerance has a direct influence on A/D converter full-scale voltage. The maximum input full-scale voltage equals $2 \times -V_{REF}$. The ADC-9012 is not designed for ratiometric operation; the range for reference input voltages should be limited to $\pm 5\%$. Figure 11 provides a good negative-five volt reference.

FIGURE 10: ADC-9012 Simplified Internal Clock Circuit

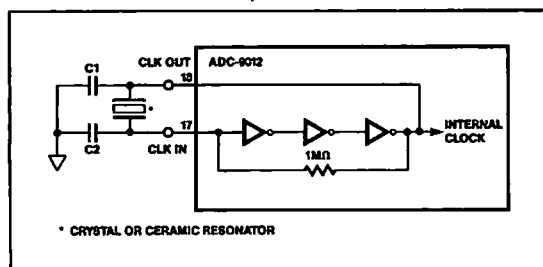
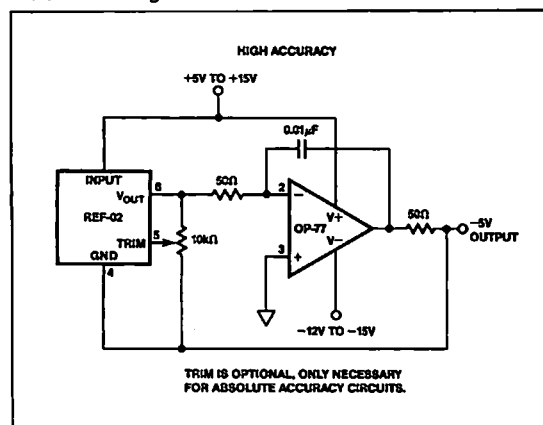


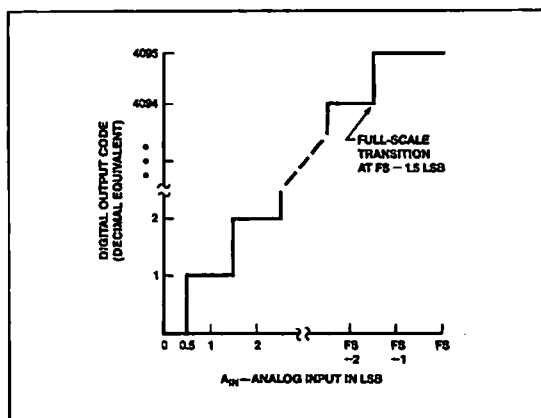
FIGURE 11: Negative-Five Volt Reference



UNIPOLAR ANALOG INPUT OPERATION

Figure 12 shows the ideal input/output characteristic for the 0 to 10 volt input range of the ADC-9012. The designed output code transitions occur midway between successive integer LSB values (i.e., 0.5 LSB, 1.5 LSBs, 2.5 LSBs, ..., FS - 1.5 LSBs). The output code is natural binary with 1 LSB = $FS/4096 = (10/4096)V = 2.44mV$. The maximum full-scale input voltage is $(10 \times 4095/4096)V = 9.9976V$, which is 0.5 LSB higher than the last code transition.

FIGURE 12: Ideal ADC-9012 Input/Output Transfer Characteristic

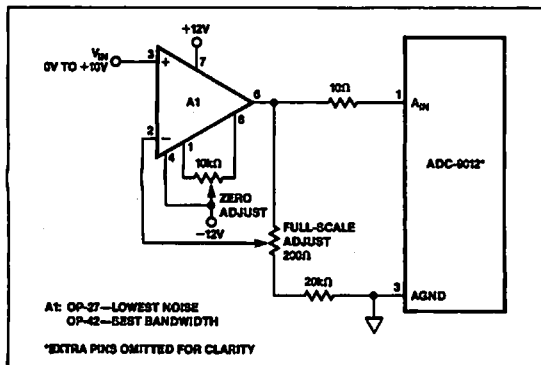


OFFSET AND FULL-SCALE ERROR ADJUSTMENT, UNIPOLAR OPERATION

In applications where absolute accuracy is important then offset and full-scale error can be adjusted to zero. Figure 13 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the null offset of the op amp driving A_{IN} .

Adjust the zero-scale first by applying 1.22mV (equivalent to 0.5 LSB input) to V_{IN} . Adjust the op amp offset control until the digital output toggles between 0000 0000 0000 and 0000 0000 0001. The next step is adjustment of full scale. Apply 9.9964V (equivalent to $FS - 1.5$ LSB) to V_{IN} and adjust R1 until the digital output toggles between 1111 1111 1110 and 1111 1111 1111.

FIGURE 13: Unipolar 0V to +10V Operation



MICROPROCESSOR INTERFACING

The ADC-9012 has self-contained logic for both 8-bit and 16-bit data bus interfacing. The output data can be formatted into either a 12-bit parallel word for a 16-bit data bus or an 8-bit data word pair for an 8-bit data bus. Data is always right justified, i.e., LSB is the most right-hand bit in a 16-bit word. For a two-byte read, only data outputs D7...D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower D7...D0/8 outputs (4 MSBs or 8 LSBs) where it can be read in two read cycles. The 4 MSBs always appear on D11...D8 whenever the three-state output drivers are turned on. See Figure 14.

Two A/D conversion modes of operation are available for both data bus sizes: the ROM mode and the Slow-Memory mode.

In the ROM mode each READ instruction obtains new, valid data assuming the minimum timing requirements are satisfied. However, since the data output from a current READ instruction was generated from a conversion initiated by a previous READ operation, the current data may be out-of-date. To be sure of obtaining up-to-date data, READ instructions may be coded in pairs (with some NOPs between them); use only the data from the second READ in each pair. The first READ starts the conversion, the second READ gets the results.

The Slow-Memory mode is the simplest mode. It is the method of choice where compact coding is essential, or where software bugs are a hazard. In this mode, a single READ instruction will initiate a data conversion, interrupt the microprocessor until completion (WAIT states are introduced), then read the results. If the system throughput tolerates WAIT states, and the hardware is correct, then the Slow-Memory mode is virtually immune to subsequent software modifications. Placing the microprocessor in the WAIT state has an additional advantage of quieting the digital system to reduce noise pickup in the analog conversion circuitry. The 12-bit parallel Slow-Memory mode provides the fastest analog sampling rate combined with digital data transfer rate for sampled-data systems.

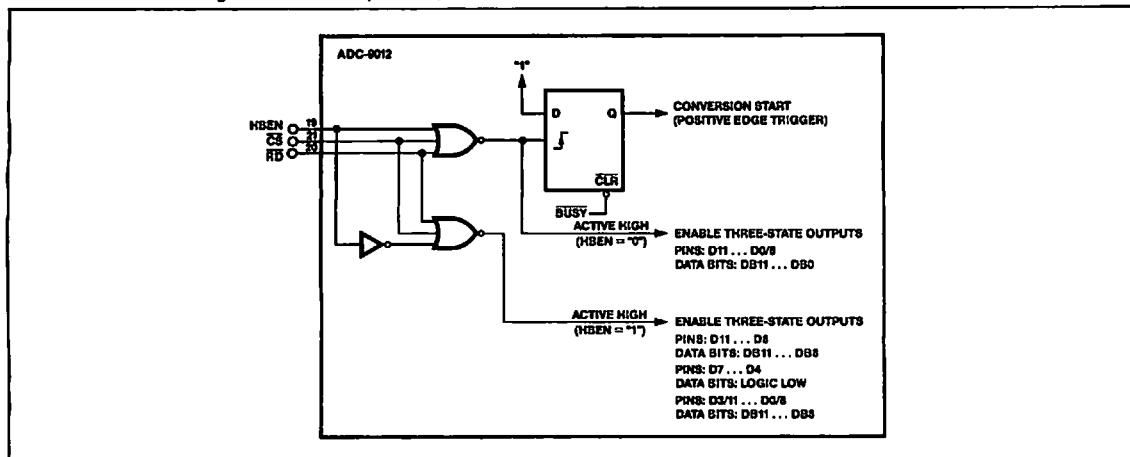
PARALLEL READ, SLOW-MEMORY MODE (HBEN = LOW)

Figure 3 shows the timing diagram and data bus status for Parallel Read, Slow-Memory Mode. CS and RD going low triggers a conversion and the ADC-9012 acknowledges by taking BUSY low. Data from the previous conversion appears on the three-state data outputs. BUSY returns high at the end of conversion, when the output latches have been updated, and the conversion result is placed on data outputs D11 ... D0/8.

TWO-BYTE READ, SLOW-MEMORY MODE

For a two-byte read only 8 data outputs D7...D0/8 are used. Conversion start procedure and data output status for the first read operation is identical to Parallel Read, Slow-Memory Mode.

FIGURE 14: Internal Logic for Control Inputs $\overline{\text{CS}}$, $\overline{\text{RD}}$, and HBEN



See Figure 4, Timing Diagram and Data Bus Status. At the end of conversion, the low data byte (DB7...DB0) is read from the A/D converter. A second READ operation with HBEN high, places the high byte on data outputs D3/11...D0/8 and disables conversion start. Note the 4 MSBs appear on data outputs D11...D8 during these two READ operations.

PARALLEL READ, ROM MODE (HBEN = LOW)

A conversion is started with a READ operation. The 12 bits of data from the previous conversion are available on data outputs D11...D0/8 (see Figure 5). This data may be disregarded if not required. A second READ operation reads the new data (DB11...DB0) and starts another conversion. A delay at least as long as the ADC-9012 conversion time must be allowed between READ operations. If a READ takes place prior to the end of 13 CLKs of the ADC conversion, the remaining bits not yet tested will be invalid.

TWO-BYTE READ, ROM MODE

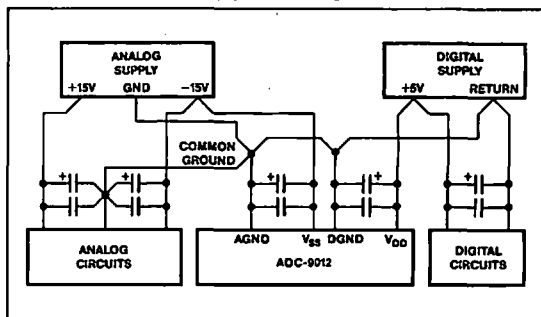
For a two-byte read-only data outputs D7...D0/8 are used. Conversion is started in the same way with a READ operation and the data output status is the same as the Parallel Read, ROM Mode. See Figure 6, Two-Byte Read Timing Diagram. Two more READ operations are required to obtain the new conversion result. A delay equal to the ADC-9012 conversion time must be allowed between conversion start and the second data READ operation. The second READ operation, with HBEN high, disables conversion start and places the high byte (4 MSBs) on data outputs D3/11...D0/8. A third READ operation accesses the low data byte (DB7...DB0) and starts another conversion. The 4 MSBs appear on data outputs D11...D8 during all three read operations above.

CIRCUIT LAYOUT GUIDELINES

As with any high speed A/D converters good circuit layout practice is essential. Wire-wrap boards are not recommended due to stray pickup of the high frequency digital noise. A PC board offers the best results. Digital and analog grounds should be separated even if they are ground planes instead of ground traces. Don't lay digital traces adjacent to high impedance analog traces. Avoid digital layouts that radiate high frequency clock signals, i.e., don't lay out digital signal lines and ground returns in the shape of a loop antenna. Shield the analog input if it comes from a different PC board source. Set up a single point ground at AGND (pin 3) of the ADC-9012. Tie all other analog grounds to this point. Also tie the logic power supply ground, but no other digital grounds to this point (see Figure 15). Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC. Their trace widths should be as wide as possible. Good power supply bypass capacitors located near the ADC package insure quiet operation. Place a 10 μ F capacitor in parallel with a 0.01 μ F ceramic capacitor across V_{DD} to ground and V_{SS} to ground (near pin 3).

In applications where the ADC-9012 data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get LSB level errors in conversion results. These errors are due to a feedthrough from the microprocessor

FIGURE 15: Power Supply Grounding



to the internal comparator. The problem can be minimized by forcing the microprocessor into a WAIT state during conversion (see Slow-Memory Mode microprocessor interfacing). An alternate method is isolation of the data bus with three-state buffers.

INTERFACING TO THE TMS32010 DSP PROCESSOR

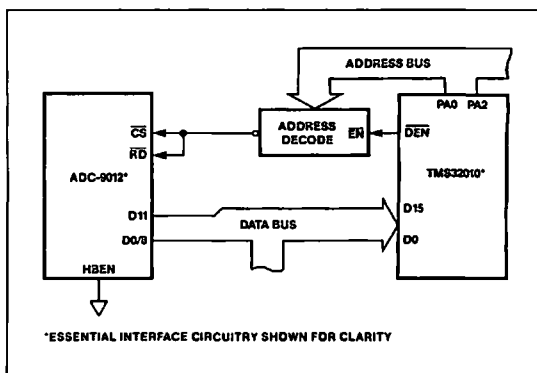
Figure 16 shows an ADC-9012 to TMS32010 interface. The ADC-9012 is operating in the ROM Mode. The interface is designed for a maximum TMS32010 clock frequency of 18.6MHz but will typically work over the full 20MHz TMS32010 clock frequency range.

The ADC-9012 is mapped at a user-selected port address (PA). The following I/O instruction starts a conversion and reads the previous conversion into the data memory.

IN DATA, PA PA = Port Address
DATA = Data Memory Location

When conversion is complete, a second I/O instruction reads the new data into the data memory and starts another conversion. Sufficient A/D conversion time must be allowed between I/O instructions. The very first data read after system power-up should be discarded.

FIGURE 16: ADC-9012 to TMS32010 DSP Processor Interface



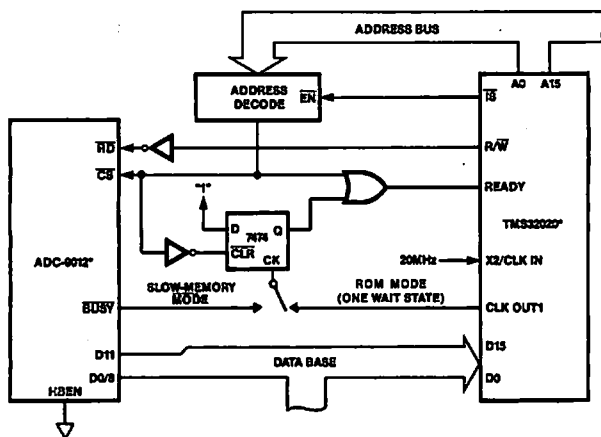
USING WAIT STATES

The TMS32020 DSP processor has the added capability of WAIT states. This feature simplifies the hardware required for slow memory devices by extending the microprocessor bus access time. Figure 15 shows an ADC-9012 to TMS32020 interface using one WAIT state to guarantee data interface at the full 20MHz clock frequency. This WAIT state extends the bus access time by 200ns. In this circuit the ADC-9012 operates in the ROM mode where each input instruction (IN DATA, PA) takes the previous conversion result and stores it in memory. The next input instruction must be delayed as long as the A/D conversion time to read a new conversion result.

SLOW-MEMORY MODE OPERATION USING WAIT STATES

The WAIT state feature of the TMS32020 can be used to operate the ADC-9012 in the Slow-Memory mode. This is accomplished by driving the clock input of the 7474 flip-flop in Figure 17, from the BUSY output of the ADC-9012, instead of the CLK OUT1 of the TMS32020. Once a conversion has started the READY input of the TMS32020 is not released until the ADC-9012 completes its 12-bit A/D conversion. This stops the TMS32020 during the conversion process reducing microprocessor system noise generation. Another advantage for the system software is the single instruction IN MEM, PA used to start, process, and read the results of the A/D conversion. This makes the software code more transportable between systems operating at different clock speeds. The disadvantage is wasted processing time.

FIGURE 17: ADC-9012 to TMS32020 Interface Using WAIT States



*ESSENTIAL INTERFACE CIRCUITRY SHOWN FOR CLARITY



PM-0820

CMOS HIGH-SPEED 8-BIT
A/D CONVERTER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Built-In Track and Hold Function
- No Missing Codes
- No External Clocking
- Operates from Single +5V Supply with 0 to 5V Analog Input Voltage
- Easily Interfaced to Microprocessors, or Stand-Alone
- Latched 3-State Outputs
- Logic Inputs/Outputs are CMOS or TTL Compatible
- No Zero or Full-Scale Adjustment Required
- Ratio-metric Operation, or Uses Reference Voltage Up to V_{CC}
- Overflow Output Available for Cascading
- Pin and Function Compatible with ADC0820, AD7820
- Conversion Speed $1.5\mu s$

ORDERING INFORMATION†

PACKAGE		OPERATING TEMPERATURE RANGE
HERMETIC DIP	PLASTIC DIP	
PM0820AR*	—	MIL
PM0820BR*	—	MIL
PM0820ER	—	IND
PM0820FR	—	IND
—	PM0820GP	COM
—	PM0820HP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

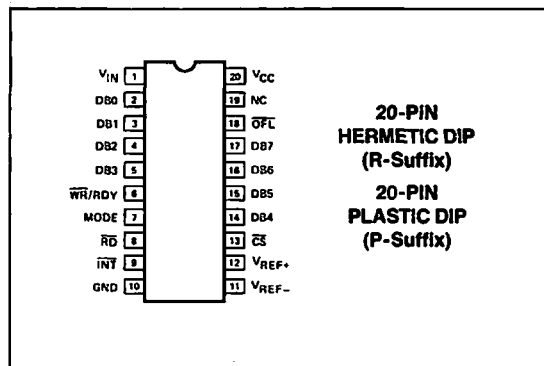
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

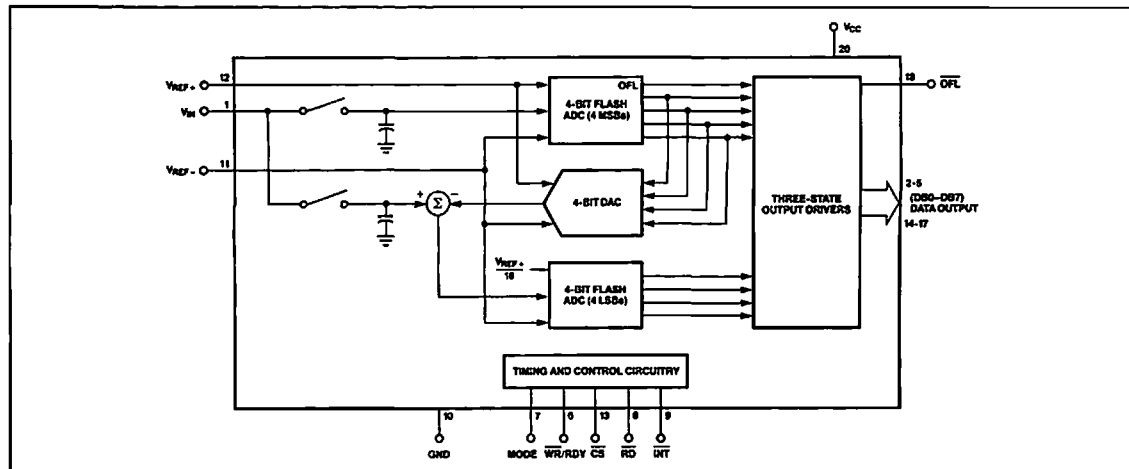
The PM-0820 is an 8-bit resolution analog-to-digital converter, with digital inputs and outputs designed for ease of use in microprocessor-based systems. A half-flash conversion technique is used, with the input signal tracked and held by on-chip circuitry. No external sample-and-hold amplifier is needed for input signals moving at less than $100mV/\mu s$.

This CMOS device offers $1.5\mu s$ conversion time and uses only $75mW$ of power. It is ideally suited to a variety of A/D applications where high speed, low power, ease of use, and economy of space are required.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

SELECTED ELECTRICAL CHARACTERISTICS at $V_{CC} = +5V$, $V_{REF+} = 5V$, $V_{REF-} = GND$, Full operating temperature range.

Resolution 8 Bits

Total Unadjusted Errors

(offset, full-scale linearity) $\pm 1/2$ LSB (grades A, E, G)

..... ± 1 LSB (grades B, F, H)

Reference Input Voltage Range GND to V_{CC}

..... (with $V_{REF+} > V_{REF-}$)

Input Voltage $V_{CC} + 0.1V$ to $GND - 0.1V$

Logic Inputs and Outputs Compatibility TTL & 5V CMOS

Conversion Time:

WR-RD Mode (pin 7 = V_{CC}) Limit $1.5\mu s$

RD Mode (pin 7 = 0V) Limit $2.5\mu s$

Access Time:

WR-RD Mode, $t_{IR} > 0$, Load $15pF$ Limit 120ns

Output Disable Time:

RD HIGH to Output Hi-Z Limit 200ns

FIGURE 1: Basic Hook-Up

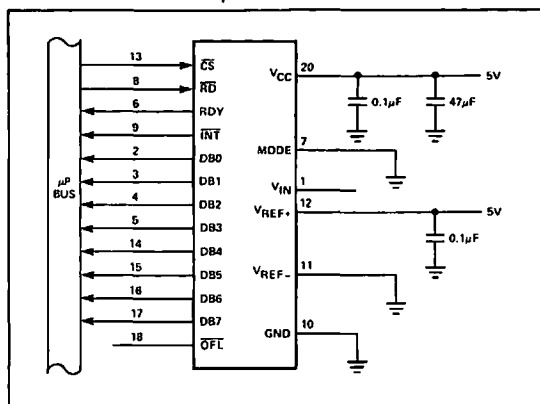


FIGURE 2: RD Mode (Pin 7 is Low)

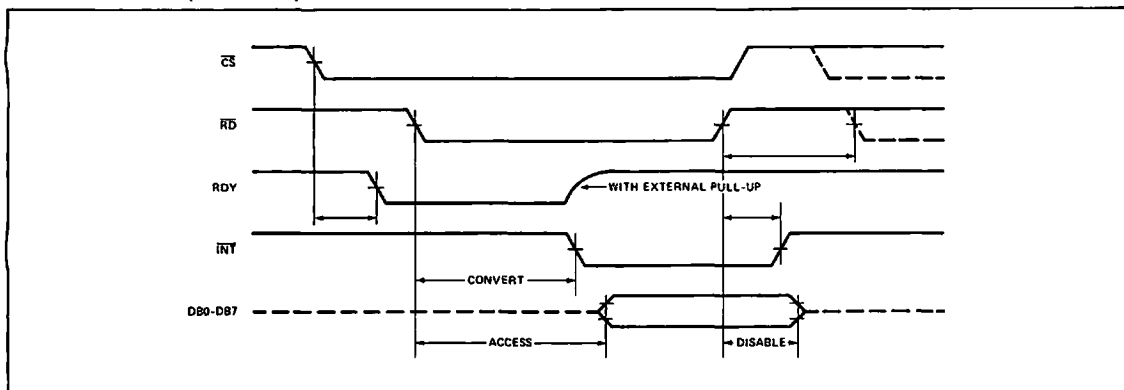


FIGURE 3: WR-RD Mode (Pin 7 is High and $t_{IR} > 0$)

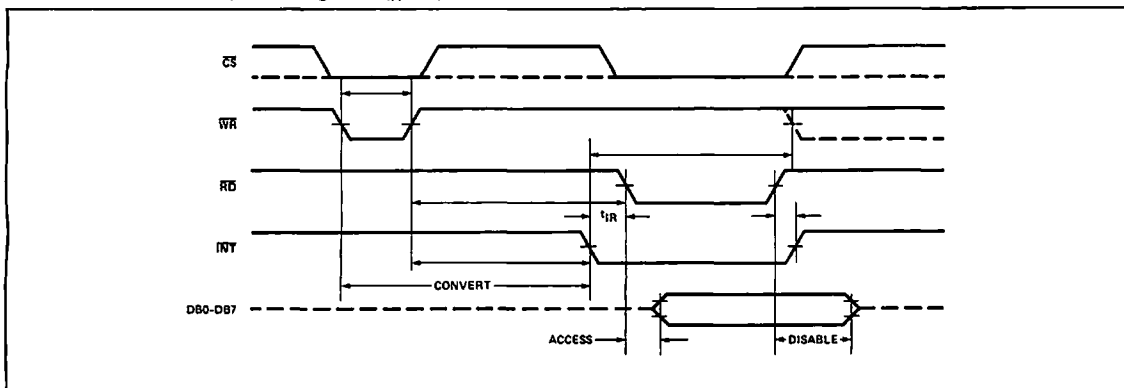
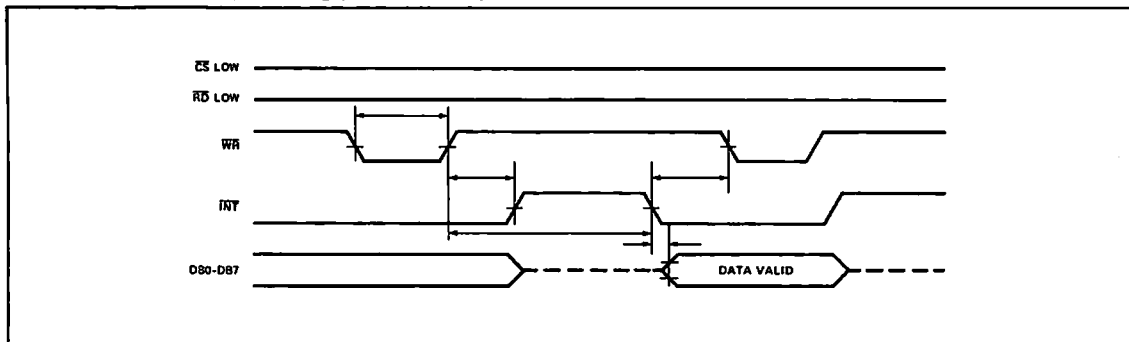


FIGURE 4: WR-RD Mode (Pin 7 is High) Stand-Alone Operation



Precision Monolithics Inc.

PM-7574

CMOS MICROPROCESSOR-COMPATIBLE
8-BIT A/D CONVERTER

FEATURES

- 8-Bit Resolution and Accuracy
- No Missing Codes Over Full Temperature Range
- 15 μ s Conversion Time
- Flexible μ P Interface
- 5mA Maximum Standby Current
- Low Cost
- Pin and Function Compatible With AD7574

ORDERING INFORMATION†

PACKAGE: 18-PIN DIP AND SO					
INL (LSB)	DNL (LSB)	MILITARY*	INDUSTRIAL	COMMERCIAL	
		TEMPERATURE -55°C TO +125°C	TEMPERATURE -40°C TO +85°C	TEMPERATURE 0°C TO 70°C	
$\pm 1/2$	$\pm 3/4$	PM7574AX	PM7574EX	PM7574GP	
$\pm 3/4$	$\pm 7/8$	PM7574BX	PM7574FX	PM7574HP	
$\pm 1/2$	$\pm 3/4$	—	—	PM7574GS††	

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The PM-7574 is a monolithic CMOS successive-approximation analog-to-digital converter. When used with a 550kHz clock, a conversion time of 15 μ s is achieved, with full accuracy over the operating temperature range.

The PM-7574 outputs use 3-state logic, allowing direct connection to the data bus or system input port. Active-LOW chip

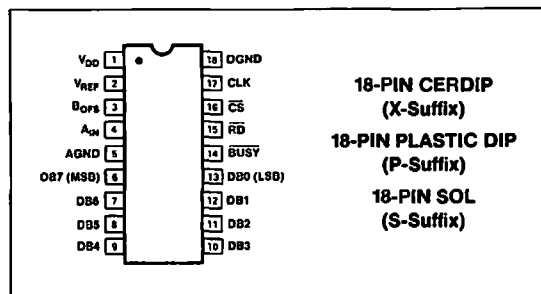
select ($\overline{CS}$) and read/write ($\overline{RD}$) inputs are used to control all operations. This simplicity permits the PM-7574 to be used as a memory-mapped input device. Depending on the control timing waveforms, the PM-7574 is interfaced like static RAM, ROM, or slow memory.

The low power consumption of the PM-7574 is derived from a single +5V supply. A negative reference voltage must also be supplied. Optimum accuracy is achieved when the reference is at -10.00V with low output resistance. For a low-cost precision -10V/-10.24V reference, ask your PMI sales representative about the REF-08.

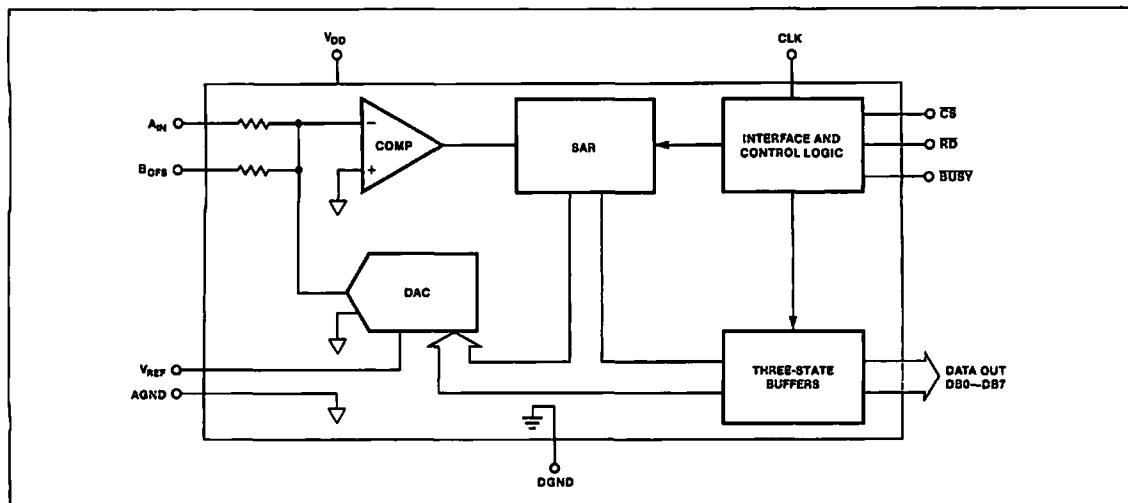
With its on-board comparator, interface logic, optional internal clock, and +5V operation, the PM-7574 is the ideal low-cost solution for microprocessor-based 8-bit A/D systems.

For new designs, PMI's ADC-908 is pin-and-function compatible with the PM-7574, but offers faster conversion time and faster microprocessor bus interface timing.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**(T_A = +25°C, unless otherwise noted.)

V _{DD} to AGND	0V, +7.0V
V _{DD} to DGND	0V, +7.0V
AGND to DGND	-0.3V, V _{DD}
CS, RD to DGND	-0.3V, V _{DD} + 0.3V
DB0-DB7 to DGND	-0.3V, V _{DD}
CLK, BUSY to DGND	-0.3V, V _{DD}
B _{OFS} , A _{IN}	±20V
V _{REF}	0V, -20V
Operating Temperature Range	
PM-7574AX, BX	-55°C to +125°C
PM-7574EX, FX	-40°C to +85°C
PM-7574GP, GS, HP	0°C to +70°C

Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C
Power Dissipation (Package)	
Ceramic (Suffix X) and Plastic (Suffix P)	
To +75°C	450mW
Derate Above +75°C by	6mW/°C
Derate Plastic Above +70°C by	8.3mW/°C
Small Outline Wide	
To +70°C	400mW
Derate Above 70°C by	10mW/°C

NOTE:

Digital pins are Zener protected. However, proper ESD handling precautions are recommended.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = -10V, Unipolar Configuration, R_{CLK} = 150kΩ, C_{CLK} = 100pF; -40°C ≤ T_A ≤ +85°C for PM-7574E/F, 0°C ≤ T_A ≤ +70°C for PM-7574G/H, -55°C ≤ T_A ≤ +125°C for PM-7574A/B, unless otherwise noted.

				PM-7574		
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	N		8	—	—	Bits
Integral Nonlinearity	INL	A/E/G Grades	-1/2	—	+1/2	LSB
		B/F/H Grades	-3/4	—	+3/4	
Differential Nonlinearity	DNL	A/E/G Grades	-3/4	—	+3/4	LSB
		B/F/H Grades	-7/8	—	+7/8	
Gain Error	G _{FSE}	A/E/G Grades T _A = +25°C	-3	—	+3	LSB
		T _A = Full Temp Range	-4.5	—	+4.5	
		B/F/H Grades T _A = +25°C	-5	—	+5	
		T _A = Full Temp Range	-6.5	—	+6.5	
Offset Error	V _{ZSE}	A/E/G Grades T _A = +25°C	-30	—	+30	mV
		T _A = Full Temp Range	-50	—	+50	
		B/F/H Grades T _A = +25°C	-60	—	+60	
		T _A = Full Temp Range	-80	—	+80	
ANALOG INPUTS						
Resistance Mismatch B _{OFS} to A _{IN}	ΔR _{AB}		-1.5	—	+1.5	%
Input Resistance at V _{REF} (Note 1)	R _{REF}		5	—	15	kΩ
Input Resistance at B _{OFS} , A _{IN}	R _{B_{OFS}} R _{IN}		10	—	30	kΩ
Reference Voltage	V _{REF}	Specified Conversion Accuracy	—	-10	—	V
Reference Voltage Range	V _{REF}	Degraded Conversion Accuracy	-5	—	-15	V
Reference Current (Note 6)	I _{REF}	Conversion Complete Prior to Reset.	—	—	2.4	mA
Nominal Analog						
Input Range	V _{INU}		—	0 to + V _{REF}	—	V
Unipolar Mode	V _{INB}		—	- V _{REF} to + V _{REF}	—	V
Bipolar Mode						
LOGIC INPUTS						
Input HIGH Voltage RD, CS Inputs	V _{IH}		2.4	—	—	V
Input LOW Voltage RD, CS Inputs	V _{IL}		—	—	0.8	V



ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{REF} = -10V$, Unipolar Configuration, $R_{CLK} = 150k\Omega$, $C_{CLK} = 100pF$; $-40^\circ C \leq T_A \leq +85^\circ C$ for PM-7574E/F, $0^\circ C \leq T_A \leq +70^\circ C$ for PM-7574G/H, $-55^\circ C \leq T_A \leq +125^\circ C$ for PM-7574A/B, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	PM-7574 TYP	MAX	UNITS
Input Current RD, CS Inputs	I_{IN}	$T_A = +25^\circ C$ $T_A = \text{Full Temp Range}$	—	—	1 10	μA
Input Capacitance RD, CS Inputs (Note 6)	C_{IN}		—	—	5	pF
Input HIGH Voltage, Clock Input	V_{IH}		3	—	—	V
Input LOW Voltage, Clock Input	V_{IL}		—	—	0.4	V
Input HIGH Current, Clock Input	I_{IH}		—	—	2	mA
Input LOW Current, Clock Input	I_{IL}	$T_A = +25^\circ C$ $T_A = \text{Full Temp Range}$	—	—	1 10	μA
LOGIC OUTPUTS						
Output HIGH Voltage BUSY, DB0-7	V_{OH}	$I_{SOURCE} = 40\mu A$	4.0	—	—	V
Output LOW Voltage BUSY, DB0-7	V_{OL}	$I_{SINK} = 1.6mA$	—	—	0.4	V
Floating Leakage Current, DB0-7	I_{LKG}	$T_A = +25^\circ C$ $T_A = \text{Full Temp Range}$	—	—	1 10	μA
Floating State Output Capacitance		(Note 6)	—	—	7	pF
POWER REQUIREMENTS						
Standby Current	I_{DD}	$V_{DD} = +4.75V$ to $+5.25V$	—	—	5	mA
DIGITAL INTERFACE TIMING						
CS Minimum Pulse Width (Note 6)	t_{CS}	$T_A = +25^\circ C$ $T_A = \text{Full Temp Range}$	100 150	—	—	ns
RD to CS Setup Time (Note 6)	t_{WCS}		0	—	—	ns
CS to BUSY Propagation Delay (Note 8)	t_{CBPD}	BUSY Load = 20pF $T_A = +25^\circ C$	—	—	120	ns
		$T_A = T_{MIN}$	—	—	120	
		$T_A = T_{MAX}$	—	—	180	
		BUSY Load = 100pF $T_A = +25^\circ C$	—	—	150	
		$T_A = T_{MIN}$	—	—	150	
		$T_A = T_{MAX}$	—	—	200	
BUSY to RD Setup Time (Notes 2, 6)	t_{BSR}		0	—	—	ns
BUSY to CS Setup Time (Note 6)	t_{BSCS}		0	—	—	ns
Data Access Time (Note 8)	t_{RAD}	$C_L = 20pF$ $T_A = +25^\circ C$	—	—	150	ns
		$T_A = T_{MIN}$	—	—	150	
		$T_A = T_{MAX}$	—	—	220	
		$C_L = 100pF$ $T_A = +25^\circ C$	—	—	300	
		$T_A = T_{MIN}$	—	—	300	
		$T_A = T_{MAX}$	—	—	400	
Data Hold Time (Notes 3, 6)	t_{RHD}	$T_A = +25^\circ C$ (Note 3)	50	—	120	ns
		$T_A = T_{MIN}$	30	—	80	
		$T_A = T_{MAX}$	80	—	140	

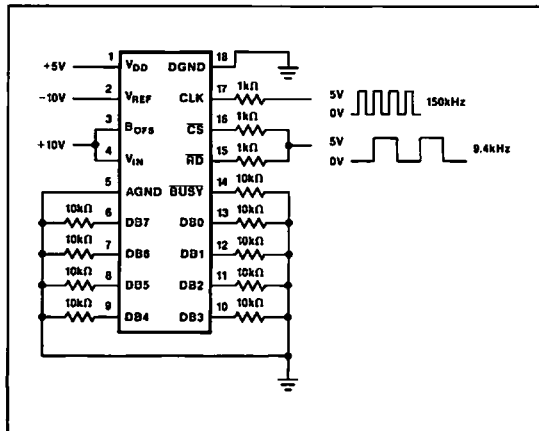


ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$, $V_{REF} = -10V$, Unipolar Configuration, $R_{CLK} = 150k\Omega$, $C_{CLK} = 100pF$; $-40^{\circ}C \leq T_A \leq +85^{\circ}C$ for PM-7574E/F, $0^{\circ}C \leq T_A \leq +70^{\circ}C$ for PM-7574G/H, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ for PM-7574A/B, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	PM-7574		UNITS
				TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Hold Time (Note 6)	t_{RHCS}	$T_A = +25^{\circ}C$	—	—	250	ns
		$T_A = T_{MIN}$	—	—	200	
		$T_A = T_{MAX}$	—	—	500	
Reset Time Requirement (Note 6)	t_{RESET}		3	—	—	μs
Conversion Time (Note 4) (Notes 4, 5, 6)	$t_{CONVERT}$	Static RAM Mode	—	—	15	μs
		External Clock				
		$f = 550kHz$	—	—	17	μs
		ROM Mode Internal Clock				
$\overline{RD}$ HIGH to $\overline{BUSY}$ Propagation Delay, ROM Mode (Notes 4, 5, 6)	t_{WBPD}	$C_L = 20pF$	—	—	1.5	μs
		$T_A = +25^{\circ}C$				
		$T_A = T_{MIN}$	—	—	1.0	μs
		$T_A = T_{MAX}$	—	—	2.0	

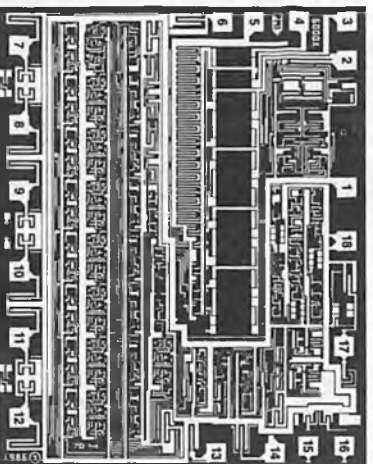
NOTES:

- For optimum gain accuracy over the full temperature range, the source resistance at pin 2 should be kept low.
- In ROM mode, $\overline{RD}$ can go LOW prior to $\overline{BUSY} = HIGH$, but must not return HIGH until $\overline{BUSY} = HIGH$.
- Output loading 10pF. A 3k Ω pullup resistor to +5V is used for V_{OL} to High-Z; for V_{OH} to High-Z, a 3k Ω pulldown to GND is used. Measured to 0.5V output change.
- When using the PM-7574 internal oscillator, actual conversion time depends on clock resistor and capacitor as well as temperature.
- ROM interface mode conversion times are typically 2 μs longer than conversion times for other modes, but the ROM interface mode includes an automatic reset in the conversion time.
- Guaranteed but not tested.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.129 X 0.103 inch, 13,287 sq. mils
(3.28 X 2.62 mm, 8.58 sq. mm)

- | | |
|---------------------|--------------|
| 1. V _{DD} | 10. DB3 |
| 2. V _{REF} | 11. DB2 |
| 3. B _{OPS} | 12. DB1 |
| 4. A _{IN} | 13. DB0(LSB) |
| 5. AGND | 14. BUSY |
| 6. DB7(MSB) | 15. RD |
| 7. DB6 | 16. CS |
| 8. DB5 | 17. CLK |
| 9. DB4 | 18. DGND |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at V_{DD} = +5V, V_{REF} = -10,000V, AGND = DGND = 0V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PM-7574G LIMIT	UNITS
STATIC ACCURACY				
Resolution	N		8	Bits MIN
Integral Nonlinearity	INL		±3/4	LSB MAX
Differential Nonlinearity	DNL		±7/8	LSB MAX
Gain Error	G _{FSE}		±5	LSB MAX
Offset Error	V _{SE}		±60	mV MAX
ANALOG INPUTS				
Resistance Mismatch B _{OPS} to A _{IN}	ΔR _{AB}		±1.5	% MAX
Input Resistance at V _{REF}	R _{REF}		5/15	kΩ MIN/MAX
Input Resistance at B _{OPS} , A _{IN}	R _{BOPS} , R _{IN}		10/30	kΩ MIN/MAX
DIGITAL INPUTS				
Input HIGH Voltage at RD, CS Inputs	V _{HI}		3	V MIN
Input LOW Voltage at RD, CS Inputs	V _{LI}		0.8	V MAX
Input Current RD, CS Inputs	I _{IN}		±1	μA MAX
Input HIGH Voltage Clock Input	V _{HI}		3	V MIN
Input LOW Voltage Clock Input	V _{LI}		0.4	V MAX
Input HIGH Current Clock Input	I _{HI}		2	mA MAX
Input LOW Current Clock Input	I _{LI}		1	μA MAX



WAFER TEST LIMITS at $V_{DD} = +5V$, $V_{REF} = -10.000V$, $AGND = DGND = 0V$, $T_A = +25^\circ C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PM-7574G LIMIT	UNITS
DIGITAL OUTPUTS				
Output HIGH Voltage BUSY, DB0-7	V_{OH}	$I_{SOURCE} = 40\mu A$	4	V MIN
Output LOW Voltage BUSY, DB0-7	V_{OL}	$I_{SINK} = 1.6mA$	0.4	V MAX
Floating Leakage Current	I_{LKG}		1	μA
POWER REQUIREMENTS				
Standby Current	I_{DD}	$V_{DD} = +4.75V$ to $5.25V$	5	mA MAX
TIMING				
Conversion Time	$t_{CONVERT}$	Static RAM Mode, External Clock, $f = 550kHz$	15	μs MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

GENERAL CIRCUIT INFORMATION

The PM-7574 is an 8-bit analog-to-digital converter which uses a successive approximation technique to convert an unknown analog input into a digital code output. The control logic inputs allow easy interface to most microprocessors while three-state outputs allow direct connection to the data bus. Most applications require only passive RC clock components, a $-10V$ reference, and a $+5V$ power supply. The RC-timed internal clock may be used, or an external clock may be applied to the ADC to maximize performance.

When a Start Conversion command is applied to the $\overline{CS}$ or $\overline{RD}$ inputs (see Operating Descriptions for details), BUSY goes LOW indicating a conversion in progress. BUSY may be used as an interrupt to halt the controlling microprocessor during conversion or may be polled to prevent premature data reads.

Starting with the most significant bit (MSB), each successive bit in the DAC is turned on (see Figure 1). The comparator then decides if the DAC output is less than or greater than the signal being converted, and that bit is latched on or off, respectively, before proceeding to the next lower bit and repeating the cycle. When all eight bits have been tested, BUSY goes HIGH, signaling a completed conversion.

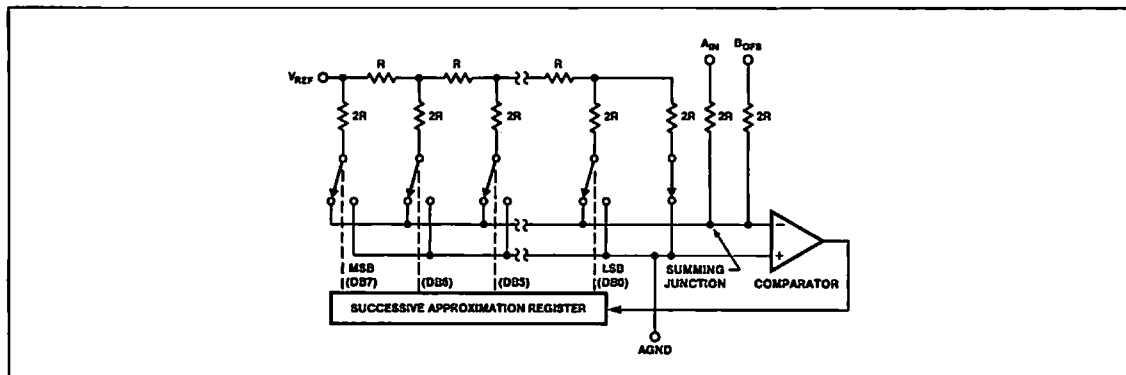
Under control of the $\overline{RD}$ input, the three-state data outputs (D0-D7) change from high-impedance to presenting the new conversion results to the data bus. Following the data read, $\overline{RD}$ returns HIGH resetting the SAR to 1000 0000 and preparing the ADC for its next conversion.

APPLICATIONS INFORMATION

The PM-7574 may be interfaced as if it were a static RAM, a ROM, or a slow-memory device. Each of these interface modes has its own timing and software requirements as described below. These requirements must be rigidly met, as improper timing may cause the PM-7574 to change modes.

HOW TO CHOOSE AN OPERATING MODE

The static-RAM interface mode offers advantages in a tightly controlled hardware and software environment, where the relationship between WRITE and READ instruction pairs is certain. As long as minimum timing is satisfied, converted data may be read at any convenient time after conversion. The use of separate commands to start a conversion, and then read the results, is conceptually easy. However, if the software is subject to uncontrolled modifications, then the paired relationship between WRITE and READ instructions may be lost. The

FIGURE 1: D/A Converter Used in PM-7574

resulting software bugs may result in converted data of unknown age, or altogether invalid data being read.

By contrast, the ROM mode may be more resistant to software bugs. As long as minimum timing is satisfied, each READ instruction obtains new, valid data. However, since the data output at any previous READ instruction is obtained from a conversion performed just after the previous READ instruction, data may be out-of-date. To be sure of obtaining up-to-date data, READ instructions may be coded in pairs (with some NOPs between them); use only the data from the second READ in each pair. The first READ starts the conversion, acting as a substitute for the static-RAM mode WRITE command; the second READ gets the results. The advantage of the ROM mode is the use of a single command, rather than the alternating READ-WRITE required by static-RAM mode.

The slow-memory mode is the simplest mode of all. It is the method of choice where compact coding is essential, or where software bugs are a hazard. In this mode, a single READ instruction will initiate a data conversion, interrupt the microprocessor until completion (WAIT states are introduced), then read the results. If the system throughput tolerates WAIT states, and the hardware is correct, then the slow-memory mode is virtually immune to subsequent software modifications.

OPERATING DESCRIPTION: STATIC-RAM MODE

In this mode, input $\overline{CS}$ is derived from the PM-7574 address decoder, and input $\overline{RD}$ is derived from an active-LOW memory READ signal. (See Figure 2.)

To start a conversion, execute a memory WRITE to the PM-7574. The completed conversion data is obtained by executing a memory READ to the PM-7574. During conversion, output $\overline{BUSY}$ will be LOW. Do not attempt to read data until $\overline{BUSY}$ returns HIGH. The required minimum time between WRITE and READ is usually obtained by including one or more NOP or other program instructions. The use of branch or conditional

commands between the WRITE and READ instructions is not recommended due to the possibility of software bugs.

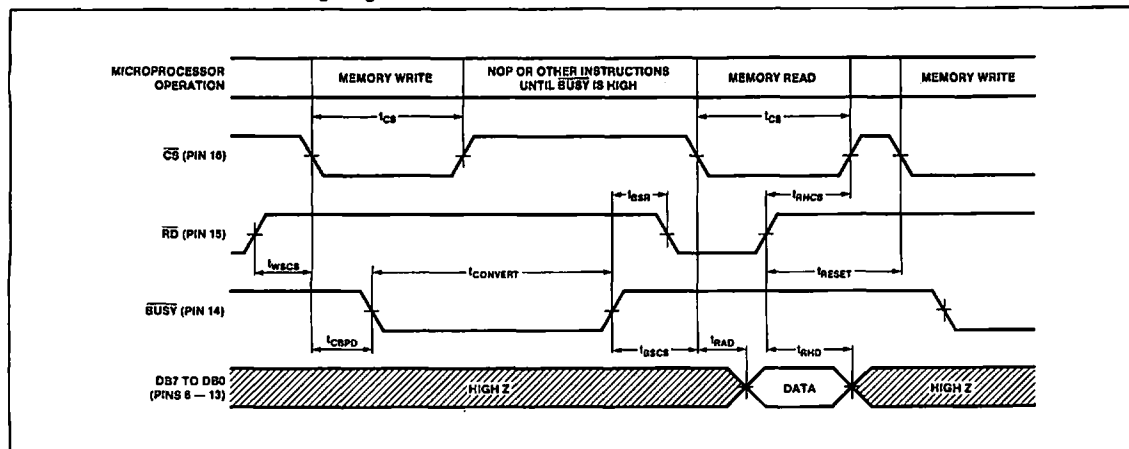
It is important that the WRITE and READ commands be alternately executed. A WRITE instruction has no effect unless the results of the previous WRITE have already been read. Once data has been read, the PM-7574 is internally reset. In other words, two or more READ operations cannot be used in succession, since only the first READ will produce valid data. A new conversion must be started using WRITE, and the conversion must be completed, before a new READ will produce valid data.

TABLE 1: Truth Table, Static RAM Mode

INPUTS		OUTPUTS		PM-7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB7-DB0	
	H		HIGH-Z	Start Convert (Write Cycle)
L		H	HIGH-Z to DATA	Read Data (Read Cycle)
L		H	DATA to HIGH-Z	Reset Converter
H	X (Note 1)	X	HIGH-Z	No Effect (Not Selected)
L	H	L	HIGH-Z	No Effect (Converter Busy)
L		L	HIGH-Z	No Effect (Converter Busy)
L		L	HIGH-Z	Conversion Error Not Allowed

NOTE 1: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or $\overline{BUSY}$.

FIGURE 2: Static RAM Mode Timing Diagram



**OPERATING DESCRIPTION: ROM MODE**

In ROM mode, input $\overline{CS}$ is tied LOW, and input $\overline{RD}$ is derived from the PM-7574 address decoder. To satisfy timing, it is recommended that the decoder be enabled by a system MEMRD (8080), VMA (6800), or similar strobe. (See Figure 3.)

TABLE 2: Truth Table, ROM Mode

INPUTS		OUTPUTS		PM-7574 OPERATION
$\overline{CS}$	$\overline{RD}$	BUSY	DB7-DB0	
L		H	HIGH-Z to DATA	Read Data
L			DATA to HIGH-Z	Reset and Start New Conversion
L		L	HIGH-Z	No Effect (Converter Busy)
L		L	HIGH-Z	Conversion Error Not Allowed

NOTE 1: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of $\overline{CS}$ or BUSY.

In ROM mode, data is read by executing a READ instruction to the PM-7574 address. At the conclusion of the READ instruction, the PM-7574 automatically resets itself and then proceeds to perform a new data conversion. Output BUSY is LOW during conversion. A new READ instruction to the PM-7574 must not be executed until BUSY returns HIGH. This requirement may be met by inserting NOP or other program instructions between consecutive READ operations. Conditional or branch instructions may be used, but keep in mind that data may become out-of-date if excessive time elapses between consecutive READ instructions.

OPERATING DESCRIPTION: SLOW-MEMORY MODE

The slow-memory mode is intended for systems in which the PM-7574 BUSY output is used as an interrupt to force the microprocessor into WAIT states during data conversion.

In slow-memory mode, inputs $\overline{CS}$ and $\overline{RD}$ are tied together. The common $\overline{RD}$ and $\overline{CS}$ signal is derived from the PM-7574 address decoder. To satisfy the timing requirements, it is advisable to latch the address using ALE (8085) or SYNC (8080). For 8080 or 8085-based systems, connect the microprocessor READY input to the PM-7574 BUSY output. (See Figure 4.)

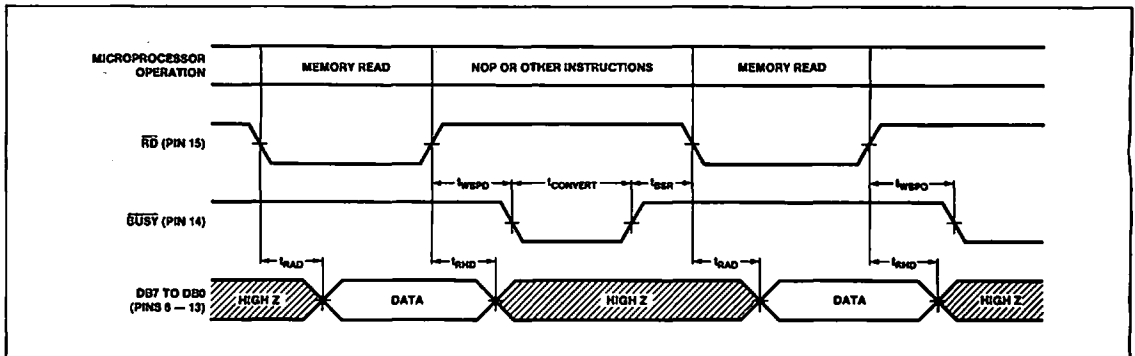
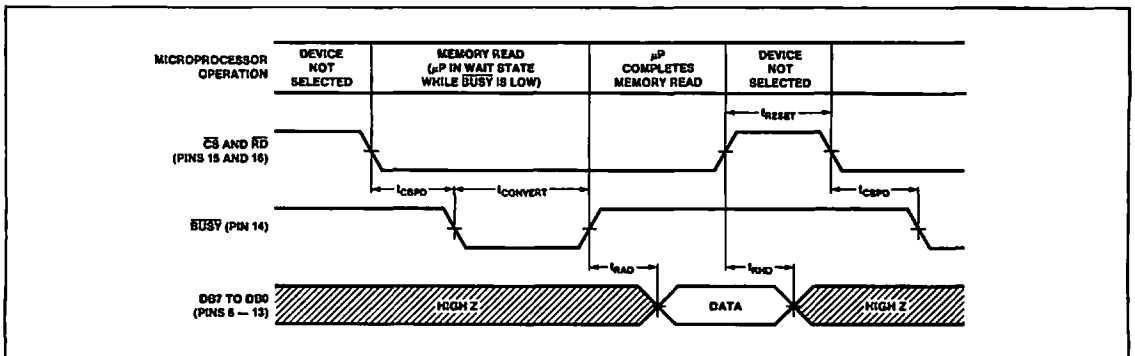
FIGURE 3: ROM Mode Timing Diagram ($\overline{CS}$ Held LOW)**FIGURE 4: Slow-Memory Mode Timing Diagram ($\overline{CS}$ and $\overline{RD}$ Tied Together)**

TABLE 3: Truth Table, Slow-Memory Mode

INPUTS CS & RD		OUTPUTS BUSY DB7-DB0	PM-7574 OPERATION
H	H	HIGH-Z	No Effect (Not Selected)
		HIGH-Z	Start Conversion
L	L	HIGH-Z	Conversion In Progress. μ P in WAIT State
L		HIGH-Z to DATA	Conversion Complete. Read Data
(Note 1)	H	DATA to HIGH-Z	Reset and Deselect Converter

NOTE 1: If $\overline{RD}$ goes LOW to HIGH, the ADC is internally reset, regardless of the states of CS or BUSY.

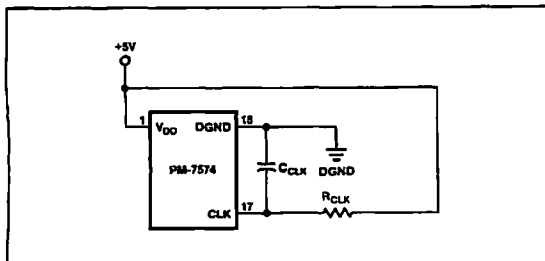
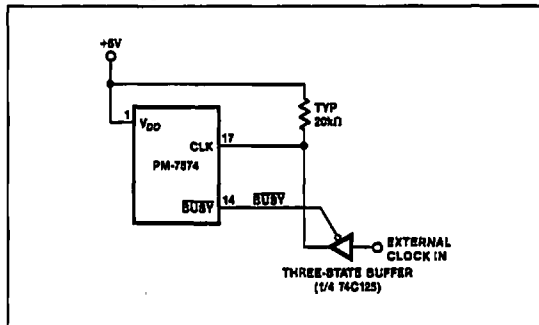
Do not execute a WRITE instruction at the PM-7574 address when in slow-memory mode, since bus conflicts will arise. In some architectures, an accidental WRITE instruction may be locked out in hardware, by proper strobing of the PM-7574 address decoder.

INITIALIZATION

In all operating modes, the PM-7574 is initialized by executing a READ instruction to the PM-7574 address. The data obtained should be ignored.

CLOCK OSCILLATOR

The PM-7574 may be used with its internal asynchronous clock oscillator. An external resistor and capacitor are required. Typical values are $R = 150k\Omega$ and $C = 100pF$, for conversion times in the $15\mu s$ range. For applications in which the fastest conversion times are required, an external clock is recommended. The external clock must be gated by the use of a 74C125-type three-state buffer, with an output pullup resistor. Optimum conversion accuracy is obtained when CS goes LOW on a positive clock edge. The maximum external clock frequency is 550kHz. (See Figure 5 and 6.)

FIGURE 5: Using the Internal Clock Oscillator

FIGURE 6: Using an External Clock


REFERENCE VOLTAGE

A negative reference voltage must be applied to the PM-7574 V_{REF} input. Optimum full-scale accuracy is obtained using $-10.00V$, although V_{REF} may be $-5.00V$, $-10.24V$, or other voltages within its specified range.

Over the full temperature range, optimum gain accuracy is obtained when the input to the V_{REF} pin is from a low-impedance source. A resistor or trimmer may be used in series with the V_{REF} pin, but this trim technique is not as accurate as a low-impedance source. (See Figure 7.)

For a cost-effective $-10.00V$ or $-10.24V$ reference with excellent accuracy and low temperature coefficient, ask for PMI's REF-08. Consult your sales representative for availability.

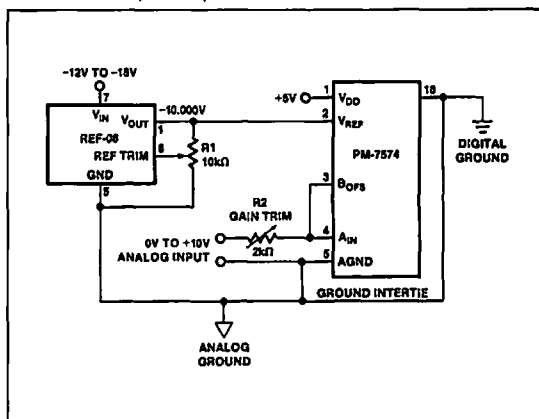
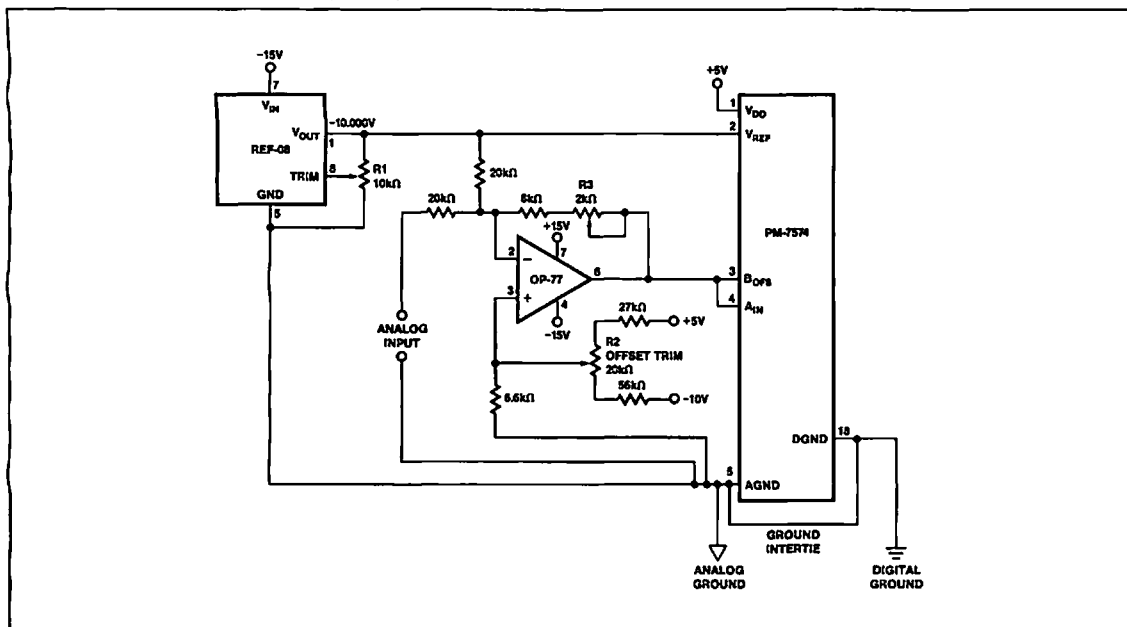
FIGURE 7: Unipolar Operation


FIGURE 9: Complementary Offset Bipolar Operation



- 2) Adjust R3 to its mid-point.
- 3) Adjust R2 until its tap is at 0V.
- 4) Ground the analog input.
- 5) While performing continuous conversions, adjust R2 until the ADC output flickers between 0111 1111 and 1000 0000.

Gain Adjustment:

- 1) Apply +9.922V across the analog input.
- 2) While performing continuous conversions, adjust R3 until DB7 to DB1 are HIGH and DB0 (LSB) flickers.

DIGITAL CONSIDERATIONS

Control Timing—Fresh data from a recent conversion must be read before beginning a new conversion. Following the data READ, as $\overline{RD}$ goes HIGH, it resets the SAR and clears the data from the previous conversion.

The timing restrictions detailed in the interface timing diagrams must be observed to prevent the PM-7574 from changing interface modes. For example, if $\overline{CS}$ is held LOW too long while in RAM mode, the converter will change to ROM mode and initiate a new conversion.

Logic Deglitching—Unrelated activity on the address bus may cause unexpected glitch inputs to the ADC. The glitches may cause unwanted READs, resets, or conversions. In ROM or RAM modes, these may be avoided by gating the address decode logic with $\overline{RD}$ or $\overline{WR}$ (8080) or $\overline{VMA}$ (6800). In slow-memory mode, $\overline{ALE}$ (8085) or $\overline{SYNC}$ (8080) may be used to latch the address.

Initialization—Following power-up, the SAR is in an unknown state. Executing a memory READ (disregard the data) will reset the ADC.

ANALOG CONSIDERATIONS

Analog Input Impedances—Low impedance sources must be used to drive the V_{REF} , A_{IN} , and B_{OUT} inputs. Excessive source impedances may cause errors due to the loading effects of the inputs' finite impedances.

Ground Management—AGND and DGND pins should be connected at or near the ADC to minimize noise effects. If the two grounds cannot be connected near the ADC, the grounds should be clamped with back-to-back Schottky diodes between the AGND and DGND pins.

Offset Correction—Conversion offset errors may be corrected by counter-offsetting the buffer amplifier driving A_{IN} . This offset correction may be accomplished by applying a correction current to the buffer's summing junction or by tapping a voltage divider sitting between V_{DD} and V_{REF} , and applying this tap voltage to the noninverting input of the buffer.

Ratiometric Operation—The R-2R type DAC in the PM-7574 permits ratiometric operation of the ADC. Performance degradation may, however, occur as V_{REF} varies from -10.000V. This decrease in performance is due to comparator limitations including offset voltage, gain, and input noise.

The PM-7574 uses the reference as a power supply for the comparator to increase speed and accuracy. Reference voltages of a magnitude less than -9V must be avoided for accurate comparator operation. For best accuracy, the use of a 0.1 μ F bypass capacitor (Pin 2 to AGND) is recommended.

Power Supply Bypassing—For best accuracy, V_{DD} (Pin 1) should be bypassed to AGND with a 0.1 μ F capacitor.

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ANALOG SWITCHES MULTIPLEXERS

INTRODUCTION

Analog multiplexers and switches find applications in data acquisition, metrology, telemetry, process control and telephony systems. Multiplexers are multiple analog switches which share a common output. An on-chip address decoder selects the appropriate input by means of a binary code. All channels may be deactivated by an enable/disable control pin.

In the past multiplexers/switches have been manufactured with hybrid, monolithic CMOS or dielectrically isolated CMOS technologies. The merging of ion implant techniques with the standard bipolar process creates a fourth technological alternative — the bipolar-JFET process. High-quality ion implanted p-channel FET's can now be compatibly processed with bipolar devices.

The cost of hybrid devices limits their use to applications which require the extremely low " R_{ON} " resistance made possible by discrete FET's. MOS technologies are inherently plagued by SCR "latch up" problems and analog signal overvoltage destruction. The use of buried layers and expensive dielectric isolation processing can eliminate the SCR failure mode, but the overvoltage blowout problems can be solved only by adding large series input resistance with each switch. This increases system errors since the equivalent " R_{ON} " may typically be over 1000 ohms.

JFET switches have no SCR "latch up" tendency and can withstand analog input overvoltages while maintaining low " R_{ON} " resistance. In addition, the special handling required with CMOS devices is not necessary with JFET switches.

In selecting analog multiplexers, attention must be paid to several key specs. Break-before-make switching insures no two-channel inputs are simultaneously connected. This prevents input sensor damage and misoperation. Acquiring analog input signals within a specified time and error band are primary concerns affected by " R_{ON} " resistance and " C_{OUT} " capacitance specifications. A low " R_{ON} " insures minimum signal attenuation and maximum accuracy. The " C_{OUT} " capacitance forms on R-C time constant

with " R_{ON} " placing fundamental limits on signal acquisition time. Low " R_{ON} " and " C_{OUT} " insures minimum elapsed time between the channel select command and the acquisition of data to within a specified error band. High cross talk and off isolation specifications prevent unselected input signals from affecting the signal path.

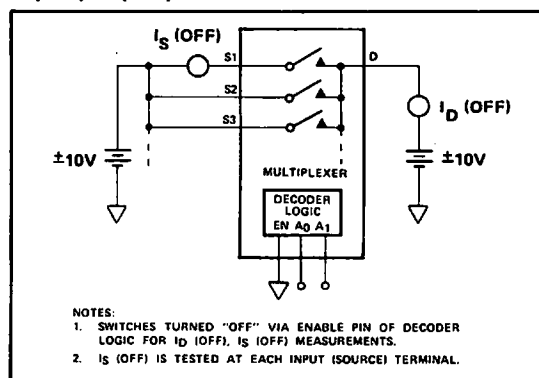
PMI offers a wide selection of single-ended and differential multiplexers and switches. Sixteen and eight-channel multiplexers as well as differential eight and four-channel devices are available. Dual and Quad SPST switches in normally closed and open configurations are also available. All devices are pin-for-pin replacements for many industry standard CMOS devices.

DEFINITIONS

Analog Current Range (I_A , I_S) — The minimum range of currents the switch is capable of conducting in the ON state without degrading ON resistance. It is measured as the value of conduction current that does not cause more than a doubling of the R_{ON} value for the product grade.

Analog Input Leakage Current ($I_{S(OFF)}$) — The algebraic sum of diode current losses from an OFF-channel source input to the power supplies, ground and through the channel. Specified

$I_{D(OFF)}$, $I_{S(OFF)}$ Test Condition Definitions





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ANALOG SWITCHES MULTIPLEXERS

as an absolute value, as the direction of current flow is not predictable.

Analog Output Leakage Current ($I_{D(OFF)}$) — The algebraic sum of diode current losses from an OFF-channel "D" output to the power supplies, ground and through the channel. Specified as an absolute value, as the direction of current flow is not predictable.

Analog Output-To-Input Capacitance ($C_{DS(OFF)}$) — The equivalent capacitance which shunts an open switch effectively between "S" and "D" output.

Analog Input Capacitance ($C_{S(ON)}$) — The capacitance between an analog "S" input and ground with the channel ON.

Analog Input Capacitance ($C_{S(OFF)}$) — The capacitance between an analog "S" input and ground with the channel OFF.

Analog Output Capacitance ($C_{D(OFF)}$) — The capacitance between the analog (DRAIN) output and ground with the channel OFF. High-frequency transmission and output settling time characteristics are highly influenced by this parameter in conjunction with R_{ON} .

Analog Output Capacitance ($C_{D(ON)}$) — The capacitance between the analog "D" output and ground with the channel ON.

Analog Voltage Range (V_A) — The range of analog-voltage amplitudes, with-respect-to ground, over which the analog switch operates (ON/OFF) within the R_{ON} and leakage specifications — $I_{S(OFF)}$, $I_{D(OFF)}$ and $I_{D(ON)} + I_{S(ON)}$.

Break-Before-Make Delay (t_{OPEN}) — The elapsed time between the turn-off of one analog input and the subsequent turn-on of another input as determined by the appropriate instantaneous change in the digital input code for both inputs measured between the outputs' 50% transition points.

Channel Capacitance ($C_{SS(OFF)}$, $C_{DD(OFF)}$) — The capacitance between the D(S) terminals of any two channels.

Charge Transfer (Q) — Charge transfer appears as a voltage step (pedestal) on the output capacitor after switch turn OFF. The undesirable charge AC couples directly from the logic-control driver to the switch contact.

Crosstalk (CT) — The proportionate amount of cross-coupling from an analog input channel to another output channel, expressed in dB.

Digital Input Capacitance (C_{DIG}) — The capacitance between a digital input and ground.

Insertion Loss — Insertion loss measures the amount of signal power absorbed by the switch ON resistance at a given measurement frequency. Insertion loss is defined in decibels as a ratio of the output-voltage amplitude (V_D) versus the input-voltage amplitude (V_S) with a specified load impedance.

$$\text{Insertion Loss (dB)} = 20 \log \frac{|V_D|}{|V_S|}$$

At low frequencies this equation simplifies to:

$$\text{Insertion Loss (dB)} = 20 \log \left(\frac{R_L}{R_L + R_{ON}} \right)$$

Logic "0" Input Current (I_{INL}) — The current flowing into a digital input when a specified low-level voltage is applied to that input.

Logic "0" Input Voltage Level (V_{INL}) — The maximum (or most-positive) digital low-level input voltage for which proper operation of the device is guaranteed.

Logic "1" Input Voltage Level (V_{INH}) — The minimum (or least-positive) digital high-level input voltage for which proper operation of the device is guaranteed.

Negative Voltage Supply (V^-) — The most negative voltage supply with respect to ground.

Positive Voltage Supply (V^+) — The most positive voltage supply with respect to ground.

ANALOG SWITCHES MULTIPLEXERS

OFF Isolation ($I_{SO(OFF)}$) — The proportionate amount of a high-frequency analog input signal which is coupled through the channel of an OFF device. This feedthrough is transmitted through $C_{DS(OFF)}$ to a load comprised of $C_{D(OFF)}$ in parallel with an external load. Isolation generally decreases by 6dB/octave with increasing frequency.

ON Resistance (R_{ON}) — The series ON - channel resistance measured between "S" input and "D" output terminals under specified conditions.

ON Resistance Match ($R_{ON\ Match}$) — The channel-to-channel matching of ON resistance when channels are operated under identical conditions.

$$R_{ON\ Match} = \frac{R_i - R_{AVG}}{R_{AVG}} \times 100\%$$

where

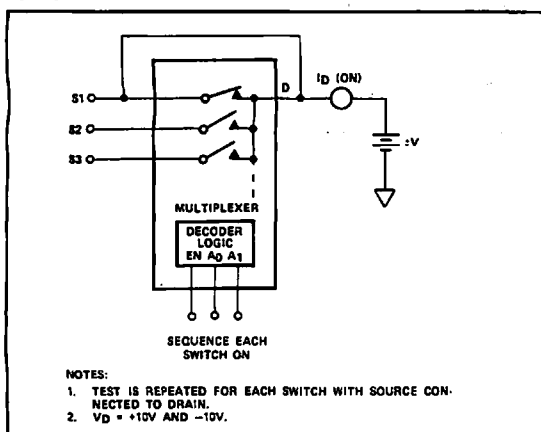
N = # of channels in package (i.e., for MUX-08

$N = 8$, for MUX-16 $N = 16$, etc.)

R_i = Each channel's ON resistance

$$R_{AVG} = \frac{1}{N} \sum_{i=1}^N R_i$$

$I_{(ON)}$ Test Condition Definitions



ON Resistance Variation (ΔR_{ON}) — The variation of ON resistance produced by the specified analog input voltage change with a constant load current.

$$\Delta R_{ON} (\%) =$$

$$\frac{R_{ON} @ V_A = -10V - R_{ON} @ V_A = +10V}{R_{ON} @ V_A = 0V} \times 100\%$$

ON Channel Analog Leakage Current ($I_{D(ON)} + I_{S(ON)}$) Current loss (or gain) through an ON-channel resistance creating a voltage offset across the device. As the direction of current flow is not predictable, only the magnitude is specified at various temperature ranges.

Output Enable Delay Time OFF ($t_{OFF(EN)}$) — **Multiplexers** — The time required to disconnect the analog output from the analog input determined by the digital address input code. It is measured from the 50% point of ENABLE input logic change to the time the output reaches 10% of the initial value.

Output Enable Delay Time ON ($t_{ON(EN)}$) — **Multiplexers** — The time required to connect the analog output to the analog input determined by the digital address input code. It is measured from the 50% point of the ENABLE input logic change to the time the output is within 90% of final value.

Output ON Switching Time (t_{ON}) — The time required to connect the analog output to the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 90% of the final value.

Output OFF Switching Time (t_{OFF}) — The time required to disconnect the analog output from the analog input. The time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

Output Settling Time (t_s) — The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. It is measured from the 50% point of the logic input change to the time the output reaches final value within specified error band.



ANALOG SWITCHES MULTIPLEXERS

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Power Supply Rejection (PSRR) — The ratio of the change in switch contact voltage (V_D) to the change in voltage supply (V_+ or V_-) that causes it.

$$+PSRR \text{ (dB)} = 20 \log \left(\frac{\Delta V_D}{\Delta V_+} \right)$$

$$-PSRR \text{ (dB)} = 20 \log \left(\frac{\Delta V_D}{\Delta V_-} \right)$$

Switching Time (t_{TRAN}) — Multiplexers — The time required to switch and slew from one

analog input channel to another analog input with a full-scale differential between inputs with a high impedance output load. The time is measured from the 50% point of the logic input change to the time the output reaches 80% of the final value.

Total Harmonic Distortion (THD) — The ratio of the signal power at the fundamental frequency to the signal power of all harmonics observed at the switch output (V_D) with a pure sinusoid applied to the switch input (V_S).

ANALOG SWITCHES/MULTIPLEXERS SELECTION GUIDE

One Channel SPST

Product	R_{ON} Max (Ω)	Switching Time (μs)		Logic Input for ON Switch	Logic Levels		Supply Current (mA)	
		t_{ON}	t_{OFF}		V_{INL}	V_{INH}	I+	I-
SW01	100	0.4	0.3	0	0.8	2.0	8.0	4.5
SW02	100	0.4	0.3	1	0.8	2.0	8.0	4.5

4-Channel SPST

Product	R_{ON} Max (Ω)	Switching Time (μs)		Logic Input for ON Switch	Logic Levels		Supply Current (mA)	
		t_{ON}	t_{OFF}		V_{INL}	V_{INH}	I+	I-
SW06	80	0.5	0.4	Note	0.8	2.0	6.0	5.0
SW201	80	0.5	0.4	0	0.8	2.0	9.0	5.0
SW202	80	0.5	0.4	1	0.8	2.0	9.0	5.0
SW7510	75	0.45	0.3	Note	0.8	2.0	9.0	5.0
SW7511	75	0.45	0.3	Note	0.8	2.0	9.0	5.0

NOTE: See individual data sheet for more details.



ANALOG SWITCHES MULTIPLEXERS

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8-Channel MUX

Product	RON Max (Ω)	Transition Time (μ s)	Logic Levels		Supply Current (mA)	
			V _{INL}	V _{INH}	I ₊	I ₋
MUX08	300	2.1	0.7	2.0	12.0	3.8
MUX88	400	2.1	0.8	2.0	15.0	5.0

Dual 4-Channel MUX

Product	RON Max (Ω)	Transition Time (μ s)	Logic Levels		Supply Current (mA)	
			V _{INL}	V _{INH}	I ₊	I ₋
MUX24	300	2.1	0.7	2.0	12.0	3.8

16-Channel MUX

Product	RON Max (Ω)	Transition Time (μ s)	Logic Levels		Supply Current (mA)	
			V _{INL}	V _{INH}	I ₊	I ₋
MUX16	380	2.0	0.7	2.0	19.0	7.0

Dual 8-Channel MUX

Product	RON Max (Ω)	Transition Time (μ s)	Logic Levels		Supply Current (mA)	
			V _{INL}	V _{INH}	I ₊	I ₋
MUX28	380	2.0	0.7	2.0	19.0	7.0

ANALOG SWITCHES/MULTIPLEXERS



SW-01/SW-02

QUAD SPST JFET ANALOG SWITCHES
(TEMPERATURE COMPENSATED R_{ON})

Precision Monolithics Inc.

FEATURES

- Low R_{ON} vs Temperature 0.03%/°C
- Low Absolute R_{ON} 85 Ω
- Low R_{ON} Variation vs Analog Signal 7%
- High Speed 300ns
- Low Leakage Current 0.2nA
- Overvoltage and Supply Loss Protected
- SW-01 Is Improved Pin Compatible Device for DG201, ADG201, LF11201
- SW-02 Is Improved Pin Compatible Device for DG202, LF11202, IH202

ORDERING INFORMATION†

FUNCTION	16-PIN HERMETIC DUAL-IN-LINE PACKAGE	
	MILITARY*	INDUSTRIAL
N.C.	SW01BQ	SW01FQ
N.O.	SW02BQ	SW02FQ

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

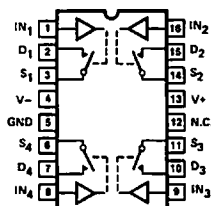
The SW-01/02 are four-channel single-pole, single-throw analog switches which offer operating characteristics unavailable in other JFET or CMOS devices. A unique circuit design provides a nearly constant R_{ON} over the full operating temperature span. R_{ON} drift typically runs under 300ppm/°C.

The SW-01/02 are pin compatible with the DG201/202. An Ion Implanted FET switch inherently exhibits low R_{ON} variations

vs. analog input signals. The junction FET construction also reduces static discharge destruction prevalent in CMOS devices.

Low R_{ON} sensitivity to temperature and voltage is complemented by guaranteed high-speed operation and low-leakage currents. Logic inputs may operate directly from either CMOS or TTL logic levels and are supply voltage independent. The SW-01/02 are protected during supply voltage power loss and against input signal overvoltages.

PIN CONNECTIONS

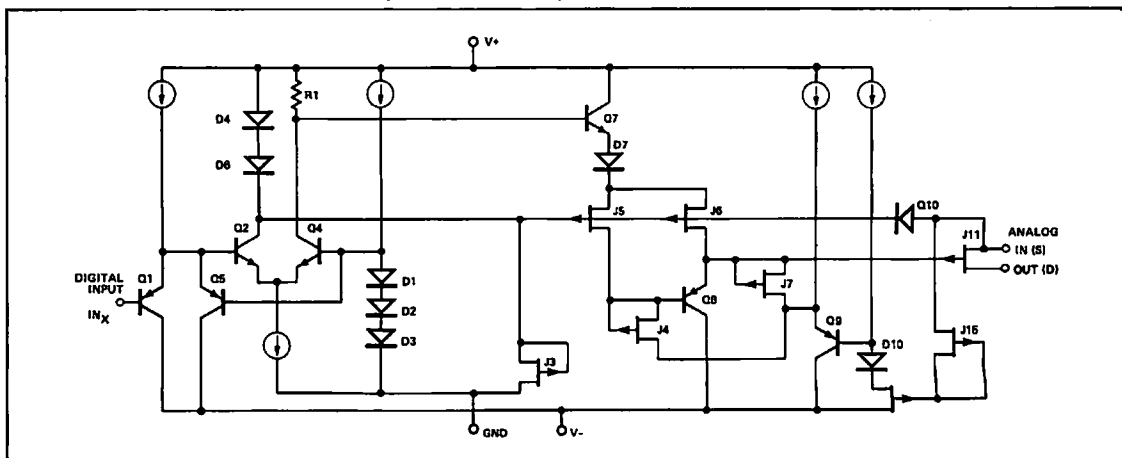


16-PIN DUAL-IN-LINE PACKAGE
(Q-Package)

LOGIC IN _y	CONTROL LOGIC	
	SW-01	SW-02
0	ON	OFF
1	OFF	ON

NOTE: IN_y = INPUT 1-4

SIMPLIFIED SCHEMATIC DIAGRAM (TYPICAL SWITCH)



**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$, unless otherwise noted).

Operating Temperature Range	
SW-01/02BQ	-55°C to $+125^\circ\text{C}$
SW-01/02FQ	-25°C to $+85^\circ\text{C}$
DICE Junction Temperature (T_J)	-65°C to $+150^\circ\text{C}$
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Power Dissipation (Q-Package)	900mW
Lead Temperature (Soldering, 60 sec)	300°C
Maximum Junction Temperature	150°C
V+ Supply to V- Supply	36V
V+ Supply to Ground	36V

Logic Input Voltage	(V- or -4V) to V+ Supply
Analogue Input Voltage	
Continuous	V- Supply -25V to V+ Supply +25V
For $V+ = V- = 0$	$\pm 15\text{V}$
Maximum Current Through Any Pin	30mA
Peak Current,	
(Pulsed at 1ms, 10% Duty Cycle)	70mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15\text{V}$, and $T_A = 25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01/02B			SW-01/02F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$-10\text{V} \leq V_A \leq 10\text{V}$, $I_D \leq 1\text{mA}$	—	85	100	—	85	120	Ω
R_{ON} Match		(Note 1)	—	4	10	—	4	10	%
Analogue Voltage Range	V_A	Full Temperature Range (Note 8)	+10 -10	+11 -15	—	+10 -10	+11 -15	—	V
ΔR_{ON} vs V_A	ΔR_{ON}	$V_A \leq 10\text{V}$, $I_D \leq 1\text{mA}$	—	7	10	—	7	10	%
Analogue Current Range	I_A	$V_A \leq 10\text{V}$	—	5	—	—	5	—	mA
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$	—	0.2	1	—	0.2	2	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$	—	0.2	1	—	0.2	2	nA
Leakage Current in "ON" Condition	$I_{D(ON)}^+$ $I_{S(ON)}$	$V_S = \pm 10\text{V}$, (Note 2)	—	—	1	—	—	2	nA
"OFF" Isolation	ISO_{OFF}	Test Figure 2	—	58	—	—	58	—	dB
Crosstalk	C_T	Test Figure 3	—	70	—	—	70	—	dB
Turn-On-Time	T_{ON}	Test Figure 1, (Note 3)	—	300	400	—	300	400	ns
Turn-Off-Time	T_{OFF}	Test Figure 1, (Note 3)	—	200	300	—	200	300	ns
Break-Before-Make Time	$T_{ON} - T_{OFF}$	Test Figure 1, (Note 7)	—	100	—	—	100	—	ns
Source Capacitance	$C_{S(OFF)}$	$V_A \leq 10\text{V}$	—	7	—	—	7	—	pF
Drain Capacitance	$C_{D(OFF)}$	$V_A \leq 10\text{V}$	—	5.5	—	—	5.5	—	pF
Logic "1" Input Voltage	V_{INH}	Full Temperature Range (Note 8)	2	—	—	2	—	—	V
Logic "0" Input Voltage	V_{INL}	Full Temperature Range (Note 8)	—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$2 \leq V_{IN} \leq 15\text{V}$	—	1	3	—	1	3	μA
Logic "0" Input Current	I_{INL}	$0 \leq V_{IN} \leq 0.8\text{V}$	—	1	3	—	1	3	μA
Positive Supply Current	I^+	(Note 5)	—	6.3	8.0	—	6.3	9.0	mA
Negative Supply Current	I^-	(Note 5)	—	3.2	4.5	—	3.2	5.5	mA
Ground Current	I_G	(Note 5)	—	3.0	4.0	—	3.0	4.5	mA

NOTES:

1. $V_A = 0\text{V}$, $I_D = 100\mu\text{A}$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

- The conditions listed specify the worst case leakage current. The leakage currents apply equally to source or drain.
- Sample tested.
- Parameter tested at $T_A = 125^\circ\text{C}$ for military temperature range device.
- Power supply and ground currents specified for switch "ON" or "OFF". The "OFF" state consumes highest power.
- $TC_R = \frac{R_{ON} @ T_H - R_{ON} @ 25^\circ\text{C}}{R_{ON} @ 25^\circ\text{C} \times (T_H - 25^\circ\text{C})} \times 100$; where $T_H = 125^\circ\text{C}$ for B grade
 $T_H = 85^\circ\text{C}$ for F grade
- Switching is guaranteed by design to be break-before-make.
- Guaranteed by leakage currents and R_{ON} tests. For normal operation analog signal voltages should be restricted to less than $(V^+) - 4\text{V}$.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, and $-55^\circ C \leq T_A \leq +125^\circ C$ for SW-01/02B and $-25^\circ C \leq T_A \leq 85^\circ C$ for SW-01/02F, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01/02B			SW-01/02F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V, I_D \leq 1mA$	—	—	120	—	—	140	Ω
R_{ON} Match		(Note 1)	—	10	15	—	10	15	%
R_{ON} Temperature Coefficient — Average	TC_R	$V_A = 0V, I_D = 100\mu A$, (Note 6)	—	0.03	0.20	—	0.03	0.15	$\%/^\circ C$
Source Current in "OFF" Condition	$I_{S\ OFF}$	$V_S = 10V, V_D = -10V$, (Note 4)	—	—	60	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D\ OFF}$	$V_S = 10V, V_D = -10V$, (Note 4)	—	—	60	—	—	60	nA
Leakage Current in "ON" Condition	$I_{D\ ON} + I_{S\ ON}$	$V_S = \pm 10V$, (Notes 2, 4)	—	—	100	—	—	100	nA
Turn-On-Time	T_{ON}	Test Figure 1, (Note 3)	—	500	600	—	500	600	ns
Turn-Off-Time	T_{OFF}	Test Figure 1, (Note 3)	—	400	500	—	400	500	ns
Break-Before-Make Time	$T_{ON} - T_{OFF}$	Test Figure 1, (Note 7)	—	100	—	—	100	—	ns
Logic "1" Input Current	I_{INH}	$2 \leq V_{IN} \leq 15V$	—	1	5	—	1	5	μA
Logic "0" Input Current	I_{INL}	$0 \leq V_{IN} \leq 0.8V$	—	—	5	—	—	5	μA
Positive Supply Current	I_+	(Note 5)	—	—	11	—	—	12	mA
Negative Supply Current	I_-	(Note 5)	—	—	6	—	—	7	mA
Ground Current	I_G	(Note 5)	—	—	5	—	—	6	mA

NOTES:

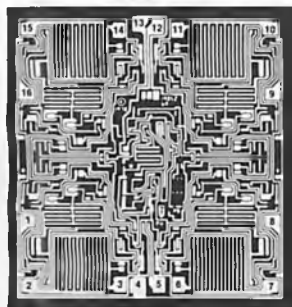
1. $V_A = 0V, I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. The conditions listed specify the worst case leakage current. The leakage currents apply equally to source or drain.
3. Guaranteed by design.
4. Parameter tested at $T_A = 125^\circ C$ for military temperature range device.
5. Power supply and ground currents specified for switch "ON" or "OFF". The "OFF" state consumes highest power.
6. $TC_R = \frac{R_{ON@T_H} - R_{ON@25^\circ C}}{R_{ON@25^\circ C} \times (T_H - 25^\circ C)} \times 100$; where $T_H = 125^\circ C$ for B grade
 $T_H = 85^\circ C$ for F grade
7. Switching is guaranteed by design to be break-before-make.



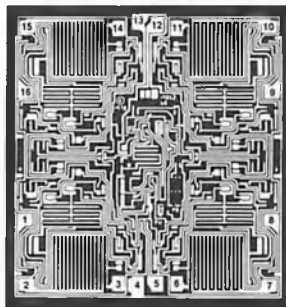
DICE CHARACTERISTICS



SW-01

DIE SIZE 0.101 × 0.097 inch, 9797 sq. mils
(2.565 × 2.464 mm, 6.320 sq. mm)

1. SWITCH (1) ADDRESS (IN1)
2. SWITCH (1) DRAIN (D1)
3. SWITCH (1) SOURCE (S1)
4. NEGATIVE SUPPLY
5. GROUND
6. SWITCH (4) SOURCE (S4)
7. SWITCH (4) DRAIN (D4)
8. SWITCH (4) ADDRESS (IN4)
9. SWITCH (3) ADDRESS (IN3)
10. SWITCH (3) DRAIN (D3)
11. SWITCH (3) SOURCE (S3)
12. NO CONNECTION
13. POSITIVE SUPPLY
14. SWITCH (2) SOURCE (S2)
15. SWITCH (2) DRAIN (D2)
16. SWITCH (2) ADDRESS (IN2)



SW-02

DIE SIZE 0.101 × 0.097 inch, 9797 sq. mils
(2.565 × 2.464 mm, 6.320 sq. mm)

1. SWITCH (1) ADDRESS (IN1)
2. SWITCH (1) DRAIN (D1)
3. SWITCH (1) SOURCE (S1)
4. NEGATIVE SUPPLY
5. GROUND
6. SWITCH (4) SOURCE (S4)
7. SWITCH (4) DRAIN (D4)
8. SWITCH (4) ADDRESS (IN4)
9. SWITCH (3) ADDRESS (IN3)
10. SWITCH (3) DRAIN (D3)
11. SWITCH (3) SOURCE (S3)
12. NO CONNECTION
13. POSITIVE SUPPLY
14. SWITCH (2) SOURCE (S2)
15. SWITCH (2) DRAIN (D2)
16. SWITCH (2) ADDRESS (IN2)

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-01/02N LIMIT	SW-01/02G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_D \leq 1mA$	100	120	Ω MAX
R_{ON} Match		$V_A = 0V$, $I_D \leq 100\mu A$	10	10	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$V_A \leq 10V$, $I_D \leq 1mA$	10	10	% MAX
Positive Supply Current	I_+	(Note 1)	8	9	mA MAX
Negative Supply Current	I_-	(Note 1)	4.5	5.5	mA MAX
Ground Current	I_G		4.0	4.5	mA MAX
Analog Voltage Range	V_A	(Note 2)	± 10	± 10	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 2)	2	2	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 2)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0 \leq V_{IN} \leq 0.8V$	3	3	μA MAX
Logic "1" Input Current	I_{INH}	$2 \leq V_{IN} \leq 15V$	3	3	μA MAX

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ and $T_A = 25^\circ C$, unless otherwise noted.

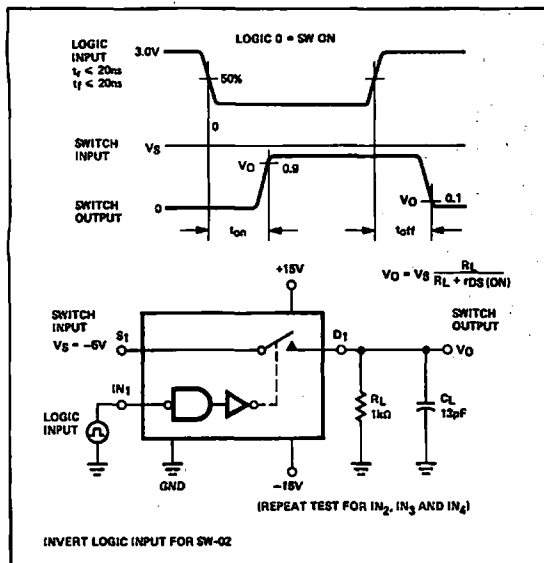
PARAMETER	SYMBOL	CONDITIONS	SW-01/02N TYPICAL	SW-01/02G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-55^\circ C \leq T_A \leq 125^\circ C$	90	90	Ω
R_{ON} Temperature Coefficient	TC_R	$V_A = 0$, $I_D = 100\mu A$	0.03	0.03	%/ $^\circ C$
Turn-On-Time	T_{ON}	$R_L = 1k$, $C_L = 13pF$	300	300	ns
Turn-Off-Time	T_{OFF}	$R_L = 1k$, $C_L = 13pF$	200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.2	0.2	nA
"OFF" Isolation	ISO_{OFF}	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

NOTES:

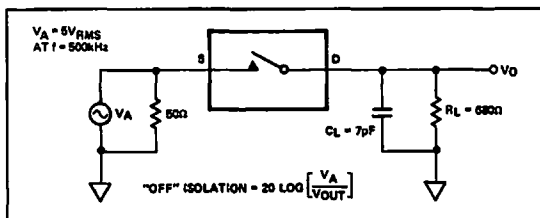
1. Power supply and ground current specified for switch "ON" or "OFF".

2. Guaranteed by R_{ON} and leakage current measurements.

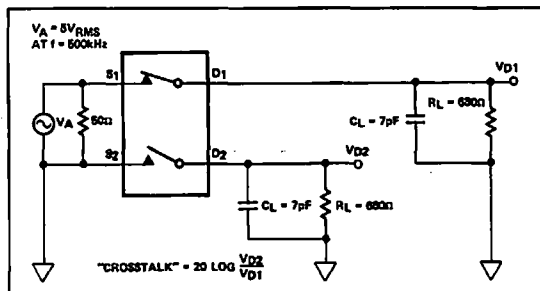
TEST CIRCUITS



TEST FIGURE 1



TEST FIGURE 2



TEST FIGURE 3

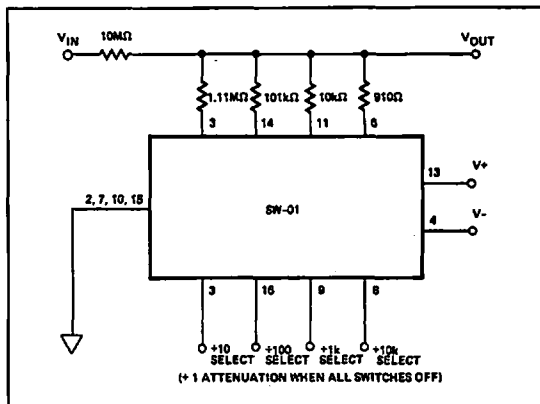
APPLICATIONS INFORMATION

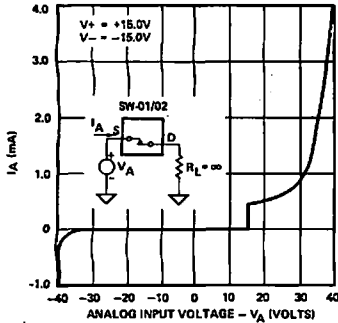
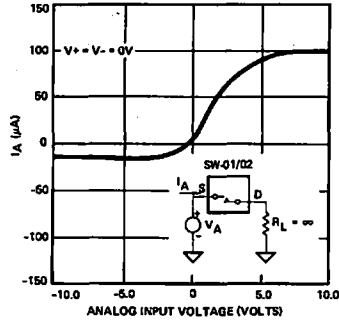
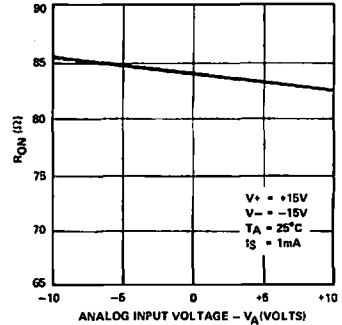
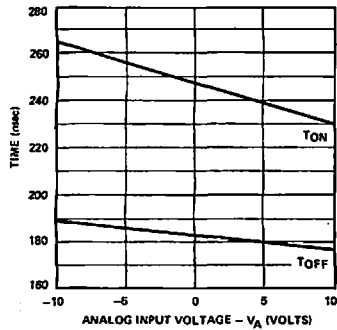
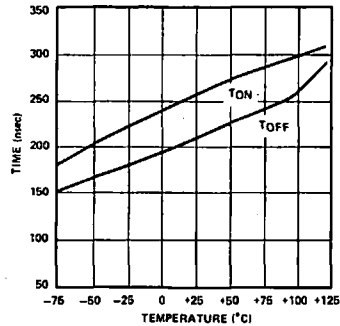
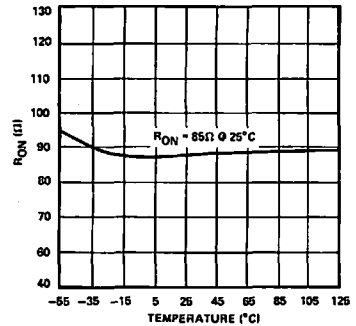
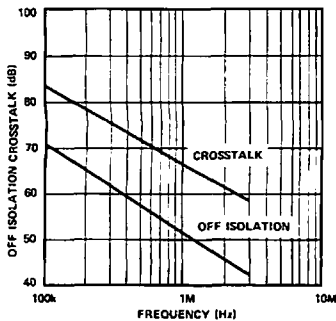
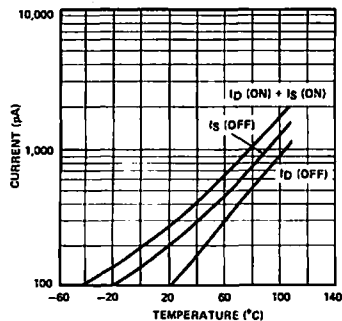
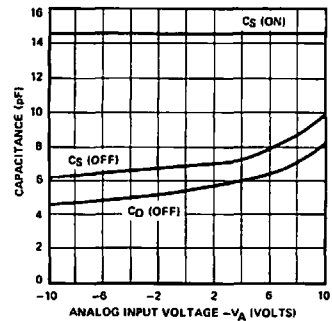
This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_p , and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

Proper switching requires the "Source" terminal to be connected to the input driving signal.

PROGRAMMABLE ATTENUATOR (1 to 0.0001)



**TYPICAL PERFORMANCE CHARACTERISTICS
(SW-01/02)****OVERVOLTAGE
CHARACTERISTIC****POWER SUPPLY
LOSS CHARACTERISTIC****"ON" RESISTANCE vs
ANALOG VOLTAGE (V_A)****SWITCHING TIME vs
ANALOG VOLTAGE****SWITCHING TIMES vs
TEMPERATURE** **R_{ON} vs TEMPERATURE****CROSSTALK AND "OFF"
ISOLATION vs FREQUENCY****LEAKAGE CURRENT vs
TEMPERATURE****SWITCH CAPACITANCE vs
ANALOG VOLTAGE**

ANALOG SWITCHES/MULTIPLEXERS



The SW-01/02 designs have been optimized for low "ON" resistance variation with temperature, signal voltage, and supply voltage changes. Fast switching response and low leakage currents at high temperature are also key performance improvements over older circuit designs.

The static-electricity-resistant JFET switches and additional overvoltage-protection circuitry make the precision switches extremely durable in most application environments.

The SW-01/02 are well suited to applications requiring analog currents $< 5\text{mA}$ with driving source impedances $< 100\Omega$. Applications using op amps, buffers or voltage sources as input drive sources are typical of those fulfilling these conditions. Within the given range of source impedance

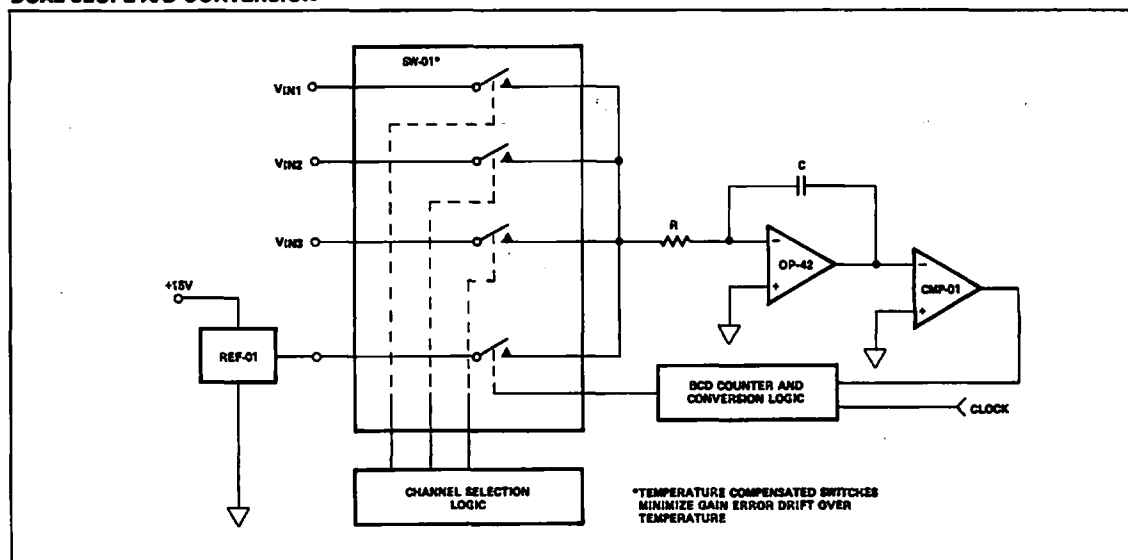
and analog current near ideal signal transfer accuracy is obtainable.

Applications needing very high analog current capability ($> 5\text{mA}$) or where the switch is driven from high source impedances ($> 100\Omega$) should use the SW-201 (Pin Compatible to SW-01) or the SW-202 (Pin Compatible to SW-02) high-current quad switches.

Although the SW-201/202 do not offer the same "ON" resistance temperature coefficient, many other premium characteristics are similar. In addition, the SW-201/202 offer exceptionally low signal distortion over a wide signal voltage and frequency range.

TYPICAL APPLICATIONS

DUAL SLOPE A/D CONVERSION

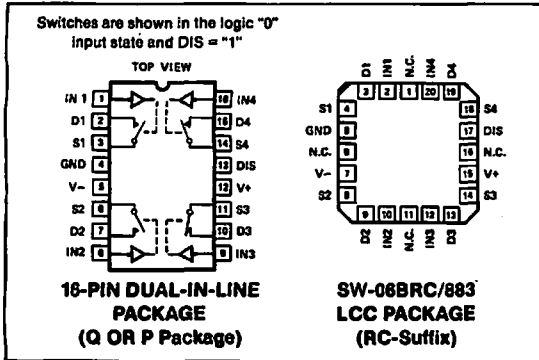


Precision Monolithics Inc.

FEATURES

- Two Normally Open and Two Normally Closed SPST Switches with Disable
- Switches can be Easily Configured as a Dual SPDT or a DPDT
- Highly Resistant to Static Discharge Destruction
- Higher Resistance to Radiation Than Analog Switches Designed with MOS Devices
- Guaranteed R_{ON} Matching 10% Max
- Guaranteed Switching Speeds $T_{ON} = 500ns$ Max
..... $T_{OFF} = 400ns$ Max
- Guaranteed Break-Before-Make Switching
- Low "ON" Resistance 80Ω Max
- Low R_{ON} Variation from Analog Input Voltage 5%
- Low Total Harmonic Distortion 0.01%
- Low Leakage Currents at High Temperature:
 $T_A = 125^\circ C$ 100nA Max
 $T_A = 85^\circ C$ 30nA Max
- Digital Inputs TTL/CMOS Compatible and Independent of $V+$
- Improved Specifications and Pin Compatible to LF-11333/13333
- Dual or Single Power Supply Operation

PIN CONNECTIONS



ORDERING INFORMATION†

PLASTIC DIP	HERMETIC DIP	LCC	OPERATING TEMPERATURE RANGE
—	SW06BQ*	SW06BRC/883	MIL
—	SW06FQ	—	IND
SW06GP	—	—	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

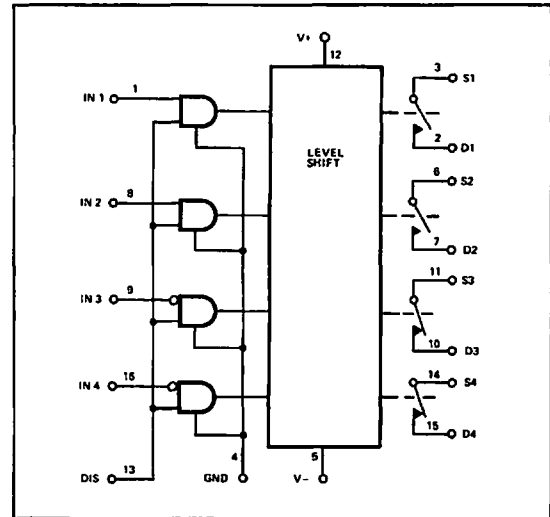
GENERAL DESCRIPTION

The SW-06 is a four channel single-pole, single-throw analog switch that employs both bipolar and ion-implanted FET devices. The SW-06 FET switches use bipolar digital logic inputs which are more resistant to static electricity than CMOS devices. Ruggedness and reliability are inherent in the SW-06 design and construction technology.

Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With $V+ = 36V$, $V- = 0V$, the analog signal range will extend from ground to +32V.

PNP logic inputs are TTL and CMOS compatible to allow the SW-06 to upgrade existing designs. The logic "0" and logic "1" input currents are at micro-ampere levels reducing loading on CMOS and TTL logic.

FUNCTIONAL DIAGRAM



TRUTH TABLE

DISABLE INPUT	LOGIC INPUT	SWITCH STATE	
		CHANNELS 1 & 2	CHANNELS 3 & 4
0	X	OFF	OFF
1 or NC	0	OFF	ON
1 or NC	1	ON	OFF

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Operating Temperature Range

SW-06BQ, BRC -55°C to +125°C

SW-06FQ -25°C to +85°C

SW-06GP 0°C to +70°C

Storage Temperature Range -65°C to +150°C

Power Dissipation (Note 2)

Q Package 900mW

P Package 500mW

Lead Temperature (Soldering 60 sec) 300°C

Maximum Junction Temperature 150°C

V+ Supply to V- Supply 36V

V+ Supply to Ground 36V

Logic Input Voltage (-4V or V-) to V+ Supply

Analog Input Voltage Range

Continuous V- Supply to V+ Supply +20V

Maximum Current Through

Any Pin Including Switch 30mA

NOTES:

1. Absolute ratings apply to both DiCE and packaged parts, unless otherwise noted.

2. Q Package derated 12mW/°C above 75°C, P Package derated 10mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS at V+ = 15V, V- = -15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06B			SW-06F			SW-06G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R _{ON}	V _S = 0V, I _S = 1mA V _S = ±10V, I _S = 1mA	—	60	80	—	60	100	—	100	150	Ω
R _{ON} Match Between Switches	R _{ON} Match	V _S = 0V, I _S = 100μA (Note 1)	—	5	10	—	5	20	—	—	20	%
Analog Voltage Range	V _A	I _S = 1mA (Note 8) I _S = 1mA	+10	+11	—	+10	+11	—	+10	+11	—	V
Analog Current Range	I _A	V _S = ±10V	10	15	—	7	12	—	5	10	—	mA
ΔR _{ON} vs Applied Voltage	ΔR _{ON}	-10V ≤ V _S ≤ 10V, I _S = 1.0mA	—	5	15	—	10	20	—	10	20	%
Source Current in "OFF" Condition	I _{S(OFF)}	V _S = 10V, V _D = -10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Drain Current in "OFF" Condition	I _{D(OFF)}	V _S = 10V, V _D = -10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Source Current in "ON" Condition	I _{S(ON)} + I _{D(ON)}	V _S = V _D = ±10V (Note 5)	—	0.3	2.0	—	0.3	2.0	—	0.3	10	nA
Logical "1" Input Voltage	V _{INH}	Full Temperature Range (Notes 6, 8)	2.0	—	—	2.0	—	—	2.0	—	—	V
Logical "0" Input Voltage	V _{INL}	Full Temperature Range (Notes 6, 8)	—	—	0.8	—	—	0.8	—	—	0.8	V
Logical "1" Input Current	I _{INH}	V _{IN} = 2.0V to 15.0V (Note 4)	—	—	5	—	—	5	—	—	10	μA
Logical "0" Input	I _{INL}	V _{IN} = 0.8V	—	1.5	5.0	—	1.5	5.0	—	1.5	10.0	μA
Turn-On-Time	t _{ON}	See Switching Time Test Circuit (Notes 6, 9)	—	340	500	—	340	600	—	340	700	ns
Turn-Off-Time	t _{OFF}	See Switching Time Test Circuit (Notes 6, 9)	—	200	400	—	200	400	—	200	500	ns
Break-Before-Make Time	t _{ON} -t _{OFF}	(Note 3)	50	140	—	50	140	—	50	140	—	ns
Source Capacitance	C _{S(OFF)}	V _S = 0V (Note 5)	—	7.0	—	—	7.0	—	—	7.0	—	pF
Drain Capacitance	C _{D(OFF)}	V _S = 0V (Note 5)	—	5.5	—	—	5.5	—	—	5.5	—	pF
Channel "ON" Capacitance	C _{D(ON)} + C _{S(ON)}	V _S = V _D = 0V (Note 5)	—	15	—	—	15	—	—	15	—	pF
"OFF" Isolation	I _{SO(OFF)}	V _S = 5V _{RMS} , R _L = 680Ω, C _L = 7pF, f = 500kHz (Note 5)	—	58	—	—	58	—	—	58	—	dB
Crosstalk	C _T	V _S = 5V _{RMS} , R _L = 680Ω, C _L = 7pF, f = 500kHz (Note 5)	—	70	—	—	70	—	—	70	—	dB
Positive Supply Current	I+	All Channels "OFF", DIS = "0" (Note 5)	—	5.0	6.0	—	5.0	9.0	—	6.0	9.0	mA
Negative Supply Current	I-	All Channels "OFF", DIS = "0" (Note 5)	—	3.0	5.0	—	4.0	7.0	—	4.0	7.0	mA
Ground Current	I _G	All Channels "ON" or "OFF" (Note 5)	—	3.0	4.0	—	3.0	4.0	—	3.0	5.0	mA



ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for SW-06BQ, $-25^\circ C \leq T_A \leq +85^\circ C$ for SW-06FQ and $0^\circ C \leq T_A \leq 70^\circ C$ for SW-06GP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06B			SW-06F			SW-06G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Temperature Range	T_A	Operating	-55	—	125	-25	—	85	0	—	70	$^\circ C$
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 1.0mA$	—	75	110	—	75	125	—	75	175	Ω
		$V_S = \pm 10V$, $I_S = 1.0mA$	—	80	110	—	80	125	—	80	175	
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 100\mu A$ (Note 1)	—	6	20	—	6	25	—	10	—	%
Analog Voltage Range	V_A	$I_S = 1.0mA$ (Note 8)	+10	+11	—	+10	+11	—	+10	+11	—	V
		$I_S = 1.0mA$	-10	-15	—	-10	-15	—	-10	-15	—	
Analog Current Range	I_A	$V_S = \pm 10.0V$	7	12	—	5	11	—	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq +10V$, $I_S = 1.0mA$	—	10	—	—	12	—	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V$, $V_O = -10V$, $T_A = \text{Max. Operating Temp.}$ (Notes 5, 7)	—	—	60	—	—	30	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_O = -10V$, $T_A = \text{Max. Operating Temp.}$ (Notes 5, 7)	—	—	60	—	—	30	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_O = \pm 10V$, $T_A = \text{Max. Operating Temp.}$ (Notes 5, 7)	—	—	100	—	—	30	—	—	60	nA
Logical "1" Input Current	I_{INH}	$V_{IN} = 2.0V$ to $15.0V$ (Note 4)	—	—	10	—	—	10	—	—	15	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8V$	—	4	10	—	4	10	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit (Notes 2, 6)	—	440	900	—	500	900	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit (Notes 2, 6)	—	300	500	—	330	500	—	—	500	ns
Break-Before-Make Time	$t_{ON} - t_{OFF}$	(Note 3)	—	70	—	—	70	—	—	50	—	ns
Positive Supply Current	I_+	All Channels "OFF" OIS = "0" (Note 5)	—	—	9.0	—	—	13.5	—	—	13.5	mA
Negative Supply Current	I_-	All Channels "OFF" DIS = "0" (Note 5)	—	—	7.5	—	—	10.5	—	—	10.5	mA
Ground Current	I_G	All Channels "ON" or "OFF" (Note 5)	—	—	6.0	—	—	7.5	—	—	7.5	mA

NOTES:

1. $V_S = 0V$, $I_S = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. Guaranteed by design.

3. Switch is guaranteed by design to provide break-before-make operation.

4. Current tested at $V_{IN} = 2.0V$. This is worst case condition.

5. Switch being tested ON or OFF as indicated, $V_{INH} = 2.0V$ or $V_{INL} = 0.8V$, per logic truth table.

6. Also applies to disable pin.

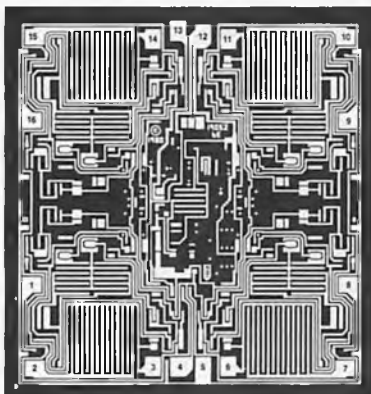
7. Parameter tested only at $T_A = +125^\circ C$ for military grade device.

8. Guaranteed by R_{ON} and leakage tests. For normal operation maximum analog signal voltages should be restricted to less than $(V_+) - 4V$.

9. Sample tested.



DICE CHARACTERISTICS



DIE SIZE 0.101×0.097 inch, 9797 sq. mils
(2.565×2.464 mm, 6.320 sq. mm)

1. IN (1)
2. D (1)
3. S (1)
4. GND
5. V- (SUBSTRATE)
6. S (2)
7. D (2)
8. IN (2)
9. IN (3)
10. D (3)
11. S (3)
12. V+
13. DISABLE
14. S (4)
15. D (4)
16. IN (4)

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = 15V$, $V_- = -15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-06N LIMIT	SW-06G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	80	100	Ω MAX
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V$, $I_S \leq 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	10	20	% MAX
Positive Supply Current	I_+	(Note 1)	6.0	9.0	mA MAX
Negative Supply Current	I_-	(Note 1)	5.0	7.0	mA MAX
Ground Current	I_G	(Note 1)	4.0	4.0	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$	± 10.0	± 10.0	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 3)	2.0	2.0	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 3)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \leq V_{IN} \leq 0.8V$	5.0	5.0	μA MAX
Logic "1" Input Current	I_{INH}	$2.0V \leq V_{IN} \leq 15V$ (Note 2)	5	5	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $T_A = 25^\circ C$, unless otherwise noted.

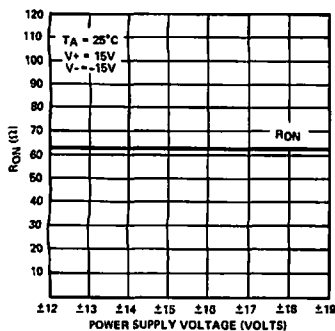
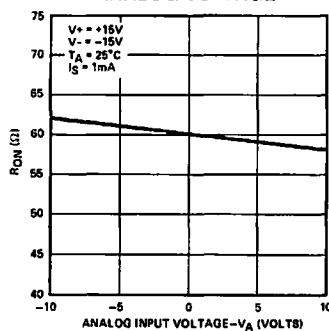
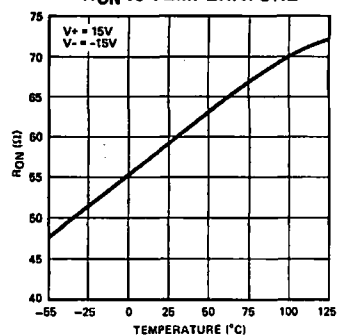
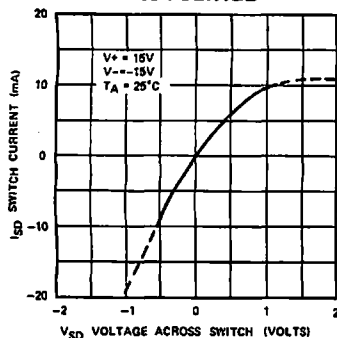
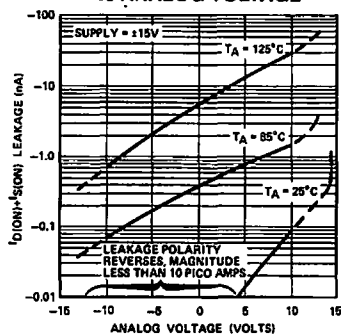
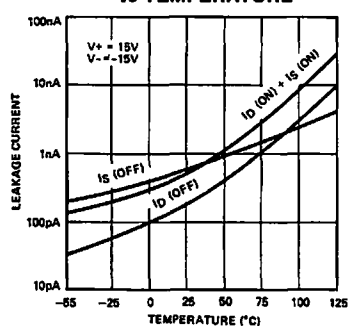
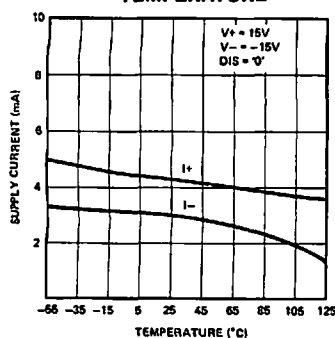
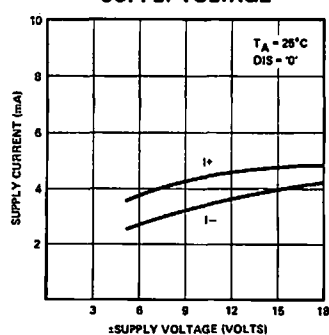
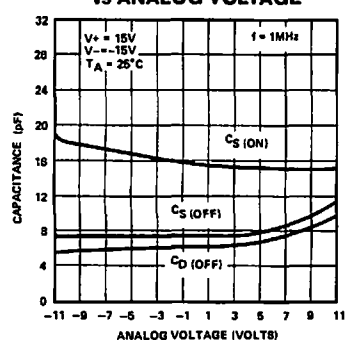
PARAMETER	SYMBOL	CONDITIONS	SW-06N TYPICAL	SW-06G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SO(OFF)}$	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

NOTES:

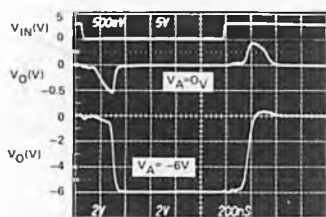
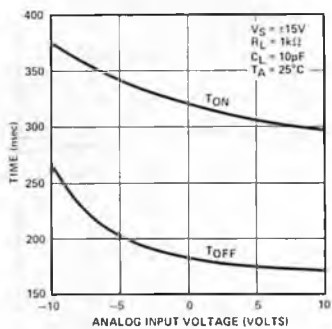
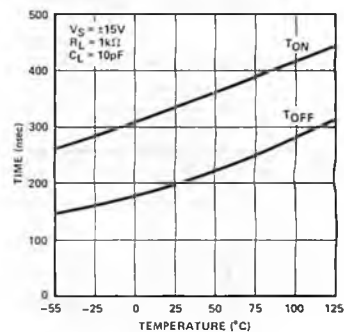
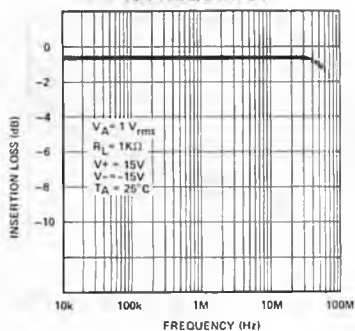
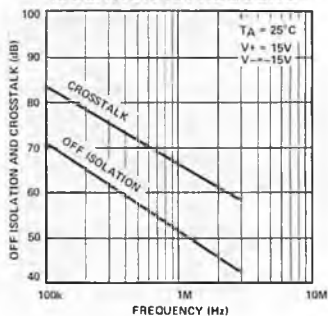
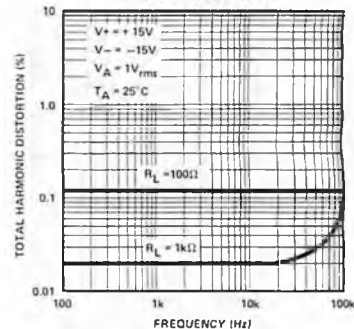
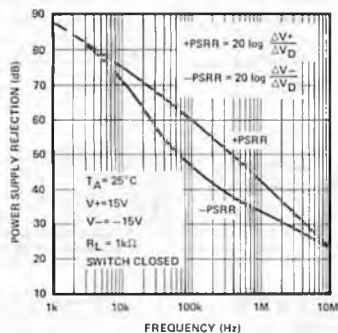
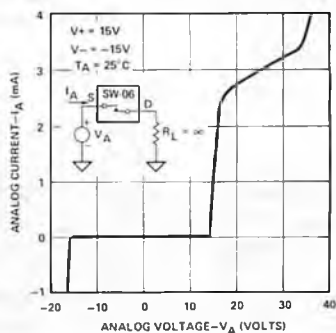
1. Power supply and ground current specified for switch "ON" or "OFF".
2. Current tested at $V_{IN} = 2.0V$. This is worst case condition.
3. Guaranteed by R_{ON} and leakage tests.



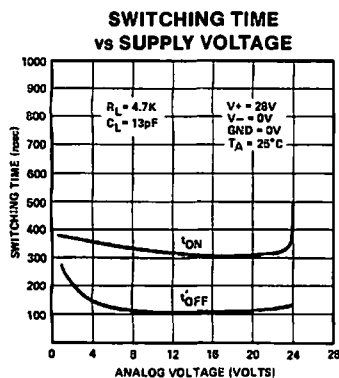
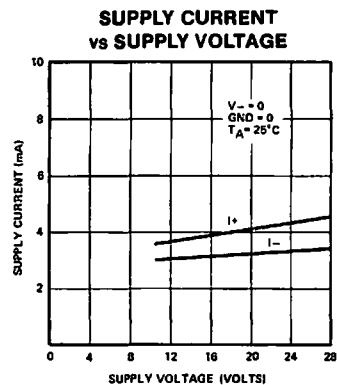
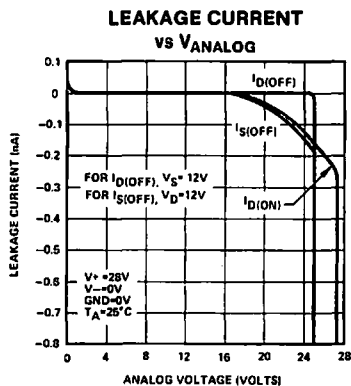
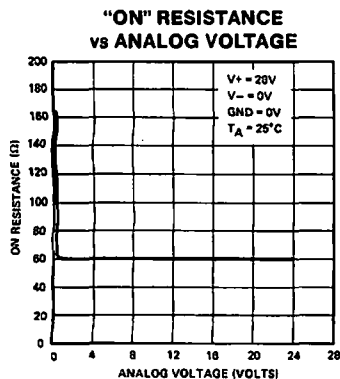
TYPICAL PERFORMANCE CHARACTERISTICS

**"ON" RESISTANCE vs
POWER SUPPLY VOLTAGE****"ON" RESISTANCE vs
ANALOG VOLTAGE** **R_{ON} vs TEMPERATURE****SWITCH CURRENT
vs VOLTAGE****LEAKAGE CURRENT
vs ANALOG VOLTAGE****LEAKAGE CURRENT
vs TEMPERATURE****SUPPLY CURRENT vs
TEMPERATURE****SUPPLY CURRENT vs
SUPPLY VOLTAGE****SWITCH CAPACITANCE
vs ANALOG VOLTAGE**

TYPICAL PERFORMANCE CHARACTERISTICS

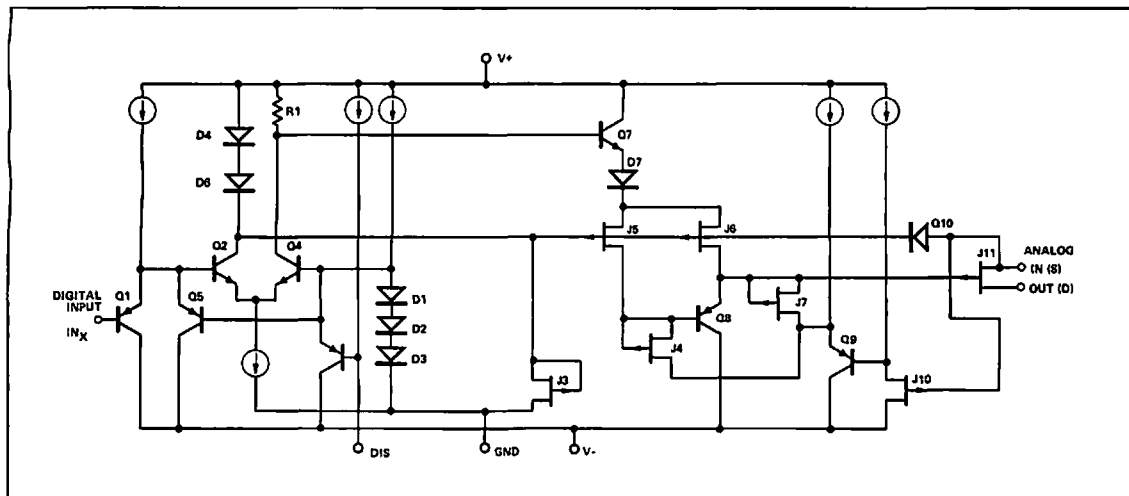
 **T_{ON}/T_{OFF}
SWITCHING RESPONSE**

**SWITCHING TIME
vs ANALOG VOLTAGE**

**SWITCHING TIME
vs TEMPERATURE**

**INSERTION LOSS
vs FREQUENCY**

**CROSSTALK AND "OFF"
ISOLATION vs FREQUENCY**

**TOTAL HARMONIC
DISTORTION**

**POWER SUPPLY REJECTION
vs FREQUENCY**

**OVERVOLTAGE
CHARACTERISTICS**


TYPICAL PERFORMANCE CHARACTERISTICS (OPERATING SINGLE SUPPLY)

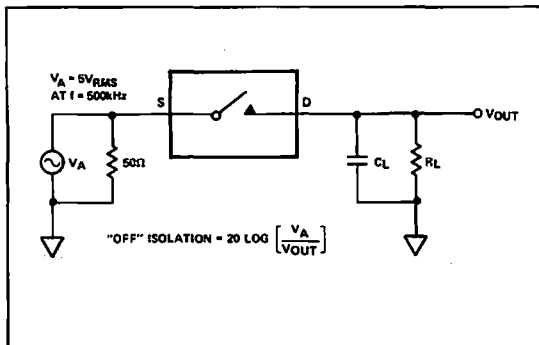


NOTE: These single-supply-operation characteristic curves are valid when the negative power supply V_- is tied to the logic ground reference pin "GND". TTL input compatibility is still maintained when "GND" is the same potential as the TTL ground. t_{OFF} is measured from 50% of logic input waveform to $0.9 V_O$. The analog voltage range extends from 0 to $V_+ - 4V$, the switch will no longer respond to logic control when V_A is within 4 volts of V_+ .

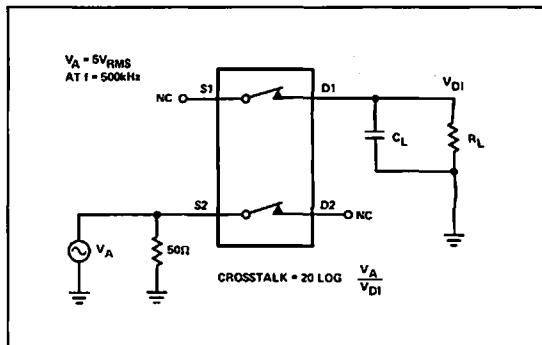
SIMPLIFIED SCHEMATIC DIAGRAM (TYPICAL SWITCH)



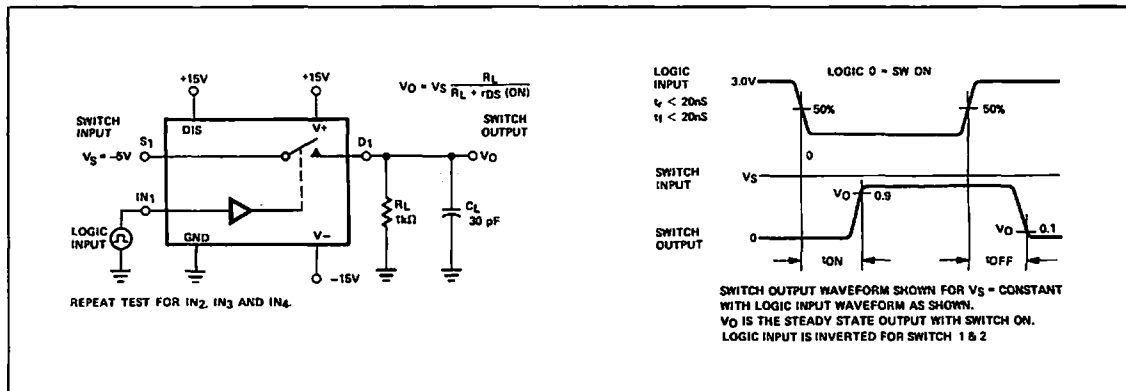
OFF ISOLATION TEST CIRCUIT



CROSSTALK TEST CIRCUIT



SWITCHING TIME TEST CIRCUIT



ANALOG CURRENT

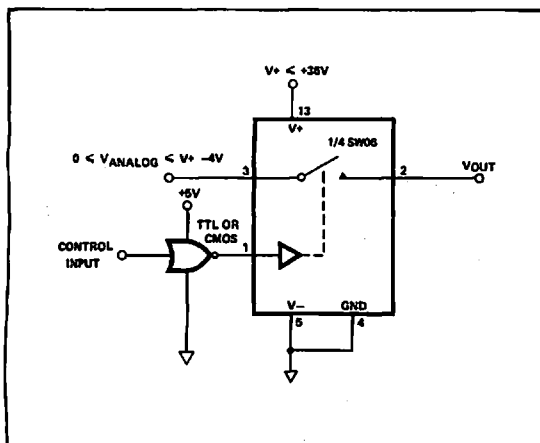
The analog switches in the ON state are JFETs biased in their triode region and act as switches for analog current up to the I_A specification (see plot of I_{DS} vs V_{DS}). Some applications require pulsed currents exceeding the I_A spec. For example, an integrator reset switch discharging a shunt capacitor will produce a peak current of $I_{A(PEAK)} = V_{CAP}/R_{OS(ON)}$. In this application, it is best to connect the source to the most positive end of the capacitor, thereby achieving the lowest switch resistance and fastest reset times. The switch can easily handle any amount of capacitor discharge current subject only to the maximum heat dissipation of the package and the maximum operating junction temperature from which repetition rates can be established.

SWITCHING

Switching time t_{ON} and t_{OFF} characteristics are plotted versus V_{ANALOG} and temperature. In all cases, t_{OFF} is designed faster than t_{ON} to insure a break-before-make interval for SPDT and DPDT applications. The disable input (DIS) has the same switching times (t_{ON} and t_{OFF}) as the logic inputs (IN_X).

TYPICAL APPLICATIONS

OPERATION FROM SINGLE POSITIVE POWER SUPPLY



Switching transients occurring at the source and drain contacts results from AC coupling of the switching FETs gate-to-source and gate-to-drain coupling capacitance. The switch turn ON will cause a negative going spike to occur and the turn OFF will cause a positive spike to occur. These spikes can be reduced by additional capacitance loading, lower values of R_L , or switching an additional switch (with its extra contact floating) to the opposite state connected to the spike sensitive node.

DISABLE NODE

This TTL compatible node is similar to the logic inputs IN_X but has an internal $2\mu A$ current source pull-up. If disable is left unconnected, it will assume the logic "1" state, then the state of the switches is controlled only by the logic inputs IN_X .

POWER SUPPLIES

This product operates with power supply voltages ranging from ± 12 to ± 18 volts; however, the specifications only guarantee device parameters with ± 15 volt $\pm 5\%$ power supplies. The power supply sensitive parameters have plots to indicate effects of supply voltages other than ± 15 volts.

4-CHANNEL SAMPLE HOLD AMPLIFIER

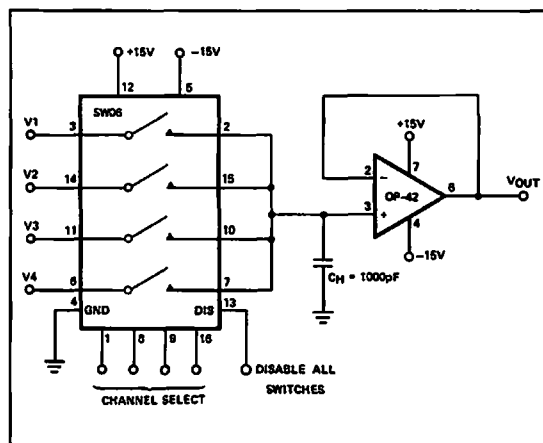
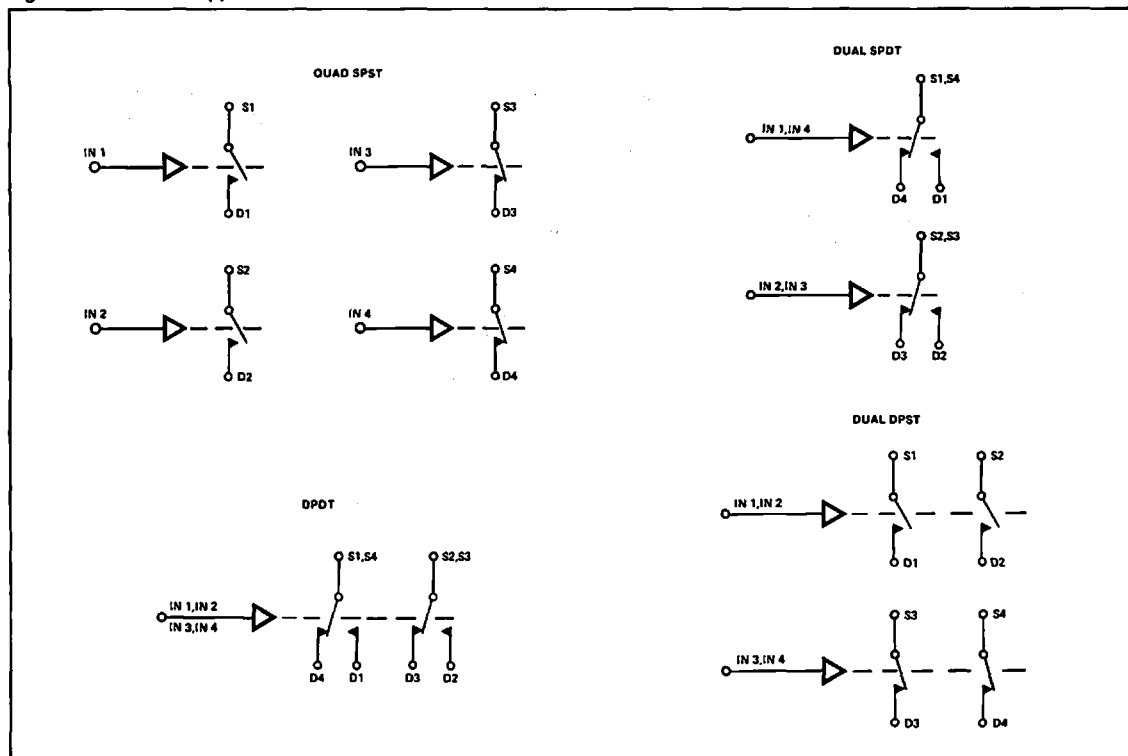


Figure 1: Functional Applications of SW-06



APPLICATIONS INFORMATION

This single analog switch product configures, by appropriate pin connections, into four switch applications. As shown in Figure 1, the SW-06 connects as a QUAD SPST, a DUAL SPDT, a DUAL DPST, or a DPDT analog switch. This versatility increases further when taking advantage of the disable input (DIS) which turns all switches OFF when taken active low.

Ion-implantation of the JFET analog switch achieves low ON resistance and tight channel to channel matching. Combining the low ON resistance and low leakage currents results in a worst case voltage error figure $V_{\text{ERROR @ } 125^{\circ}\text{C}} = I_{\text{D(ON)}} \times R_{\text{SD(ON)}} = 100\text{nA} \times 100\Omega = 11 \text{ microvolts}$. This amount of error is negligible considering dissimilar-metal thermally-induced offsets will be in the 5 to 15 microvolt range.

LOGIC INPUTS

The logic inputs (IN_x) and disable input (DIS) are referenced to a TTL logic threshold value of two forward diode drops (1.4V at 25°C) above the GND terminal. These inputs use PNP transistors which draw maximum current at a logic "0" level and drops to a leakage current of a reverse biased diode as the logic input voltage raises above 1.4 volts. Any logic input voltage greater than 2.0 volts becomes logic "1", less than 0.8 volts becomes logic "0" resulting in full TTL noise immunity not available from similar CMOS input analog

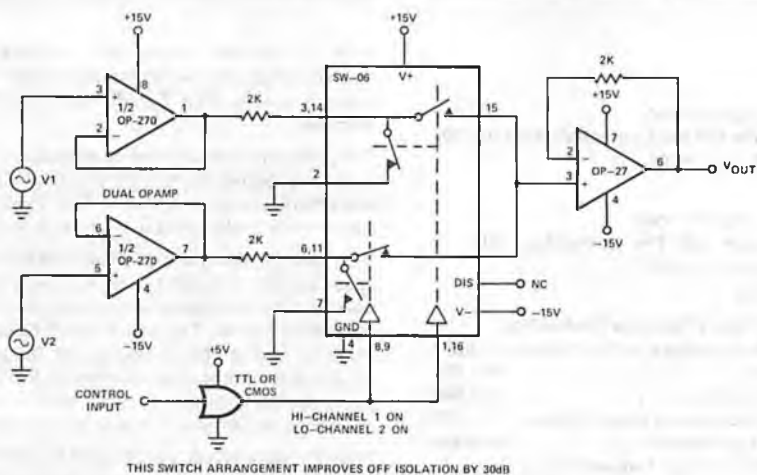
switches. The PNP transistor inputs require such low input current that the SW-06 approaches fan-ins of CMOS input devices. These bipolar logic inputs exceed any CMOS input circuit in resistance to static voltage and radiation susceptibility. No damage will occur to the SW-06 if logic high voltages are present when the SW-06 power supplies are OFF. When the V+ and V- supplies are OFF, the logic inputs present a reverse bias diode loading to active logic inputs. Input logic thresholds are independent of V+ and V- supplies making single V+ supply operation possible by simply connecting GND and V- together to the logic ground supply.

ANALOG VOLTAGE AND CURRENT

ANALOG VOLTAGE

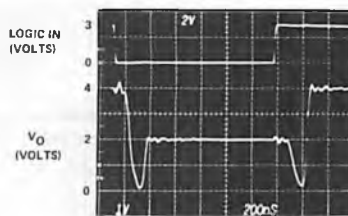
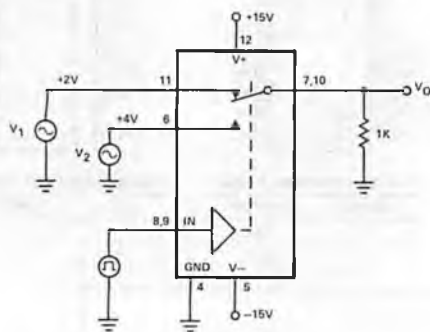
These switches have constant ON resistance for analog voltages from the negative power supply (V-) to within 4 volts of the positive power supply. This characteristic shown in the plots results in good total harmonic distortion, especially when compared to CMOS analog switches that have a 20 to 30 percent variation in ON resistance versus analog voltage. Positive analog input voltages should be restricted to 4 volts less than V+ assuring the switch remains open circuit in the OFF state. No increase in switch ON resistance occurs when operating at supply voltages less than ±15 volts (see plot). Small signals have a 3dB down frequency of 70MHz (see insertion loss versus frequency plot).

HIGH OFF ISOLATION SELECTOR SWITCH (Shunt-Series Switch)



THIS SWITCH ARRANGEMENT IMPROVES OFF ISOLATION BY 30dB

SINGLE POLE DOUBLE THROW SELECTOR SWITCH WITH BREAK-BEFORE-MAKE INTERVAL



During the BBM interval the $1\text{k}\Omega$ resistor pulls the output to ground assuring that no shorting between V_1 and V_2 occurs.



SW-201/SW-202

QUAD SPST JFET
ANALOG SWITCHES

Precision Monolithics Inc.

FEATURES

SW-201

- Normally "ON" for Logic 0 Input
- Improved Performance and Pin Compatible With DG-201, LF11201/13201, HI201, and IH201

SW-202

- Normally "OFF" for Logic 0 Input
- Improved Performance and Pin Compatible With LF11202/12202/13202 and IH202

Both SW-201 and SW-202

- Highly Resistant to Static Discharge Destruction
- Guaranteed Break-Before-Make Switching ($t_{OFF} < t_{ON}$)
- Low "ON" Resistance 80Ω Max
- Guaranteed R_{ON} Matching 15% Max
- Low R_{ON} Variation from Analog Input Voltage 5%
- High Analog Current Operation 10mA Min
- Low Leakage Currents at High Temperatures:
 $T_A = 125^\circ\text{C}$ 60nA Max
 $T_A = 85^\circ\text{C}$ 30nA Max
- Guaranteed Switching Speeds:
 $t_{ON} = 500\text{ns}$ Max $t_{OFF} = 400\text{ns}$ Max
- Digital Inputs are TTL and CMOS Compatible
- Dual or Single Supply Operation

ORDERING INFORMATION†

DIP PACKAGE	SWITCH CONFIGURATION		OPERATING TEMPERATURE RANGE
	NC	NO	
16-PIN EPOXY	SW201GP	SW202GP	COM

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The SW-201 and SW-202 each consist of four independent, single-pole, single-throw (SPST) analog switches, which may be independently digitally controlled. Each SW-201

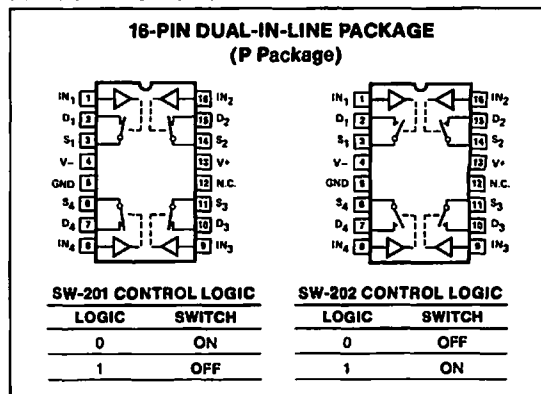
switch is normally closed (NC), whereas each SW-202 is normally open (NO) when the corresponding digital control input is a zero. The SW-201 and SW-202 are otherwise identical.

The judicious combination of bipolar and FET devices in a single monolithic IC results in a product with performance characteristics and ruggedness that are superior to those of a similar circuit fabricated using CMOS technology.

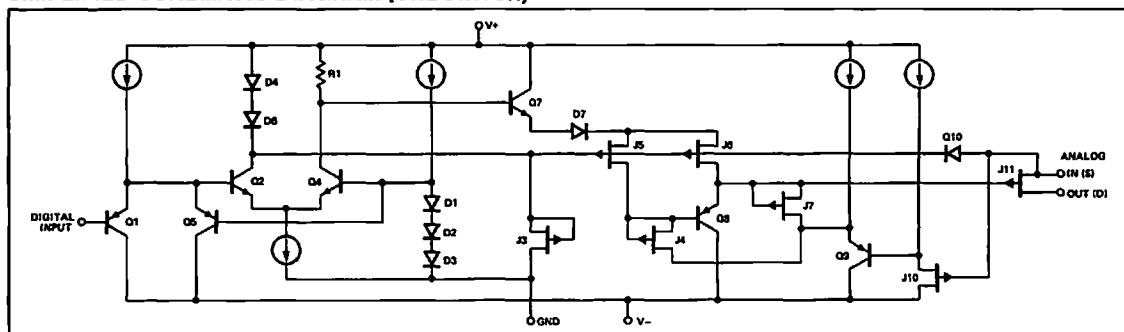
Increased reliability is complemented by excellent electrical specifications. Potential error sources are reduced by minimizing "ON" resistance and controlling leakage currents at high temperatures. The switching FET exhibits minimal R_{ON} variation over a 20V analog signal range and with power supply voltage changes. Operation from a single positive power supply voltage is possible. With $V^+ = 36\text{V}$, $V^- = 0\text{V}$, the analog signal range will extend from ground to +32V.

The PNP logic inputs are TTL and CMOS compatible. Logic input currents are at micro-ampere levels which improves circuit fan in.

PIN CONNECTIONS



SIMPLIFIED SCHEMATIC DIAGRAM (ONE SWITCH)



Manufactured under the following patent: 4,228,367

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Operating Temperature Range	SW-201GP, SW-202GP	0°C to +70°C
DICE Junction Temperature (T_J)		-65°C to +150°C
Storage Temperature Range		-65°C to +150°C
P-Suffix		-65°C to +125°C
Power Dissipation (Note 2)		900mW
Lead Temperature (Soldering, 60 sec)		300°C
Maximum Junction Temperature		150°C
V+ Supply to V- Supply		36V
V+ Supply to Ground		36V
Logic Input Voltage		(-4V or V-) to V+ Supply

Analog Input Voltage Range

Continuous	V- Supply to V+ Supply +20V
1% Duty Cycle and Driving all 4 Inputs with 500μsec pulse	V- Supply -15V to V+ Supply +20V
Maximum Current Through Any Pin	30mA

NOTES:

1. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Derated 12mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS at $V_{\pm} = \pm 15V$ and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201G SW-202G			UNITS
			MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_A = 0V, I_S = 1mA$ $V_A = \pm 10V, I_S = 1mA$	—	100	150	Ω
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V, I_D = 100\mu A$; (Note 1)	—	—	20	%
Analog Voltage Range	V_A	$I_S = 1.0mA$ (Note 6) $I_S = 1.0mA$	+10 -10	+11 -15	—	V
Analog Current Range	I_A	$V_S = \pm 10V$	5	10	—	mA
ΔR_{ON} vs Applied Voltage	ΔR_{ON}	$V_S \leq 10V, I_S = 1mA$	—	10	20	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$; (Note 5)	—	—	10	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$; (Note 5)	—	—	10	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = \pm 10V$; (Note 5)	—	—	10	nA
Logical "1" Input Current	I_{INH}	$V_{IN} = 2V$ to $15V$; (Note 4)	—	—	10	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8$	—	1.5	10.0	μA
Turn-On-Time	t_{ON}	See Switching Time Test Circuit; (Note 7)	—	340	700	ns
Turn-Off-Time	t_{OFF}	See Switching Time Test Circuit; (Note 7)	—	200	500	ns
Break-Before-Make Time	$t_{ON} - t_{OFF}$	(Note 3)	50	140	—	ns
Source Capacitance	$C_{S(OFF)}$	$V_A = 0V$; (Note 5)	—	7	—	pF
Drain Capacitance	$C_{D(OFF)}$	$V_A = 0V$; (Note 5)	—	5.5	—	pF
Channel "ON" Capacitance	$C_{D(ON)} + C_{S(ON)}$	$V_S = V_D = 0V$; (Note 5)	—	15	—	pF
"OFF" Isolation	$I_{SO(OFF)}$	$V_S = 5V_{RMS}, R_L = 680\Omega$, $C_L = 7pF, f = 500kHz$; (Note 5)	—	58	—	dB
Crosstalk	C_T	$V_S = 5V_{RMS}, R_L = 680\Omega$, $C_L = 7pF, f = 500kHz$; (Note 5)	—	70	—	dB
Positive Supply Current	I_+	All Channels "ON"; (Note 5)	—	4	12	mA
Negative Supply Current	I_-	All Channels "ON"; (Note 5)	—	1	6.5	mA
Positive Supply Current	I_+	All Channels "OFF"; (Note 5)	—	6	12	mA
Negative Supply Current	I_-	All Channels "OFF"; (Note 5)	—	4	8	mA
Ground Current	I_G	All Channels "ON" or "OFF"	—	3	6	mA

**ELECTRICAL CHARACTERISTICS** at $V_{\pm} = \pm 15V$; $0^{\circ}C \leq T_A \leq 70^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201G SW-202G			UNITS
			MIN	TYP	MAX	
Temperature Range	T_A	Operating	0	—	70	$^{\circ}C$
"ON" Resistance	R_{ON}	$V_A = 0V, I_D = 1mA$ $V_A = \pm 10V, I_D = 1mA$	—	—	175	Ω
R_{ON} Match Between Switches	R_{ON} Match	$V_A = 0V, I_D = 100\mu A$; (Note 1)	—	10	—	%
Analog Voltage Range	V_A	$I_S = 1.0mA$ (Note 6) $I_S = 1.0mA$	+10 -10	+11 -15	—	V
Analog Current Range	I_A	$V_S = \pm 10.0V$	—	11	—	mA
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$V_S \leq +10V$ $I_S = 1mA$	—	15	—	%
Source Current in "OFF" Condition	$I_{S(OFF)}$	$V_S = 10V, V_D = -10V$; (Note 5) $T_A = \text{Max. Operating Temp.}$	—	—	60	nA
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V, V_D = -10V$; (Note 5) $T_A = \text{Max. Operating Temp.}$	—	—	60	nA
Leakage Current in "ON" Condition	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = \pm 10V$, (Note 5) $T_A = \text{Max. Operating Temp.}$	—	—	60	nA
Logical "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	V
Logic "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.8	V
Logical "1" Input Current	I_{INH}	$V_{IN} = 2V$ to $15V$, (Note 4)	—	—	15	μA
Logical "0" Input Current	I_{INL}	$V_{IN} = 0.8$	—	5	15	μA
Turn-On-Time	t_{ON}	See Switching Test Circuit, (Note 2)	—	—	1000	ns
Turn-Off-Time	t_{OFF}	See Switching Test Circuit, (Note 2)	—	—	500	ns
Break-Before-Make Time	$t_{ON} - t_{OFF}$	(Note 3)	—	50	—	ns
Positive Supply Current	I_+	All Channels "ON", (Note 5)	—	—	15.8	mA
Negative Supply Current	I_-	All Channels "ON", (Note 5)	—	—	14.5	mA
Positive Supply Current	I_+	All Channels "OFF", (Note 5)	—	—	18	mA
Negative Supply Current	I_-	All Channels "OFF", (Note 5)	—	—	14.5	mA
Ground Current	I_G	All Channels "ON" or "OFF"	—	—	10.0	mA

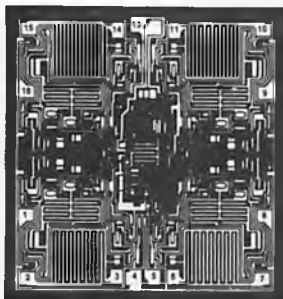
NOTES:

1. $V_A = 0V, I_D = 100\mu A$. Specified as a percentage of $R_{AVERAGE}$ where:

$$R_{AVERAGE} = \frac{R_{ON1} + R_{ON2} + R_{ON3} + R_{ON4}}{4}$$

2. Guaranteed by design.
 3. Switch is guaranteed by design to provide break-before-make operation.
 4. Current tested at $V_{IN} = 2V$. This is worst case condition.
 5. Switch being tested ON or OFF as indicated, $V_{INH} = 2V$ or $V_{INL} = 0.8V$, per logic truth table.
 6. Guaranteed by R_{ON} and leakage tests. For normal operation analog signal voltages should be restricted to less than $(V_+ - 4V)$.
 7. Sample tested.

DICE CHARACTERISTICS



DIE SIZE 0.101 × 0.097 Inch, 9797 sq. mils
(2.565 × 2.464 mm, 6.320 sq. mm)

- | | |
|-------------------|---------|
| 1. IN1 | 9. IN3 |
| 2. D1 | 10. D3 |
| 3. S1 | 11. S3 |
| 4. V- (SUBSTRATE) | 12. V+ |
| 5. GND | 14. S4 |
| 6. S2 | 15. D4 |
| 7. D2 | 16. IN4 |
| 8. IN2 | |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = 15V$, $V_- = -15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N LIMIT	SW-201G SW-202G LIMIT	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	80	100	Ω MAX
R_{ON} Mismatch	R_{ON} Match	$V_A = 0V$, $I_S \leq 100\mu A$	15	20	% MAX
ΔR_{ON} vs V_A	ΔR_{ON}	$V_S \leq 10V$, $I_S = 1mA$	15	20	% MAX
Positive Supply	I_+	(Note 1)	9	10.5	mA MAX
Negative Supply Current	I_-	(Note 1)	6	7	mA MAX
Ground Current	I_G		4	4	mA MAX
Analog Voltage Range	V_A	$I_S = 1mA$ (Note 3)	± 10	± 10	V MIN
Logic "1" Input Voltage	V_{INH}	(Note 3)	2	2	V MIN
Logic "0" Input Voltage	V_{INL}	(Note 3)	0.8	0.8	V MAX
Logic "0" Input Current	I_{INL}	$0V \leq V_{IN} \leq 0.8V$	5	5	μA MAX
Logic "1" Input Current	I_{INH}	$2V \leq V_{IN} \leq 15V$, (Note 2)	5	5	μA MAX
Analog Current Range	I_A	$V_S = \pm 10V$	10	7	mA MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS $V_+ = 15V$, $V_- = -15V$ and $T_A = 25^\circ C$, unless otherwise noted.

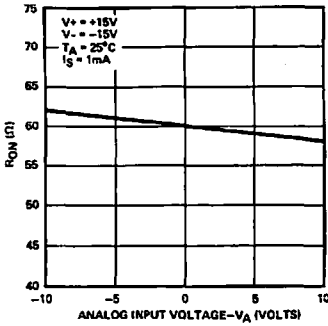
PARAMETER	SYMBOL	CONDITIONS	SW-201N SW-202N TYPICAL	SW-201G SW-202G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$-10V \leq V_A \leq 10V$, $I_S \leq 1mA$	60	60	Ω
Turn-On-Time	t_{ON}		340	340	ns
Turn-Off-Time	t_{OFF}		200	200	ns
Drain Current in "OFF" Condition	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$	0.3	0.3	nA
"OFF" Isolation	$I_{SD(OFF)}$	$f = 500kHz$, $R_L = 680\Omega$	58	58	dB
Crosstalk	C_T	$f = 500kHz$, $R_L = 680\Omega$	70	70	dB

NOTES:

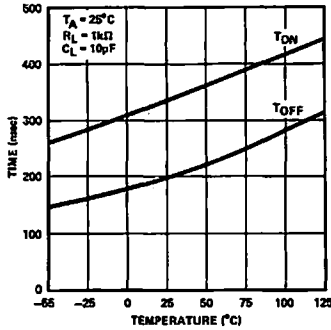
- Power supply and ground current specified for switch "ON" or "OFF".
- Current tested at $V_{IN} = 2V$. This is worst case condition.
- Guaranteed by R_{ON} and leakage tests.

TYPICAL PERFORMANCE CHARACTERISTICS

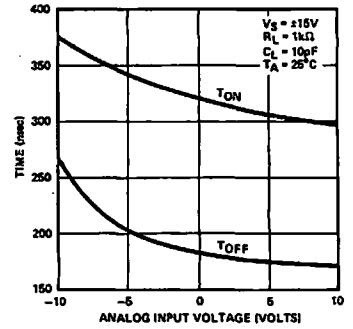
**"ON" RESISTANCE vs
ANALOG VOLTAGE (V_A)**



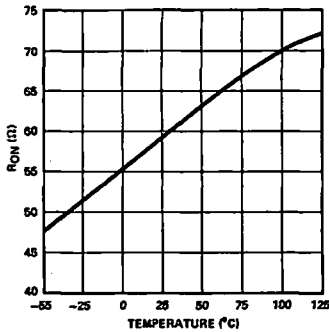
**SWITCHING TIME vs
TEMPERATURE**



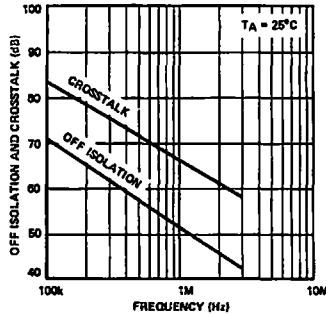
**SWITCHING TIME vs
ANALOG VOLTAGE**



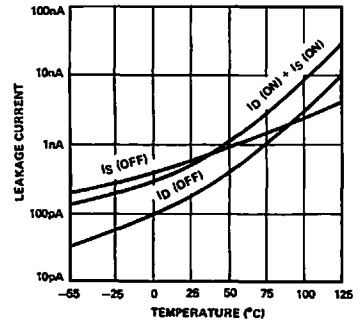
R_{ON} vs TEMPERATURE



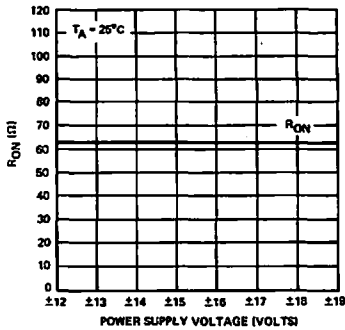
**CROSSTALK AND "OFF"
ISOLATION vs FREQUENCY**



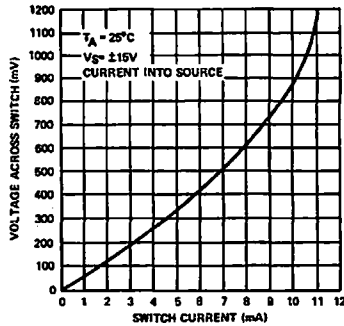
**LEAKAGE CURRENT vs
TEMPERATURE**



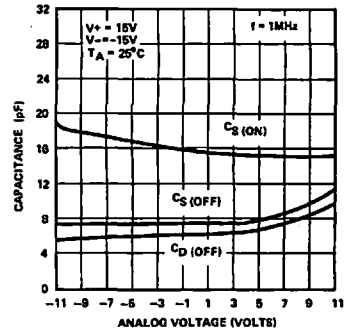
**"ON" RESISTANCE vs
POWER SUPPLY VOLTAGE**



**SWITCH CURRENT vs
VOLTAGE**

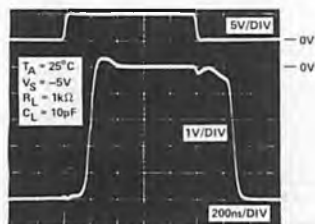


**SWITCH CAPACITANCE vs
ANALOG VOLTAGE**



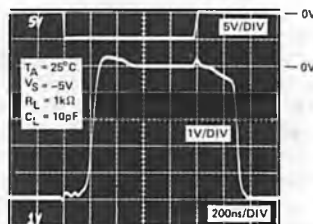
TYPICAL PERFORMANCE CHARACTERISTICS

SW-201

 t_{ON}/t_{OFF} SWITCHING RESPONSE


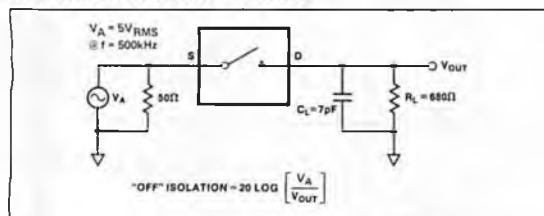
TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (11V/DIV)

SW-202

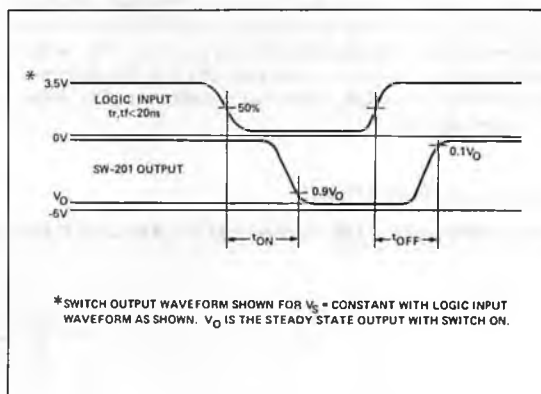
 t_{ON}/t_{OFF} SWITCHING RESPONSE


TOP TRACE: LOGIC INPUT (5V/DIV)
BOTTOM TRACE: SWITCH OUTPUT (11V/DIV)

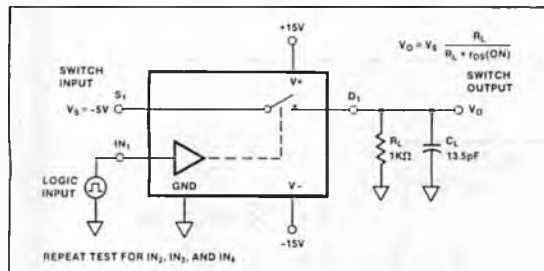
OFF ISOLATION TEST CIRCUIT



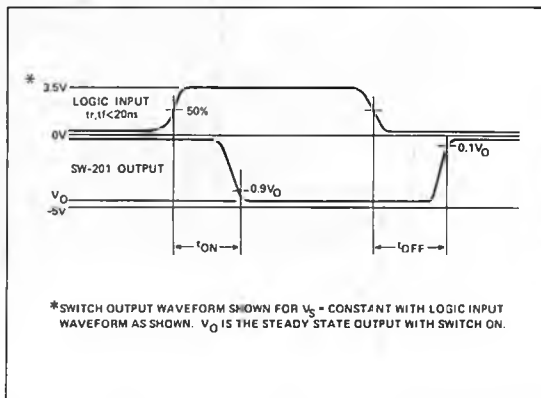
SW-201 WAVEFORMS



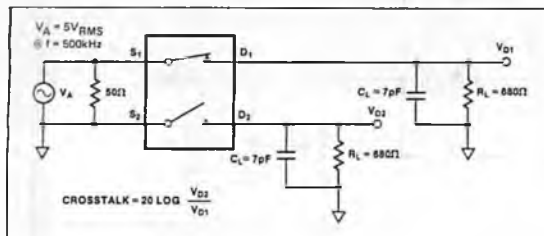
SWITCHING TIME TEST CIRCUIT



SW-202 WAVEFORMS



CROSSTALK TEST CIRCUIT

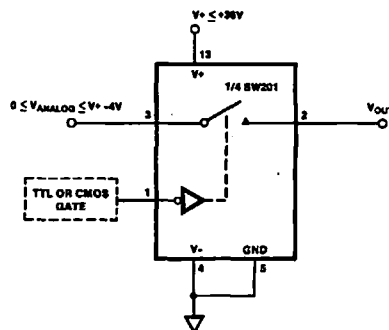


APPLICATIONS INFORMATION

This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing rather than CMOS, special handling is not necessary to prevent damage to these switches. Because the digital inputs only require a 2V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode as the input voltage is raised above $\approx 1.4V$.

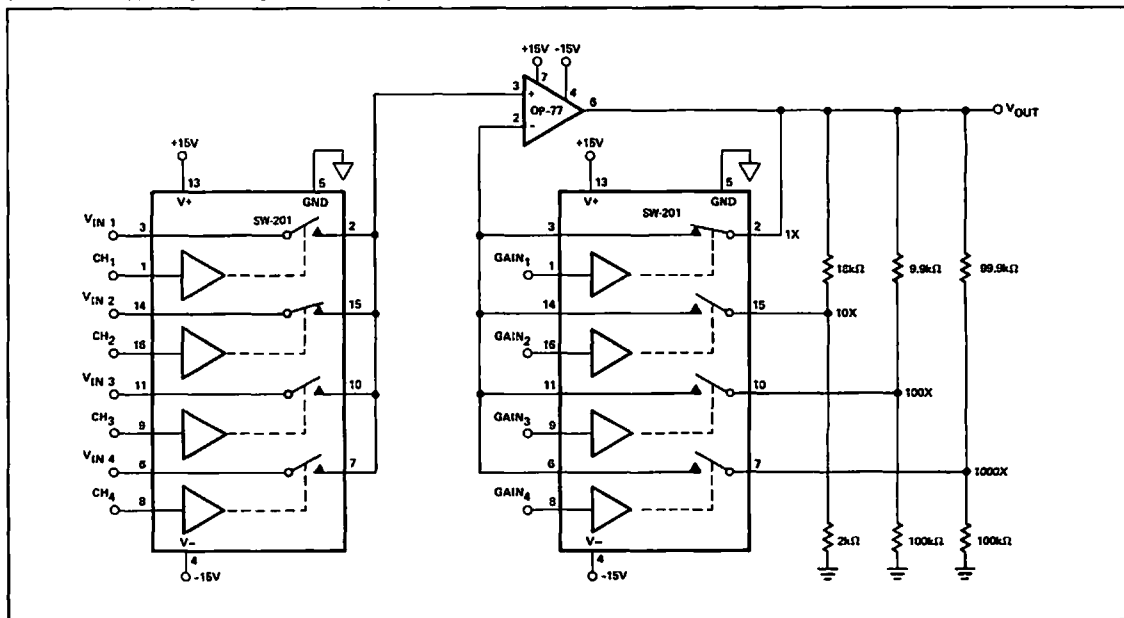
The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. For normal operation, however, positive input voltages should be restricted to $11V$ (or $4V$ less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P , and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

OPERATION FROM SINGLE POSITIVE POWER SUPPLY



TYPICAL APPLICATIONS

PROGRAMMABLE GAIN NONINVERTING AMPLIFIER WITH SELECTABLE INPUTS



FEATURES

- Pin Compatible with AD7510 DI, AD7511 DI
- JFET Switches Rather than CMOS
- Highly Resistant to Static Discharge Damage
- Radiation Resistant
- No SCR Latch-up Problems
- Low "ON" Resistance — 75Ω Max
- Superior "OFF" Isolation and Crosstalk
- Digital Inputs Compatible with TTL and CMOS
- No Pull-Up Resistors Required to Insure Break-Before-Make Action with TTL Inputs

ORDERING INFORMATION†

TYPICAL 25°C RESISTANCE	PACKAGE HERMETIC DIP	TEMPERATURE RANGE
60Ω	SW7510AQ* SW7510EQ	MIL IND
80Ω	SW7510BQ* SW7510FQ	MIL IND
60Ω	SW7511AQ* SW7511EQ	MIL IND
80Ω	SW7511BQ* SW7511FQ	MIL IND

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

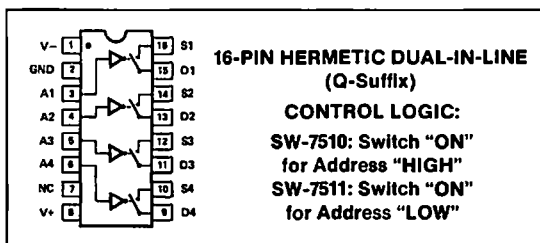
GENERAL DESCRIPTION

The SW-7510/7511 are monolithic linear devices, each containing four independently selectable SPST analog switches. The SW-7510 operates normally-open with logic-low inputs. The SW-7511 operates normally-closed with logic-low inputs. All logic inputs are fully TTL input compatible.

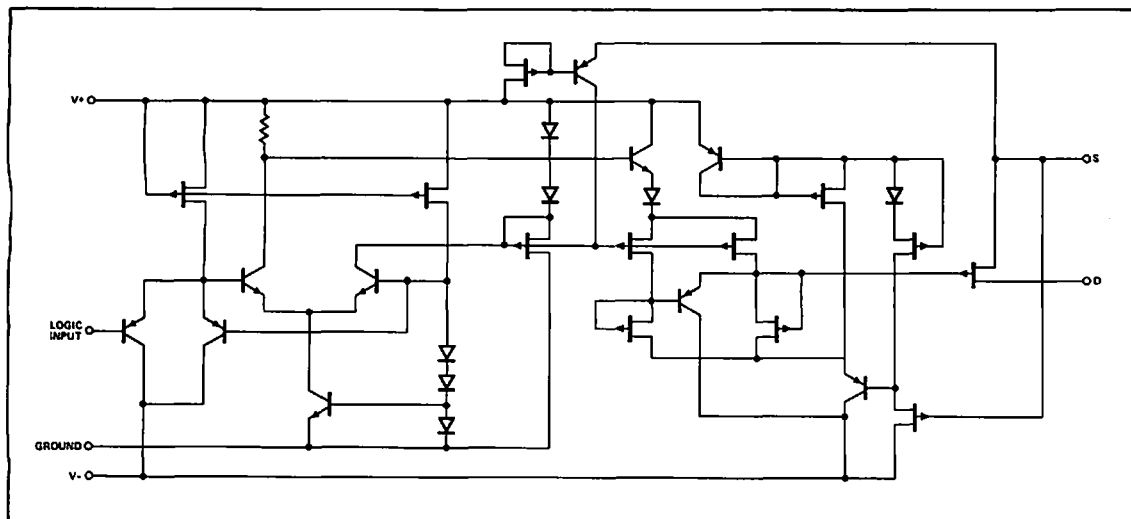
Performance advantages include exceptionally high "OFF" isolation, low leakage current and low crosstalk. Data conversion, position controllers, choppers, demodulators and programmable-gain amplifiers are popular SW-7510/7511 circuit applications.

The PMI Bipolar-JFET process reduces susceptibility to electrostatic destruction and offers a high resistance to radiation exposure. Plus, total freedom from the intrinsic SCR latch-up problems encountered in equivalently manufactured CMOS products.

PIN CONNECTIONS



SCHEMATIC DIAGRAM (Typical SW-7510 Switch)



**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$, unless otherwise noted).

Operating Temperature Range..

SW-7510/7511AQ, BQ -55°C to $+125^\circ\text{C}$ SW-7510/7511EQ, FQ -25°C to $+85^\circ\text{C}$ DICE Junction Temperature (T_J) -65°C to $+150^\circ\text{C}$ Storage Temperature Range -65°C to $+150^\circ\text{C}$

Power Dissipation 500mW

Derate above 100°C 10mW/ $^\circ\text{C}$ Lead Temperature (Soldering, 60 sec) 300°C Maximum Junction Temperature 150°C

V+ Supply to V- Supply 36V

V+ Supply to Ground 36V

Logic Input Voltage (-2V or V-) to V+ Supply

Analog Input Voltage

Continuous V- Supply to V+ Supply +20V

1% Duty Cycle and Driving

all 4 Inputs with

500 μs pulse V- Supply -15V to V+ Supply +20V

Maximum Current Through Any Pin 25mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15\text{V}$ and $T_A = +25^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-7510A/E SW-7511A/E			SW-7510B/F SW-7511B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_D = 0\text{V}$, $I_{DS} = 1\text{mA}$	—	60	75	—	80	100	Ω
ΔR_{ON} vs. V_D (V_S)	ΔR_{ON}	$V_D \leq 10\text{V}$, $I_D = 1\text{mA}$	—	15	—	—	15	—	%
R_{ON} Match of Switches	R_{ON} Match	$V_D = 0\text{V}$, $I_{DS} = 1\text{mA}$	—	1.5	10	—	1.5	10	%
Analog Voltage Range	V_A	$I_S = 1\text{mA}$ (Note 5)	+10 -10	+11 -15	—	+10 -10	+11 -15	—	V
"OFF" Leakage Current	$I_{S(OFF)}$, $I_{D(OFF)}$	$V_S = +10\text{V}$, $V_D = -10\text{V}$, (Note 1)	—	—	1.0	—	—	3.0	nA
"ON" Leakage Current	$I_{S(ON)}$, $I_{D(ON)}$	$V_S = V_D = +10\text{V}$, (Note 1)	—	—	1.0	—	—	3.0	nA
Logic "1" Voltage	V_{INH}	(Note 5)	2.0	—	—	2.0	—	—	V
Logic "0" Voltage	V_{INL}	(Note 5)	—	—	0.8	—	—	0.8	V
Logic "0" Current	I_{INL}	$V_{IN} = +0.4\text{V}$	—	1.5	3.5	—	1.5	3.5	μA
Logic Input Capacitance	C_{DIG}	$V_{IN} = +0.4\text{V}$	—	1.5	—	—	1.5	—	pF
"ON" Switching Time	t_{ON}	$V_S = -5\text{V}$, $R_L = 1\text{k}\Omega$, $C_L = 7\text{pF}$, (Note 4)	—	350	450	—	450	550	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5\text{V}$, $R_L = 1\text{k}\Omega$, $C_L = 7\text{pF}$, (Note 4)	—	260	300	—	350	450	ns
"OFF" Isolation	ISO_{OFF}	(Note 2)	—	68	—	—	68	—	dB
Crosstalk	C_T	(Note 3)	—	70	—	—	70	—	dB
Analog "OFF" Capacitance	$C_{S(OFF)}$, $C_{D(OFF)}$	$V_S = 1\text{V}$, $V_D = 0$	—	6.5	—	—	6.5	—	pF
Analog "ON" Capacitance	$C_{S(ON)}$, $C_{D(ON)}$	$V_S = 0\text{V}$, $V_D = 0$	—	14	—	—	14	—	pF
Feedthrough Capacitance	$C_{DS(OFF)}$	$V_S = 0\text{V}$	—	0.8	—	—	0.8	—	pF
Channel Capacitance	$C_{SS(OFF)}$	$V_S = 0\text{V}$	—	0.4	—	—	0.4	—	pF
	$C_{DD(OFF)}$	$V_S = 0\text{V}$	—	0.4	—	—	0.4	—	
Positive Supply Current	I_+	Logic Inputs at "0" or "1"	—	5.0	9.0	—	3.0	9.0	mA
Negative Supply Current	I_-	Logic Inputs at "0" or "1"	—	2.8	5.0	—	1.7	5.0	mA

NOTES:

- The conditions listed specify the worst case leakage currents. The leakage currents apply equally to source (S) or drain (D).
- OFF isolation is measured by driving the source of any OFF switch and observing the voltage which appears on the drain. The conditions are: $R_L = 680\Omega$, $C_L = 7\text{pF}$, $V_S = 5\text{V}_{RMS}$, $f = 100\text{kHz}$.
- Crosstalk is measured by driving source of any OFF switch and observing voltage which appears on any other "ON" output drain. The conditions are: $R_L = 680\Omega$, $C_L = 7\text{pF}$, $V_S = 5\text{V}_{RMS}$, $f = 100\text{kHz}$.
- Sample tested.
- Guaranteed by R_{ON} and leakage tests. For normal operation maximum analog signal voltages should be restricted to less than $(V_+) - 4\text{V}$.



ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for SW-7510AQ, BQ and SW-7511AQ, BQ; and $-25^\circ C \leq T_A \leq +85^\circ C$ for SW-7510EQ, FQ and SW-7511EQ, FQ, unless otherwise noted.

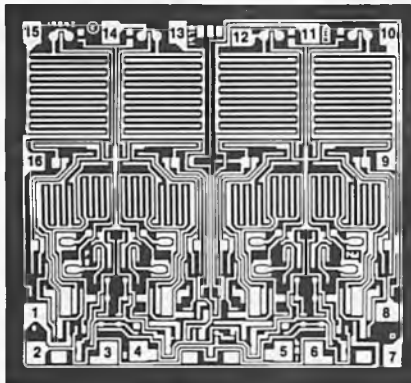
PARAMETER	SYMBOL	CONDITIONS	SW-7510A/E SW-7511A/E			SW-7510B/F SW-7511B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	—	—	100	—	—	150	Ω
ΔR_{ON} vs. Temperature	ΔR_{ON} Drift	$V_D = 0V$, $I_{DS} = 1mA$	—	0.4	—	—	0.5	—	$\%/^\circ C$
Analog Voltage Range	V_A	$I_S = 1mA$ (Note 4)	+10 -10	+11 -15	—	+10 -10	+11 -15	—	V
"OFF" Leakage Current	$I_{S(OFF)}$, $I_{D(OFF)}$	$V_S = +10V$, $V_D = -10V$, (Notes 1, 3)	—	—	90	—	—	100	nA
"ON" Leakage Current	$I_{S(ON)} + I_{D(ON)}$	$V_S = V_D = +10V$, (Notes 1, 3)	—	—	90	—	—	100	nA
Logic "1" Voltage	V_{INH}	(Note 4)	2.0	—	—	2.0	—	—	V
Logic "0" Voltage	V_{INL}	(Note 4)	—	—	0.8	—	—	0.8	V
Logic "0" Current	I_{INL}	$V_{IN} = +0.4V$	—	—	5.0	—	—	7.0	μA
"ON" Switching Time	t_{ON}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$ (Note 2)	—	—	600	—	—	1000	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$ (Note 2)	—	—	500	—	—	750	ns
Positive Supply Current	I_+	Logic Inputs at "0" or "1"	—	—	13	—	—	13	mA
Negative Supply Current	I_-	Logic Inputs at "0" or "1"	—	—	7.5	—	—	7.5	mA

NOTES:

1. The conditions listed specify the worst case leakage currents. The leakage currents apply equally to source (S) or drain (D).
2. Guaranteed by design.
3. Tested at $125^\circ C$ only for "A" and "B" grades.
4. Guaranteed by R_{ON} and leakage tests.



DICE CHARACTERISTICS



DIE SIZE 0.095×0.087 Inch, 8265 sq. mils
(2.413×2.210 mm, 5.333 sq. mm)

SW-7510/SW-7511

- | | |
|--------------------------------|-----------------|
| 1. NEGATIVE SUPPLY (SUBSTRATE) | 9. DRAIN (D4) |
| 2. GROUND | 10. SOURCE (S4) |
| 3. ADDRESS (A1) | 11. DRAIN (D3) |
| 4. ADDRESS (A2) | 12. SOURCE (S3) |
| 5. ADDRESS (A3) | 13. DRAIN (D2) |
| 6. ADDRESS (A4) | 14. SOURCE (S2) |
| 7. DISABLE (NO CONNECT) | 15. DRAIN (D1) |
| 8. POSITIVE SUPPLY | 16. SOURCE (S1) |

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = +15V$, $V_- = -15V$, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-7510N/ SW-7511N LIMIT	SW-7510G/ SW-7511G LIMIT	UNITS
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	75	100	Ω MAX
Logic "1" Voltage	V_{INH}	Note 1)	2.0	2.0	V MIN
Logic "0" Voltage	V_{INL}	Note 1)	0.8	0.8	V MAX
Logic "0" Current	I_{INL}	$V_{IN} = +0.4V$	3.5	3.5	μA MAX
Positive Supply Current	I_+	Logic Inputs at "0"	9	9	mA MAX
Negative Supply Current	I_-	Logic Inputs at "0"	5	5	mA MAX

NOTES:

1. Guaranteed by R_{ON} and leakage tests

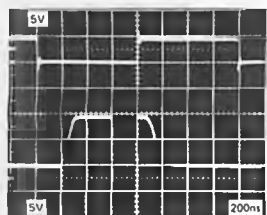
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = +15V$, $V_- = -15V$ and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SW-7510N/ SW-7511N TYPICAL	SW-7510G/ SW-7511G TYPICAL	UNITS
"ON" Resistance	R_{ON}	$V_D = 0V$, $I_{DS} = 1mA$	60	80	Ω
R_{ON} vs. Temperature	R_{ON} Drift	$V_D = 0V$, $I_{DS} = 1mA$	0.4	0.5	%/ $^\circ C$
"ON" Switching Time	t_{ON}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$	350	450	ns
"OFF" Switching Time	t_{OFF}	$V_S = -5V$, $R_L = 1k\Omega$, $C_L = 7pF$	260	350	ns

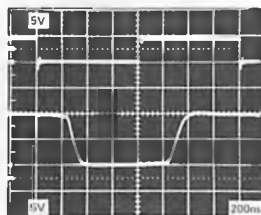
TYPICAL PERFORMANCE CHARACTERISTICS (Apply to all models, unless otherwise noted)

LARGE-SIGNAL SWITCHING



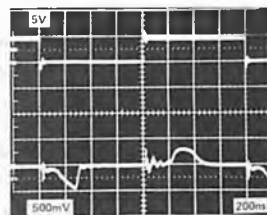
$V_A = +10V, R_L = 1k\Omega, C_L = 13pF$

LARGE-SIGNAL SWITCHING



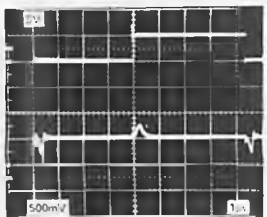
$V_A = -10V, R_L = 1k\Omega, C_L = 100pF$

SMALL-SIGNAL SWITCHING



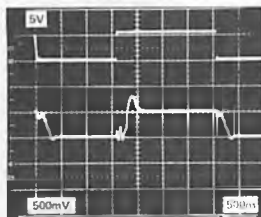
$V_A = 0V, R_L = 1k\Omega, C_L = 13pF$

SMALL-SIGNAL SWITCHING WITH FILTERING



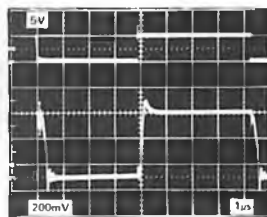
$V_A = 0V, R_L = 1k\Omega, C_L = 100pF$

SMALL-SIGNAL SWITCHING



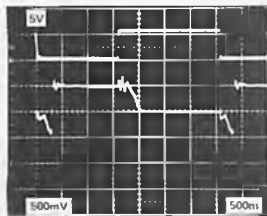
$V_A = -500mV, R_L = 1k\Omega, C_L = 13pF$

SMALL-SIGNAL SWITCHING WITH FILTERING



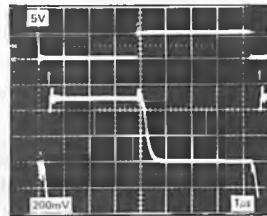
$V_A = -500mV, R_L = 1k\Omega, C_L = 100pF$

SMALL-SIGNAL SWITCHING



$V_A = 500mV, R_L = 1k\Omega, C_L = 13pF$

SMALL-SIGNAL SWITCHING WITH FILTERING



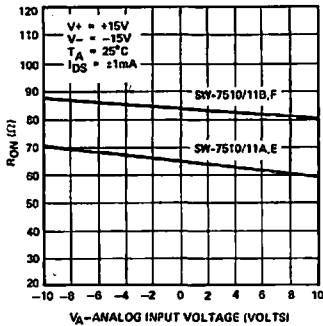
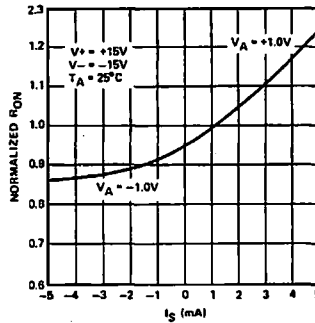
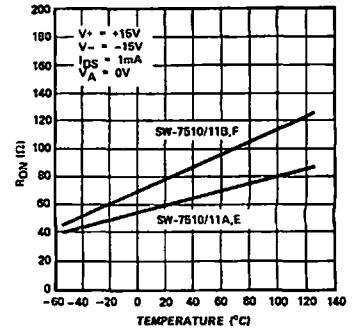
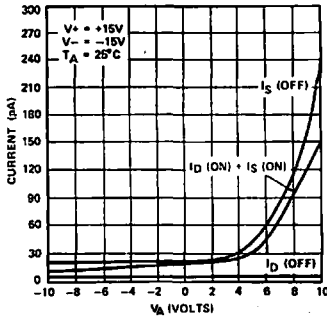
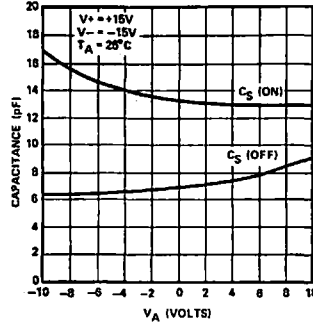
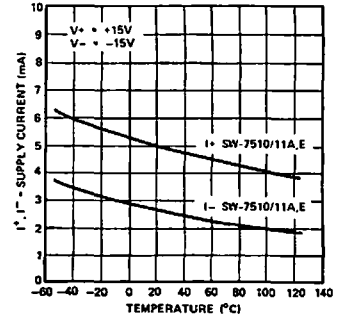
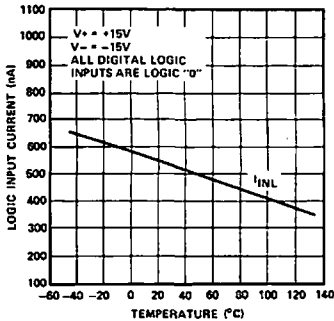
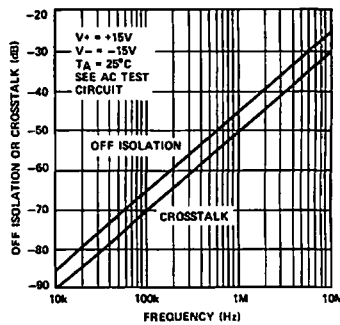
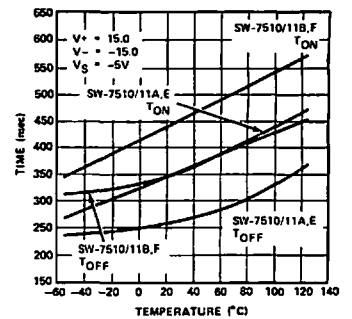
$V_A = 500mV, R_L = 1k\Omega, C_L = 100pF$

NOTE:

Upper Photo Traces: Logic Control Signal A_X (5V/DIV)

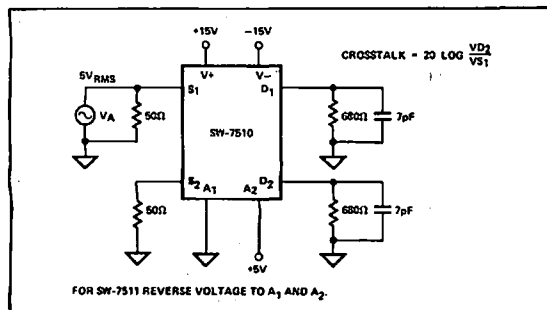
Lower Photo Traces: Switch Outputs V_O

TYPICAL PERFORMANCE CHARACTERISTICS (Apply to all models, unless otherwise noted)

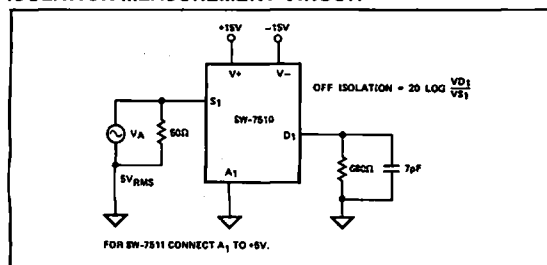
"ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)

NORMALIZED R_{ON} vs SWITCH CURRENT (I_S)

 R_{ON} vs TEMPERATURE

SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE

SWITCH CAPACITANCES vs ANALOG VOLTAGE (V_A)

SUPPLY CURRENTS vs TEMPERATURE

DIGITAL INPUT CURRENT I_{INL} vs TEMPERATURE

CROSSTALK AND "OFF" ISOLATION vs FREQUENCY

SWITCHING TIMES vs TEMPERATURE


AC TEST CIRCUITS

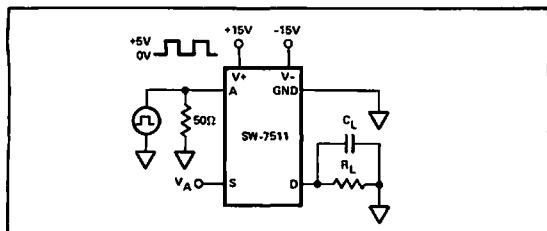
CROSSTALK MEASUREMENT CIRCUIT



ISOLATION MEASUREMENT CIRCUIT



SWITCHING TIME TEST CIRCUIT



APPLICATIONS INFORMATION

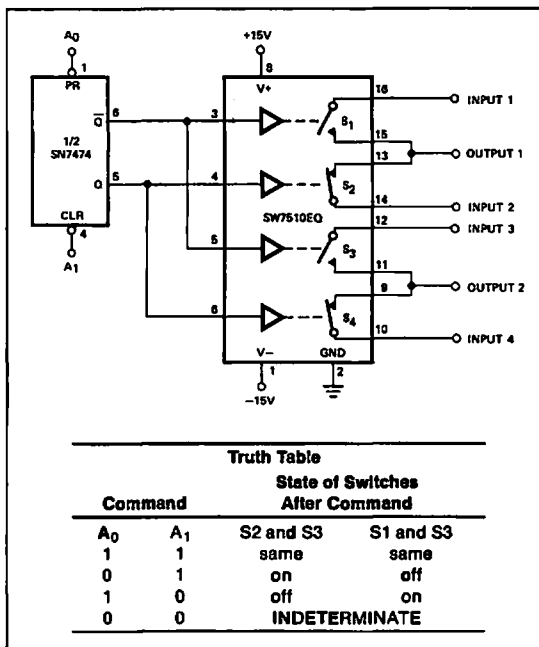
This analog switch employs ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS switches. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with

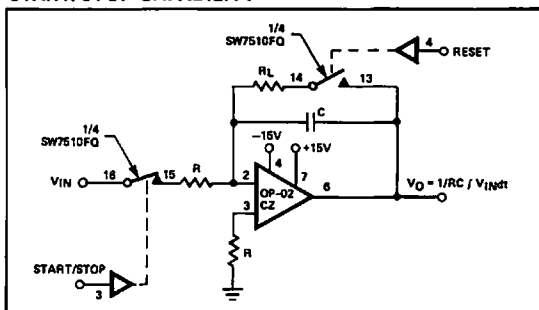
$V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P , and prevents that channel from being falsely turned ON. Individual switches are "ON" without power applied.

Proper switching requires the "Source" terminal be connected to the input driving signal.

LATCHING DPDT SWITCH



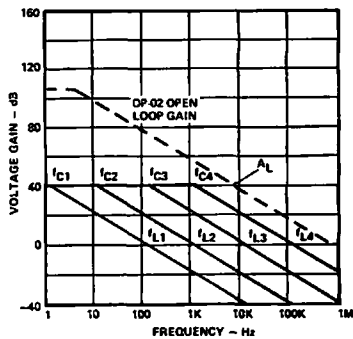
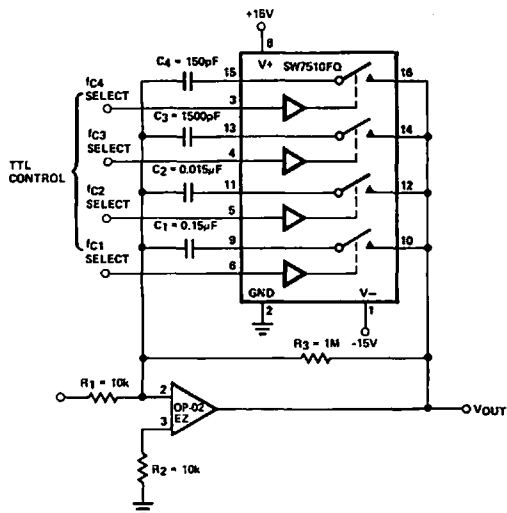
INTEGRATOR WITH ANALOG RESET AND START/STOP CAPABILITY



NOTE: Applications show SW-7510. For SW-7511 applications the logic is inverted.

TYPICAL APPLICATIONS

ACTIVE LOW-PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY



A_L (VOLTAGE GAIN BELOW BREAK FREQUENCY) =

$$\frac{R_3}{R_1} = 100 \text{ (40dB)}$$

$$f_C \text{ (BREAK FREQUENCY)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (UNITY GAIN FREQUENCY)} = \frac{1}{2\pi R_1 C_X}$$

NOTE: Applications show SW-7510. For SW-7511 applications the logic is inverted.



MUX-08/MUX-24

8-CHANNEL/DUAL 4-CHANNEL JFET ANALOG MULTIPLEXERS
(OVERVOLTAGE AND POWER SUPPLY LOSS PROTECTED)

Precision Monolithics Inc.

FEATURES

- JFET Switches Rather Than CMOS
- Low "ON" Resistance 220Ω Typ
- Highly Resistant to Static Discharge Damage
- No SCR Latch-Up Problems
- Digital Inputs Compatible With TTL and CMOS
- 125°C Temperature Tested Dice Available
- MUX-08 Pin Compatible With DG508, HI-508A, IH5108, IH6108, LF11508/12508/13508, AD7506
- MUX-24 Pin Compatible With DG509, HI-509A, IH5208, IH6208, LF11509/12509/13509, AD7507
- Available in Surface Mount Packages

ORDERING INFORMATION†

25°C ON RESISTANCE	PACKAGE			TEMPERATURE RANGE
	CERDIP	PLASTIC	LCC	
220Ω	MUX08AQ*	—	—	MIL
	MUX08EQ	—	—	IND
	—	MUX08EP	—	COM
300Ω	MUX08BQ*	—	MUX08BRC/883	MIL
	MUX08FQ	—	—	IND
	—	MUX08FP	—	COM
	—	MUX08FS††	—	COM
220Ω	MUX24AQ*	—	—	MIL
	MUX24EQ	—	—	IND
	—	MUX24EP	—	COM
300Ω	MUX24BQ*	—	—	MIL
	MUX24FQ	—	—	IND
	—	MUX24FP	—	COM
	—	MUX24FS††	—	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The MUX-08 is a monolithic eight-channel analog multiplexer which connects a single output to one of the eight analog inputs depending upon the state of a 3-bit binary address.

The MUX-24 is a monolithic four-channel differential analog multiplexer configured in a double pole, four-position (plus OFF) electronic switch array. A two-bit binary input address connects a pair of independent analog inputs from each four-channel input section to the corresponding pair of independent analog outputs.

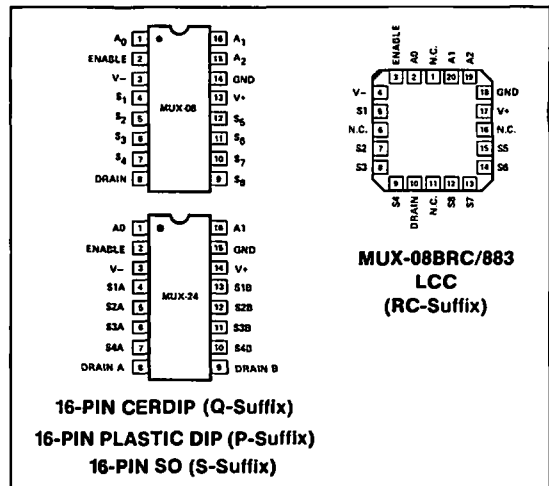
All switches in the MUX-08/MUX-24 are turned OFF by applying logic "0" to the ENABLE pin, thereby providing a package select function.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance, low leakage currents and fast settling time

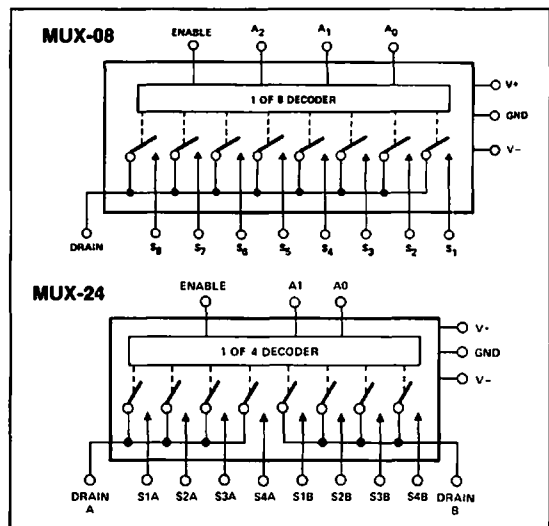
with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors over the full operating temperature range.

For single sixteen-channel and dual eight-channel models, refer to the MUX-16/MUX-28 data sheet.

PIN CONNECTIONS



FUNCTIONAL DIAGRAMS



ANALOG SWITCHES/MULTIPLEXERS

13

**ABSOLUTE MAXIMUM RATINGS** (Note)

Operating Temperature Range

MUX-08/24-AQ, BQ, BRC -55°C to +125°C

MUX-08/24-EQ, FQ -25°C to +85°C

MUX-08/24-EP, FP, FS 0°C to +70°C

DICE Junction Temperature (T_J) -65°C to +150°C

Storage Temperature Range -65°C to +150°C

P-Suffix -65°C to +125°C

Power Dissipation 500mW

Derate above 100°C 10mW/°C

Lead Temperature (Soldering, 60 sec) 300°C

Maximum Junction Temperature 150°C

V+ Supply to V- Supply 36V

Logic Input Voltage (-4V or V-) to V+ Supply

Analog Input Voltage V- Supply -20V to V+ Supply +20V

Maximum Current Through Any Pin 25mA

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.**ELECTRICAL CHARACTERISTICS** at V+ = +15V, V- = -15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08A/E MUX-24A/E			MUX-08B/F MUX-24B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_S \leq 10V, I_S \leq 200\mu A$	—	220	300	—	300	400	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V, I_S = 200\mu A$	—	1	5	—	3	7	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V, I_S = 200\mu A$	—	7	15	—	9	20	%
Analog Voltage Range	V_A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V
Source Current (Switch "OFF")	$I_{S,OFF}$	$V_S = 10V, V_D = -10V$ (Note 1)	—	0.01	1.0	—	0.01	2.0	nA
Drain Current (Switch "OFF")	$I_{D,OFF}$	$V_S = 10V, V_D = -10V$ (Note 1)	MUX-08 MUX-24	— 0.05	1.0 1.0	—	0.1 0.05	2.0 2.0	nA
Leakage Current (Switch "ON")	$I_{D,ON} + I_{S,ON}$	$V_D = 10V$ (Note 1)	MUX-08 MUX-24	— 0.05	1.0 1.0	—	0.1 0.05	2.0 2.0	nA
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V	—	1	10	—	1	10	μA
Digital "0" Enable Current	$I_{INL,EN}$	$V_{EN} = 0.4V$	—	4	10	—	4	10	μA
Digital Input Capacitance	C_{DIG}		—	3	—	—	3	—	pF
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Notes 2, 5) Figure 1 (Test Circuit)	—	1.5 1.0	2.1 1.3	—	1.5 1.0	2.1 1.3	μs
Output Settling Time	t_S	10V Step to 0.10% 10V Step to 0.05% 10V Step to 0.02%	—	2.2 2.7 3.4	— — —	—	2.2 2.7 3.4	— — —	μs
Break-Before-Make Delay	t_{OPEN}	Figure 3 (Test Circuit)	—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	$t_{ON,EN}$	(Note 5) Figure 2 (Test Circuit)	—	1	2	—	1	2	μs
Enable Delay "OFF"	$t_{OFF,EN}$	(Note 5) Figure 2 (Test Circuit)	MUX-08 MUX-24	— 0.2	0.1 0.5	—	0.2 0.3	0.4 0.6	μs
"OFF" Isolation	ISO_{OFF}	(Note 4) Figure 5 (Test Circuit)	MUX-08 MUX-24	— 66	— —	—	60 66	— —	dB
Crosstalk	CT	(Note 3) Figure 4 (Test Circuit)	MUX-08 MUX-24	— 76	— —	—	70 76	— —	dB
Source Capacitance	$C_{S,OFF}$	Switch "OFF"; $V_S = 0V, V_D = 0V$	MUX-08 MUX-24	— 2	2.5 —	—	2.5 2	— —	pF
Drain Capacitance	$C_{D,OFF}$	Switch "OFF"; $V_S = 0V, V_D = 0V$	MUX-08 MUX-24	— 4	7 —	—	7 4	— —	pF
Input to Output Capacitance	$C_{DS,OFF}$	(Note 4)	MUX-08 MUX-24	— 0.15	0.3 —	—	0.3 0.15	— —	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I^+	$V^+ = 15V$ $V^+ = 5V$	—	10 8	12 —	—	6 5	12 —	mA
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I^-	$V^+ = -15V$ $V^+ = -5V$	—	3.0 2.5	3.8 —	—	2.0 1.8	3.8 —	mA

NOTES: See next page.

**ELECTRICAL CHARACTERISTICS** at $V_+ = 15V$, $V_- = -15V$ and $-55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08A/ MUX-24A			MUX-08B/ MUX-24B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_S \leq 10V$, $I_S \leq 200\mu A$	—	—	400	—	—	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$	—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)	—	—	25	—	—	50	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24		— —	100 50	— —	500 500	nA
Leakage Current (Switch "ON")	$I_{D(ON)} + I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24		— —	100 50	— —	500 500	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.7	—	—	0.7	V
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA
Positive Supply Current	I_+	All Digital Inputs Logic "0" or "1"	—	—	15	—	—	15	mA
Negative Supply Current	I_-	All Digital Inputs Logic "0" or "1"	—	—	5	—	—	5	mA

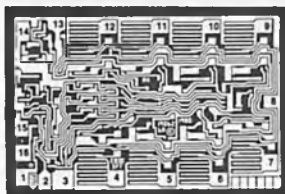
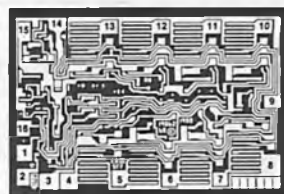
ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $-25^\circ C \leq T_A \leq +85^\circ C$ for MUX-08EQ, FQ and MUX-24EQ, FQ; $0^\circ C \leq T_A \leq +70^\circ C$ for MUX-08EP, FP, FS and MUX-24EP, FP, FS unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08E/ MUX-24E			MUX-08F/ MUX-24F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_S \leq 10V$, $I_S \leq 200\mu A$	—	—	400	—	—	500	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$	—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)	+10 -10	+10.4 -15	—	+10 -10	+10.4 -15	—	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)	—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Notes 1, 7)	MUX-08 MUX-24		— —	100 50	— —	100 50	nA
Leakage Current (Switch "ON")	$I_{D(ON)} + I_{S(ON)}$	$V_D = 10V$ (Notes 1, 7)	MUX-08 MUX-24		— —	100 50	— —	100 50	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.8	—	—	0.8	V
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to 15V	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA
Positive Supply Current	I_+	All Digital Inputs Logic "0" or "1"	—	—	15	—	—	15	mA
Negative Supply Current	I_-	All Digital Inputs Logic "0" or "1"	—	—	5	—	—	5	mA

NOTES:

- Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
- $R_L = 10M\Omega$, $C_L = 10pF$.
- Crosstalk is measured by driving channel 8 with channel 4 "ON".
 $R_L = 1M\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, $f = 500kHz$.

- "OFF" isolation is measured by driving channel 8 with ALL channels "OFF".
 $R_L = 1k\Omega$, $C_L = 10pF$, $V_S = 5V$ RMS, $f = 500kHz$. C_{OS} is computed from the OFF isolation measurement.
- Sample tested.
- Guaranteed by leakage current and R_{ON} tests.
- Leakage tests are performed only on military temperature grades at $125^\circ C$.

**DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)****MUX-08****MUX-24**

DIE SIZE 0.093 × 0.059 inch, 5487 sq. mils
(2.362 × 1.500 mm, 3543 sq. mm)

- | | |
|-------------------|---------|
| 1. A0 | 9. S8 |
| 2. ENABLE | 10. S7 |
| 3. V- (SUBSTRATE) | 11. S6 |
| 4. S1 | 12. S5 |
| 5. S2 | 13. V+ |
| 6. S3 | 14. GND |
| 7. S4 | 15. A2 |
| 8. DRAIN | 16. A1 |

- | | |
|-------------------|------------|
| 1. A0 | 9. DRAIN B |
| 2. ENABLE | 10. S4 B |
| 3. V- (SUBSTRATE) | 11. S3 B |
| 4. S1 A | 12. S2 B |
| 5. S2 A | 13. S1 B |
| 6. S3 A | 14. V+ |
| 7. S4 A | 15. GND |
| 8. DRAIN A | 16. A1 |

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_+ = 15V$, $V_- = -15V$, $T_A = 25^\circ C$, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT LIMIT	MUX-08/ MUX-24N LIMIT	MUX-08/ MUX-24G LIMIT	UNITS
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 200\mu A$, $T_A = 125^\circ C$	300 400	300 —	400 —	Ω MAX
Digital "1" Input Voltage	V_{INH}	(Note 2)	2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}	(Note 2)	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	$V_{IN} = 0.4V$, $T_A = 125^\circ C$	10 20	10 —	10 —	μA MAX
Digital "0" Enable Current	$I_{INL,EN}$	$V_{IN} = 0.4V$, $T_A = 125^\circ C$	10 20	10 —	10 —	μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I_+	$T_A = 125^\circ C$	12 15	12 —	12 —	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I_-	$T_A = 125^\circ C$	3.8 5	3.8 —	3.8 —	mA MAX
Analog Input Range	V_A	(Note 2)	± 10	± 10	± 10	V MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $T_A = 25^\circ C$ for MUX-08/24N & G, $T_A = 125^\circ C$ for MUX-08/24NT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-08/ MUX-24NT TYPICAL	MUX-08/ MUX-24N TYPICAL	MUX-08/ MUX-24G TYPICAL	UNITS
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Note 1)	1.7 1.1	1.3 0.9	2.1 1.3	μs
Output Settling Time	t_S	10V Step to 0.1% (Note 1)	2.1	1.5	1.9	μs
Break-Before-Make Delay	t_{OPEN}	(Note 1)	0.8	0.8	1.0	μs
Crosstalk	CT	(Note 1)	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$	2	2	6	%
Leakage Current (Switch "ON")	$I_{D,ON}$	$V_D = 10V$ (Note 1)	20	0.5	0.5	nA
Analog Input Range	V_A		+10.4/-15	+10.4/-15	+10.4/-15	V

NOTES:

1. The data shown is extrapolated from measurements made on the packaged devices.

2. Guaranteed by leakage current and R_{ON} tests.

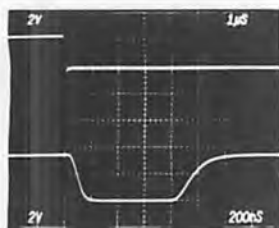
MUX-08
LOGIC STATE

A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

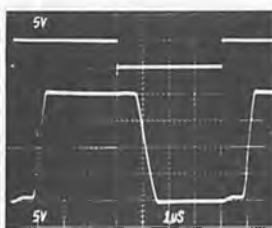
MUX-24
LOGIC STATE

A ₁	A ₀	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

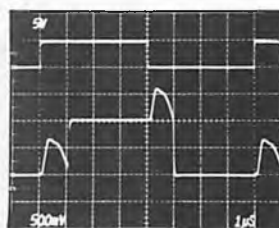
TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

MUX-08
BREAK-BEFORE-MAKE
SWITCHING

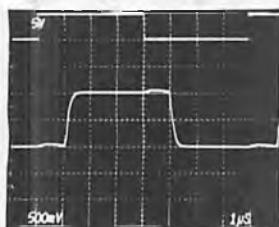
R_L = 1kΩ, C_L = 10pF, V_I = 10V
VOLTAGE = 2V/DIV
TIME = 200ns/DIV

MUX-08
LARGE-SIGNAL SWITCHING

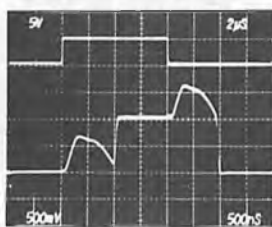
R_L = 1MΩ, C_L = 10pF, V_I = -10V, V_G = +10V
VOLTAGE = 5V/DIV
TIME = 1μs/DIV

MUX-08
SMALL-SIGNAL SWITCHING

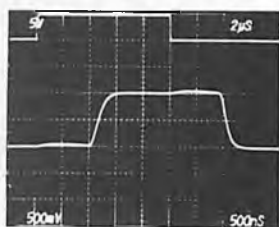
R_L = 1MΩ, C_L = 10pF, V_I = -500mV, V_G = +500mV
VOLTAGE = 500mV/DIV
TIME = 1μs/DIV

MUX-08
SMALL-SIGNAL SWITCHING
WITH FILTERING

R_L = 1MΩ, C_L = 500pF, V_I = 500mV, V_G = +500mV
VOLTAGE = 500mV/DIV
TIME = 1μs/DIV

MUX-08
SMALL-SIGNAL SWITCHING
WITH 2μs SAMPLE TIME

R_L = 1MΩ, C_L = 10pF, V_I = -500mV, V_G = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

MUX-08
SMALL-SIGNAL SWITCHING
WITH FILTERING AND
2.5μs SAMPLE TIME

R_L = 1MΩ, C_L = 500pF, V_I = -500mV, V_G = +500mV
VOLTAGE = 500mV/DIV
TIME = 500ns/DIV

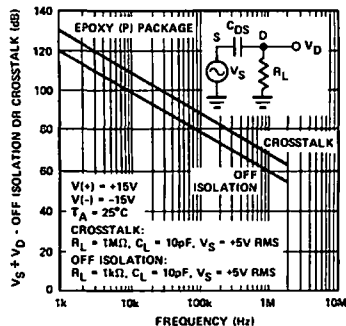
NOTE:

Top waveforms: Digital Input 5V/DIV

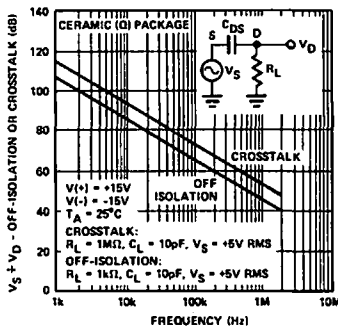
Bottom waveforms: Multiplexer Output

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

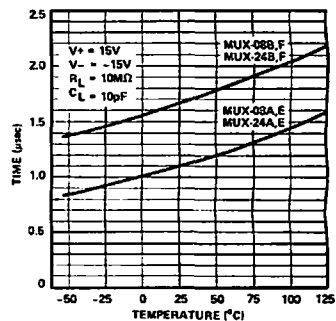
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



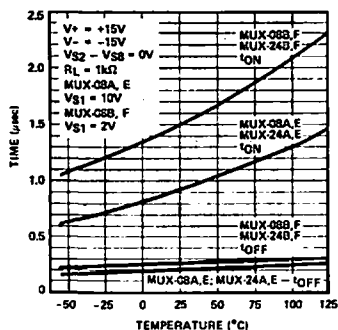
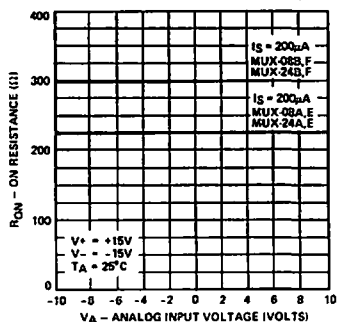
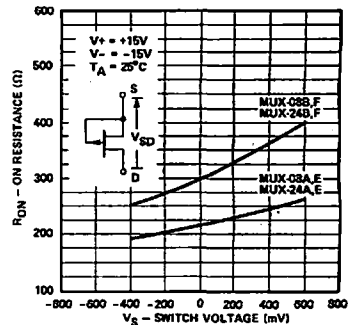
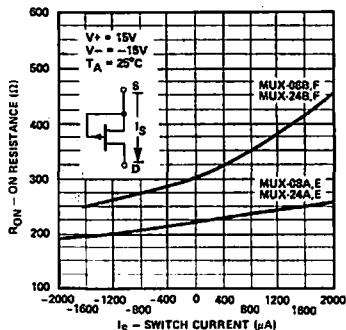
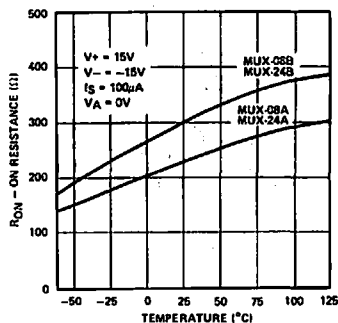
MUX-08 CROSSTALK AND OFF ISOLATION PERFORMANCE OF CHANNEL 8



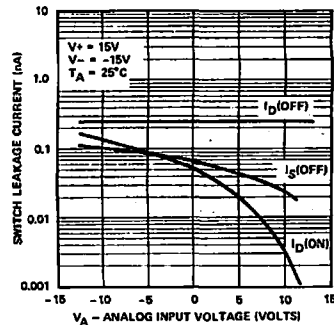
TRANSITION TIMES vs TEMPERATURE



ENABLE DELAY TIMES vs TEMPERATURE

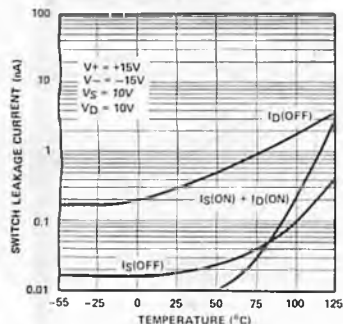
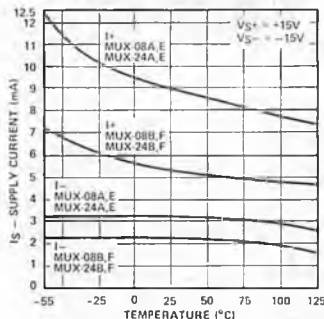
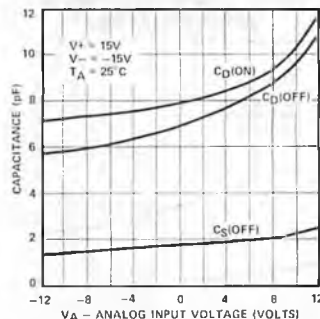
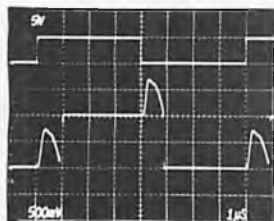

 "ON" RESISTANCE (R_{ON}) vs ANALOG VOLTAGE (V_A)

 R_{ON} vs SWITCH VOLTAGE (V_{SD})

 R_{ON} vs SWITCH CURRENT (I_S)

 R_{ON} vs TEMPERATURE


SWITCH LEAKAGE CURRENTS vs ANALOG INPUT VOLTAGE

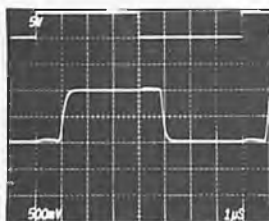




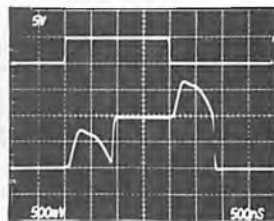
TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

SWITCH LEAKAGE CURRENTS
vs TEMPERATURESUPPLY CURRENTS
vs TEMPERATUREMUX-08
SWITCH CAPACITANCES
vs ANALOG INPUT VOLTAGEMUX-24
SMALL-SIGNAL SWITCHING

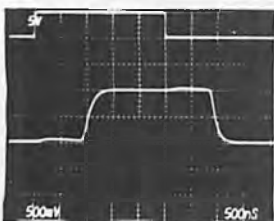
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
VOLTAGE = 500mV/DIV, TIME = 1μs/DIV

MUX-24
SMALL-SIGNAL SWITCHING
WITH FILTERING

$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
VOLTAGE = 500mV/DIV, TIME = 1μs/DIV

MUX-24
SMALL-SIGNAL SWITCHING
WITH 2μs SAMPLE TIME

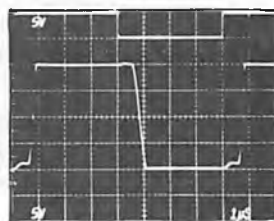
$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24
SMALL-SIGNAL SWITCHING
WITH FILTERING
AND 2.5μs SAMPLE TIME

$R_L = 1M\Omega$, $C_L = 500pF$, $V_1 = -500mV$,
 $V_4 = +500mV$
VOLTAGE = 500mV/DIV, TIME = 500ns/DIV

MUX-24
BREAK-BEFORE-MAKE
SWITCHING

$R_L = 1k\Omega$, $C_L = 10pF$, $V_1 = +10V$,
 $V_4 = +10V$
VOLTAGE = 2V/DIV, TIME = 200ns/DIV

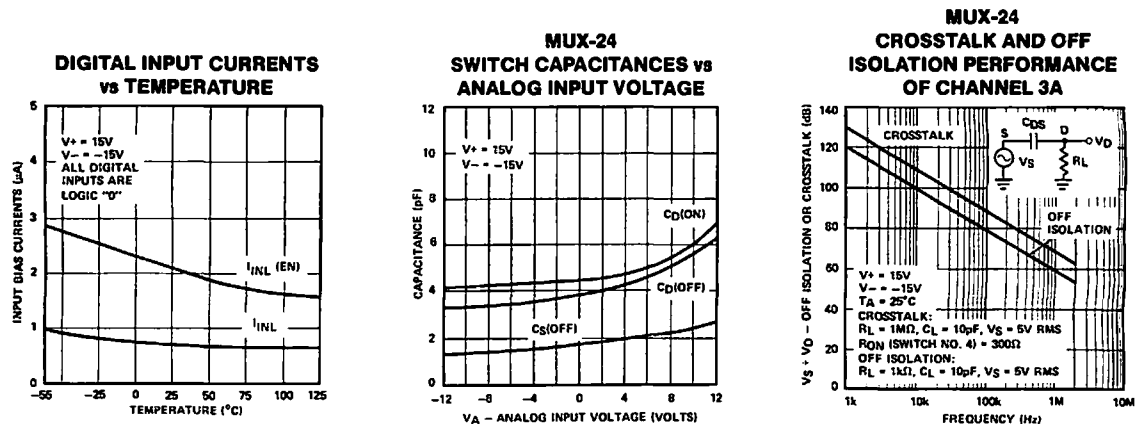
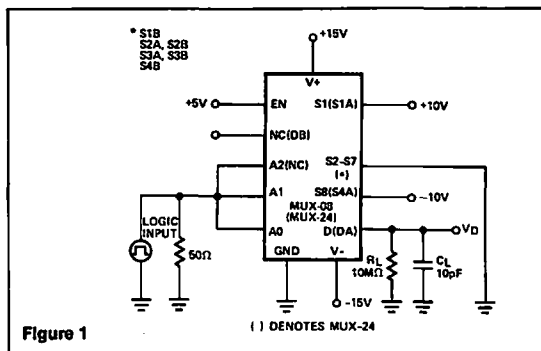
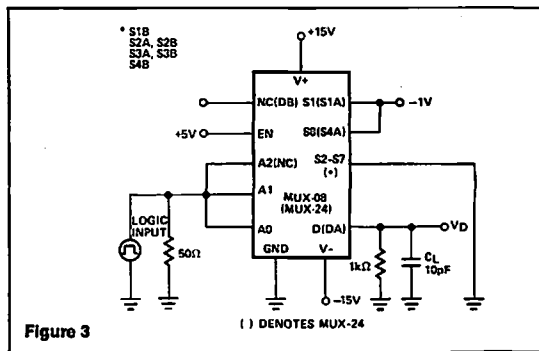
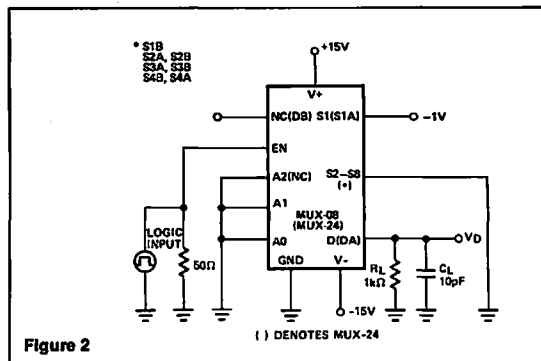
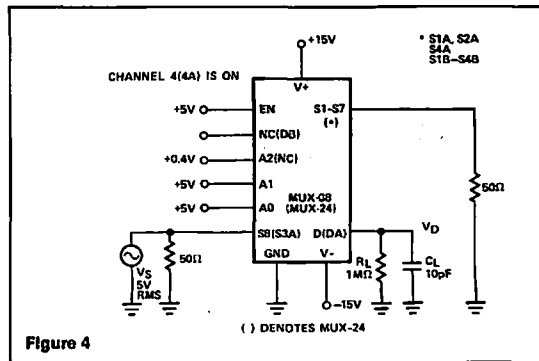
MUX-24
LARGE-SIGNAL SWITCHING

$R_L = 1M\Omega$, $C_L = 10pF$, $V_1 = -10V$, $V_4 = +10V$
VOLTAGE = 5V/DIV, TIME = 1μs/DIV

NOTE:

Top waveforms: Digital Input 5V/DIV

Bottom waveforms: Multiplexer Output

TYPICAL PERFORMANCE CHARACTERISTICS (Applies to all grades, unless otherwise noted.)

A.C. TEST CIRCUITS
TRANSITION TIME TEST CIRCUIT

BREAK-BEFORE-MAKE TEST CIRCUIT

ENABLE DELAY TIME TEST CIRCUIT

CROSSTALK MEASUREMENT CIRCUIT


A.C. TEST CIRCUITS

OFF-ISOLATION MEASUREMENT CIRCUIT

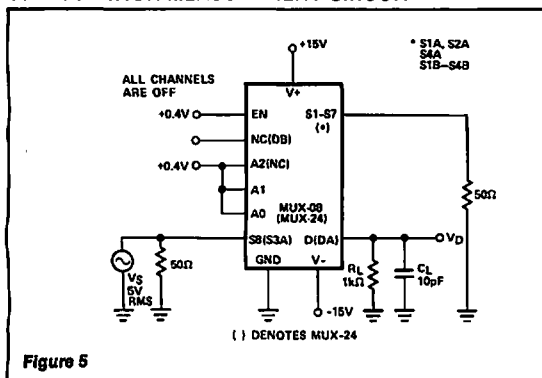
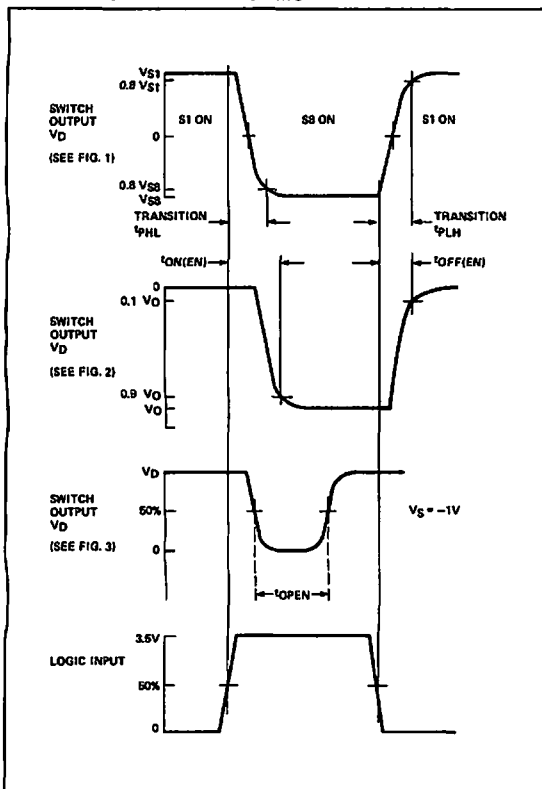


Figure 5

SWITCHING TIME WAVEFORMS



APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Fabricated with Bipolar-JFET processing, special handling as required with CMOS devices, is not necessary to prevent damage to this multiplexer. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal operation, however, positive input voltages should be restricted to $11V$ (or $4V$ less than the positive supply). This assures that the V_{GS} of an "OFF" switch remains greater than its V_p , and prevents that channel from being falsely turned "ON". When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an "ON" switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a $0.01\mu F$ capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_8 = +10V$, the logic input was driven at a $1kHz$ rate. The positive-going slew rate was $0.3V/\mu s$ which is equivalent to a normal I_{OSS} of $3mA$. The negative-going slew rate was $0.7V/\mu s$ which is equivalent to a "reverse" I_{OSS} of $7mA$. Note that when switch 1 is first turned "ON" it has a drop of $-20V$ across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{OSS} .

CROSSTALK AND OFF-ISOLATION

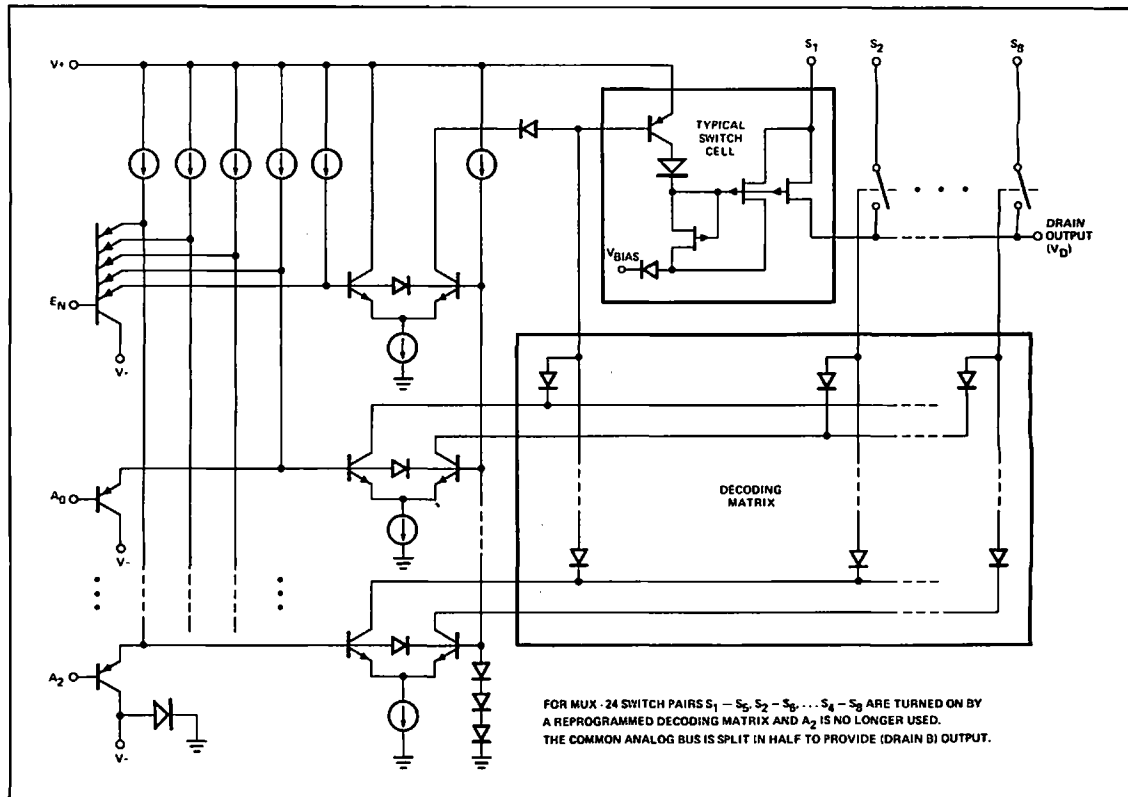
Crosstalk and off-isolation performance is influenced by the type of package selected. Epoxy (P) packaged devices typically exhibit a 12dB improvement in off-isolation ($f = 500\text{kHz}$) performance when compared to ceramic (Q) packaged devices. Epoxy packaged devices typically exhibit a 15dB improvement in crosstalk ($f = 500\text{kHz}$) performance when compared to ceramic (Q) packaged devices.

SINGLE SUPPLY OPERATION OF JFET MULTIPLEXERS

PMI's JFET multiplexers will operate from a single positive supply voltage with the negative supply pin at ground potential. The analog signal range will include ground.

For complete single supply operation information, refer to application note, AN-32.

SIMPLIFIED MUX-08 SCHEMATIC



The simplified MUX-08/MUX-24 schematic shows that logic trip points are determined by two forward diode drops. An internal clamping diode between V- and ground prevents excessive current flow between V+ and ground in the event that V- becomes open circuit. The decoding matrix is accomplished by a programmed diode array. The switch cell consists of P channel JFET's with appropriate blocking diodes which ruggedizes the circuit's overvoltage and supply loss characteristics.

DIFFERENTIAL MULTIPLEXERS

One characteristic unique to differential multiplexers (MUX-24) is the ability to reject common-mode signals from becoming differential error signals. Common-mode rejection is a parameter which defines the amount of rejection in terms of dB. The MUX-24 exhibits a 106dB at 60Hz and 101dB at 400Hz of CMRR using the test circuit of Figure 6.

CMRR TEST CIRCUIT

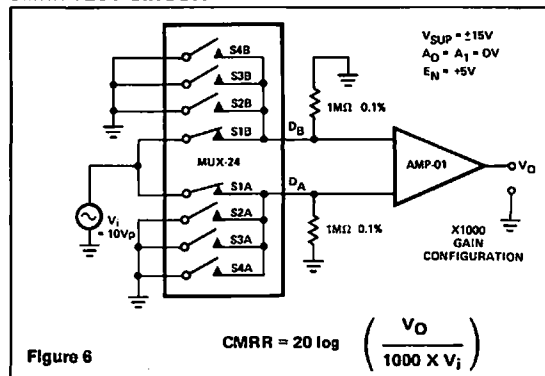
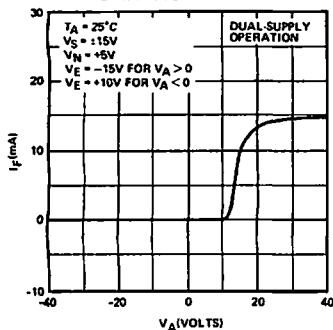


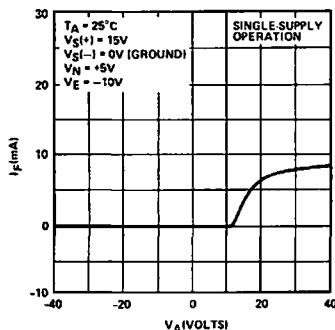
Figure 6

TYPICAL PERFORMANCE CHARACTERISTICS

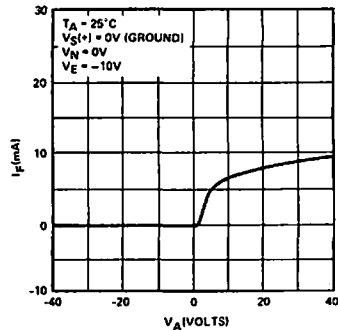
OVERVOLTAGE V-I CHARACTERISTIC



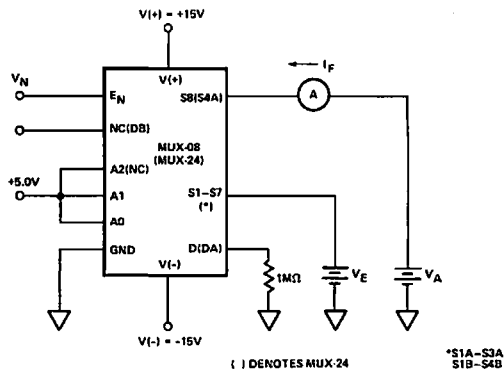
OVERVOLTAGE V-I CHARACTERISTIC



POWER-LOSS V-I CHARACTERISTIC



OVERVOLTAGE/POWER-LOSS MEASUREMENT TEST CIRCUIT



ANALOG SWITCHES/MULTIPLEXERS



MUX-16/MUX-28

16-CHANNEL/DUAL 8-CHANNEL
JFET ANALOG MULTIPLEXERS (OVERVOLTAGE PROTECTED)

Precision Monolithics Inc.

FEATURES

- JFET Switches Rather Than CMOS
- Highly Resistant To Static Discharge Damage
- No SCR Latch-up Problems
- Low "ON" Resistance — 290Ω Typical
- Low Leakage Current
- Digital Inputs Compatible With TTL and CMOS
- Break-Before-Make Action
- 125° C Temperature-Tested Dice Available
- Overvoltage Protected
- Supply Loss Protection
- MUX-16 Pin Compatible With DG506, HI-506A, AD7506
- MUX-28 Pin Compatible With DG507, HI-507A, AD7507

ORDERING INFORMATION†

25° C RESISTANCE	PACKAGE		TEMPERATURE RANGE
	HERMETIC DIP	LCC	
290Ω	MUX16AT*	—	MIL
290Ω	MUX16ET	—	IND
400Ω	MUX16BT*	MUX16BTC/883	MIL
400Ω	MUX16FT	—	IND
290Ω	MUX28AT*	—	MIL
290Ω	MUX28ET	—	IND
400Ω	MUX28BT*	MUX28BTC/883	MIL
400Ω	MUX28FT	—	IND

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

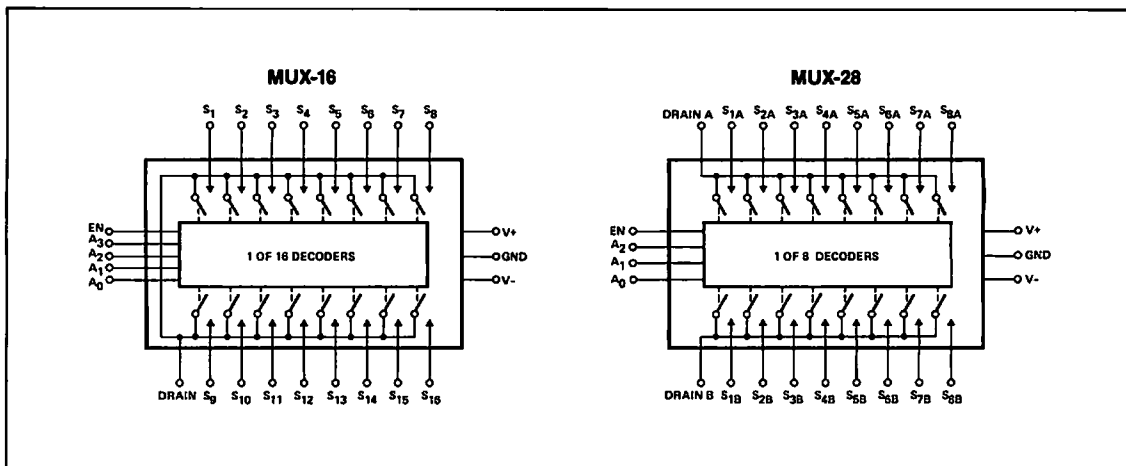
GENERAL DESCRIPTION

The MUX-16 is a monolithic 16-channel analog multiplexer which connects a single output to 1 of the 16 analog inputs depending upon the state of a 4-bit binary address. Disconnection of the output is provided by a logical "0" at the ENABLE input, thereby providing a package selection function.

The MUX-28 is a monolithic 8-channel differential analog multiplexer configured in a double pole, 8-position (plus OFF) electronic switch array. A 3-bit binary input address connects a pair of independent analog inputs from each 8-channel input section to the corresponding pair of independent analog outputs. Disconnection of both inputs is provided by a logical "0" at the ENABLE input, thereby offering a package select function.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, these devices offer low, constant "ON" resistance. Performance advantages include low leakage currents and fast settling time with low crosstalk to satisfy a wide variety of applications. These multiplexers do not suffer from latch-up or static discharge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action without the need for external pull-up resistors. For single 8-channel and dual 4-channel models, refer to the MUX-08/MUX-24 data sheet.

FUNCTIONAL DIAGRAMS




ABSOLUTE MAXIMUM RATINGS (Ratings apply to both DICE and packaged parts, unless otherwise noted.)

Operating Temperature Range, MUX-16/28-AT, BT, BTC	-55°C to +125°C
MUX-16/28-ET, FT	-25°C to +85°C
Junction Temperature (T _J)	-65°C to +150°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	1200mW
Derate Above 75°C	16mW/°C

Lead Temperature (Soldering, 60 sec)	300°C
Maximum Junction Temperature	150°C
V ⁺ Supply to V ⁻ Supply	36V
Logic Input Voltage	(V ⁻ or -4V) to V ⁺ Supply
Analog Input Voltage	V ⁻ Supply -20V to V ⁺ Supply +20V
Maximum Current Through Any Pin	25mA

ELECTRICAL CHARACTERISTICS at V_S = ±15V and T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16A/E MUX-28A/E			MUX-16B/F MUX-28B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R _{ON}	V _S ≤ 10V, I _S ≤ 200μA	—	290	380	—	400	580	Ω
ΔR _{ON} With Applied Voltage	ΔR _{ON}	-10V ≤ V _S ≤ 10V, I _S = 200μA	—	1.5	5	—	1.5	5	%
R _{ON} Match Between Switches	R _{ON} Match	V _S = 0V, I _S = 200μA	—	7	15	—	9	20	%
Analog Voltage Range	V _A	(Note 6)	+10 -10	+11 -15	—	+10 -10	+11 -15	—	V
Source Current (Switch "OFF")	I _S (OFF)	V _S = 10V, V _D = -10V (Note 1)	—	0.01	1	—	0.01	2	nA
Drain Current (Switch "OFF")	I _D (OFF)	V _S = 10V, V _D = -10V (Note 1)	MUX-16	—	0.2	1	—	0.2	nA
			MUX-28	—	0.1	1	—	0.1	
Leakage Current (Switch "ON")	I _D (ON) + I _S (ON)	V _D = 10V (Note 1)	MUX-16	—	0.2	1	—	0.2	nA
			MUX-28	—	0.1	1	—	0.1	
Digital Input Current	I _{IN}	V _{IN} = 0.4V to 15V	—	1	10	—	1	10	μA
Digital "0" Enable Current	I _{INL} (EN)	V _{EN} = 0.4V	—	4	10	—	4	10	μA
Digital Input Capacitance	C _{DIG}		—	3	—	—	3	—	pF
Switching Time (t _{TRAN})	t _{PHL} t _{PLH}	(Notes 2, 5) Figure 1 (Test Circuits)	—	1.4	2.0	—	1.8	2.5	μs
			—	1.2	1.8	—	1.6	2.2	
Output Settling Time	t _S	10V Step to 0.10%	—	2.6	—	—	2.7	—	μs
		10V Step to 0.05%	—	3.2	—	—	3.4	—	
		10V Step to 0.02%	—	4.0	—	—	7.2	—	
Break-Before-Make Delay	t _{OPEN}	Figure 3	—	0.7	—	—	1	—	μs
Enable Delay "ON"	t _{ON, EN}	(Note 5) Figure 2 (Test Circuits)	—	1	2	—	1.2	2.5	μs
Enable Delay "OFF"	t _{OFF, EN}	(Note 5) Figure 2 (Test Circuits)	MUX-16	—	0.25	0.5	—	0.25	μs
			MUX-28	—	0.25	0.5	—	0.25	
"OFF" Isolation	ISO _{OFF}	(Note 4) Figure 4 (Test Circuits)	—	66	—	—	66	—	dB
Crosstalk	CT	(Note 3) Figure 5 (Test Circuits)	—	75	—	—	75	—	dB
Source Capacitance	C _{S, OFF}	Switch "OFF", V _S = 0V, V _D = 0V	—	2.5	—	—	2.5	—	pF
Drain Capacitance	C _{D, OFF}	Switch "OFF", V _S = 0V, V _D = 0V	MUX-16	—	13	—	—	13	pF
			MUX-28	—	8	—	—	8	
Input to Output Capacitance	C _{DS, OFF}	(Note 4)	—	0.15	—	—	0.15	—	pF
Positive Supply Current (All Digital Inputs Logic "0" or "1")	I ⁺	V ⁺ = 15V	MUX-16	—	15	19	—	9	mA
			MUX-28	—	15	19	—	8	
		V ⁺ = 5V	MUX-16	—	12	—	—	8	
			MUX-28	—	12	—	—	7	
Negative Supply Current (All Digital Inputs Logic "0" or "1")	I ⁻	V ⁻ = -15V	MUX-16	—	5	7	—	3.5	mA
			MUX-28	—	5	7	—	3	
		V ⁻ = -5V	MUX-16	—	4	—	—	3	
			MUX-28	—	4	—	—	2.5	

NOTES:

- Conditions applied to leakage tests insure worst case leakages.
- R_L = 10MΩ, C_L = 10pF.
- Crosstalk is measured by driving channel 8 (8B) with channel 7 (7B) ON.
R_L = 1MΩ, C_L = 10pF, V_S = 5V RMS, f = 500kHz.

- "OFF" isolation is measured by driving channel 8 (8B) with ALL channels OFF. R_L = 1kΩ, C_L = 10pF, V_S = 5V RMS, f = 500kHz. C_{DS} is computed from the OFF isolation measurement.
- Sample tested.
- Guaranteed by leakage current and R_{ON} tests.

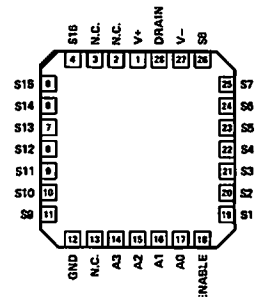
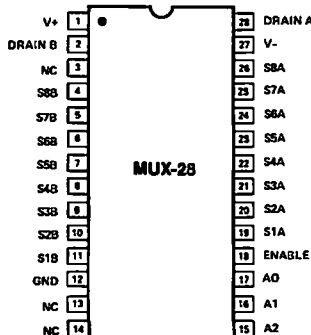
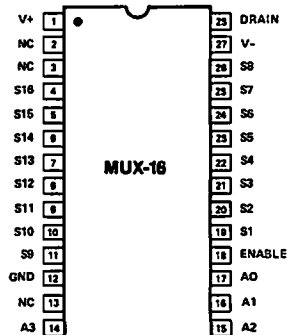


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-55^\circ C \leq T_A \leq +125^\circ C$ for MUX-16AT/BT/BTC and MUX-28AT/BT/BTC; and $-25^\circ C \leq T_A \leq +85^\circ C$ for MUX-16ET/FT and MUX-28ET/FT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16A/E MUX-28A/E			MUX-16B/F MUX-28B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_S \leq 10V$, $I_S \leq 200\mu A$	—	—	500	—	—	800	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$	—	2	—	—	5.5	—	%
R_{ON} Match Between Switches	R_{ON} Match	$V_S = 0V$, $I_S = 200\mu A$	—	10	—	—	15	—	%
Analog Voltage Range	V_A	(Note 6)	+10 -10	+11 -15	—	+10 -10	+11 -15	—	V
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	25	—	—	50	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10V$, $V_D = -10V$ (Note 1)	—	—	75	—	—	250	nA
Leakage Current (Switch "ON")	$I_{D(ON)} + I_{S(ON)}$	$V_D = 10V$ (Note 1)	—	—	75	—	—	250	nA
Digital "1" Input Voltage	V_{INH}	(Note 6)	2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 6)	—	—	0.7	—	—	0.7	V
Digital Input Current	I_{IN}	$V_{IN} = 0.4V$ to $15V$	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.4V$	—	—	20	—	—	20	μA
Positive Supply Current	I_+	All Digital Inputs Logic "0" or "1"	—	—	24	—	—	24	mA
Negative Supply Current	I_-	All Digital Inputs Logic "0" or "1"	—	—	8.2	—	—	8.2	mA

PIN CONNECTIONS & TRUTH TABLES

28-PIN HERMETIC DUAL-IN-LINE (T Suffix)

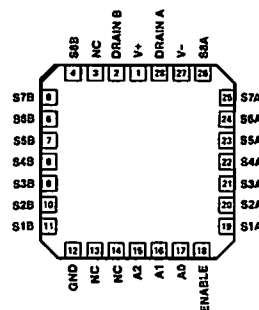
MUX-16BTC/883
LCC
(TC-Suffix)

MUX-16

"ON" CHANNEL					"ON" CHANNEL				
A ₃	A ₂	A ₁	A ₀	EN	A ₃	A ₂	A ₁	A ₀	EN
X	X	X	X	L	NONE	H	L	L	H
L	L	L	L	H	1	H	L	L	H
L	L	L	H	H	2	H	L	H	L
L	L	H	L	H	3	H	L	H	H
L	L	H	H	H	4	H	H	L	L
L	H	L	L	H	5	H	H	L	H
L	H	L	H	H	6	H	H	H	L
L	H	H	L	H	7	H	H	H	H
L	H	H	H	H	8				

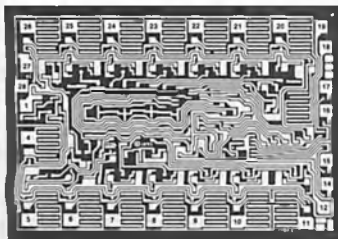
MUX-28

"ON" CHANNEL PAIR					"ON" CHANNEL PAIR				
A ₂	A ₁	A ₀	EN	CHANNEL PAIR	A ₂	A ₁	A ₀	EN	CHANNEL PAIR
X	X	X	L	NONE	X	X	X	L	NONE
L	L	L	H	1	L	L	L	H	1
L	L	H	H	2	L	L	H	H	2
L	H	L	H	3	L	H	L	H	3
L	H	H	H	4	L	H	H	H	4
H	L	L	H	5	H	L	L	H	5
H	L	H	H	6	H	L	H	H	6
H	H	L	H	7	H	H	L	H	7
H	H	H	H	8	H	H	H	H	8

MUX-28BTC/883
LCC
(TC-Suffix)

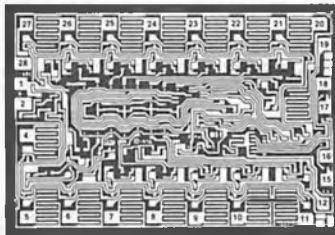


DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



MUX-16

MUX-28



DIE SIZE 0.110 × 0.076 inch, 8360 sq. mils
(2.794 × 1.930 mm, 5392 sq. mm)

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

1. POSITIVE SUPPLY
4. SOURCE 16 (S16)
5. SOURCE 15 (S15)
6. SOURCE 14 (S14)
7. SOURCE 13 (S13)
8. SOURCE 12 (S12)
9. SOURCE 11 (S11)
10. SOURCE 10 (S10)
11. SOURCE 9 (S9)
12. GROUND
14. ADDRESS BIT 3 (A3)
15. ADDRESS BIT 2 (A2)
16. ADDRESS BIT 1 (A1)
17. ADDRESS BIT 0 (A0)
18. ENABLE
19. SOURCE 1 (S1)
20. SOURCE 2 (S2)
21. SOURCE 3 (S3)
22. SOURCE 4 (S4)
23. SOURCE 5 (S5)
24. SOURCE 6 (S6)
25. SOURCE 7 (S7)
26. SOURCE 8 (S8)
27. NEGATIVE SUPPLY (SUBSTRATE)
28. DRAIN

1. POSITIVE SUPPLY
2. DRAIN B
4. SOURCE 8 (S8B)
5. SOURCE 7 (S7B)
6. SOURCE 6 (S6B)
7. SOURCE 5 (S5B)
8. SOURCE 4 (S4B)
9. SOURCE 3 (S3B)
10. SOURCE 2 (S2B)
11. SOURCE 1 (S1B)
12. GROUND
15. ADDRESS BIT 2 (A2)
16. ADDRESS BIT 1 (A1)
17. ADDRESS BIT 0 (A0)
18. ENABLE
19. SOURCE 1 (S1A)
20. SOURCE 2 (S2A)
21. SOURCE 3 (S3A)
22. SOURCE 4 (S4A)
23. SOURCE 5 (S5A)
24. SOURCE 6 (S6A)
25. SOURCE 7 (S7A)
26. SOURCE 8 (S8A)
27. NEGATIVE SUPPLY (SUBSTRATE)
28. DRAIN A

WAFER TEST LIMITS at $V_+ = 15V$, $V_- = -15V$, $T_A = 25^\circ C$ for MUX-16/28 N and G, $T_A = 125^\circ C$ for MUX-16/28 NT and GT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT LIMIT	MUX-16/ MUX-28N LIMIT	MUX-16/ MUX-28GT LIMIT	MUX-16/ MUX-28G LIMIT	UNITS
"ON" Resistance	R_{ON}	$V_S = 0V$, $I_S = 200\mu A$	540	380	800	580	Ω MAX
Digital "1" Input Voltage	V_{INH}		2	2	2	2	V MIN
Digital "0" Input Voltage	V_{INL}		0.8	0.8	0.8	0.8	V MAX
Digital "0" Input Current	I_{INL}	$V_{IN} = 0.4V$	20	10	20	10	μA MAX
Digital "0" Enable Current	I_{INLENI}	$V_{EN} = 0.4V$	20	10	20	10	μA MAX
Positive Supply Current (All Digital Inputs Logic "0")	I_+		24	19	24	19	mA MAX
Negative Supply Current (All Digital Inputs Logic "0")	I_-		8.2	7	8.2	7	mA MAX
Analog Input Range	V_A	(Note 2)	± 10	± 10	± 10	± 10	V MIN

NOTE:

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_+ = 15V$, $V_- = -15V$ and $T_A = 25^\circ C$ for MUX-16/28 N and G, $T_A = 125^\circ C$ for MUX-16/28 NT and GT, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-16/ MUX-28NT TYPICAL	MUX-16/ MUX-28N TYPICAL	MUX-16/ MUX-28GT TYPICAL	MUX-16/ MUX-28G TYPICAL	UNITS
Switching Time (t_{TRAN})	t_{PHL} t_{PLH}	(Note 1) Figure 1	2 1.8	1 0.9	2.6 2.4	1.5 1.4	μs
Output Settling Time	t_S	10V Step to 0.1% (Note 1)	2.5	1.5	2.9	1.9	μs
Break-Before-Make Delay	t_{OPEN}	(Note 1) Figure 3 (Test Circuits)	0.8	0.8	1	1	μs
Crosstalk	CT	(Note 1) Figure 5 (Test Circuits)	70	70	70	70	dB
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10V \leq V_S \leq 10V$, $I_S = 200\mu A$	1.5	1.5	1.5	1.5	%
Leakage Current (Switch "ON")	$I_{D(ON)}$	$V_D = 10V$ (Note 1)	20	0.2	20	0.2	nA
Analog Input Range	V_A	(Note 2)	+11 -15	+11 -15	+11 -15	+11 -15	V

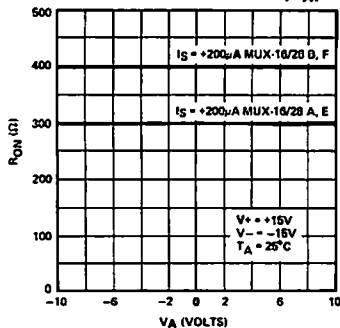
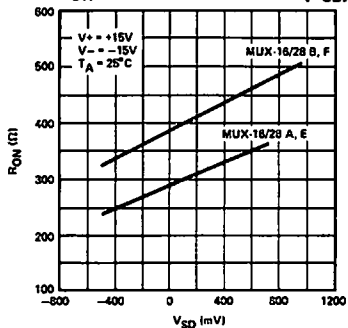
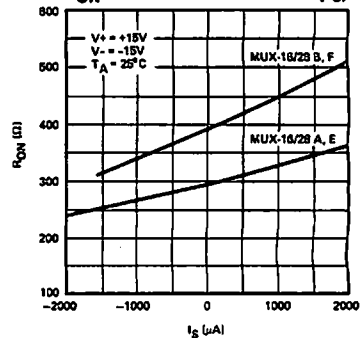
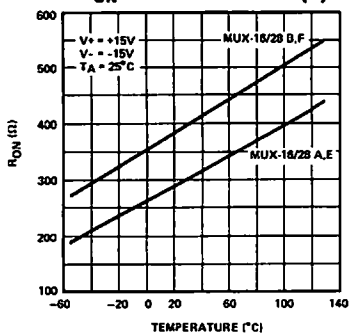
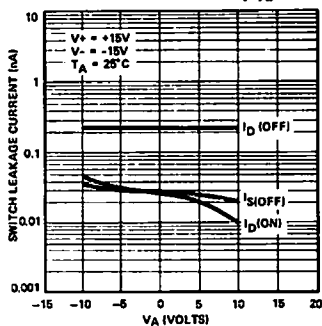
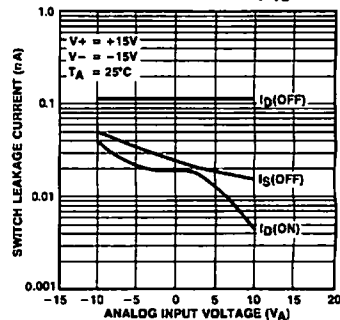
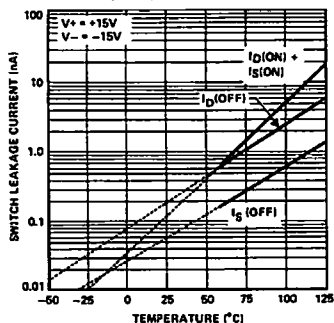
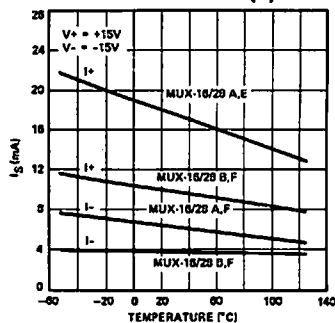
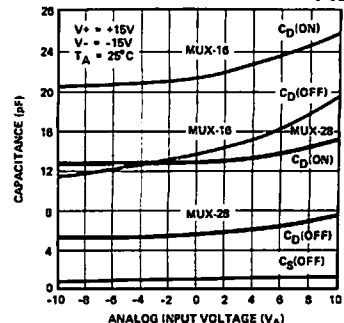
NOTES:

1. The data shown is extrapolated from measurements made on the packaged devices.

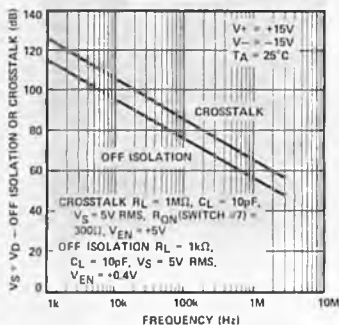
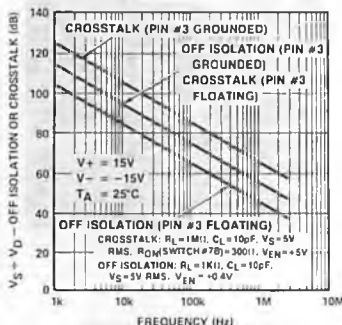
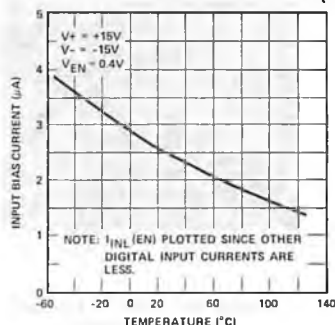
2. Guaranteed by R_{ON} and leakage current tests.

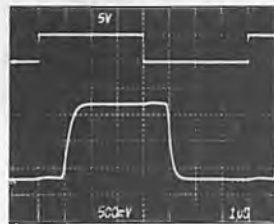
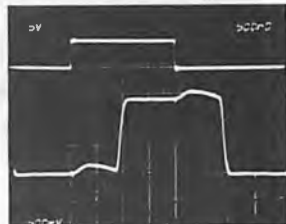
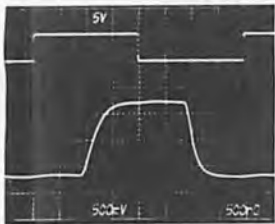
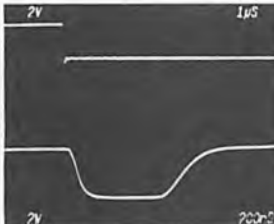
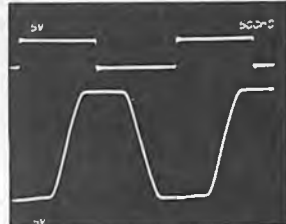


TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

**"ON" RESISTANCE (R_{ON})
vs ANALOG VOLTAGE (V_A)** **R_{ON} vs SWITCH VOLTAGE (V_{SD})** **R_{ON} vs SWITCH CURRENT (I_S)** **R_{ON} vs TEMPERATURE (T)****MUX-16 SWITCH LEAKAGE
CURRENTS vs ANALOG
INPUT VOLTAGE (V_A)****MUX-28 SWITCH LEAKAGE
CURRENTS vs ANALOG
INPUT VOLTAGE (V_A)****SWITCH LEAKAGE CURRENTS
vs TEMPERATURE****SUPPLY CURRENTS vs
TEMPERATURE (T)****SWITCH CAPACITANCES vs
ANALOG INPUT VOLTAGE (V_A)**

TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

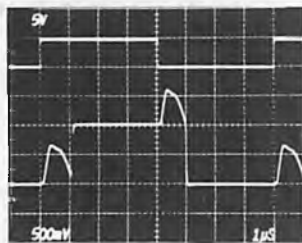
**MUX-16
OFF PERFORMANCE OF
CHANNEL 8**

**MUX-28
OFF PERFORMANCE OF
CHANNEL 8**

**DIGITAL INPUT BIAS
CURRENTS vs TEMPERATURE (T)**

MUX-16 DYNAMIC CHARACTERISTIC CURVES
SMALL-SIGNAL SWITCHING

 $R_L = 1M\Omega, C_L = 10pF, V_1 = -500mV, V_{16} = +500mV$
**SMALL-SIGNAL SWITCHING
WITH FILTERING**

 $R_L = 1M\Omega, C_L = 500pF, V_1 = -500mV, V_{16} = +500mV$
**SMALL-SIGNAL SWITCHING
WITH 2μs SAMPLE TIME**

 $R_L = 1M\Omega, C_L = 10pF, V_1 = -700mV, V_{16} = +700mV$
**SMALL-SIGNAL SWITCHING
WITH FILTERING AND
2μs SAMPLE TIME**

 $R_L = 1M\Omega, C_L = 500pF, V_1 = -700mV, V_{16} = +700mV$
**BREAK-BEFORE-MAKE
SWITCHING**

 $R_L = 1k\Omega, C_L = 10pF, V_1 = V_{16} = +10V$
LARGE-SIGNAL SWITCHING

 $R_L = 1M\Omega, C_L = 10pF, V_1 = -10V, V_{16} = +10V$
NOTE:

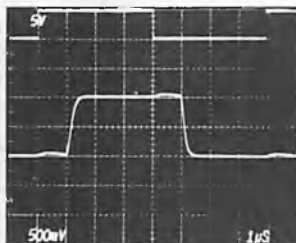
Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplexer Output (V_D)

MUX-28 DYNAMIC CHARACTERISTIC CURVES

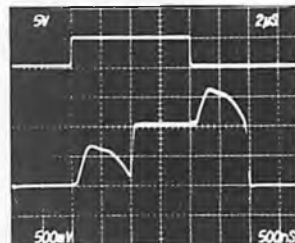
SMALL-SIGNAL SWITCHING


 $R_L = 1M\Omega, C_L = 10pF, V_1 = -500mV, V_G = +500mV$

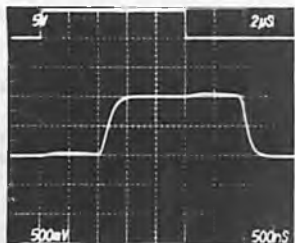
SMALL-SIGNAL SWITCHING WITH FILTERING


 $R_L = 1M\Omega, C_L = 500pF, V_1 = -500mV, V_G = +500mV$

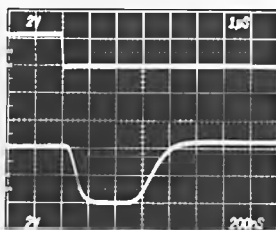
SMALL-SIGNAL SWITCHING WITH 2μs SAMPLE TIME


 $R_L = 1M\Omega, C_L = 10pF, V_1 = -700mV, V_G = +700mV$

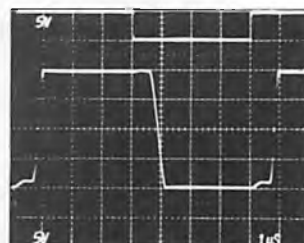
SMALL-SIGNAL SWITCHING WITH FILTERING AND 2.5μs SAMPLE TIME


 $R_L = 1M\Omega, C_L = 500pF, V_1 = -700mV, V_G = +700mV$

BREAK-BEFORE-MAKE SWITCHING


 $R_L = 1K\Omega, C_L = 10pF, V_1 = V_G = +10V$

LARGE-SIGNAL SWITCHING


 $R_L = 1M\Omega, C_L = 10pF, V_1 = -10V, V_G = +10V$

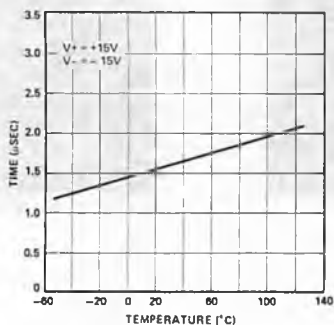
NOTE:

Top Waveforms: Digital Input 5V/Div

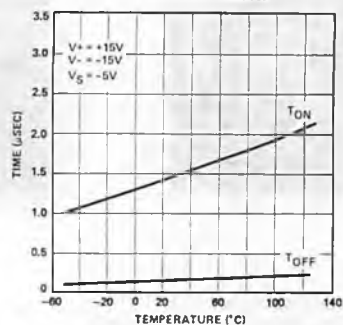
 Bottom Waveforms: Multiplexer Output (V_D)

TYPICAL PERFORMANCE CHARACTERISTICS (apply to all grades, unless otherwise noted.)

TRANSITION TIME vs TEMPERATURE

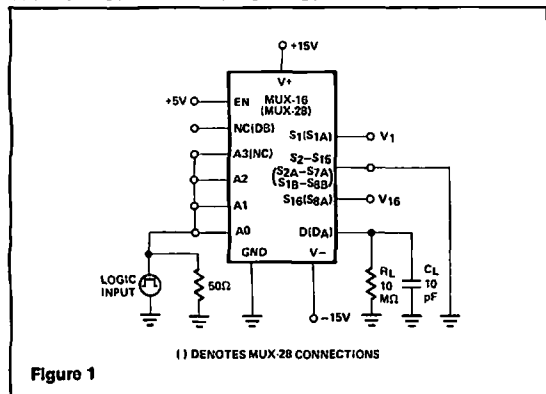


ENABLE DELAY TIME vs TEMPERATURE

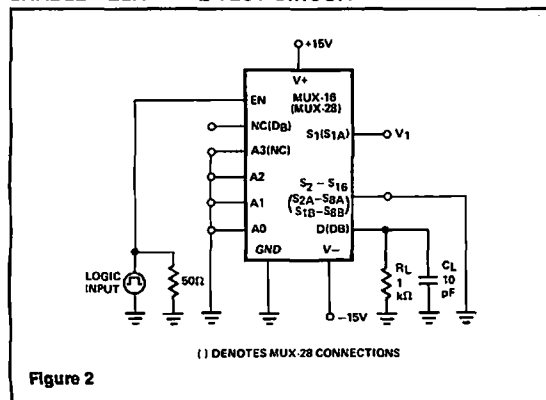


A.C. TEST CIRCUITS

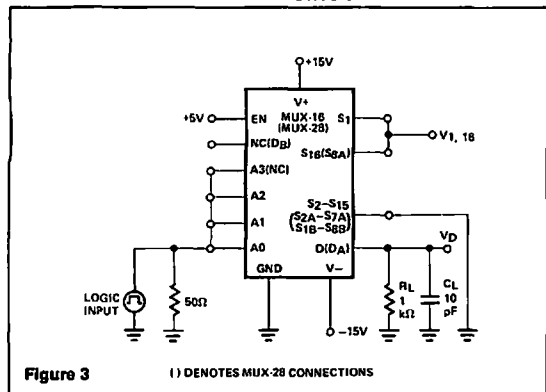
TRANSITION TIME TEST CIRCUIT



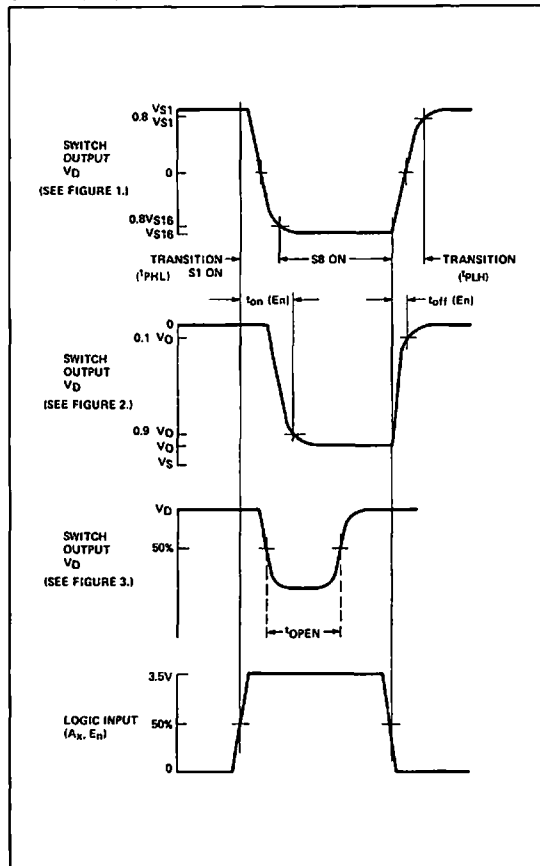
ENABLE DELAY TIME TEST CIRCUIT



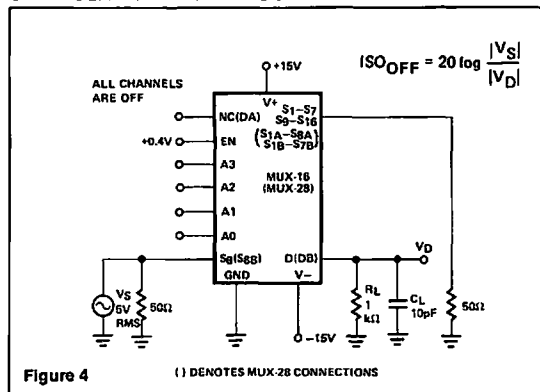
BREAK-BEFORE-MAKE TEST CIRCUIT



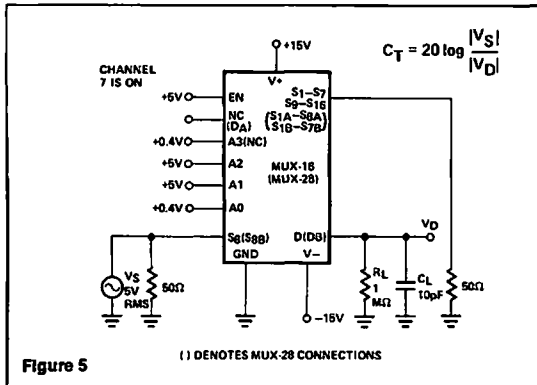
SWITCHING TIME WAVEFORMS



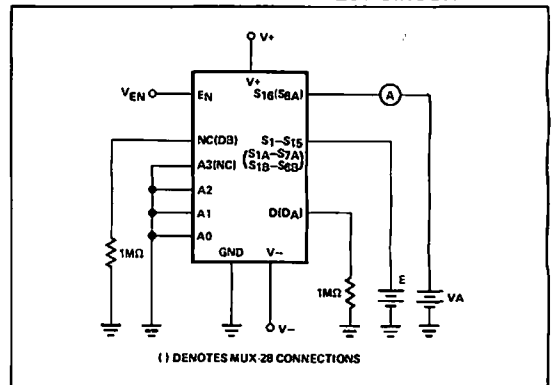
OFF ISOLATION TEST CIRCUIT



CROSSTALK MEASUREMENT CIRCUIT



OVERVOLTAGE MEASUREMENT TEST CIRCUIT



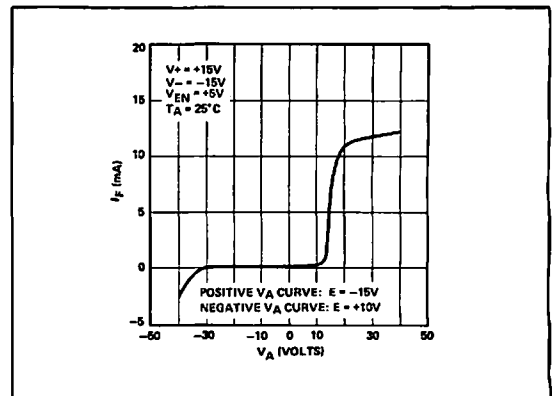
APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make (B.B.M.) action. The turn-off time is much faster than the turn-on time to guarantee B.B.M. over the full operating temperature and input voltage range. Fabricated with JFET processing rather than CMOS, special handling is not necessary to prevent damage to this multiplexer. Because the digital inputs only require a 2.0V logic "1" input level, power-consuming pullup resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

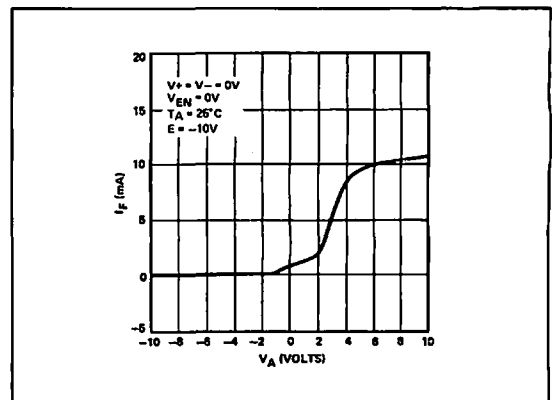
The "ON" resistance, R_{ON} of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. The overvoltage and supply-loss V-I characteristics shown indicate typical performance when the multiplexer is subjected to abnormal signals. For normal operation, however, positive input voltages should be restricted to 11V (or 4V less than the positive supply). This assures that the V_{GS} of an OFF FET switch remains greater than its V_p , preventing that channel from being falsely turned ON.

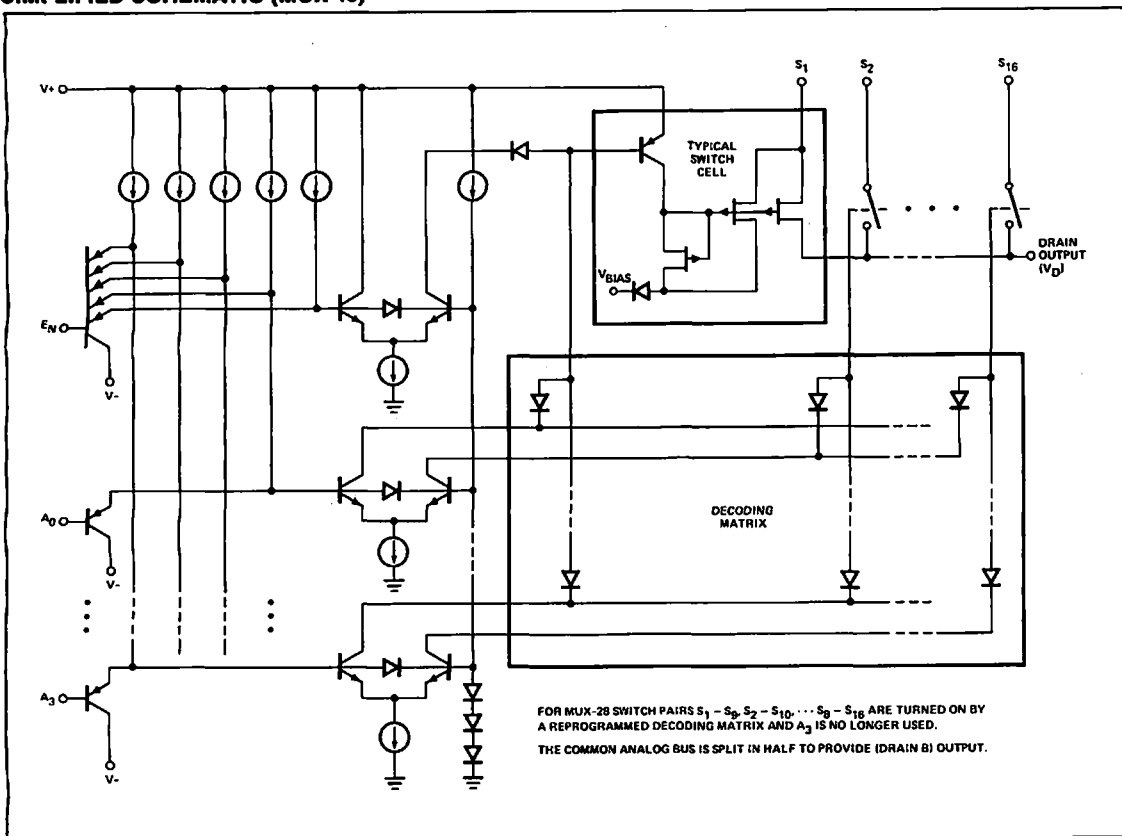
When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output has been loaded with a $0.01\mu F$ capacitor in the circuit of Figure 1. With $V_1 = -10V$ and $V_{16} = +10V$, the logic input was driven at a 1kHz rate. The positive-going slew rate was $0.3V/\mu Sec$ which is equivalent to a normal I_{DSS} of 3mA. The negative-going slew rate was $0.7V/\mu sec$ which is equivalent to a "reverse" I_{DSS} of 7mA. Note that when switch one (1) is first turned ON it has a drop of $-20V$ across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS} .

OVERVOLTAGE V-I CHARACTERISTIC



SUPPLY-LOSS V-I CHARACTERISTIC



SIMPLIFIED SCHEMATIC (MUX-16)




MUX-88

8-CHANNEL ANALOG MULTIPLEXER FOR PCM CODECS (OVERVOLTAGE PROTECTED)

Precision Monolithics Inc.

FEATURES

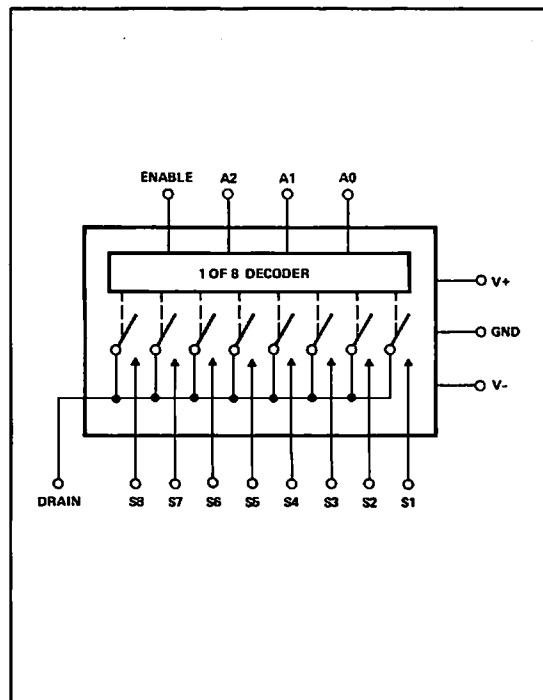
- Compatible with Standards for Noise and Crosstalk in Telephony Systems
- Pin Compatible with DG508, HI-508A, LF11508
- JFET Switches Rather Than CMOS
- Low "ON" Resistance — 220Ω Typical
- Low Output Leakage Current — 100nA Max
- Digital Inputs Compatible with TTL and CMOS
- Input Overvoltage and Supply Loss Protected

ORDERING INFORMATION†

R _{ON}	MODEL	TEMP RANGE
400Ω	MUX-88EQ	IND
520Ω	MUX-88FQ	IND

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

FUNCTIONAL DIAGRAM



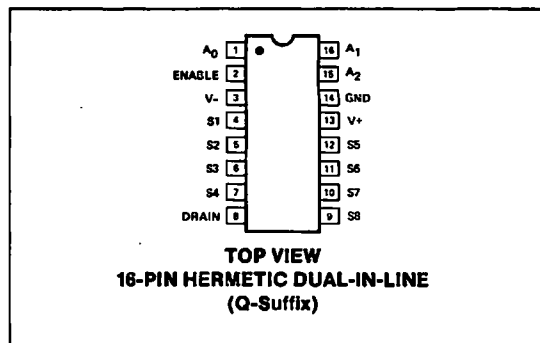
GENERAL DESCRIPTION

The MUX-88 is a monolithic eight-channel analog multiplexer ideally suited to shared-channel PCM CODEC systems. One-of-eight channels is selected upon the decoding of a 3 bit binary address. An enable input (E_n) disables all switches when logic low providing package select. All logic control inputs have true TTL input compatibility eliminating the need for pull-up resistors necessary for some CMOS equivalent products.

Fabricated with Precision Monolithics' high performance Bipolar-JFET technology, this device offers low "ON" resistance, low leakage, fast settling time and excellent crosstalk isolation (98dB @ 20kHz). These characteristics make this device suitable for meeting system level communication requirements in shared-channel PCM CODECs.

Additional ruggedization results from built-in overvoltage, supply loss, and latch-up free circuit characteristics.

PIN CONNECTIONS



TRUTH TABLE

A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

**ABSOLUTE MAXIMUM RATINGS** ($T_A = 25^\circ\text{C}$, unless otherwise noted)

Operating Temperature Range,

MUX-88EQ, FQ -25°C to $+85^\circ\text{C}$ Storage Temperature Range -65°C to $+150^\circ\text{C}$

Power Dissipation 500mW

Derate above 100°C 10mW/ $^\circ\text{C}$ Lead Temperature (Soldering, 60 sec) 300°C

V+ Supply to V- Supply 36V

V+ Supply to Ground 18V

Logic Input Voltage (Note 5) (V- or -4V) to V+

Analog Input Voltage V- Supply -20V to V+ Supply +20V

Maximum Current Through Any Pin 25mA

ELECTRICAL CHARACTERISTICS for $V+ = -15\text{V}$ and $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MUX-88E			MUX-88F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"ON" Resistance	R_{ON}	$V_S = 0\text{V}$, $I_S = 200\mu\text{A}$	—	—	400	—	—	520	Ω
ΔR_{ON} With Applied Voltage	ΔR_{ON}	$-10\text{V} \leq V_S \leq 10\text{V}$, $I_S = 200\mu\text{A}$	—	1.5	—	—	4.5	—	%
R_{ON} Match Between Switches	$R_{ON \text{ Match}}$	$V_S = 0\text{V}$, $I_S = 200\mu\text{A}$	—	25	—	—	30	—	Ω
Source Current (Switch "OFF")	$I_{S(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$, (Note 1)	—	—	10	—	—	10	nA
Drain Current (Switch "OFF")	$I_{D(OFF)}$	$V_S = 10\text{V}$, $V_D = -10\text{V}$, (Note 1)	—	—	100	—	—	100	nA
Leakage Current (Switch "ON")	$I_{D(ON)} + I_{S(ON)}$	$V_D = 10\text{V}$, (Note 1)	—	—	100	—	—	100	nA
Digital "1" Input Voltage	V_{INH}	(Note 5)	2	—	—	2	—	—	V
Digital "0" Input Voltage	V_{INL}	(Note 5)	—	—	0.8	—	—	0.8	V
Digital Input Current	I_{IN}	$V_{IN} = 0.7\text{V}$ to $+5\text{V}$	—	—	20	—	—	20	μA
Digital "0" Enable Current	$I_{INL(EN)}$	$V_{EN} = 0.7\text{V}$	—	—	20	—	—	20	μA
Positive Supply Current	I^+	All Digital Inputs Logic "0"	—	—	15	—	—	15	mA
Negative Supply Current	I^-	All Digital Inputs Logic "0"	—	—	5	—	—	5	mA
Switching Time (t_{TRAN})	t_{PHL}	Figure 1, (Note 2)	—	1.8	2.1	—	2.2	2.5	μs
	t_{PLH}		—	1.3	1.6	—	1.7	2.0	
Output Settling Time	t_S	10V Step 0.10%	—	1.3	—	—	1.7	—	μs
		10V Step 0.05%	—	1.5	—	—	1.9	—	
		10V Step 0.02%	—	2.3	—	—	2.5	—	
Break-Before-Make Delay	t_{OPEN}		—	0.8	—	—	1.0	—	μs
Enable Delay "ON"	$t_{ON(EN)}$		—	1.0	—	—	1.2	—	μs
Enable Delay "OFF"	$t_{OFF(EN)}$		—	0.2	—	—	0.2	—	μs
"OFF" Isolation	ISO_{OFF}	(Note 4)	—	88	—	—	88	—	dB
Crosstalk	CT	(Note 3)	—	88	—	—	88	—	dB
Source Capacitance	$C_{S(OFF)}$	Switch "OFF", $V_S = 0\text{V}$, $V_D = 0\text{V}$	—	2.5	—	—	2.5	—	pF
Drain Capacitance	$C_{D(OFF)}$	Switch "OFF", $V_S = 0\text{V}$, $V_D = 0\text{V}$	—	7	—	—	7	—	pF
Input to Output Capacitance	$C_{DS(OFF)}$	(Note 4)	—	0.3	—	—	0.3	—	pF

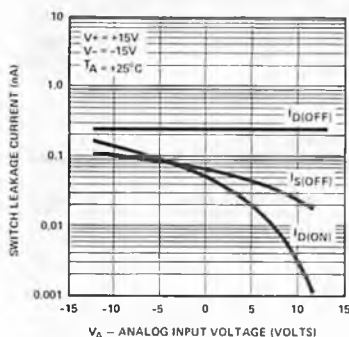
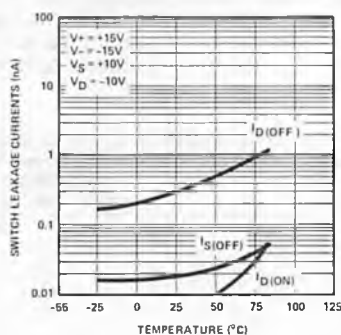
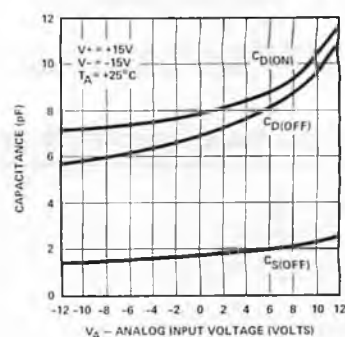
NOTES:

- Conditions applied to leakage tests insure worst case leakages. Exceeding 11V on the analog input may cause an "OFF" channel to turn "ON".
- Sample tested. The measurement conditions of Figure 1 insure worst case transition time.
- Crosstalk is measured by driving channel 8 with channel 4 ON.
 $R_L = 1\text{M}\Omega$, $C_L = 10\text{pF}$, $V_S = 5\text{V RMS}$, $f = 20\text{kHz}$. (See Figure 2)
- OFF isolation is measured by driving channel 8 with ALL channels OFF.
 $R_L = 1\text{k}\Omega$, $C_L = 10\text{pF}$, $V_S = 5\text{V RMS}$, $f = 20\text{kHz}$. C_{DS} is computed from the OFF isolation measurement.
- Guaranteed by R_{ON} and leakage current testing. For normal operation maximum analog signal voltages should be restricted to less than $(V+) - 4\text{V}$.

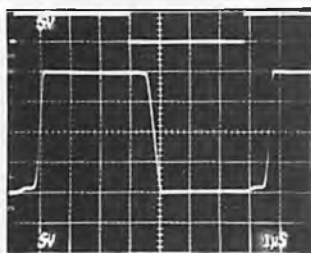
DICE

For applicable DICE information see MUX-08/MUX-24 data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS

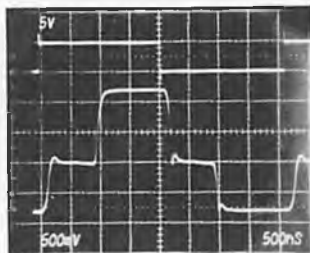
 SWITCH LEAKAGE CURRENTS
vs ANALOG INPUT VOLTAGE

 SWITCH LEAKAGE CURRENTS
vs TEMPERATURE

 SWITCH CAPACITANCE vs
ANALOG INPUT VOLTAGE


LARGE-SIGNAL SWITCHING

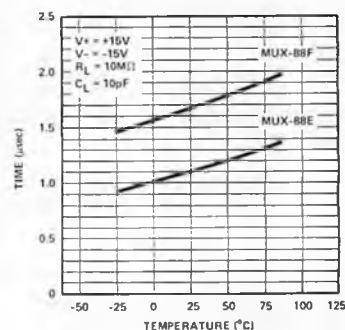


* $R_L = 10M\Omega$, $C_L = 10pF$, $V_I = -10V$, $V_B = +10V$
Voltage = 5V/Div, Time = 1μs/Div, See
Transition Time Circuit of Figure 1.

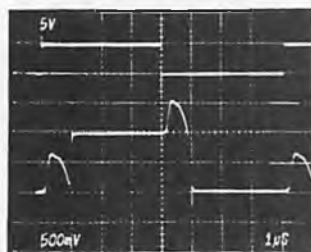
BREAK-BEFORE-MAKE SWITCHING



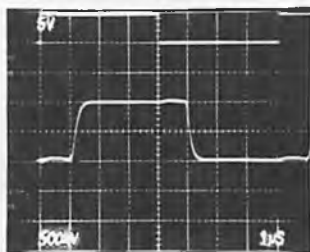
*Voltage = 500mV/Div, Time = 500ns/Div, See
Break-Before-Make Circuit of Figure 3.

 TRANSITION TIMES
vs TEMPERATURE


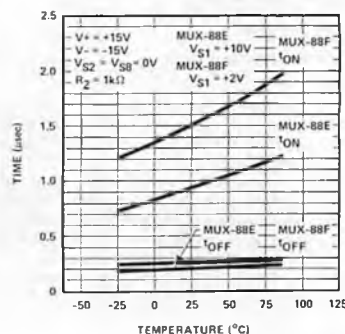
SMALL-SIGNAL SWITCHING



* $R_L = 1M\Omega$, $C_L = 10pF$, $V_I = -500mV$,
 $V_{SB} = +500mV$ Voltage = 500mV/Div,
Time = 1μs/Div, See Transition Circuit of
Figure 1.

 SMALL-SIGNAL SWITCHING
WITH FILTERING


* $R_L = 1M\Omega$, $C_L = 500pF$, $V_I = -500mV$,
 $V_{SB} = 500mV$ Voltage = 500mV/Div,
Time = 1μs/Div, See Transition Time
Circuit of Figure 1.

 ENABLE DELAY TIME
vs TEMPERATURE


NOTE:

*Top Waveforms: Digital Input 5V/Div
Bottom Waveforms: Multiplex Output

A.C. TEST CIRCUITS

TRANSITION TIME

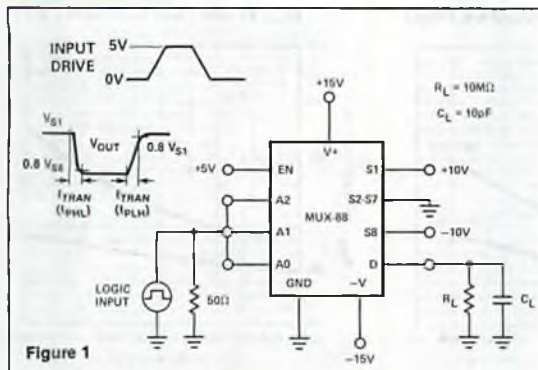


Figure 1

CROSSTALK MEASUREMENT CIRCUIT

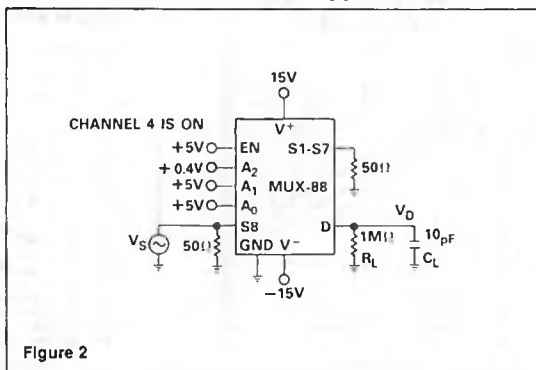


Figure 2

BREAK-BEFORE-MAKE DELAY

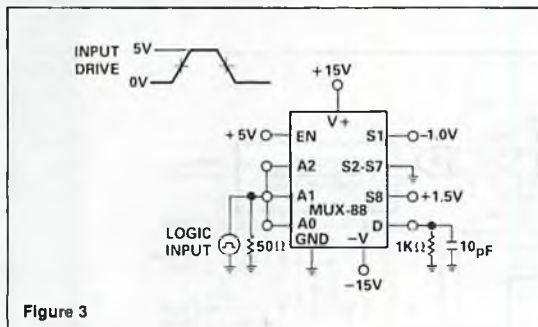


Figure 3

OFF ISOLATION MEASUREMENT CIRCUIT

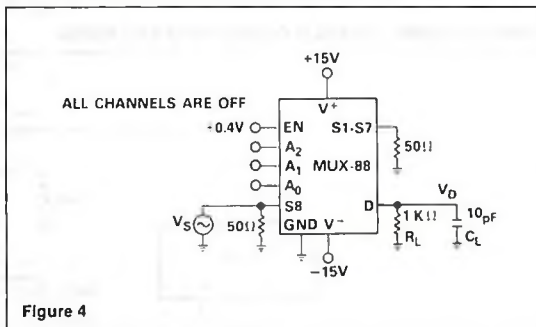


Figure 4

APPLICATIONS INFORMATION

These analog multiplexers employ ion-implanted JFETs in a switch configuration designed to assure break-before-make action. The turn-off time is much faster than the turn-on time to guarantee this feature over the full operating temperature and input voltage range. Because the digital inputs only require a 2V logic "1" input level, power-consuming pull-up resistors are not required for TTL compatibility to insure break-before-make switching as is most often the case with CMOS multiplexers. The digital inputs utilize PNP input transistors where input current is maximum at the logic "0" level and drops to that of a reverse-biased diode (about 10nA) as the input voltage is raised above $\approx 1.4V$.

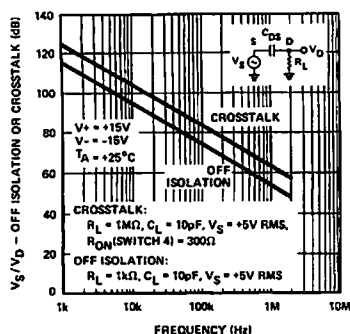
The "ON" resistance, R_{ON} , of the analog switches is constant over the wide input voltage range of $-15V$ to $+11V$ with $V_{SUPPLY} = \pm 15V$. Higher input voltage is tolerable provided that some form of current limiting is employed (such as that of an op-amp output stage) to avoid exceeding junction temperature and power dissipation requirements. For normal

operation, however, positive input voltages should be restricted to $11V$ (or $4V$ less than the positive supply). This assures that the V_{GS} of an OFF switch remains greater than its V_P , and prevents that channel from being falsely turned ON.

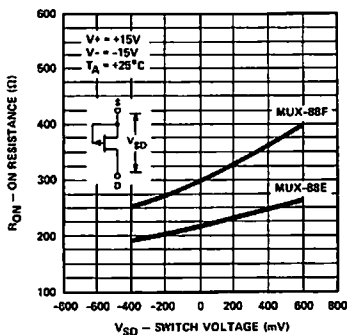
When operating with negative input voltages, the gate-to-channel diode will be turned on if the voltage drop across an ON switch exceeds $-0.6V$. While this condition will cause an error in the output, it will not damage the switch. In lab tests, the multiplexer output load capacitor has increased to $0.01\mu F$ in the Transition Time circuit, Figure 1. With $V_{S1} = -10V$ and $V_{S8} = +10V$, the logic input was driven at a $1kHz$ rate. The positive-going slew rate was $0.3V/\mu sec$ which is equivalent to a normal I_{DSS} of $3mA$. The negative-going slew rate was $0.7V/\mu sec$ which is equivalent to a "reverse" I_{DSS} of $7mA$. Note that when switch 1 is first turned ON it has a drop of $-20V$ across its terminals. In spite of that fact, the current is limited to approximately twice its normal I_{DSS} .

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

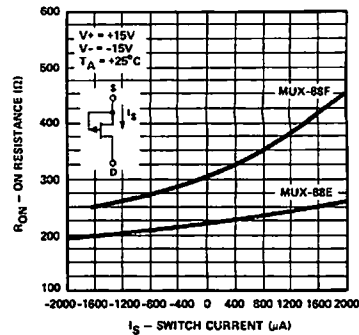
OFF PERFORMANCE OF CHANNEL 8



R_{ON} vs SWITCH VOLTAGE (V_{SD})

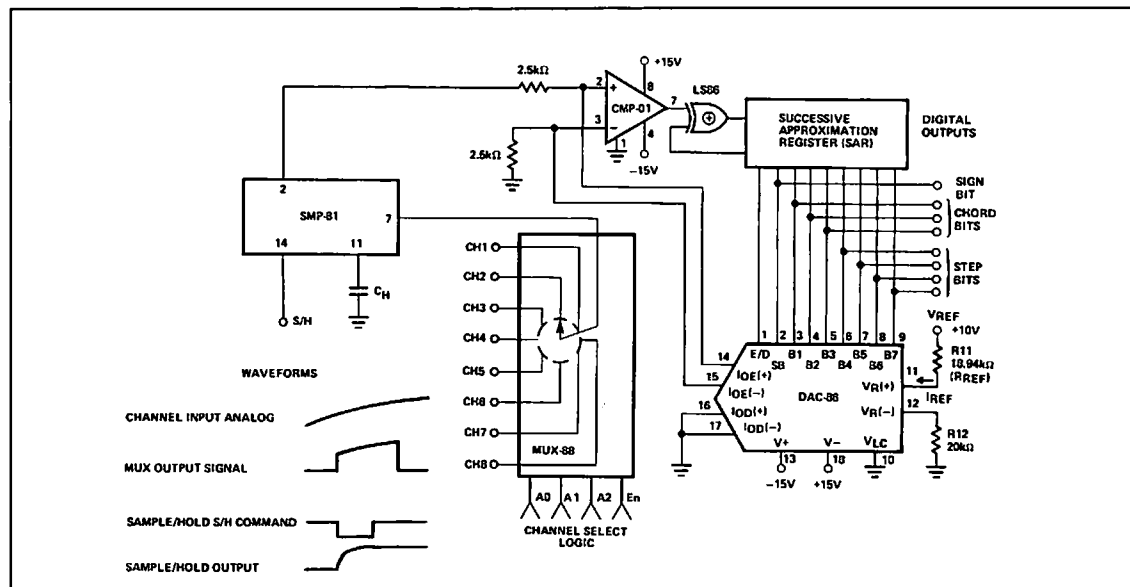


R_{ON} vs SWITCH CURRENT (I_S)



TYPICAL APPLICATION

EIGHT-CHANNEL SHARED CODEC PCM ENCODER



CROSSTALK IN PCM SYSTEMS

In PAM or PCM systems crosstalk specifications for components, such as multiplexers, are related to overall system crosstalk specifications in a complex manner. Component specification must, of necessity, refer to the operation of the multiplexer in a non-sampling mode of operation. When rapid sequential sampling takes place, such as would be the case with a typical shared-channel CODEC, crosstalk will be caused by the off isolation properties of the

multiplexer as well as by storage elements on chip and PC card stray capacitance. For example, the capacitance has the effect of conferencing the channels and increasing crosstalk. Thus, system crosstalk in a shared-channel PCM CODEC is influenced by multiplexed characteristics as well as PC card layout and the timing relationship between the multiplexer and the sample-hold circuit.

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SAMPLE-AND-HOLD AMPLIFIERS

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Precision Monolithics Inc.

SAMPLE-AND-HOLD AMPLIFIERS

INTRODUCTION

Sample-and-hold amplifiers "sample" an analog input signal and then "hold" the instantaneous input value upon the command of a logic control signal. Basically the sample-and-hold is an "analog memory" where a capacitor serves as the storage element. Applications in which a time varying input cannot be tolerated require sample-and-hold circuits. A fast successive-approximation analog-to-digital converter is one application. Data acquisition, data distribution, analog delay and telephony require sample-and-hold circuits to "freeze" the analog signal for further signal processing.

PMI sample-and-hold amplifiers are functionally identical to track-and-hold circuits. They continuously track input signals during the sample mode. PMI circuits should not be confused with AC controlled sample-and-holds. When an AC controlled sample-and-hold is commanded to sample, it will take a fast sample and immediately return to the hold mode. It can not continuously track an input signal.

A sample-and-hold circuit consists of an amplifier, switch, and capacitor. Many specifications are similar to those of switches and operational amplifiers — bias currents, voltage gain, and charge injection are examples. These and other specifications pertaining uniquely to sample-and-hold circuits are defined below.

The SMP-10 and SMP-11 are precision sample-and-hold amplifiers with high accuracy, low droop rate, and fast signal acquisition time. These circuits contain a high impedance input buffer, a diode bridge switch, a transconductance or "Super-Charger" circuit to enhance slewing and a high speed output amplifier. The "Super-Charger" is capable of supplementing the capacitor charging current whenever the difference between input and output levels exceeds a given threshold. Settling to final value is under control of currents from the diode

bridge, thus minimizing overshoot and instability. The inherent low offset voltage errors and low charge injection allows the residual zero-scale errors to be actively trimmed using PMI's zener-zapping technology without degrading temperature performance. "Super Beta" transistors provides the high input-impedance amplifier needed for low droop rate and minimal signal loading.

The SMP-10 and SMP-11 have different droop rate and settling hold mode times specifications.

The SMP-81 is characterized for the sampling requirements found in telecommunications applications.

In addition to precision sample-and-hold amplifiers, a product with related capabilities is available: the PKD-01 monolithic peak detector. This device performs the peak detector function with accuracies approaching those obtainable with high cost hybrid modules at a cost approaching the low cost, low performance discrete designs. A data sheet for the PKD-01 is located in this section of the catalog.

DEFINITIONS

Acquisition Time (t_{aq})— The minimum time for the output voltage to begin tracking the input voltage, to within a specified error band, after the inception of the sample command. By convention, acquisition time is defined for sampling of a DC level. For instance a circuit which is "holding" a 10V output signal, and operating with zero input volts, is switched to the sample mode. The acquisition time is then the time required for the output to decrease to within a $\pm 10\text{mV}$ (0.01%FS) band about ground potential (see timing diagram).

Aperture Jitter (Δt_a) — The maximum amount of deviation in aperture time from sample to sample. Errors resulting from aperture jitter increase



Precision Monolithics Inc.

SAMPLE-AND-HOLD AMPLIFIERS

in proportion to the slew rate of the sampled analog input signal. Also called aperture uncertainty time.

Aperture Time (t_{ap}) — The time between the inception of the hold command and the time the circuit output ceases tracking the input signal (see timing diagram).

Change In Hold Step (ΔV_{HS}) — Actual hold step less the hold step measured after sampling $V = 0$. A change in hold step has two components: the first is a function of input voltage, the second is a function of the rise time of the S/H voltage. Note that rise time of S/H voltage $dV_{(S/H)}/dt$ also effects ZERO-SCALE ERROR.

Charge Transfer (Q_t) — The amount of charge transferred to the holding capacitor due to the action of the switch. Charge is transferred to C_H when the circuit is switched to the hold mode. Charge transfer causes a change in output voltage V_{ZS} as defined by the equation:

$$V_{ZS}(V) = \frac{Q_t(pC)}{C_H(pF)}$$

Note that for $Q_t = 5pC$ and $C_H = 5000pF$ offset error = 1mV. The SMP-10/11/81 has been factory nulled for $C_H = 5000pF$. For other values of C_H the zero-scale shift can be calculated from the equation:

$$\Delta V_{ZS}(V) = \frac{Q_t}{C_H} - 1mV$$

Droop Rate (dV_{CH}/dt) — Droop rate dV_{CH}/dt is the rate of change of output voltage while the circuit is in the hold mode. dV_{CH}/dt is a direct function of droop current I_{DR} :

$$\frac{dV_{CH}}{dt} = \frac{I_{DR}}{C_H}$$

where dV_{CH}/dt is expressed in $\mu V/ms$, I_{DR} in nanoamperes and C_H in microfarads (see timing diagram).

Feedthrough Attenuation Ratio (F_A) — Feedthrough attenuation is a measurement of the off-isolation of the analog switch (specified in dB). The parameter is a direct function of feedthrough capacitance.

Full Power Bandwidth (F_p) — The maximum frequency at which rated output voltage E_p can

be supplied without significant distortion. Full power bandwidth F_p is related to slew rate SR by the following equation:

$$F_p = \frac{SR}{2\pi E_p}$$

Using this equation F_p of 160kHz can be computed. This is applicable only for pulsed conditions. Power dissipation limits F_p to 100kHz for C.W. operation.

Gain Error — Voltage difference between input and output voltage measured over a specified voltage range, assuming the ideal gain is unity.

Hold Capacitor Charging Current (I_{CH}) — The current I_{CH} which charges, or discharges, the hold capacitor C_H while the circuit is in the sample mode.

Hold Mode Settling Time (t_{HM}) — The time for all output transients to settle within a specified error band. Measured from the inception of the hold command (see timing diagram).

Hold Step (V_{HS}) — Magnitude of step caused in the output voltage by switching the circuit from sample mode to hold mode. Hold step is sometimes called pedestal error, or sample to hold offset (see timing diagram).

Input Bias Current (I_B) — Input terminal current with input voltage held at zero volts.

Input Resistance (R_{IN}) — AC impedance measured as a ratio of input voltage V_{IN} to input current I_{IN} .

Leakage (Droop) Current (I_{DR}) — The current which flows out of holding capacitor C_H while the circuit is operating in the hold mode. In general droop current I_{DR} is defined positive when its direction is into the C_H pin. This parameter is sometimes called drift current.

Linearity Error — The maximum deviation from an ideal straight line drawn between the output voltage when $V_{IN} = 0$ and the output voltage when $V_{IN} =$ maximum analog voltage, expressed as a percentage of the maximum analog voltage.

Output Resistance (R_o) — An AC change in output voltage as a result of an AC change in load current.

SAMPLE-AND-HOLD AMPLIFIERS

Power Supply Rejection Ratio (PSRR) — The change in output voltage for a change in power supply voltage when the circuit is in the sample mode. The best power supply rejection ratio PSRR is obtained with the power supply voltage changing at a very low rate (DC). For essentially DC conditions PSRR for the hold mode of operation is essentially the same as the PSRR for the sample mode. PSRR is degraded as the frequency of the disturbance increases.

Sample Hold Current Ratio (I_{CH}/I_{DH}) — The ratio of the peak charging current available to the droop current.

Signal Transfer Nonlinearity — The total input to output, hold mode error caused by gain nonlinearity, feedthrough, thermal transient, charge transfer and droop rate. These error terms cannot be corrected by offset and gain adjustments.

Slew Rate (SR) — The maximum possible rate of change of the output voltage when supplying the rated output. For a sample-and-hold circuit, slew rate must be defined with a specified value of holding capacitor C_H . Slew rate can either be measured by operating the circuit in the sample mode and applying a step function to the input,

or by applying an input voltage which differs from the output voltage, with the circuit in the hold mode, then switching to the sample mode and observing the rate of change of the output voltage.

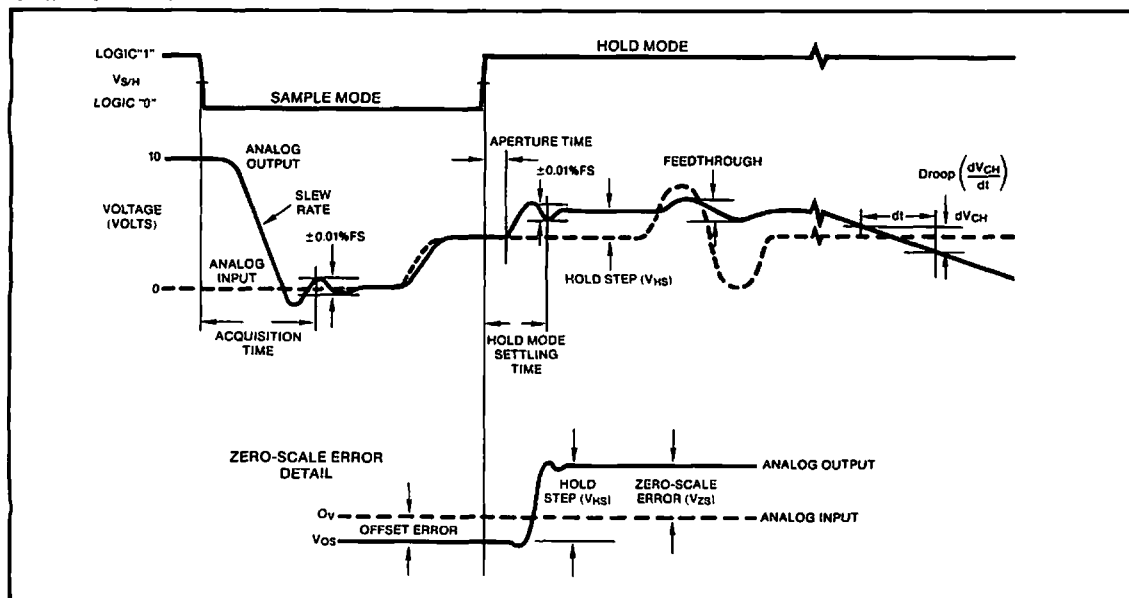
Total Error — The algebraic sum of the following factors:

- i. ZERO-SCALE ERROR
- ii. Gain Error
- iii. Hold Step Change versus $\frac{dV(S/H)}{dt}$
- iv. Hold Step Change versus V_{IN}

Voltage Gain (A_v) — The ratio of the output voltage to the input voltage with the circuit operating in the sample mode.

Zero-Scale Error (V_{zs}) — The magnitude of the output voltage when the circuit is switched from sample to hold mode while holding the input at zero volts. ZERO-SCALE ERROR V_{zs} is the algebraic sum of the offset voltage and the charge transfer hold step voltage (see timing diagram). V_{zs} can be adjusted to zero (see ZERO-SCALE ERROR null adjustment).

TIMING DIAGRAM





SAMPLE-AND-HOLD AMPLIFIERS

Precision Monolithics Inc.

SAMPLE-AND-HOLD AMPLIFIER SELECTION GUIDE

Product	V_{ZS} mV	I_B nA	I_{DR} nA	Droop Rate mV/ms	A_V V/V	PSRR dB
SMP10	1.5	65	0.10	0.020	0.99963	82
SMP11	1.5	65	1.00	0.200	0.99963	82
SMP81	1.6	225	10.00	2.00	0.99960	80
PKD-01	4	150	—	0.07	18,000	86



Precision Monolithics Inc.

SMP-10/SMP-11

LOW-DROOP-RATE/ACCURATE
SAMPLE-AND-HOLD AMPLIFIERS

FEATURES

SMP-10

- Low Droop Rate 5.0 $\mu\text{V/ms}$
- Linearity Error 0.005%
- High Sample/Hold Current Ratio 2×10^9

SMP-11

- Low Droop Rate over Temperature 2400 $\mu\text{V/ms}$
- High Sample/Hold Current Ratio 1.7×10^8

BOTH SMP-10 AND SMP-11

- Fast Acquisition Time, 10V Step to 0.1% 3.5 μs
- High Slew Rate 10V/ μs
- Low Aperture Time 50ns
- Trimmed for Minimum Zero-Scale Error 0.45mV
- Feedthrough Attenuation Ratio 96dB
- Low Power Dissipation 160mW
- DTL, TTL & CMOS Compatible Logic Input
- HA-2420, HA-2425, SHM-IC-1, and AD583 Socket Compatible

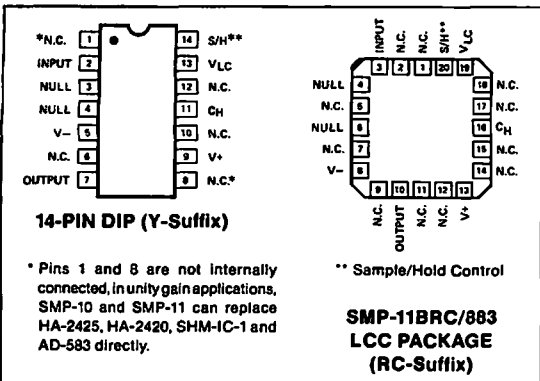
ORDERING INFORMATION†

$T_A = +25^\circ\text{C}$		PACKAGE		OPERATING TEMPERATURE RANGE
V_{ZS} (mV)	DROOP RATE IN $\mu\text{V/ms}$	14-PIN DIP HERMETIC	LCC	
1.5	20	SMP10AY*		MIL
3.0	50	SMP10BY*		MIL
1.5	20	SMP10EY		COM
3.0	50	SMP10FY		COM
1.5	200	SMP11AY*		MIL
3.0	500	SMP11BY*	SMP11BRC/883	MIL
1.5	200	SMP11EY		COM
3.0	500	SMP11FY		COM
7.0	900	SMP11GY		COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

PIN CONNECTIONS



GENERAL DESCRIPTION

The SMP-10/11 are precision sample-and-hold amplifiers that provide the high accuracy, the low droop rate and the fast acquisition time required in data acquisition and signal processing systems. Both devices are essentially noninverting unity gain circuits consisting of two very high input impedance buffer amplifiers connected together by a diode bridge switch.

HIGH ACCURACY AND LOW DROOP RATE

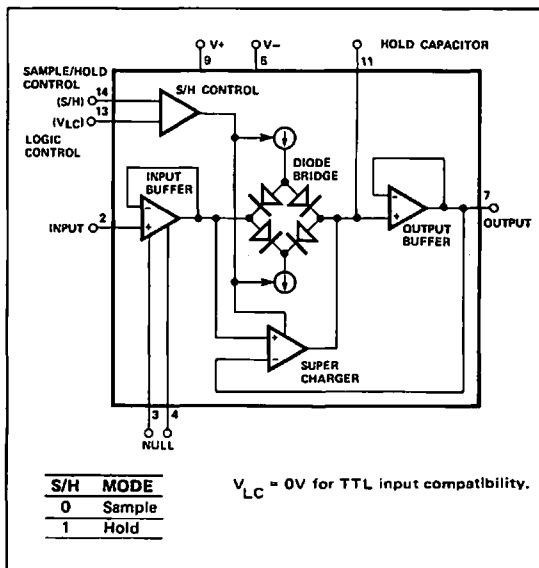
The high input impedance and the low droop rates of the SMP-10 and the SMP-11 are achieved by using bipolar Darlington circuits and an ion implant process that creates "super beta" transistors.

The output buffer's input stage converts to a super beta Darlington configuration during the hold mode, which results in a very low droop rate with no penalty in acquisition time. The use of bipolar transistors achieves a low change in droop rate over the operating temperature range.

FAST ACQUISITION

A unique super charger provides up to 50mA of charging current to the hold capacitor, which results in smooth, fast charging with minimum noise. As the hold capacitor voltage nears its final value, the low current diode bridge controls the final settling time. This unique combination of linear functions in a monolithic circuit enables the system designer to achieve superior performance.

FUNCTIONAL DIAGRAM



Manufactured under the following patents: 4,109,215 and 4,142,117.

SAMPLE-AND-HOLD AMPLIFIERS

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**ABSOLUTE MAXIMUM RATINGS** (Note)

Supply Voltage (V_+ minus V_-) 36V
 Power Dissipation 500mW
 Derate Above 100°C 10mW/°C
 Input Voltage Equal to Supply Voltage
 Logic and Logic Reference Voltage Equal to Supply Voltage
 Output Short-Circuit Duration Indefinite
 Hold Capacitor Short-Circuit Duration 60 sec
 Storage Temperature Range -65°C to +150°C

Lead Temperature (Soldering, 60 sec) 300°C
 Operating Temperature Range

SMP-10AY, BY -55°C to +125°C

SMP-10EY, FY 0°C to +70°C

SMP-11AY, BY, BRC -55°C to +125°C

SMP-11EY, FY, GY 0°C to +70°C

DICE Junction Temperature (T_J) -65°C to +150°C

NOTE: Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10A/E SMP-11A/E			SMP-10B/F SMP-11B/F			SMP-11G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero-Scale Error (Hold Mode)	V_{ZS}	$V_{IN} = 0$ $V_{S/H} = 3.5V$, (Note 2)	—	0.45	1.5	—	0.60	3.0	—	1.5	7.0	mV
Input Bias Current	I_B	$V_{IN} = 0$	—	35	65	—	55	90	—	90	160	nA
Leakage (Droop) Current	I_{DR}	SMP-10 SMP-11	—	—	0.10 1.00	—	—	0.25 2.50	—	—	— 4.5	nA
Droop Rate	dV_{CH}/dt	SMP-10 SMP-11	—	5 60	20 200	—	5 70	50 500	—	— 80	— 900	$\mu V/ms$
Input Resistance	R_{IN}	(Note 1)	2.0	3.0	—	1.4	2.5	—	—	2.0	—	G Ω
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$	0.99963	0.99983	—	0.99953	0.99978	—	0.99940	0.99975	—	V/V
Acquisition Time	t_{aq}	10V step to within 10mV of final value (0.1%)	—	3.5	—	—	3.5	—	—	3.5	—	μs
		10V step to within 1.0mV of final value (0.01%)	—	5.0	—	—	5.0	—	—	5.0	—	μs
Aperture Time	t_{sp}		—	50	—	—	50	—	—	50	—	ns
Hold Mode Settling Time	t_{hm}	Settling to 1mV of final value.	SMP-10	7	—	—	7	—	—	7	—	μs
			SMP-11	1.5	—	—	1.5	—	—	1.5	—	μs
Charge Transfer	Q_t	$V_{IN} = 0$ $V_{S/H} = 3.5V$	—	5	—	—	5	—	—	5	—	pC
Slew Rate	SR	$V_{IN} = \pm 10V$ $R_L = 2.5k\Omega$	—	10	—	—	10	—	—	10	—	V/ μs
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3V$	30	50	—	20	50	—	—	50	—	mA
Sample/Hold Current Ratio	I_{CH}/I_{DR}		SMP-10	3×10^8	2×10^9	—	8×10^7	8×10^8	—	—	—	mA/mA
			SMP-11	—	1.7×10^8	—	—	1.5×10^8	—	1.5×10^8	—	
Feedthrough Attenuation Ratio	F_A	Input = 20V _{p-p} 1kHz $R_L = 5k\Omega$, (Note 1)	86	96	—	80	90	—	—	90	—	dB
Full Power Bandwidth	F_P	$\pm 10V_{p-p}$ (Dissipation Limited)	—	100	—	—	100	—	—	100	—	kHz
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	± 11	± 11.5	—	± 10.5	± 11.5	—	± 10.5	± 11.5	—	V
Output Resistance	R_O		—	0.15	—	—	0.15	—	—	0.15	—	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	82	92	—	77	92	—	72	92	—	dB
Power Consumption (DC)	P_D	Sample Mode $V_{IN} = 0$	—	160	180	—	170	210	—	180	240	mW

NOTES:

- Guaranteed by design.
- Measured 500 μs after hold command.



ELECTRICAL CHARACTERISTICS — SMP-10 ONLY at $V_S = \pm 15V$, $C_H = 0.005\mu F$, $V_{LC} = 0V$, $T_A = 25^\circ C$, device fully warmed-up, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10A/E			SMP-10B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Hold Step	V_{HS}	$V_{IN} = 0$	-1.0	+1.5	+4.0	-3.0	+1.5	+6.0	mV
Linearity Error	NL	$V_{IN} = \pm 10V$, $R_L = 5k\Omega$	—	0.005	—	—	0.007	—	% of 10V
Output Noise	$E_{N(RMS)}$	Wideband Noise 100Hz to 100kHz Sample Mode	—	40	—	—	50	—	μV_{RMS}

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $0^\circ C \leq T_A \leq +70^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10E SMP-11E			SMP-10F SMP-11F			SMP-11G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$, (Note 1)	—	0.75	2.0	—	1.0	4.0	—	2.7	10	mV
Input Bias Current	I_B	$V_{IN} = 0V$	—	50	90	—	80	140	—	120	250	nA
Leakage (Droop) Current	I_{DR}	SMP-10	—	0.05	0.25	—	0.060	0.65	—	—	—	nA
		SMP-11	—	0.5	1.8	—	0.6	2.8	—	0.7	5	
Droop Rate	dV_{CH}/dt	SMP-10	—	10	50	—	16	130	—	—	—	$\mu V/ms$
		SMP-11	—	100	360	—	120	560	—	140	1000	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$	0.99955	0.99976	—	0.99950	0.99972	—	0.99930	0.99970	—	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	80	90	—	75	80	—	70	90	—	dB
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$	—	-1	-2	—	-1	-3	—	-1	-4	μA
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$	—	-5	-15	—	-5	-15	—	-5	-15	μA
		Hold Mode $V_{S/H} = 5.0V$	—	0.2	—	—	0.2	—	—	0.2	—	nA
Differential Logic Threshold	V_{TH}		0.8	1.3	2.0	0.8	1.3	2.0	0.8	1.3	2.0	V

NOTES:

1. Measured 500 μs after hold command.

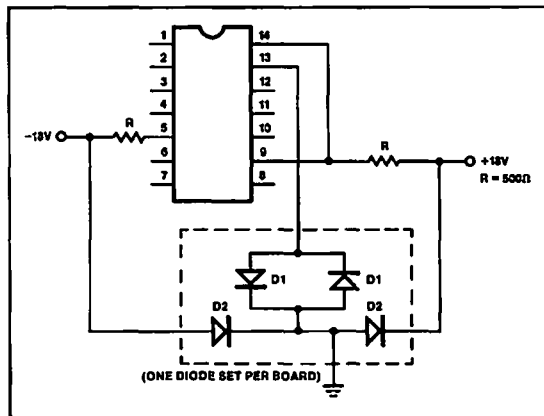


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10A SMP-11A			SMP-10B SMP-11B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$, (Note 1)	—	1.25	3.0	—	1.60	5.5	mV
Input Bias Current	I_B	$V_{IN} = 0V$	—	90	180	—	160	280	nA
Leakage (Droop) Current	I_{DR}	$T_A = -55^\circ C$	—	0.050	0.50	—	0.080	1.22	nA
		$T_A = +125^\circ C$	—	12	20	—	16	25	
		$T_A = \text{Full Range}$	—	12	20	—	16	25	
Droop Rate	dV_{CH}/dt	$T_A = -55^\circ C$	—	10	100	—	16	250	$\mu V/ms$
		$T_A = +125^\circ C$	—	2400	4000	—	3200	5000	
		$T_A = \text{Full Range}$	—	2400	4000	—	3200	5000	
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$	0.99950	0.99972	—	0.99940	0.99968	—	V/V
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	78	88	—	72	90	—	dB
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$	—	-1	-3	—	-1	-5	μA
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$	—	-5	-15	—	-5	-15	μA
		Hold Mode $V_{S/H} = 5.0V$	—	0.2	—	—	0.2	—	nA
Differential Logic Threshold	V_{TH}		0.6	1.3	2.0	0.6	1.3	2.0	V

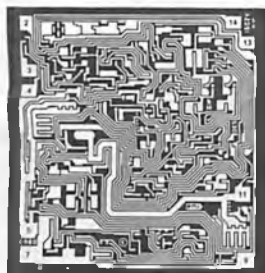
NOTES:

1. Measured 500 μs after hold command.

BURN-IN CIRCUIT



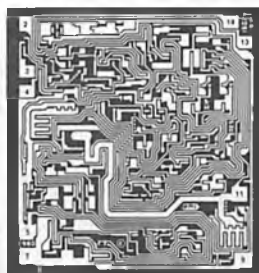
DICE CHARACTERISTICS



SMP-10

2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY (SUBSTRATE)
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR (C_H)
13. LOGIC THRESHOLD CONTROL (V_{LC})
14. SAMPLE/HOLD COMMAND

DIE SIZE 0.088 × 0.083 inch, 7304 sq. mils
(2.235 × 2.108 mm, 4.711 sq. mm)



SMP-11

2. INPUT
3. NULL
4. NULL
5. NEGATIVE SUPPLY (SUBSTRATE)
7. OUTPUT
9. POSITIVE SUPPLY
11. HOLD CAPACITOR (C_H)
13. LOGIC THRESHOLD CONTROL (V_{LC})
14. SAMPLE/HOLD COMMAND

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-10N SMP-11N LIMIT	SMP-10G SMP-11G LIMIT	UNITS
Zero-Scale Error	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$ Hold Mode, (Note 2)	1.5	3.0	mV MAX
Input Bias Current	I_B	$V_{IN} = 0V$	60	90	nA MAX
Leakage (Droop) Current	I_{DR}	SMP-10 SMP-11	0.10 1	0.25 2.5	nA MAX
Droop Rate	dV_{CH}/dt	SMP-10 SMP-11	20 200	50 500	$\mu V/ms$ MAX
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$ or $V_{IN} = \pm 5V$	0.99963	0.99953	V/V MIN
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3V$	30	20	mA MIN
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	± 11	± 10.5	V MIN
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	82	77	dB MIN
Power Consumption	P_D	Sample Mode $V_{IN} = 0$	180	210	mW MAX
Logic Control Input Current	I_{LC}	$V_{LC} = 0V$	-2	-3	μA MAX
Logic Input	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$	-15	-15	μA MAX
		Hold Mode $V_{S/H} = 5V$	0	0	nA MAX
Differential Logic Threshold	V_{TH}	$V_{LC} = 0$	2.0	2.0	V MAX
			0.8	0.8	V MIN

NOTES:

1. Measured 500 μs after hold command.

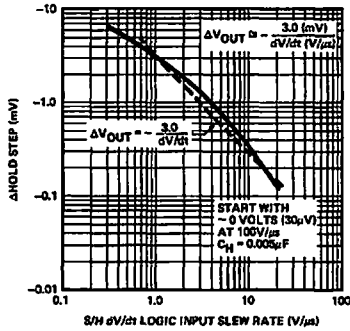
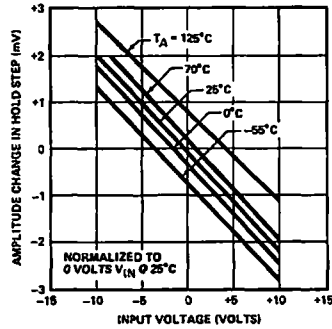
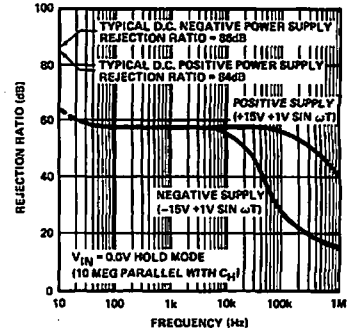
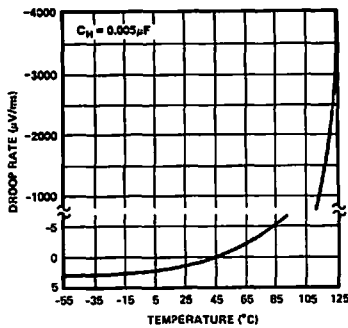
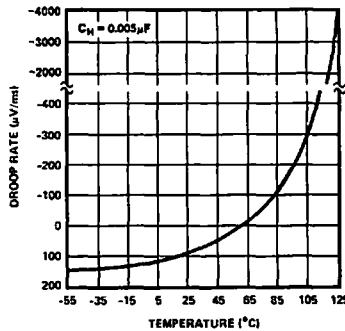
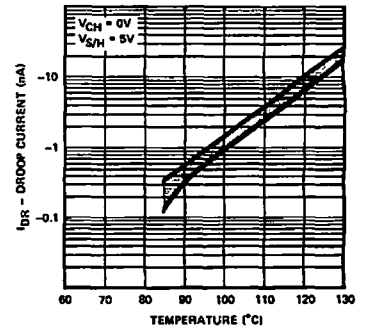
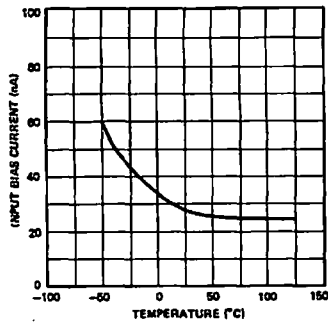
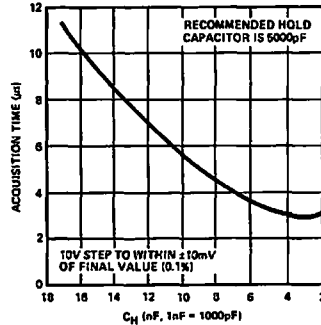
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $T_A = 25^\circ C$, unless otherwise noted.

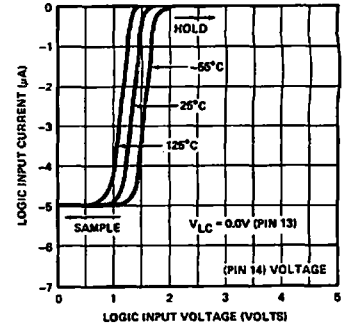
PARAMETER	SYMBOL	CONDITIONS	SMP-10N SMP-11N TYPICAL	SMP-10G SMP-11G TYPICAL	UNITS
Acquisition Time	t_{AQ}	10V step to 0.1% of final value	3.5	3.5	μs
Aperture Time	t_{AP}		50	50	ns
Charge Transfer	Q_t	$V_{IN} = 0$, $V_{S/H} = 3.5V$	5	5	pC
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L = 2.5k\Omega$	10	10	V/ μs



TYPICAL PERFORMANCE CHARACTERISTICS

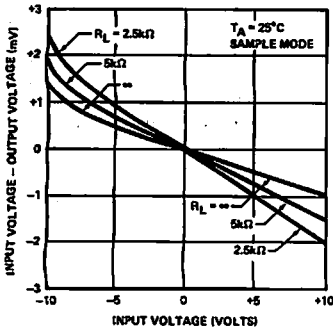
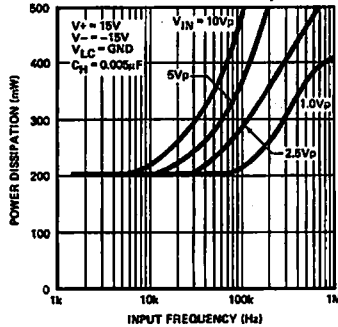
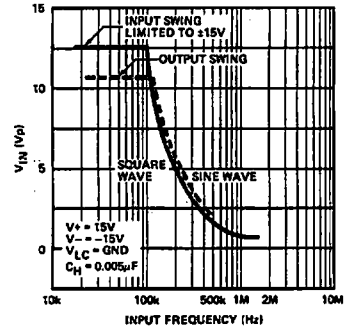
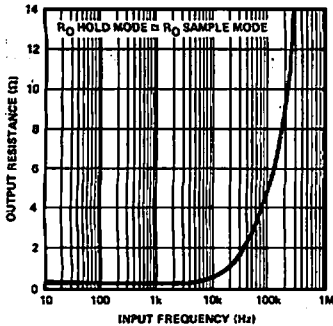
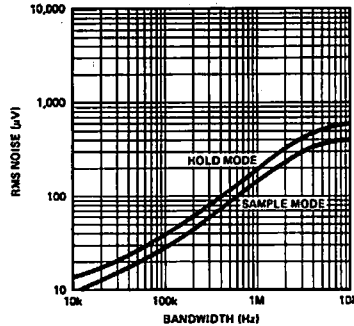
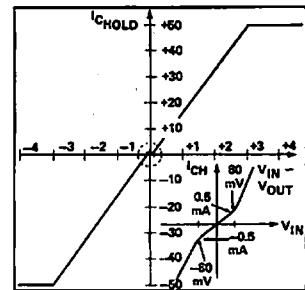
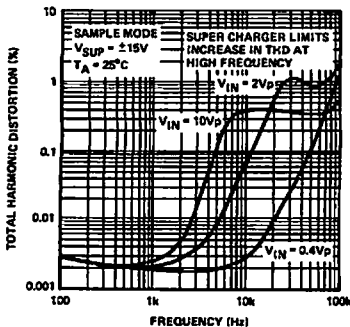
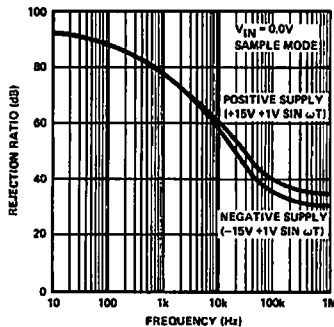
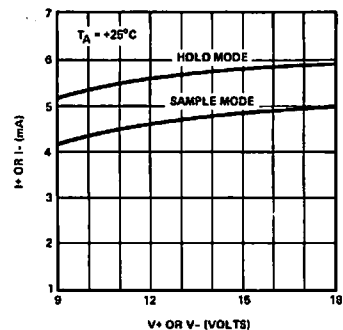
CHANGE IN HOLD STEP
vs $S/H \frac{dV}{dt}$ AMPLITUDE CHANGE IN
HOLD STEP vs
INPUT VOLTAGEHOLD MODE
POWER SUPPLY REJECTIONSMP-10
DROOP RATE
vs TEMPERATURESMP-11
DROOP RATE
vs TEMPERATUREDROOP CURRENT
vs TEMPERATUREINPUT BIAS CURRENT
vs TEMPERATUREACQUISITION TIME
vs HOLD CAPACITOR

LOGIC INPUT CURRENT

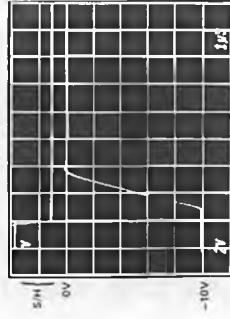
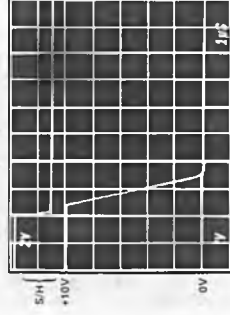
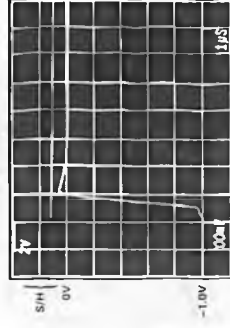
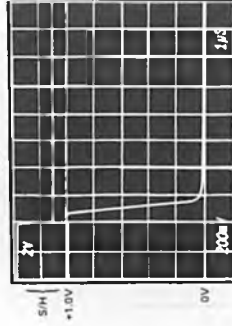
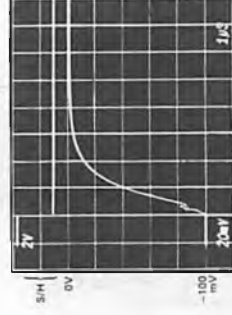
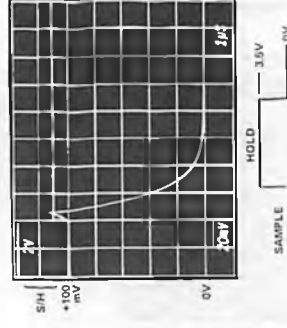


TYPICAL PERFORMANCE CHARACTERISTICS

GAIN ERROR


POWER DISSIPATION vs
INPUT FREQUENCY = $V_p \sin \omega t$

MAXIMUM INPUT SIGNAL
AMPLITUDE vs FREQUENCY

OUTPUT RESISTANCE
vs FREQUENCY

OUTPUT WIDEBAND NOISE
vs BANDWIDTH (0.1Hz TO
FREQUENCY INDICATED)

HOLD CAPACITOR
CHARGING CURRENT vs
INPUT OUTPUT VOLTAGE

TOTAL HARMONIC
DISTORTION vs FREQUENCY

SAMPLE MODE
POWER SUPPLY REJECTION

POWER SUPPLY CURRENT
vs POWER SUPPLY VOLTAGE


SMP-10/SMP-11 ACQUISITION TIMES

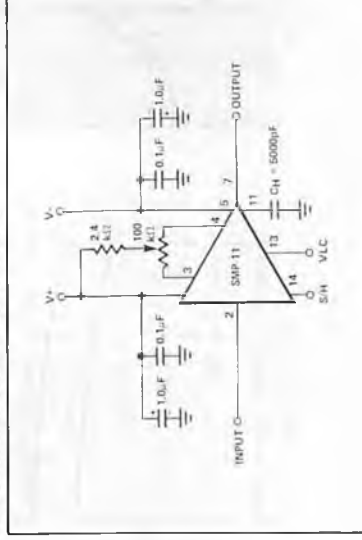
ACQUISITION TIME
-10V to 0VACQUISITION TIME
+10V to 0VACQUISITION TIME
-1.0V to 0VACQUISITION TIME
+1.0V to 0VACQUISITION TIME
-100mV to 0VACQUISITION TIME
+100mV to 0V

APPLICATIONS INFORMATION

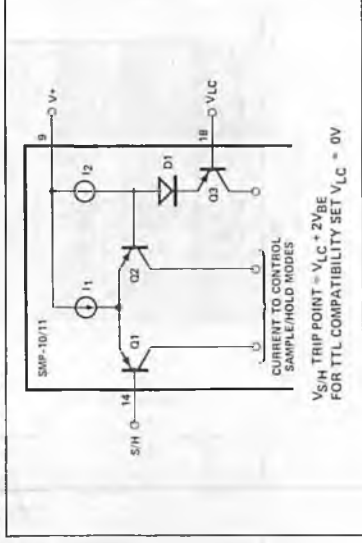
During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero.

As shown in the Figure, the sample/hold mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high-speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground V_{LC} (Pin 13). For CMOS, HTL and HN1L interface, the appropriate

ZERO-SCALE NULL ADJUSTMENT



LOGIC CONTROL

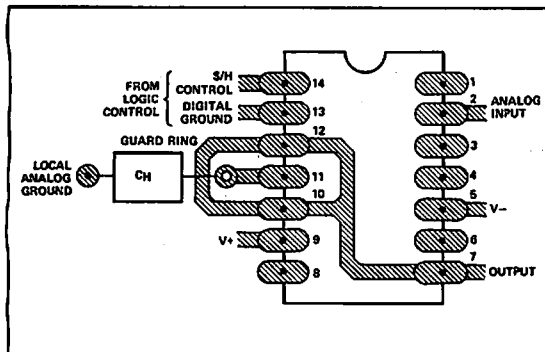


V_{SH} TRIP POINT = $V_{LC} + 2V_{BE}$
FOR TTL COMPATIBILITY SET $V_{LC} = 0V$

threshold voltage, allowing for 2 diode drops for D1 and V_{BE} of Q3, should be applied to V_{LC} .

For proper operation, the V_{LC} (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample-and-hold control voltage (S/H) must always be at least 2.8V above the negative supply.



GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path.

HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample-and-hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The devices have been internally trimmed for $C_H = 5000\text{pF}$. Other values of C_H will cause a zero-scale shift, which can be calculated from the following equation:

$$\Delta V_{ZS}(\text{mV}) = \frac{5 (\text{pC}) \times 10^3}{C_H (\text{pF})} - 1$$

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.



SMP-81

TELECOMMUNICATIONS SAMPLE-AND-HOLD AMPLIFIER

Precision Monolithics Inc.

FEATURES

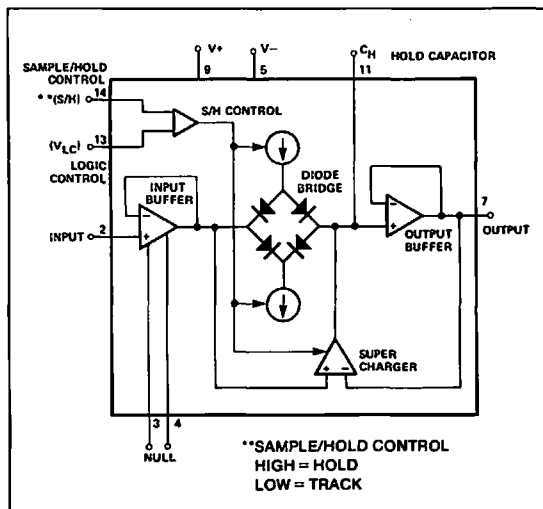
- Meets System Performance Requirements in Multi-Channel CODECs
- Trimmed for Minimum Zero-Scale Error 0.6mV
- Low Droop Rate Over Temperature 1600 μ V/ms
- Low Aperture Time 50ns
- Fast Acquisition Time 10V Step to 0.1% 3.5 μ s
- High Slew Rate 10V/ μ s
- High Sample-Current to Hold-Current Ratio .. 1.7×10^8
- DTL, TTL & CMOS Compatible Logic Input
- HA-2425, DATEL SHM-IC-1, and AD-583 Socket Compatible*
- Low Power Dissipation
- Low Cost
- Feedthrough Attenuation Ratio 96dB

ORDERING INFORMATION†

V_{ZS} (mV)	HERMETIC 14-PIN DIP	OPERATING TEMPERATURE RANGE
1.6	SMP-81EY	IND
3.5	SMP-81FY	IND

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION

The SMP-81 precision sample-and-hold amplifier provides the high accuracy, low droop rate and fast acquisition ideally required for PCM encoders. The SMP-81 is a non-inverting unity gain circuit consisting of two buffer amplifiers of very high input impedance connected by a diode bridge switch.

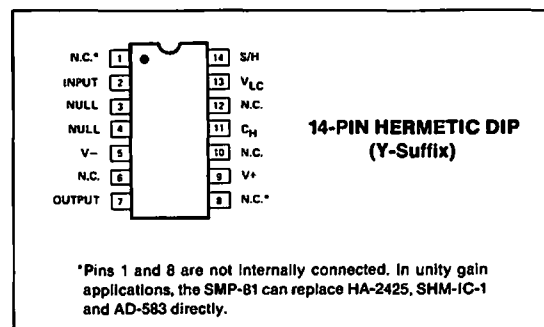
HIGH ACCURACY AND LOW DROOP RATE

The high input impedance and low droop rate of the SMP-81 are achieved by PMI's ion implant super beta process. The high input impedance permits high source impedance applications without degrading accuracy, and low droop rate. Other features of the SMP-81 include high accuracy, 0.6mV of combined offset voltage and step transfer error, and very low feedthrough. A diode bridge switch design allows minimum charge transfer step. On-chip zener-zap trimming eliminates nulling for most applications.

FAST ACQUISITION

A unique super charger or transconductance amplifier provides up to 50mA charging current to the hold capacitor. As a result, smooth charging of the hold capacitor is achieved with minimum noise. The super charger, in conjunction with the high slewing rate input and output buffer amplifiers, permits fast acquisition operation. The adjustable logic input threshold makes the SMP-81 compatible to all logic families.

PIN CONNECTIONS



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (V+ minus V-) 36V
 Power Dissipation 500mW
 Derate Above 100° C 10mW/° C
 Input Voltage Equal to Supply Voltage
 Logic and Logic Control Voltage .. Equal to Supply Voltage

Output Short-Circuit Duration Indefinite
 Hold Capacitor Short-Circuit Duration 60sec
 Operating Temperature Range -25° C to +85° C
 Storage Temperature Range -65° C to +150° C
 Lead Temperature (Soldering, 60 sec) 300° C

ELECTRICAL CHARACTERISTICS at $V_S \pm 15V$, $C_H = 0.005\mu F$, V_{LC} connected to ground, $-25^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	SMP-81E			SMP-81F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Zero-Scale Error (Hold Mode)	V_{ZS}	$V_{IN} = 0$, $V_{S/H} = 3.5V$ (500 μ sec after Hold Command)	—	0.6	1.6	—	0.9	3.5	mV
Input Bias Current	I_B	$V_{IN} = 0$	—	105	225	—	120	450	nA
Leakage (Droop) Current	I_{DR}		—	0.5	10	—	0.5	20	nA
Droop Rate	dV_{CH}/dt		—	1600	2000	—	2000	4000	$\mu V/ms$
Input Resistance	R_{IN}	(See Note)	0.6	2.0	—	0.3	1.4	—	G Ω
Voltage Gain	A_V	Sample Mode $V_{IN} = \pm 10V$, $R_L = 5k\Omega$ or $V_{IN} = \pm 5V$, $R_L = 2.5k\Omega$	0.99960	0.99960	—	0.99955	0.99978	—	V/V
Acquisition Time	t_{aq}	10V step to within 10mV of final value (0.1%)	—	3.5	—	—	3.5	—	μs
Aperture Time	t_{ap}		—	50	—	—	50	—	nsec
Charge Transfer	Q_t	$V_{IN} = 0$, $V_{S/H} = 3.5V$	—	5	—	—	5	—	pC
Slew Rate	SR	$V_{IN} = \pm 10V$, $R_L = 2.5k\Omega$	—	10	—	—	10	—	V/ μs
Hold Capacitor Charging Current	I_{CH}	$V_{IN} - V_{OUT} \geq \pm 3$ volts	30	50	—	20	50	—	mA
Feedthrough Attenuation Ratio	F_A	Input -20V _{p-p} 1kHz, $R_L = 5K\Omega$ (See Note)	86	96	—	80	90	—	dB
Full Power Bandwidth	F_P	$\pm 10V_{p-p}$ (Dissipation Limited)	—	100	—	—	100	—	kHz
Input Voltage Range and/or Output Voltage Swing		$R_L = 2.5k\Omega$	± 10	± 11.5	—	± 10	± 11.5	—	V
Output Resistance	R_O		—	0.15	—	—	0.15	—	Ω
Power Supply Rejection Ratio	PSRR	Sample Mode $V_S = \pm 9V$ to $\pm 18V$	80	90	—	75	90	—	dB
Power Consumption (DC)	P_D	Sample Mode $V_{IN} = 0$	—	160	180	—	170	210	mW
Logic Control Input Current	I_{LC}		-6	-3	—	-9	-3	—	μA
Logic Input Current	$I_{S/H}$	Sample Mode $V_{S/H} = 0.6V$ Hold Mode $V_{S/H} = 5.0V$	—	-15	-45	—	-15	-45	μA
			—	0.6	—	—	0.6	—	nA
Differential Logic Threshold	V_{TH}		0.8	1.3	2.0	0.8	1.3	2.0	V
Hold Mode Settling Time	t_{HM}	5V step to within 1mV of final value	—	1.5	—	—	1.5	—	μs

NOTE: Guaranteed by design.

DICE

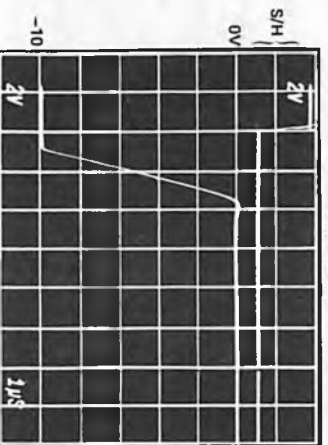
For applicable DICE information, see SMP-11 Data Sheet.



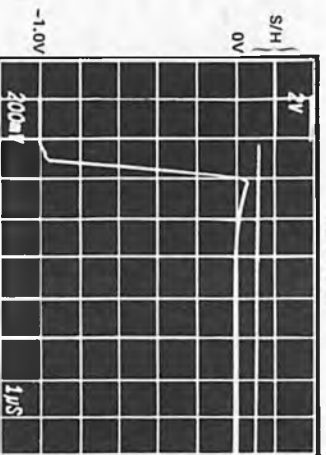
TYPICAL PERFORMANCE CHARACTERISTICS

SMP-81 ACQUISITION TIMES

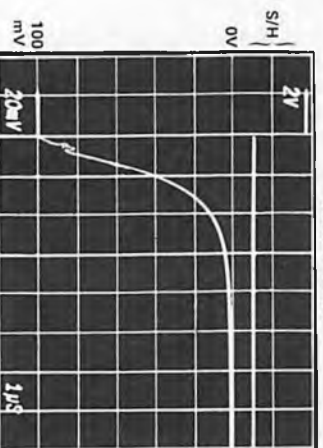
ACQUISITION TIME
- 10V TO 0V



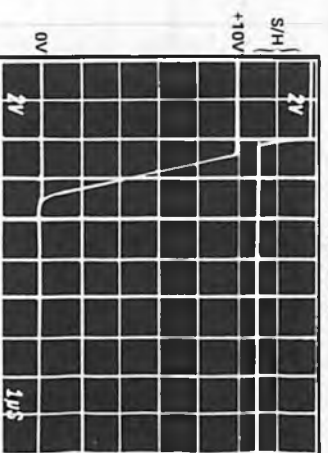
ACQUISITION TIME
- 1.0V TO 0V



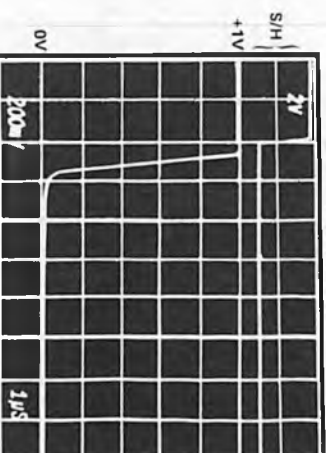
ACQUISITION TIME
- 100mV TO 0V



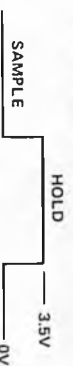
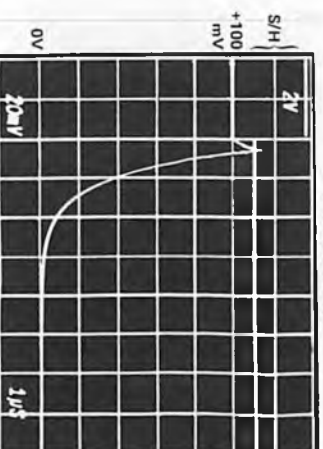
ACQUISITION TIME
+ 10V TO 0V



ACQUISITION TIME
+ 1.0V TO 0V

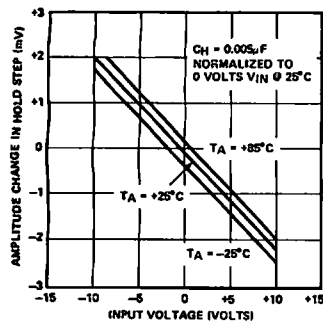


ACQUISITION TIME
+ 100mV TO 0V

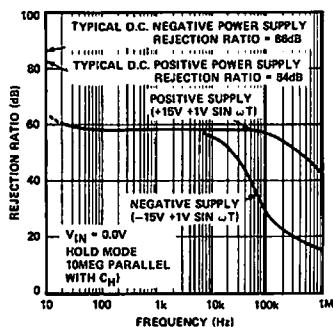


TYPICAL PERFORMANCE CHARACTERISTICS

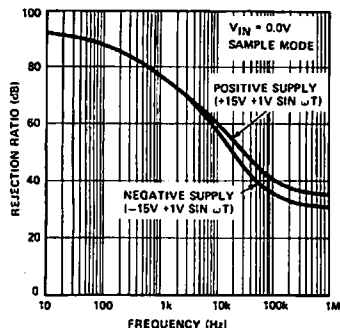
AMPLITUDE CHANGE IN HOLD STEP vs INPUT VOLTAGE



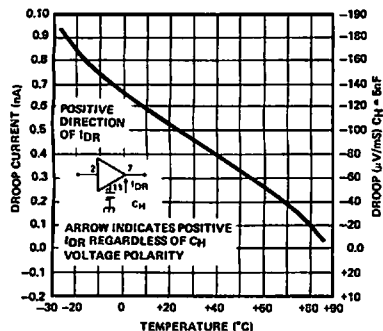
HOLD-MODE POWER SUPPLY REJECTION



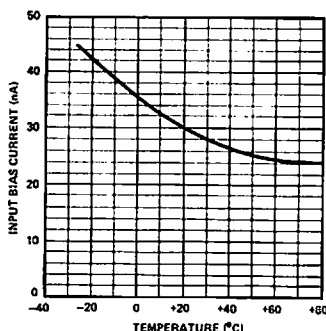
SAMPLE-MODE POWER SUPPLY REJECTION



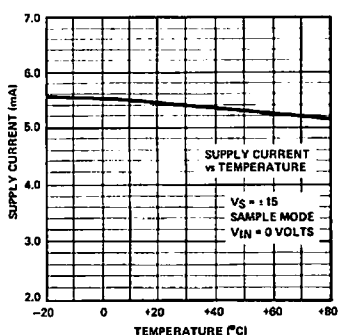
LEAKAGE (DROOP) CURRENT vs TEMPERATURE



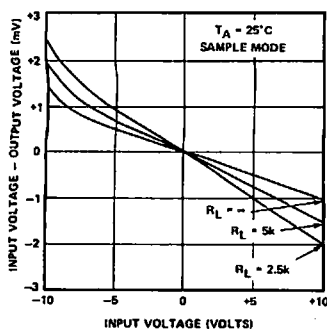
INPUT BIAS CURRENT vs TEMPERATURE



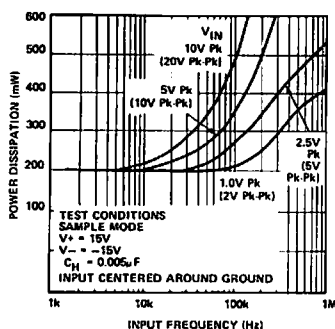
SAMPLE-MODE SUPPLY CURRENT vs TEMPERATURE



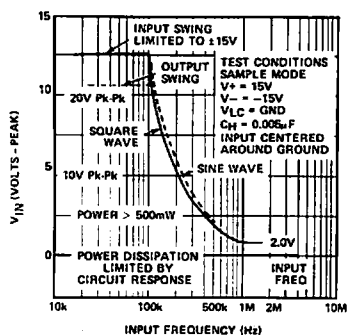
GAIN ERROR

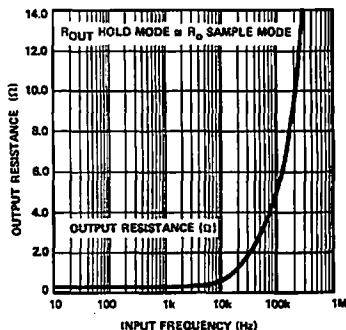
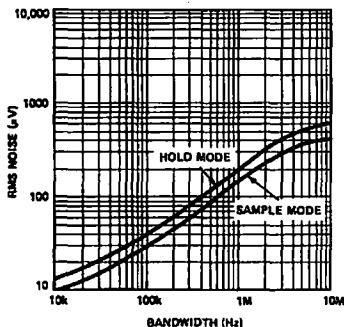
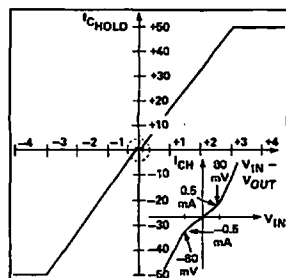
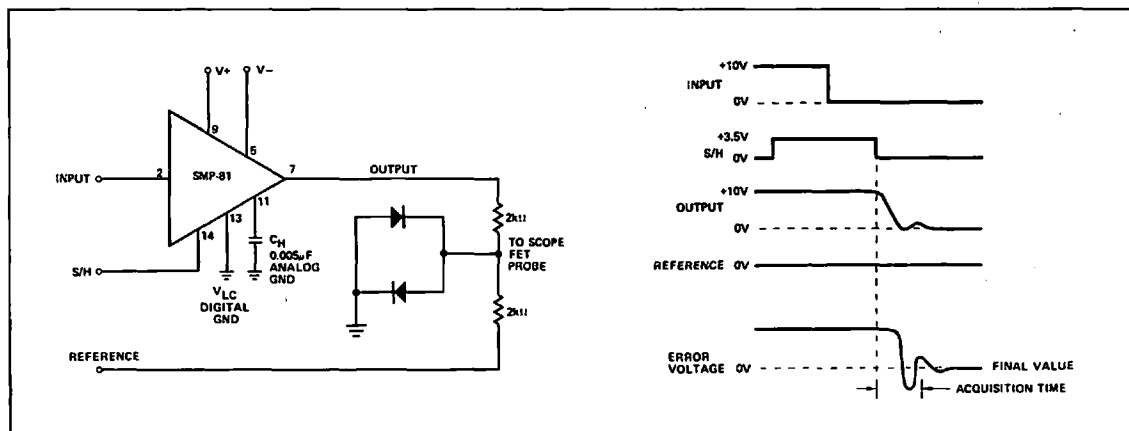


POWER DISSIPATION vs FREQUENCY INPUT = $V_p \sin \omega t$



MAXIMUM INPUT SIGNAL AMPLITUDE vs FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS
**OUTPUT RESISTANCE
vs FREQUENCY**

**OUTPUT WIDEBAND NOISE
vs BANDWIDTH (0.1Hz
TO FREQUENCY INDICATED)**

**HOLD CAPACITOR CHARGING
CURRENT vs
INPUT OUTPUT VOLTAGE**

ACQUISITION TIME TEST CIRCUIT

APPLICATIONS INFORMATION
HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) acts as a memory element and also as a compensating capacitor for the sample-and-hold amplifier. For stable operation, a minimum value of 2000pF is recommended, with no limit set for the maximum value. The SMP-81 is internally trimmed for $C_H = 5000\text{pF}$. Other values of C_H will cause a zero-scale shift, which can be calculated from the following equation:

$$\Delta V_{ZS} (\text{mV}) = \frac{5 (\text{pC}) \times 10^3}{C_H (\text{pF})} - 1$$

A C_H of 5000pF has been empirically determined to be an optimum value for 8-channel shared CODEC operation.

The hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, polystyrene capacitors are recommended, while teflon capacitors are recommended for higher temperature applications.

SMP-81 LOGIC CONTROL

The sample/hold mode control of the SMP-81 incorporates a unique logic input circuit, which enables direct interface to all popular logic families and provides maximum noise immunity. As shown in Figure 1, the mode control is accomplished by steering the current (I_1) through Q1 or Q2, thus providing high speed switching and a predictable logic threshold. For TTL and DTL interface, simply ground V_{LC} (pin 13). For CMOS, HTL and HN1L interface, the appropriate threshold voltage, allowing for 2 diode drops for D1 and V_{BE} of Q3, should be applied to V_{LC} .

SAMPLE/HOLD MODE INTERFACE CIRCUITRY

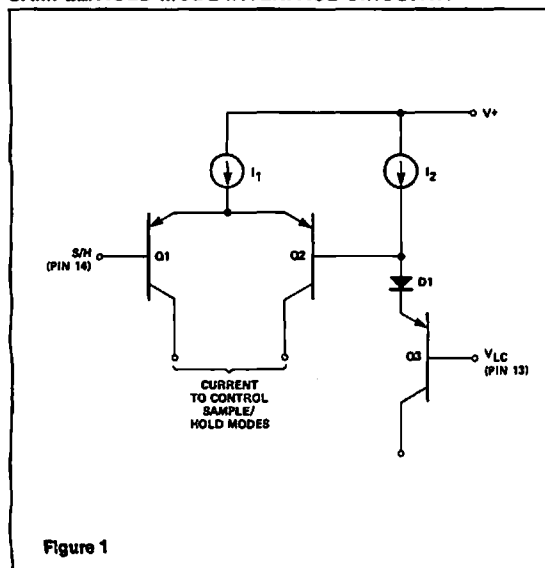


Figure 1

For proper operation, the V_{LC} (logic control) must always be at least 3.5V below the positive supply and 2.0V above the negative supply.

Sample-and-hold control voltage (S/H) must always be at least 2.8V above the negative supply.

ZERO-SCALE ERROR NULL ADJUSTMENT

During the null adjustment, the amplifier should be switched continuously between the "sample" and "hold" mode. The error should be adjusted to read zero when the unit is in the "hold" mode. In this way, both offset voltage errors and charge transfer errors are adjusted to zero. Figure 2 shows the recommended 10k Ω trim pot connected to $V+$ if user needs better V_{ZS} than 1.6mV.

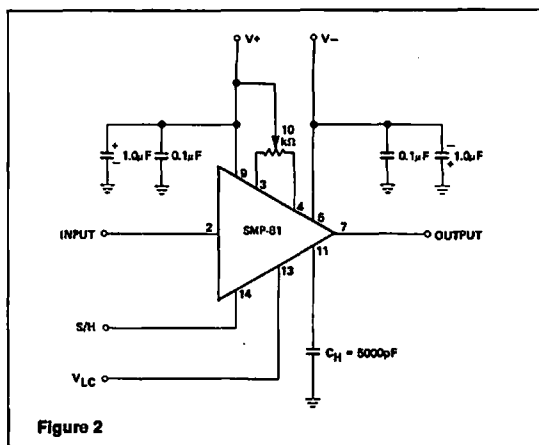


Figure 2

GUARDING AND GROUNDING LAYOUT

The use of a ground plane is strongly recommended to minimize ground path resistances. Separate analog and digital grounds should be used, and it is advisable to keep these two ground systems isolated until they are tied back to the common system ground. Digital currents should not flow back to the system ground through the analog ground path. A guard trace surrounding the hold capacitor node pin 11, minimizes PC board leakage problems, see Figure 3.

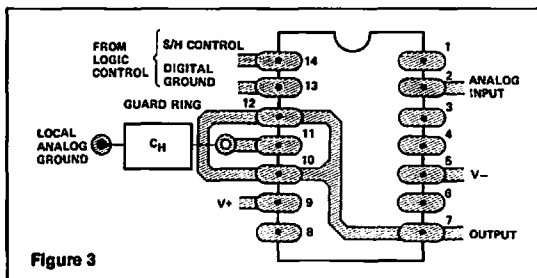
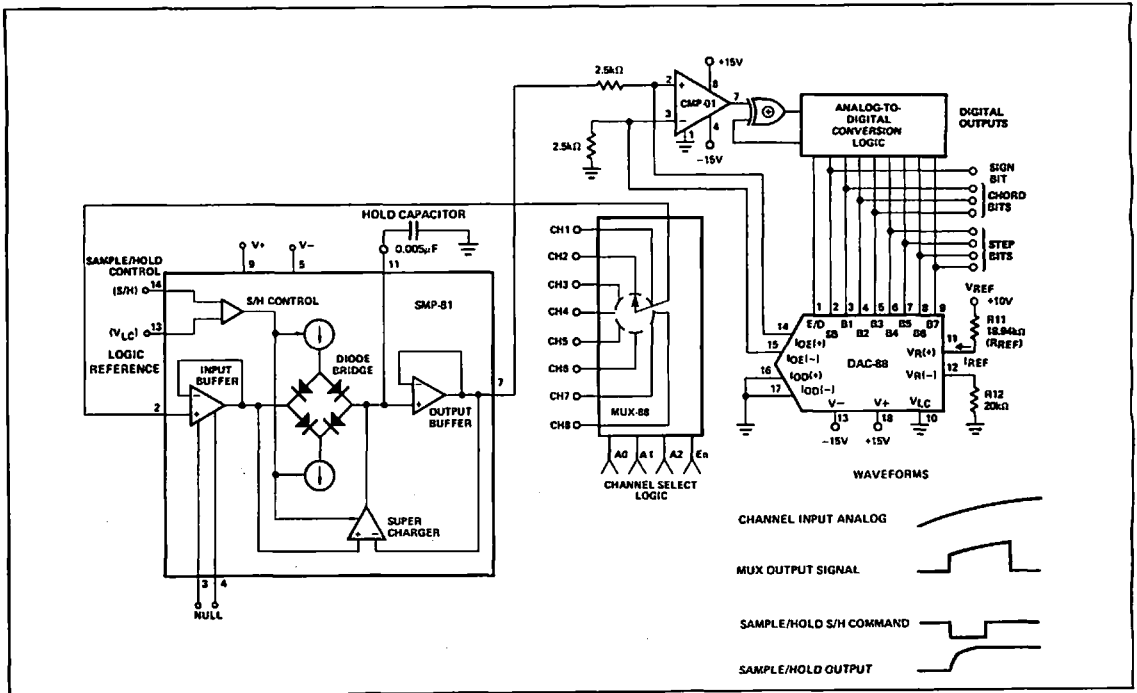


Figure 3



TYPICAL APPLICATION

EIGHT-CHANNEL SHARED CODEC PCM ENCODER





PKD-01

MONOLITHIC PEAK DETECTOR (WITH RESET-AND-HOLD MODE)

Precision Monolithics Inc.

FEATURES

- Monolithic Design for Reliability and Low Cost
- High Slew Rate 0.5V/ μ s
- Low Droop Rate
 - $T_A = 25^\circ\text{C}$ 0.1mV/ms
 - $T_A = 125^\circ\text{C}$ 10mV/ms
- Low Zero-Scale Error 4mV
- Digitally Selected Hold and Reset Modes
- Reset to Positive or Negative Voltage Levels
- Logic Signals TTL and CMOS Compatible
- Uncommitted Comparator on Chip

ORDERING INFORMATION†

25°C V _z (mV)	PACKAGE		OPERATING TEMPERATURE RANGE
	14-PIN DUAL-IN-LINE PACKAGE	HERMETIC* PLASTIC	
4	PKD01AY*	—	MIL
7	PKD01BY*	—	MIL
4	PKD01EY	—	IND
7	PKD01FY	—	IND
4	—	PKD01EP	COM
7	—	PKD01FP	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

The PKD-01 tracks an analog input signal until a maximum amplitude is reached. The maximum value is then retained as a peak voltage on a hold capacitor. Being a monolithic circuit, the PKD-01 offers significant performance and package density advantages over hybrid modules and discrete designs without sacrificing system versatility. The matching characteristics attained in a monolithic circuit provide inherent advantages when charge injection and droop rate error reduction are primary goals.

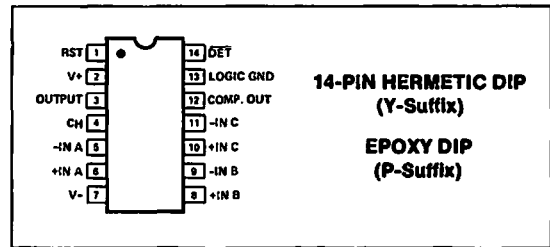
Innovative design techniques maximize the advantages of monolithic technology. Transconductance (g_m) amplifiers were chosen over conventional voltage amplifier circuit building blocks. The " g_m " amplifiers simplify internal frequency compensation, minimize acquisition time and maximize circuit accuracy. Their outputs are easily switched by low glitch current steering circuits. The steered outputs are clamped to reduce charge injection errors upon entering the hold mode or exiting the reset mode. The inherently low zero-scale error is reduced further by active "Zener-Zap" trimming to optimize overall accuracy.

The output buffer amplifier features an FET input stage to reduce droop rate error during lengthy peak hold periods. A bias current cancellation circuit minimizes droop error at high ambient temperatures.

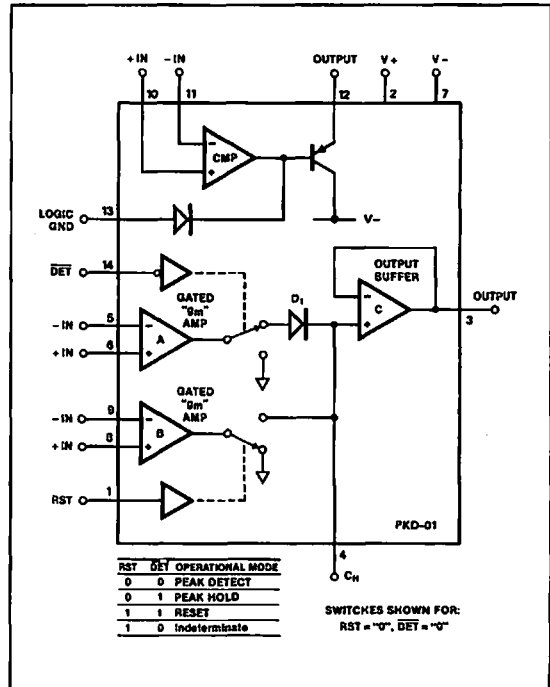
Through the $\overline{\text{DET}}$ control pin, new peaks may either be detected or ignored. Detected peaks are presented as positive output levels. Positive or negative peaks may be detected without additional active circuits since amplifier A can operate as an inverting or noninverting gain stage.

An uncommitted comparator provides many application options. Status indication and logic shaping/shifting are typical examples.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



SAMPLE-AND-HOLD AMPLIFIERS

14

ABSOLUTE MAXIMUM RATINGS (Note 2)

Supply Voltage	±18V
Power Dissipation	500mW
Input Voltage	Equal to Supply Voltage
Logic and Logic Ground	
Voltage	Equal to Supply Voltage
Output Short-Circuit Duration	Indefinite
Amplifier A or B Differential Input Voltage	±24V
Comparator Differential Input Voltage	±24V
Comparator Output Voltage	
.....	Equal to Positive Supply Voltage
Hold Capacitor Short-Circuit Duration	Indefinite
Lead Temperature (Soldering, 60 sec)	300°C
Storage Temperature Range	
PKD01AY, PKD01BY	-65°C to +150°C
PKD01EY, PKD01FY	-65°C to +150°C
PKD01EP, PKD01FP	-65°C to +125°C

Operating Temperature Range

PKD01AY, PKD01BY	-55°C to +125°C
PKD01EY, PKD01FY	-25°C to +85°C
PKD01EP, PKD01FP	0°C to +70°C
Dice Junction Temperature	-65°C to +150°C

PACKAGE (Note 1)	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
14-Pin DIP (Y)	80°C	10mW/°C
14-Pin DIP (P)	50°C	8mW/°C

NOTES:

1. Maximum package power dissipation vs. ambient temperature.
2. Absolute ratings apply to both packaged parts and DICE, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E			PKD-01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"g _m " AMPLIFIERS A, B									
Zero-Scale Error	V _{ZS}		—	2	4	—	3	7	mV
Input Offset Voltage	V _{OS}		—	2	3	—	3	6	mV
Input Bias Current	I _B		—	80	150	—	80	250	nA
Input Offset Current	I _{OS}		—	20	40	—	20	75	nA
Voltage Gain	A _V	R _L = 10kΩ, V _O = ±10V	18	25	—	10	25	—	V/mV
Open-Loop Bandwidth	BW	A _V = 1	—	0.4	—	—	0.4	—	MHz
Common-Mode Rejection Ratio	CMRR	−10V ≤ V _{CM} ≤ +10V	80	90	—	74	90	—	dB
Power Supply Rejection Ratio	PSRR	±9V ≤ V _S ≤ ±18V	66	96	—	76	96	—	dB
Input Voltage Range	V _{CM}	(Note 1)	±10	±11	—	±10	±11	—	V
Slew Rate	SR		—	0.5	—	—	0.5	—	V/μs
Feedthrough Error		ΔV _{IN} = 20V, DET = 1, RST = 0, (Note 1)	66	80	—	66	80	—	dB
Acquisition Time to 0.1% Accuracy	t _{aq}	20V Step, A _{VCL} = +1, (Note 1)	—	41	70	—	41	70	μs
Acquisition Time to 0.01% Accuracy	t _{aq}	20V Step, A _{VCL} = +1, (Note 1)	—	45	—	—	45	—	μs
COMPARATOR									
Input Offset Voltage	V _{OS}		—	0.5	1.5	—	1	3	mV
Input Bias Current	I _B		—	700	1000	—	700	1000	nA
Input Offset Current	I _{OS}		—	75	300	—	75	300	nA
Voltage Gain	A _V	2kΩ Pull-up Resistor to 5V	5	7.5	—	3.5	7.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	−10V ≤ V _{CM} ≤ +10V	82	106	—	82	106	—	dB
Power Supply Rejection Ratio	PSRR	±9V ≤ V _S ≤ ±18V	76	90	—	76	90	—	dB
Input Voltage Range	V _{CM}	(Note 1)	±11.5	±12.5	—	±11.5	±12.5	—	V

NOTES:

1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The

warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.

3. DET = 1, RST = 0.

**ELECTRICAL CHARACTERISTICS** at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E			PKD-01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	80	—	25	80	μA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	7	12	45	7	12	45	mA
Response Time	t_s	5mV Overdrive, (Note 3) 2k Ω Pull-up Resistor to 5V	—	150	—	—	150	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	1.6	10	—	1.6	10	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_J = 25^\circ C$, $T_A = 25^\circ C$ (See Note 2)	—	0.01	0.07	—	0.01	0.1	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$\overline{DET} = 1$ $R_L = 2.5k$	± 11.5	± 12.5	—	± 11	± 12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		7	15	40	7	15	40	mA
Switch Aperture Time	t_{sp}		—	75	—	—	75	—	ns
Switch Switching Time	t_s		—	50	—	—	50	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2.5	—	—	2.5	—	V/ μs
Power Supply Current	I_{SY}	No Load	—	5	7	—	6	9	mA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $-55^\circ C \leq T_A \leq 125^\circ C$ for PKD-01AY, PKD-01BY, $-25^\circ C \leq T_A \leq 85^\circ C$ for PKD-01EY, PKD-01FY and $0^\circ C \leq T_A \leq 70^\circ C$ for PKD-01EP, PKD-01FP.

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E			PKD-01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"g _m " AMPLIFIERS A, B									
Zero-Scale Error	V _{ZS}		—	4	7	—	6	12	mV
Input Offset Voltage	V _{OS}		—	3	6	—	5	10	mV
Average Input Offset Drift	TCV _{OS}	(Note 1)	—	−9	−24	—	−9	−24	μV/°C
Input Bias Current	I _B		—	160	250	—	160	500	nA
Input Offset Current	I _{OS}		—	30	100	—	30	150	nA
Voltage Gain	A _V	R _L = 10kΩ, V _O = ±10V	7.5	9	—	5	9	—	V/mV
Common-Mode Rejection Ratio	CMRR	−10V ≤ V _{CM} ≤ +10V	74	82	—	72	80	—	dB
Power Supply Rejection Ratio	PSRR	±9V ≤ V _S ≤ ±18V	80	90	—	70	90	—	dB
Input Voltage Range	V _{CM}	(Note 1)	±10	±11	—	±10	±11	—	V
Slew Rate	SR		—	0.4	—	—	0.4	—	V/μs
Acquisition Time to 0.1% Accuracy	t _{aq}	20V Step, A _{VCL} = +1, (Note 1)	—	60	—	—	60	—	μs
COMPARATOR									
Input Offset Voltage	V _{OS}		—	2	2.5	—	2	5	mV
Average Input Offset Drift	TCV _{OS}	(Note 1)	—	−4	−6	—	−4	−6	μV/°C
Input Bias Current	I _B		—	1000	2000	—	1100	2000	nA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $-55^\circ C \leq T_A \leq 125^\circ C$ for PKD-01AY, PKD-01BY, $-25^\circ C \leq T_A \leq 85^\circ C$ for PKD-01EY, PKD-01FY and $0^\circ C \leq T_A \leq 70^\circ C$ for PKD-01EP, PKD-01FP. (Continued)

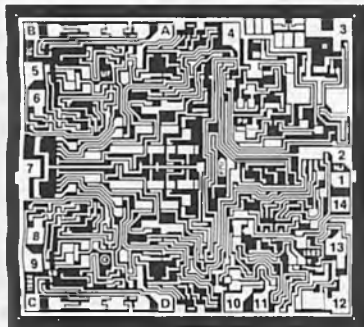
PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E			PKD-01B/F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Current	I_{OS}		—	100	600	—	100	600	nA
Voltage Gain	A_V	2k Ω Pull-up Resistor to 5V	4	6.5	—	2.5	6.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	80	100	—	80	92	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	72	82	—	72	86	—	dB
Input Voltage Range	V_{CM}	(Note 1)	± 11	—	—	± 11	—	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	100	—	100	180	μA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	6	10	45	6	10	45	mA
Response Time	t_s	5mV Overdrive, 2k Ω Pull-up Resistor to 5V	—	200	—	—	200	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	2.5	15	—	2.5	15	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_J = \text{Max. Operating Temp}$ $T_A = \text{Max. Operating Temp.}$ $DET = 1$, (Note 2)	—	1.2	10	—	3	15	mV/ms
			—	2.4	20	—	6	20	
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11	± 12	—	± 10.5	± 12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		6	12	40	6	12	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2	—	—	2	—	V/ μs
Power Supply Current	I_{SY}	No Load	—	5.5	8	—	6.5	10	mA

NOTES:

- Guaranteed by design.
- Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
- $DET = 1$, $RST = 0$.



DICE CHARACTERISTICS



1. RST (RESET CONTROL)
2. V+
3. OUTPUT
4. C_H (HOLD CAPACITOR)
5. INVERTING INPUT (A)
6. NONINVERTING INPUT (A)
7. V-
8. NONINVERTING INPUT (B)
9. INVERTING INPUT (B)
10. COMPARATOR NONINVERTING INPUT
11. COMPARATOR INVERTING INPUT
12. COMPARATOR OUTPUT
13. LOGIC GROUND
14. DET (PEAK DETECT CONTROL)
A,B (A) NULL
C,D (B) NULL

DIE SIZE 0.101 × 0.091 inch, 9191 sq. mils
(2.565 × 2.311mm, 5.93 sq mm)

For additional DICE ordering information, refer
to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero-Scale Error	V_{ZS}		7	mV MAX
Input Offset Voltage	V_{OS}		6	mV MAX
Input Bias Current	I_B		250	nA MAX
Input Offset Current	I_{OS}		75	nA MAX
Voltage Gain	A_V	$R_L = 10k\Omega$, $V_O = \pm 10V$	10	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	74	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	V MIN
Feedthrough Error		$\Delta V_{IN} = 20V$, DET = 1, RST = 0, (Note 1)	66	dB MIN
COMPARATOR				
Input Offset Voltage	V_{OS}		3	mV MAX
Input Bias Current	I_B		1000	nA MAX
Input Offset Current	I_{OS}		300	nA MAX
Voltage Gain	A_V	2k Ω Pull-up Resistor to 5V, (Note 1)	3.5	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	82	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	V MIN
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 5V	0.4 -0.2	V MAX V MIN
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	80	μA MAX
Output Short- Circuit Current	I_{SC}	$V_{OUT} = 5V$	45 7	mA MAX mA MIN

NOTES:

1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The

warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.

3. DET = 1, RST = 0.

**WAFER TEST LIMITS** at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
DIGITAL INPUTS-RST, DET (See Note 3)				
Logic "1" Input Voltage	V_H		2	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1	μA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	μA MAX
MISCELLANEOUS				
Droop Rate	V_{DR}	$T_J = 25^\circ C$, $T_A = 25^\circ C$ (See Note 2)	0.1	mV/ms MAX
			0.20	mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11	V MIN
Short-Circuit Current: Amplifier C	I_{SC}		40	mA MAX
			7	mA MIN
Power Supply Current	I_{SY}	No Load	9	mA MAX

NOTES:

1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than

1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures. Ambient (T_A) temperature specifications are not subject to production testing.

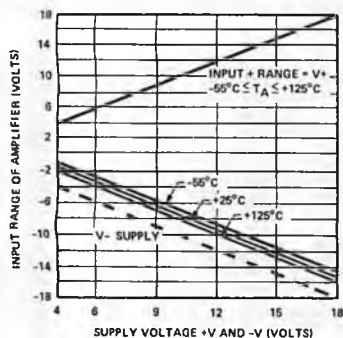
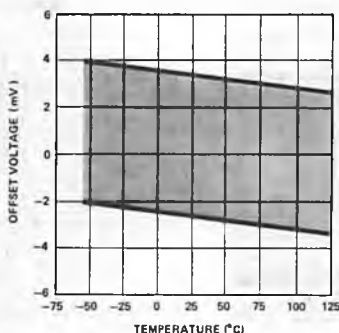
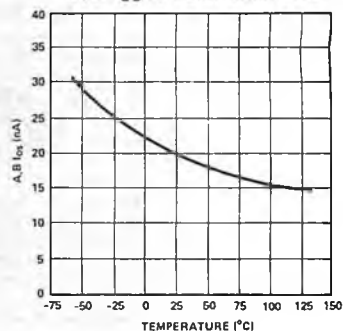
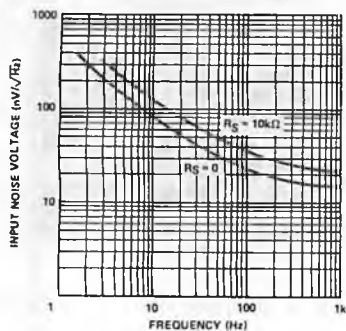
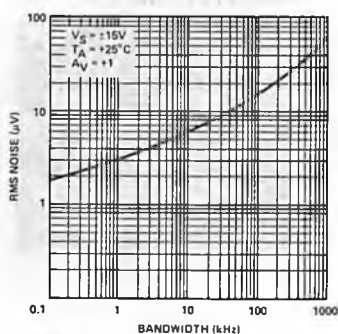
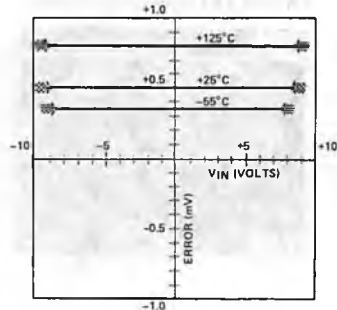
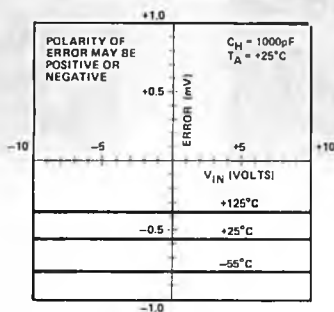
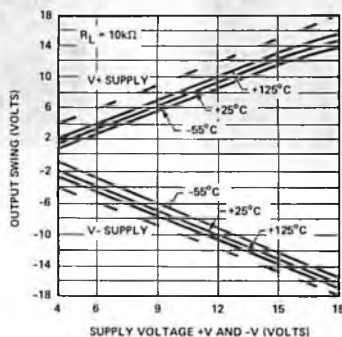
3. DET = 1, RST = 0.

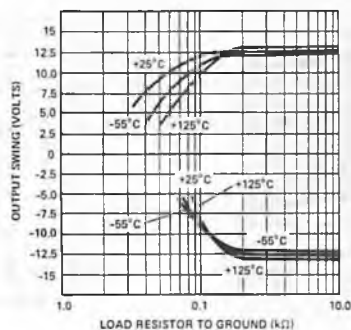
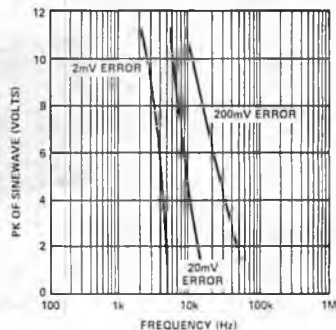
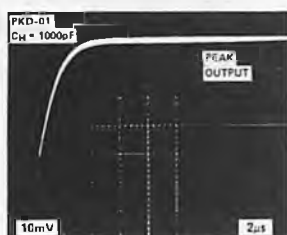
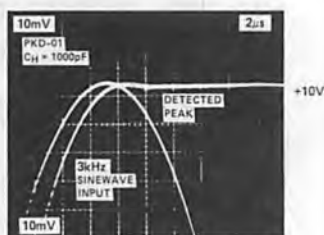
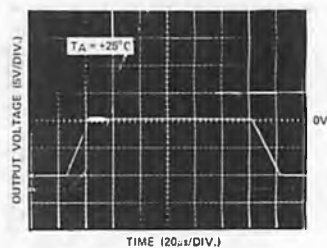
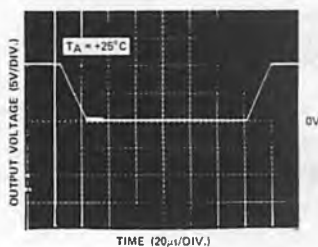
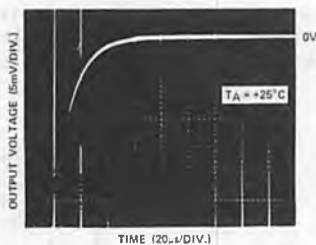
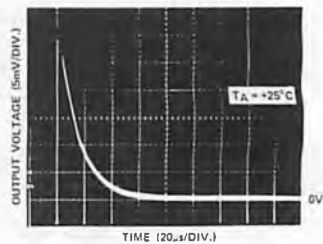
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

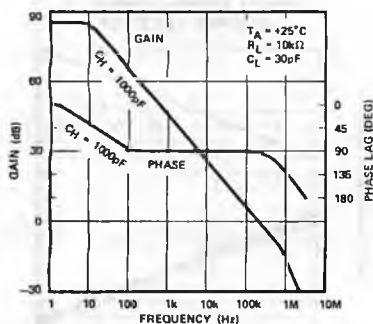
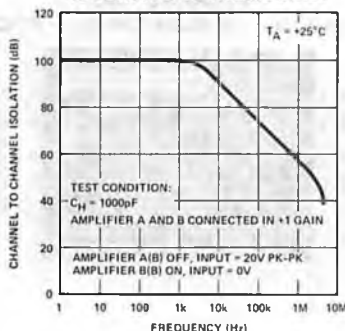
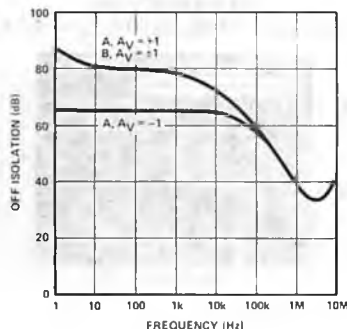
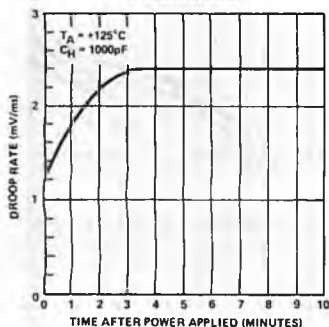
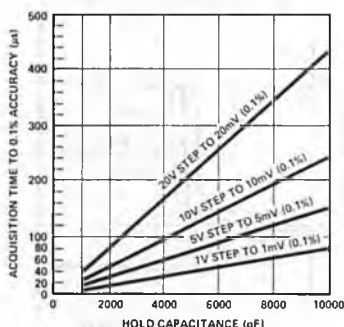
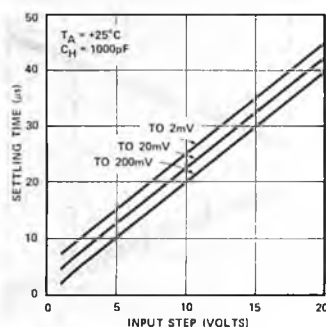
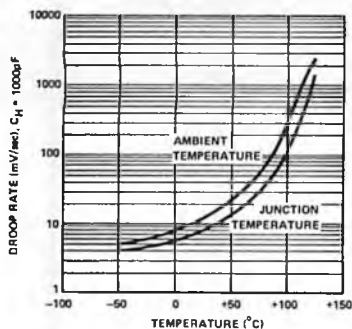
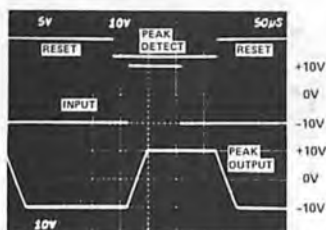
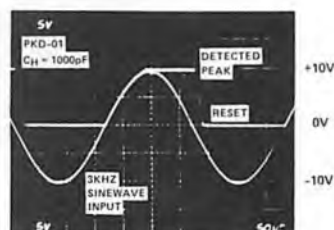
TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, and $T_A = 25^\circ C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	PKD-01N TYPICAL	UNITS
"σ_m" AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/ μs
Acquisition Time	t_a	0.1% Accuracy, 20V step, $A_{VCL} = 1$, (Note 1)	41	μs
Acquisition Time	t_a	0.01% Accuracy, 20V step, $A_{VCL} = 1$, (Note 1)	45	μs
COMPARATOR				
Response Time		5mV Overdrive, 2k Ω Pull-up Resistor to +5V	150	ns
MISCELLANEOUS				
Switch Aperture Time	t_{sp}		75	ns
Switching Time	t_s		50	ns
Buffer Slew Rate	SR	$R_L = 2.5k\Omega$	2.5	V/ μs

TYPICAL PERFORMANCE CHARACTERISTICS

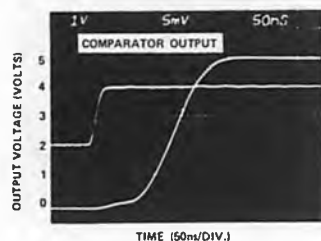
 A AND B INPUT RANGE
vs SUPPLY VOLTAGE

 A AND B AMPLIFIERS OFFSET
VOLTAGE vs TEMPERATURE

 A, B I_{OS} vs TEMPERATURE

 INPUT SPOT NOISE
vs FREQUENCY

 WIDEBAND NOISE
vs BANDWIDTH

 AMPLIFIER B CHARGE INJECTION
ERROR vs INPUT VOLTAGE
AND TEMPERATURE

 AMPLIFIER A CHARGE INJECTION
ERROR vs INPUT VOLTAGE
AND TEMPERATURE

 OUTPUT VOLTAGE SWING vs
SUPPLY VOLTAGE (DUAL
SUPPLY OPERATION)


TYPICAL PERFORMANCE CHARACTERISTICS
**OUTPUT VOLTAGE vs
LOAD RESISTANCE**

**OUTPUT ERROR vs
FREQUENCY AND
INPUT VOLTAGE**

PKD-01 SETTLING RESPONSE

PKD-01 SETTLING RESPONSE

**LARGE-SIGNAL
INVERTING RESPONSE**

**LARGE-SIGNAL
NONINVERTING RESPONSE**

**SETTLING TIME FOR -10V
TO 0V STEP INPUT**

**SETTLING TIME FOR +10V
TO 0V STEP INPUT**


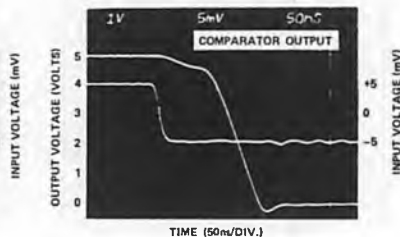
TYPICAL PERFORMANCE CHARACTERISTICS
**SMALL-SIGNAL OPEN LOOP
GAIN/PHASE vs FREQUENCY**

**CHANNEL TO CHANNEL
ISOLATION vs FREQUENCY**

**OFF ISOLATION
vs FREQUENCY**

**DROOP RATE vs TIME AFTER
POWER ON**

**ACQUISITION TIME vs EXTERNAL
HOLD CAPACITOR AND
ACQUISITION STEP**

**ACQUISITION TIME vs INPUT
VOLTAGE STEP SIZE**

**DROOP RATE
vs TEMPERATURE**

ACQUISITION OF STEP INPUT

**ACQUISITION OF
SINEWAVE PEAK**


TYPICAL PERFORMANCE CHARACTERISTICS

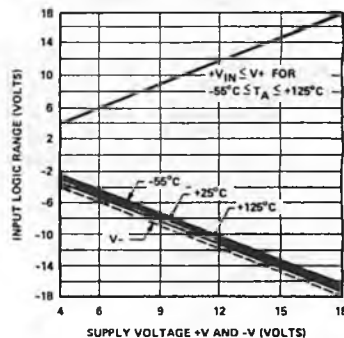
COMPARATOR OUTPUT
RESPONSE TIME
($2k\Omega$ PULL-UP RESISTOR, $T_A = +25^\circ\text{C}$)



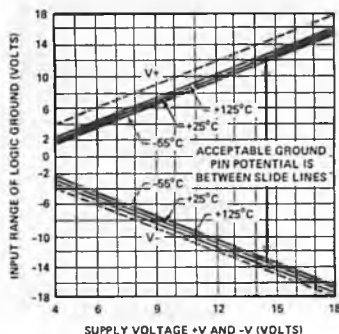
COMPARATOR OUTPUT
RESPONSE TIME
($2k\Omega$ PULL-UP RESISTOR, $T_A = +25^\circ\text{C}$)



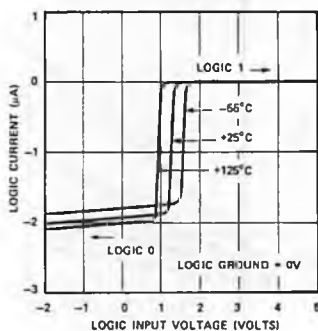
INPUT LOGIC RANGE vs
SUPPLY VOLTAGE



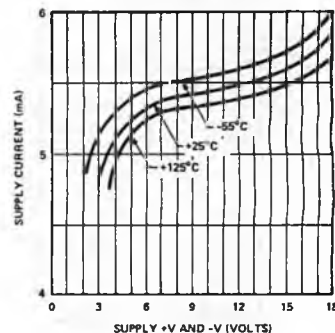
INPUT RANGE OF LOGIC
GROUND vs SUPPLY VOLTAGE



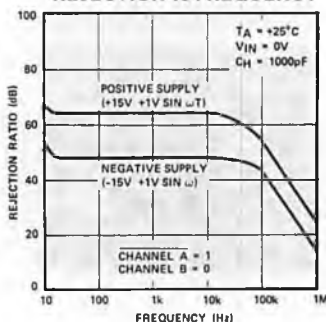
LOGIC INPUT CURRENT vs
LOGIC INPUT VOLTAGE



SUPPLY CURRENT vs
SUPPLY VOLTAGE

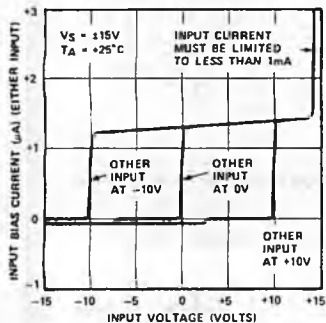


HOLD MODE POWER SUPPLY
REJECTION vs FREQUENCY

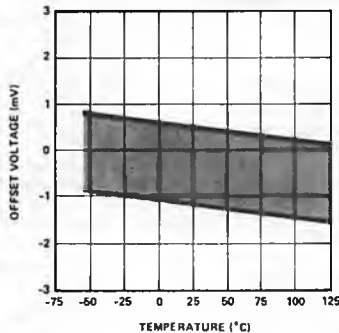
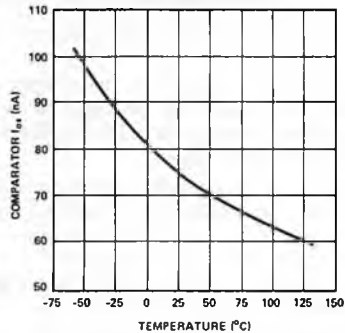
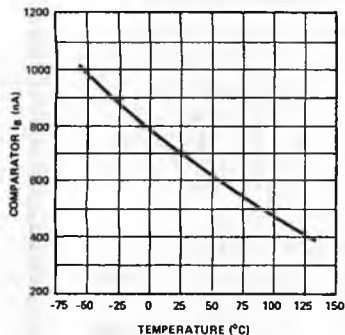


TYPICAL PERFORMANCE CHARACTERISTICS

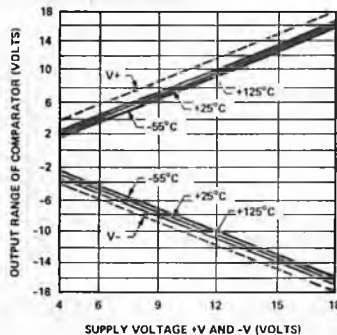
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



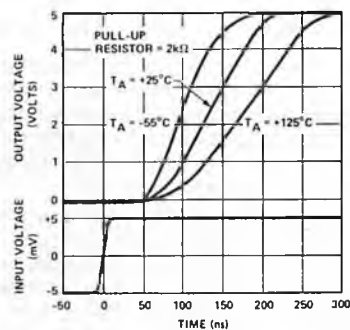
COMPARATOR OFFSET VOLTAGE vs TEMPERATURE


 COMPARATOR I_{OS} vs TEMPERATURE

 COMPARATOR I_B vs TEMPERATURE


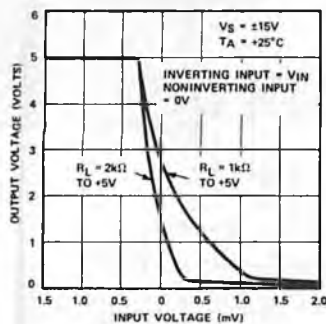
OUTPUT SWING OF COMPARATOR vs SUPPLY VOLTAGE



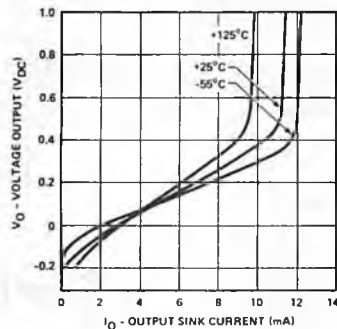
COMPARATOR RESPONSE TIME vs TEMPERATURE



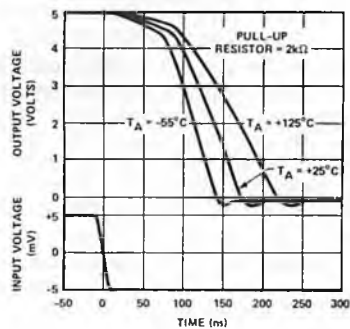
COMPARATOR TRANSFER CHARACTERISTIC



COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



COMPARATOR RESPONSE TIME vs TEMPERATURE



THEORY OF OPERATION

The typical peak detector uses voltage amplifiers and a diode or an emitter follower to charge the hold capacitor, C_H , unidirectionally (Figure 1). The output impedance of A plus D_1 's dynamic impedance, r_d , make up the resistance which determines the feedback loop pole. The dynamic impedance is $r_d = \frac{kT}{qI_d}$. I_d is the capacitor charging current.

The pole moves toward the origin of the S plane as I_d goes to zero. The pole movement in itself will not significantly lengthen the acquisition time since the pole is enclosed in the system feedback loop.

When the moving pole is considered with the typical frequency compensation of voltage amplifiers there is however, a loop stability problem. The necessary compensation can increase the required acquisition time. PMI's approach replaces the input voltage amplifier with a transconductance amplifier; Figure 2.

The PKD-01 transfer function can be reduced to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 + \frac{sC_H}{g_m} + \frac{1}{g_m R_{OUT}}} = \frac{1}{1 + \frac{sC_H}{g_m}}$$

Where: $g_m \approx 1\mu A/mV$, $R_{OUT} \approx 20M\Omega$.

The diode in series with A's output (Figure 2) has no effect because it is a resistance in series with a current source. In addition to simplifying the system compensation, the input transconductance amplifier output current is switched by current steering. The steered output is clamped to reduce and match any charge injection.

Fig. 3 shows a simplified schematic of the reset "g_m" amplifier. B. In the track mode, Q_1 & Q_4 are ON and Q_2 & Q_3 are OFF. A current of $2I$ passes through D_1 . I is summed at "B" and passes through Q_1 , and is summed with $g_m V_{IN}$. The current sink can absorb only $3I$, thus, the current passing through D_2 can only be: $2K - g_m V_{IN}$. The net current into the hold capacitor node then, is $g_m V_{IN}$ ($C_H = 2I - (2I - g_m V_{IN})$). The hold mode, Q_2 & Q_3 are ON while Q_1 & Q_4 are OFF. The net current into the top of D_1 is $-I$ until D_3 turns ON. With Q_1 OFF, the bottom of D_2 is pulled up with a current I until D_4 turns ON, thus D_1 & D_2 are reverse biased by $\sim 0.6V$ and charge injection is independent of input level.

The monolithic layout results in points A and B having equal nodal capacitance. In addition, matched diodes D_1 and D_2 have equal diffusion capacitance. When the transconductance amplifier outputs are switched open, points A and B are ramped equally but in opposite phase. Diode clamps D_3 and D_4 cause the swings to have equal amplitudes. The net charge injection (voltage change) at node C is therefore zero.

The peak transconductance amplifier, A, is shown in Figure 4. Unidirectional hold capacitor charging requires diode D_1 to be connected in series with the output. Upon entering the peak hold mode D_1 is reverse biased. The voltage clamp limits charge injection to approximately $1pC$ and the hold step to $0.6mV$.

Minimizing acquisition time dictated a small C_H capacitance. A $1000pF$ value was selected. Droop rate was also minimized

by providing the output buffer with an FET input stage. A current cancellation circuit further reduces droop current and minimizes the gate current's tendency to double for every $10^\circ C$ temperature change.

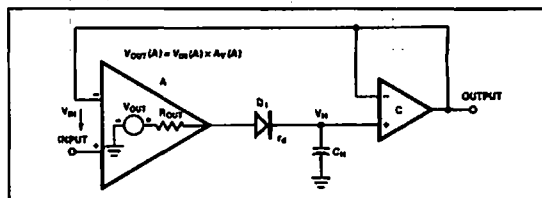


Figure 1. Conventional Voltage Amplifier Peak Detector

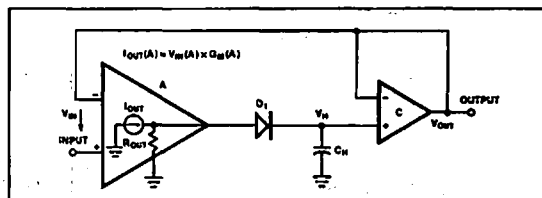


Figure 2. Transconductance Amplifier Peak Detector

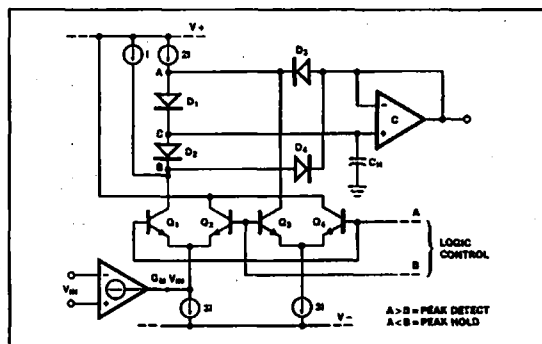


Figure 3. Transconductance Amplifier with Low Glitch Current Switch

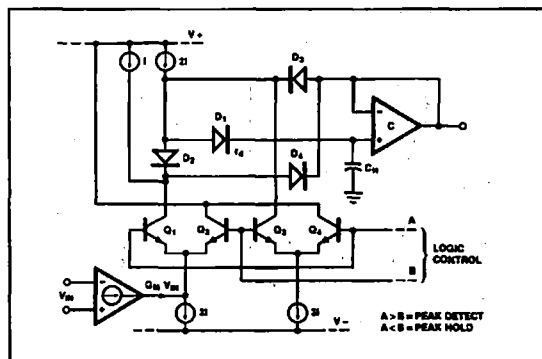


Figure 4. Peak Detecting Transconductance Amplifier with Switched Output

APPLICATIONS INFORMATION

OPTIONAL OFFSET VOLTAGE ADJUSTMENT

Offset voltage is the primary zero scale error component since a variable voltage clamp limits voltage excursions at D_1 's anode and reduces charge injection. The PKD-01 circuit gain and operational mode (positive or negative peak detection) determine the applicable null circuit. Figures A through D are suggested circuits. Each circuit corrects amplifier C offset voltage error also.

A. NULLING GATED OUTPUT g_m AMPLIFIER A. Diode D_1 must be conducting to close the feedback circuit during

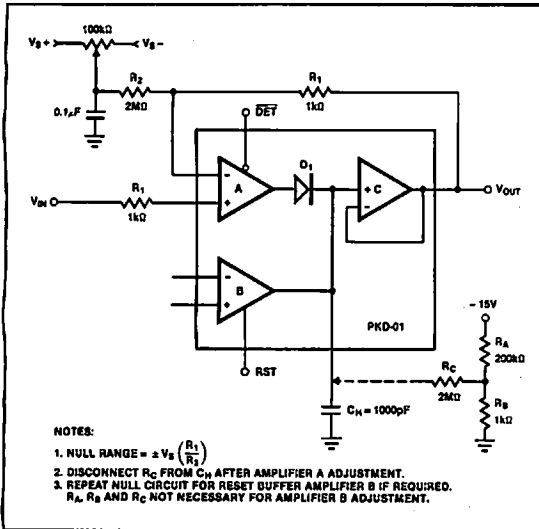


Figure A. V_{OS} Null Circuit for Unity Gain Positive Peak Detector

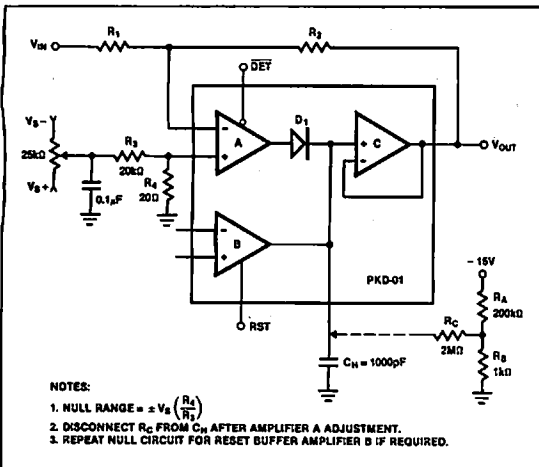


Figure C. V_{OS} Null Circuit for Negative Peak Detector

amplifier A V_{OS} adjustment. Resistor network $R_A - R_C$ cause D_1 to conduct slightly. With $DET = 0$ and $V_{IN} = 0V$ monitor the PKD-01 output. Adjust the null potentiometer until $V_{OUT} = 0V$. After adjustment, disconnect R_C from C_H .

B. NULLING GATED g_m AMPLIFIER B. Set amplifier B signal input to $V_{IN} = 0V$ and monitor the PKD-01 output. Set $DET = 1$, $RST = 1$ and adjust the null potentiometer for $V_{OUT} = 0V$. The circuit gain — inverting or noninverting — will determine which null circuit illustrated in Figures A through D is applicable.

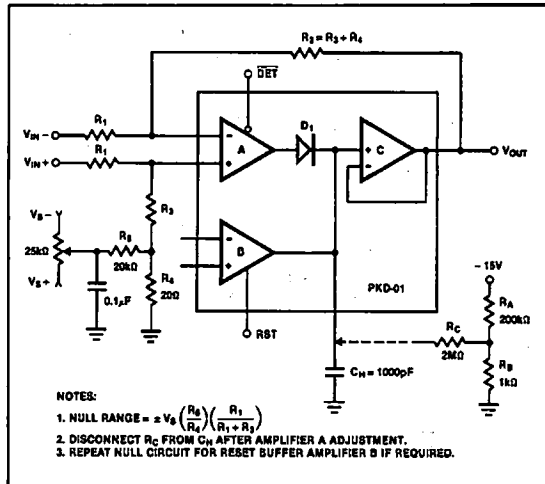


Figure B. V_{OS} Null Circuit for Differential Peak Detector

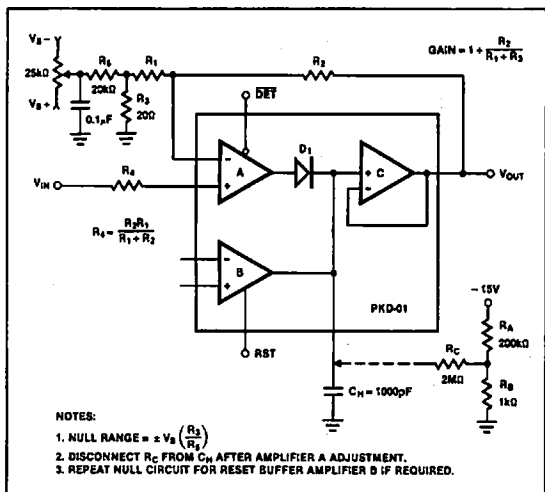


Figure D. V_{OS} Null Circuit for Positive Peak Detector With Gain

PEAK HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) serves as the peak memory element and compensating capacitor. Stable operation requires a minimum value of 1000pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase.

Zero scale error is internally trimmed for $C_H = 1000\text{pF}$. Other C_H values will cause a zero scale shift which can be approximated with the following equation.

$$\Delta V_{ZS}(\text{mV}) = \frac{1 \times 10^3(\text{pC})}{C_H(\text{nF})} - 0.6\text{mV}$$

The peak hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the common system ground. This avoids digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point. To minimize gain errors and maintain the PKD-01's inherently low droop rate, guarding Pin 4 as shown in Figure 2 is recommended.

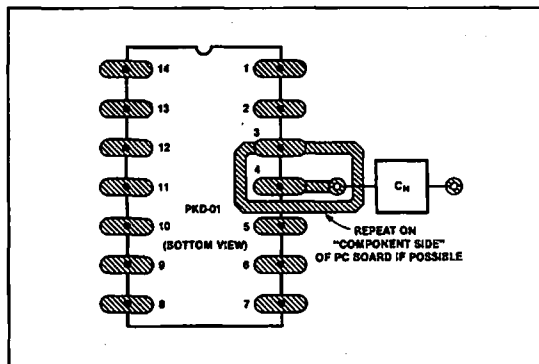


Figure 2. C_H terminal (Pin 4) guarding. See text.

COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

The maximum comparator high output voltage (V_{OH}) should be limited to:

$$V_{OH}(\text{maximum}) < V^+ - 2.0\text{V}$$

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1 .

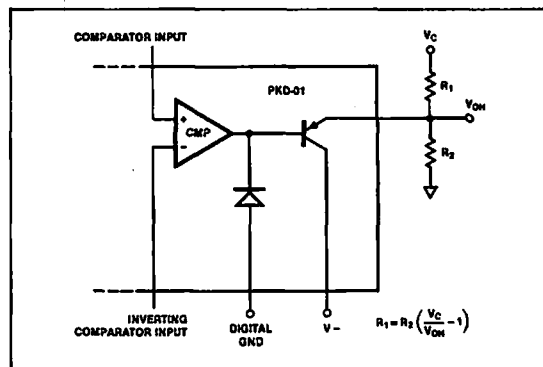


Figure 1

Table I.

V_C	V_{OH}	R_1	R_2
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{\text{SINK}}}$$

$$R_2 \approx \left(\frac{1}{\frac{V_C}{V_{OH}} - 1} \right)$$

PEAK DETECTOR LOGIC CONTROL (RST, DET)

The transconductance amplifier outputs are controlled by the digital logic signals RST and DET. The PKD-01 operational mode is selected by steering the current (I_1) through Q_1 and Q_2 , thus providing high-speed switching and a predictable logic threshold. The logic threshold voltage is 1.4 volts when digital ground is at zero volts.

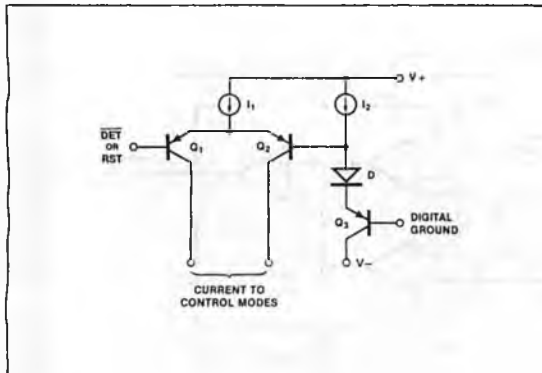
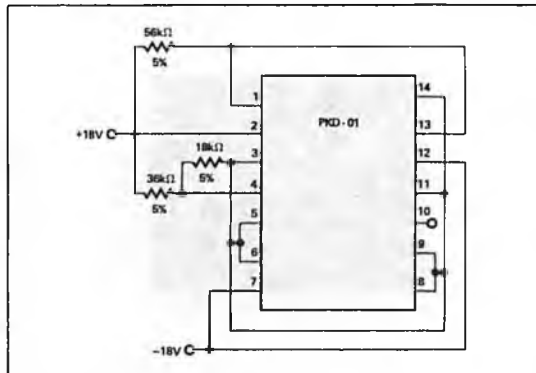
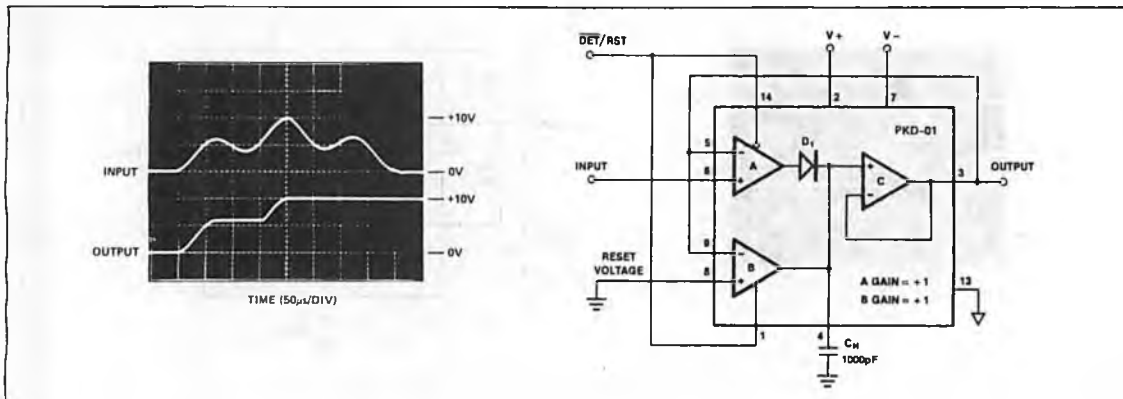
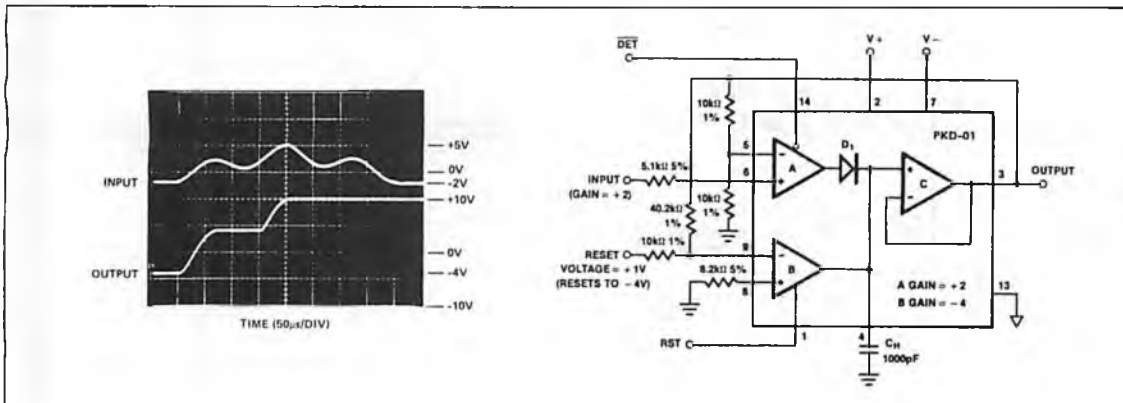
Other threshold voltages (V_{TH}) may be selected by applying the formula:

$$V_{TH} \approx 1.4\text{V} + \text{Digital Ground Potential.}$$

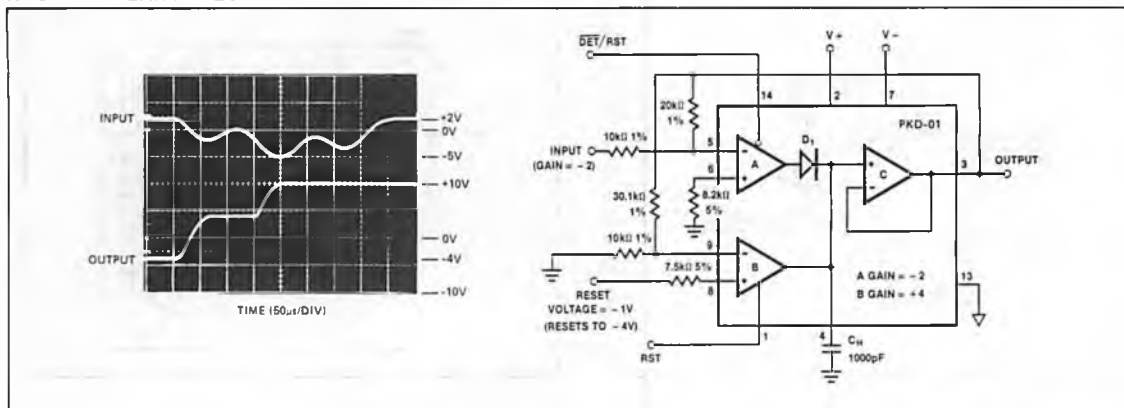
For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The RST or DET signal must always be at least 2.8V above the negative supply.

Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is referenced to digital ground and will follow any changes in digital ground potential:

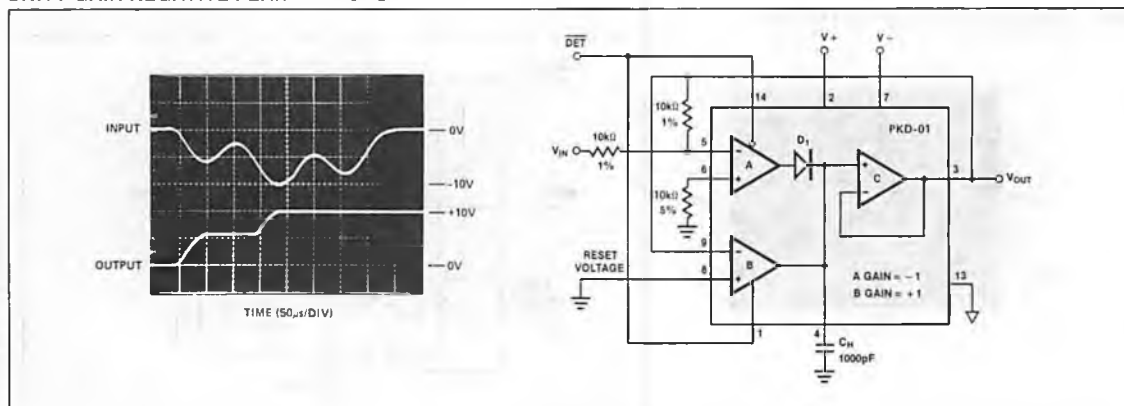
$$V_{OL} \approx 0.2\text{V} + \text{Digital Ground Potential.}$$

PKD-01 LOGIC CONTROL

BURN-IN CIRCUIT

TYPICAL CIRCUIT CONFIGURATIONS
UNITY GAIN POSITIVE PEAK DETECTOR

POSITIVE PEAK DETECTOR WITH GAIN


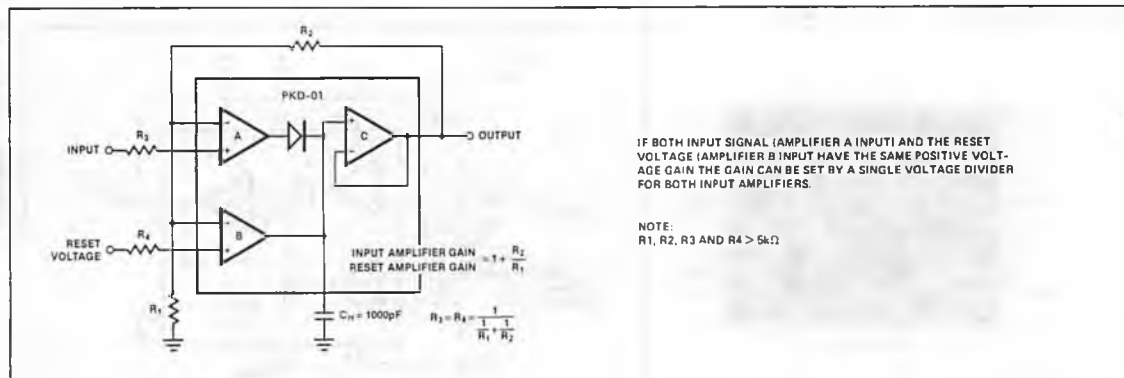
NEGATIVE PEAK DETECTOR WITH GAIN



UNITY GAIN NEGATIVE PEAK DETECTOR



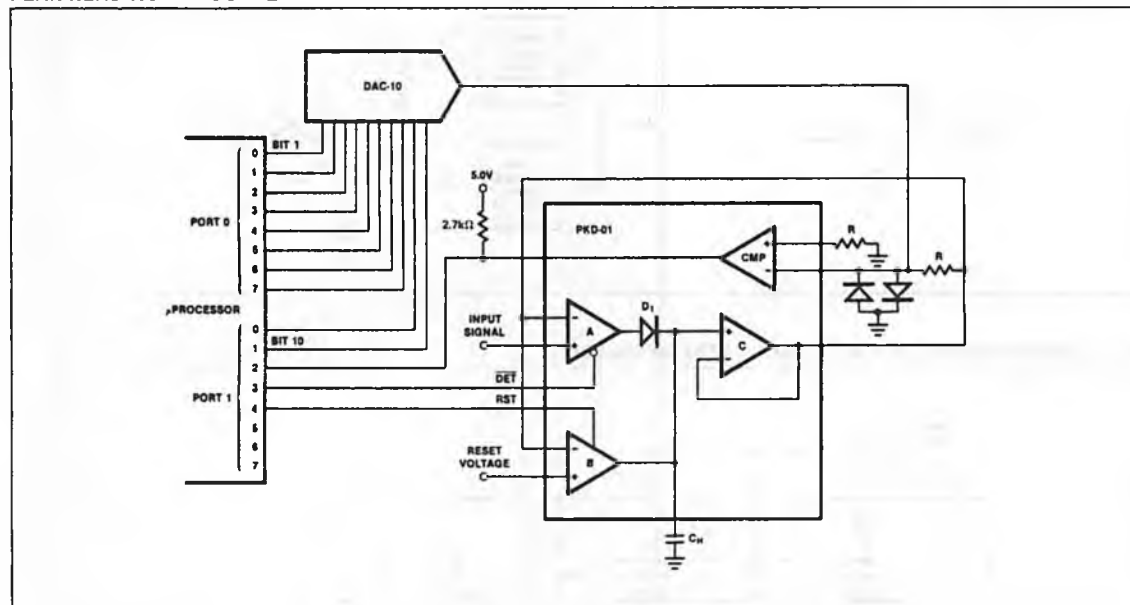
ALTERNATE GAIN CONFIGURATION



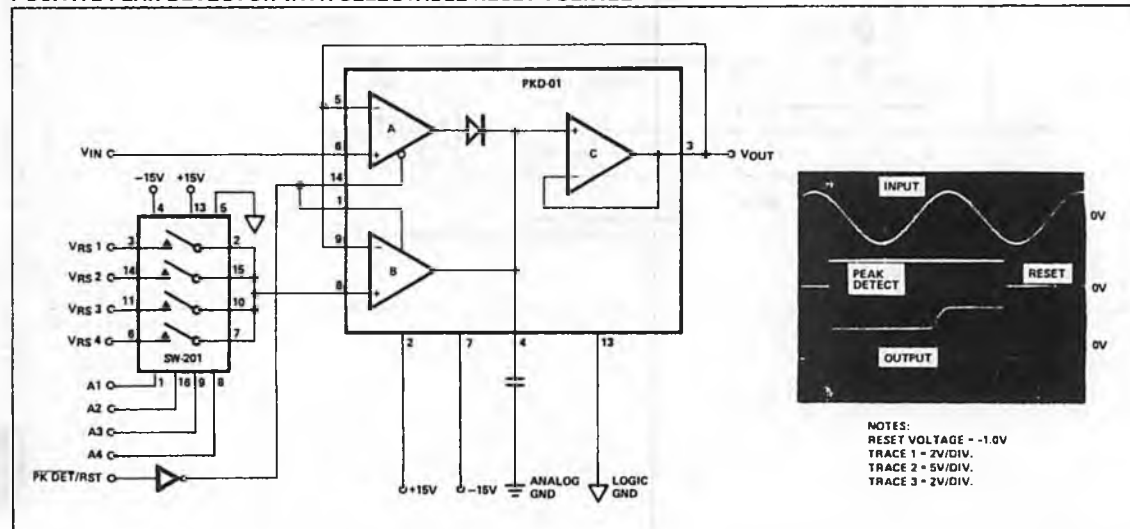
The diagram shows a circuit for detecting peak-to-peak levels. It consists of two main integrated circuits: a SN-02 comparator and a PKD-01 peak detector. The SN-02 is configured with its non-inverting input (pin 1) connected to the input signal through a resistor R. Its inverting input (pin 2) is connected to a +15V supply through a resistor R. The output of the SN-02 (pin 14) is connected to the input of the PKD-01 (pin 9). The PKD-01 is powered by +15V (pin 2) and -15V (pin 7). Its output (pin 3) is labeled 'OUTPUT'. A 'PEAK DETECTOR RESET' signal (pin 14) is connected to the input signal through a resistor R. The PKD-01 also has a pin 13 connected to ground through a 1000pF POLYSTYRENE capacitor. A 10.5kΩ resistor is connected between the +15V supply and pin 5 of the PKD-01. A 'POS/NEG PEAK DETECTOR' output is shown at the top left, connected to the input signal line.

NOTES:
 1. DEVICE IS RESET TO 0 VOLTS.
 2. DETECTED PEAKS ARE PRESENTED AS POSITIVE OUTPUT LEVELS.
 3. R = 10kΩ.

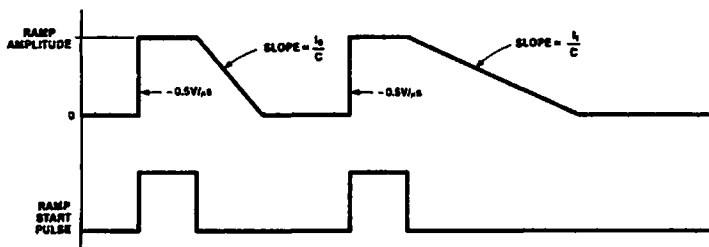
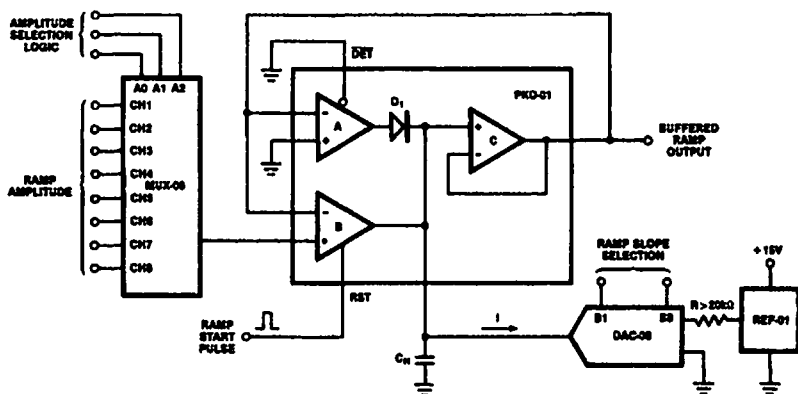
PEAK READING A/D CONVERTER



POSITIVE PEAK DETECTOR WITH SELECTABLE RESET VOLTAGE



PROGRAMMABLE LOW FREQUENCY RAMP GENERATOR



NOTES:
1. NEGATIVE SLOPE OF RAMP IS SET BY DAC-08 OUTPUT CURRENT.
2. DAC-08 IS DIGITALLY CONTROLLED CURRENT GENERATOR.
THE MAXIMUM FULL SCALE CURRENT MUST BE LESS THAN 0.5mA.

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*Indicates new product or product whose data sheet has been finalized since the 1986 data book.



COMMUNICATIONS PRODUCTS

Precision Monolithics Inc.

INTRODUCTION

PMI's line of communications products serve the needs of the serial data transmission networks used in telecommunications and LAN's. They perform the difficult interfacing function between the analog nature of a transmission line and the digital world of the microprocessor. The repeater products regenerate data which has been attenuated and distorted along the transmission line and retransmit the information synchronized to the original clock rate. The receiver products terminate the transmission line and separate the incoming clock and data information into microprocessor-compatible signals. Both are compatible with NRZ and RZ data transmissions, and both operate transparent to data formatting.

The RPT-82/RPT-83 are monolithic PCM repeaters used to regenerate alternate-mark-inversion pulses in PCM carrier systems at T1 (1.544Mbps) and T148 (2.048Mbps) data rates. These repeaters contain a high gain preamplifier and ALBO circuitry to achieve over 40dB of input signal dynamic range. RPT-86/RPT-87 are next generation PCM repeaters similar to the RPT-82/RPT-83 with many additional performance enhancements. These repeaters operate from a single 5.6V supply and are compatible with T1, T148, and the higher data rate T1C (3.152Mbit) systems. The RPT-86/RPT-87 both contain dual ALBO ports for an increased dynamic range of over 50dB. They also exhibit greatly improved stability versus temperature and supply voltage fluctuations. Both the RPT-83 and RPT-87 also contain a clock shutdown function to prevent the transmission of false data when the incoming signal falls below a usable level.

The LIU-01 is a versatile serial data receiver. It also contains dual ALBO ports for over 60dB of dynamic range and will operate at data rates from under 50Kbps to over 4Mbps. Unlike the repeaters, the LIU-01 presents both data and clock as TTL/CMOS compatible outputs. It also outputs a LOSS OF CARRIER signal indicating that the incoming signal has fallen below a usable level.

DEFINITIONS

ALBO Diode impedance — The small-signal impedance of the ALBO diode measured from the ALBO input to ground. The AC impedance is the parallel combination of two diode-connected transistors and approximately 3pF of stray capacitance. The impedance of the transistors is inversely proportional to the current flowing through them, $R_D = 13/I_D$, where R_D is the ALBO diode impedance in ohms and I_D is the ALBO diode current in mA.

ALBO Threshold — The differential voltage, measured between the preamp outputs, that is required to activate the internal peak detector which drives current through the ALBO diodes.

AMI — Alternate Mark Inversion. A form of digital signal transmission where each successive 1-bit is of opposite polarity.

Automatic Line Build Out, ALBO — An automatic-gain-control circuit which operates by simulating the attenuation and frequency distortion of an extension of the transmission line.

Bipolar Violation, BPV — The transmission of two consecutive pulses of the same polarity.

Bit Error Rate, BER — A count of the errored data bits received per second of transmission.

Clock Threshold — The differential voltage, measured between the preamp outputs, that is required to activate the clock synchronization circuitry.

Data Threshold — The differential voltage, measured between the preamp outputs, that is required to activate the data detection circuitry.

Equalizing Network — A network which compensates for the amplitude and phase response of the transmission cable over the operating bandwidth.

Loss of Carrier, LOC — An output indicating that the incoming signal has fallen below a usable level. This signal is active low.

Maximum Density — An input signal pattern consisting of all 1's.

Minimum Density — For T1 format, this is a repeating signal pattern consisting of two 1's followed by fourteen 0's.



COMMUNICATIONS PRODUCTS

Precision Monolithics Inc.

Oscillator Bias Voltage — A DC level used to set the center point of an LC oscillator tank's operation.

Output-Pulse Rise (Fall) Time — Measured from the 10% to 90% points.

Output-Pulse-Width Differential — In a T1 carrier system, a typical transmitted data pulse width is 324nsec. The pulse-width differential is the difference in pulse width of two successive outputs.

Preamplifier Bandwidth — 3dB bandwidth of the preamplifier circuit.

Quasi-Random Signal Source, QRSS — A signal consisting of random 1's and 0's.

RCLK — Received clock extracted from the incoming data signal.

RNEG — Received data extracted from negative incoming signal levels.

RPOS — Received data extracted from positive incoming signal levels.



RPT-82/RPT-83

PCM
REPEATERS

Precision Monolithics Inc.

FEATURES

- Automatic ALBO Function
- Clock-Shutdown Circuit (RPT-83)
- Low-Power Operation (100mW)
- Pin Compatible with XR-C277

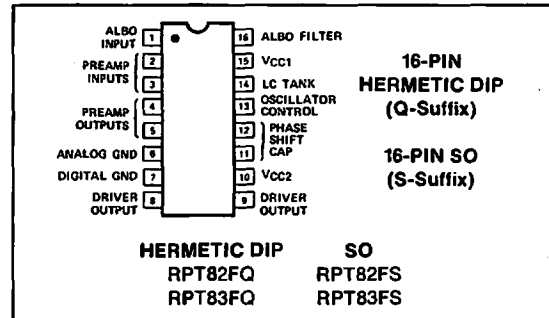
GENERAL DESCRIPTION

The RPT-82/83 are integrated circuits that perform the active functions required for regenerative PCM repeaters. They can operate from less than 100kHz to greater than 3MHz. In PCM systems, information is transmitted by the presence or absence of bipolar pulses in specified time slots. The RPT-82/83 repeaters automatically adjust gain to optimize signal levels, determine if a pulse is present or not, and retransmit the reconstructed pulses.

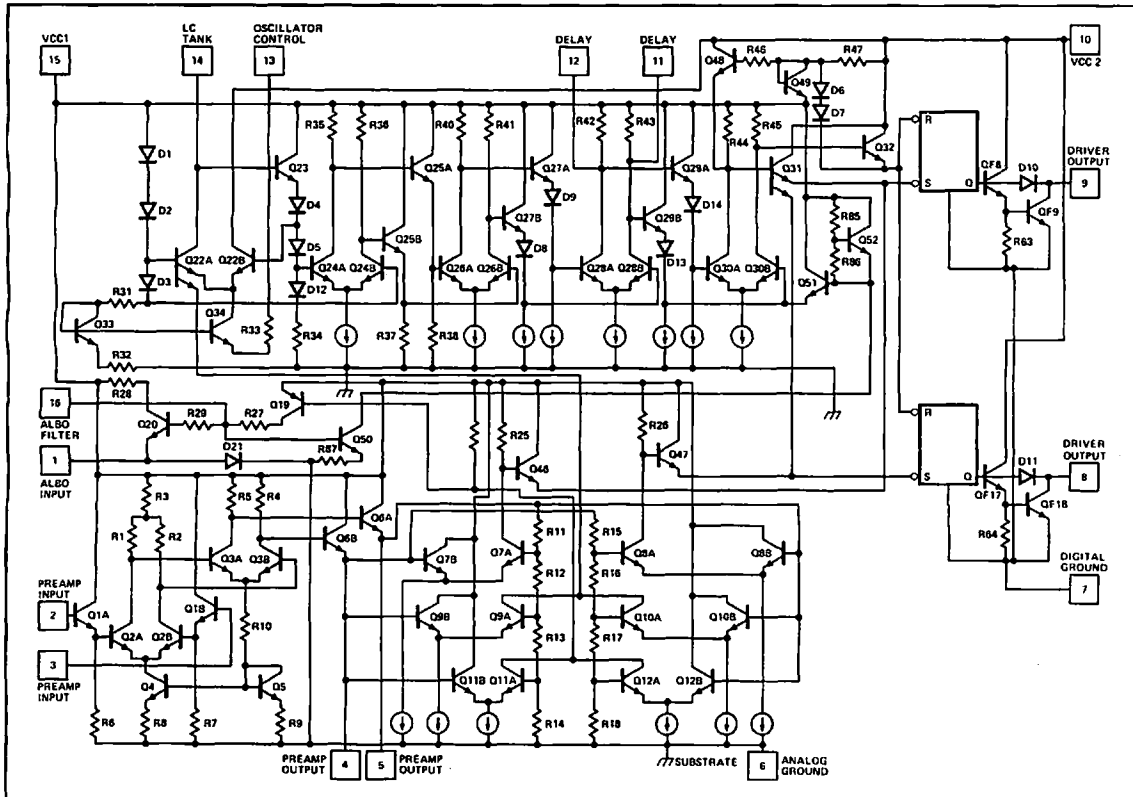
The difference between the RPT-82 and the RPT-83 is that the RPT-83 contains a clock-shutdown circuit. This shutdown circuit senses the incoming signal level and disables the clock

drive if the incoming signal is below the level where accurate reconstruction is possible. This prevents noise or cross-talk from appearing as a valid signal that would be retransmitted.

PIN CONNECTIONS & ORDERING INFORMATION



RPT-83 SIMPLIFIED SCHEMATIC



COMMUNICATIONS PRODUCTS

15

**ABSOLUTE MAXIMUM RATINGS**

Pin 10 to Pin 7 or 6	16.0V, -0.2V
Pin 15 to Pin 7 or 6	8.0V, -0.2V
Maximum Voltage at Pins 8 or 9	30V, -0.2V
Maximum Voltage at Pins 2, 3, 4, 5, 11, 12, 14	V_{CC2}
Maximum Sinking Current at Pin 8 or 9	300mA

Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	500mW
Lead Soldering Temperature	300°C

ELECTRICAL CHARACTERISTICS at $V_{CC1} = 4.4V$, $V_{CC2} = 6.8V$, $-40^\circ C \leq T_A \leq +85^\circ C$, unless otherwise noted. $V_{pin\ 6} = V_{pin\ 7} = V_{pin\ 13} = GND$.

PARAMETER	SYMBOL	CONDITIONS	RPT-82/RPT-83			UNITS
			MIN	TYP	MAX	
SUPPLY						
Supply Current	I _{CC1}	T _A = 25° C (Note 1)	5.0	8.5	9.5	mA
Supply Current	I _{CC2}	T _A = 25° C (Note 1)	1.0	2.5	3.5	mA
Total Supply Current	I _{CC1} + I _{CC2}	T _A = 25° C (Note 1)	6	11	13	mA
PREAMPLIFIER						
Preamplifier Open-Loop Gain $\frac{\Delta V_{pin\ 6}}{\Delta V_{pin\ 2}}$	A ₀	Measure $\Delta V_{pin\ 2}$ necessary to change pins from 1.8V to 3.2V	44	48	51	dB
Preamplifier Bandwidth	B _W	3dB Points (Note 2)	3	5	—	MHz
Preamplifier Input Impedance	Z _{IN}		—	600	—	kΩ
Preamplifier Input Offset Voltage	V _{OS}	V _{pin 2} - V _{pin 3} (Note 1)	—	1	15	mV
Preamplifier Output Impedance	Z _{OUT}	(Note 2)	—	80	150	Ω
Preamplifier Output High	V _{OHA}	V _{pin 4} with V _{pin 2} = 2.5V, V _{pin 3} = 2.7V, T _A = 25° C.	3.35	3.45	3.75	V
Preamplifier Output Low	V _{OHL}	V _{pin 4} with V _{pin 2} = 2.5V, V _{pin 3} = 2.3V, T _A = 25° C.	1.0	1.4	1.45	V
Preamplifier Input Bias Current	I _B	I _{pin 2} or I _{pin 3} (Note 1)	—	1	4	μA
Preamplifier Input Offset Current	I _{OS}	I _{pin 2} - I _{pin 3} (Note 1)	—	0.05	2	μA
OUTPUT DRIVE						
Output Voltage Swing	V _{OP}	V _{pin 8} High - V _{pin 8} Low, V _{pin 9} High - V _{pin 9} Low	—	6	—	V
Output Voltage, Low	V _{OL}	T _A = 25° C, I _{LOAD} = 15mA	0.5	0.8	1.1	V
Differential Output Voltage, Low	V _{OLD}	T _A = 25° C, I _{LOAD} = 15mA	—	0.02	0.15	V
Output Leakage Current	I _{OH}	V _{pin 14} = 4.9V, V _{pin 8} = V _{pin 9} = 20V, (Note 1) T _A = 25° C	—	0.05	50	μA
Output Pulse Rise-Time	T _{OS}	(Note 2)	—	30	50	ns
Output Pulse Fall-Time	T _{of}	(Note 2)	—	10	60	ns
Output Pulse Width	P _w	At f = 1.544 MHz	—	324	—	ns
Pulse-Width Differential	P _{wD}	(Note 2)	—	3	12	ns
Bipolar Violations at Maximum Density	BV ₁ MAX		—	0	—	—
Bipolar Violations with Quasi-Random Input Pattern	BV _R MAX		—	0	—	—
CLOCK CIRCUIT						
Tank Emitter-Follower Base Current	I _{TB}	I _{pin 14} , V _{pin 14} = 4.9V (Note 1)	—	4	15	μA
Tank Input Impedance	Z _{INT}	Measured from pin 14 to pin 15	—	300	—	kΩ
Oscillator Bias Current	I _{OSC}	V _{pin 14} = 3.9V (I _{OSC} - I _{TB}) (Note 1)	10	30	50	μA
Oscillator Injection Current	I _{INJ}	Set V _{pin 4} - V _{pin 5} = ± 1.4V, V _{pin 14} = 3.9V (I _{INJ} - I _{OSC})	60	160	190	μA
Delay Circuit Resistor	R _d	Measured from pin 11 or pin 12 to pin 15, T _A = 25° C	3.2	4.0	4.8	kΩ

NOTES:

- $V_{pin\ 2} = 2.5V$; adjust $V_{pin\ 3}$ until $V_{pin\ 4} = V_{pin\ 5}$.
- Sample tested.

**ELECTRICAL CHARACTERISTICS** at $V_{CC1} = 4.4V$, $V_{CC2} = 6.8V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$, unless otherwise noted. $V_{pin 6} = V_{pin 7} = V_{pin 13} = GND$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	RPT-82/RPT-83			UNITS
			MIN	TYP	MAX	
MISCELLANEOUS						
ALBO Threshold	V_{TA}	Differential voltage, measured between pins 4 and 5, required to activate the Peak Detector. $T_A = 25^{\circ}C$	1.35	1.5	1.65	V
Clock Threshold	V_{TC}	Differential voltage, measured between pins 4 and 5, required to activate the Clock Detector. $T_A = 25^{\circ}C$	0.85	1.0	1.2	V
Data Threshold	V_{TL}	Differential voltage, measured between pins 4 and 5, required to activate the Data Detector. $T_A = 25^{\circ}C$	0.65	0.75	0.85	V
Clock Threshold as % of ALBO Voltage	V_{TC}	$T_A = 25^{\circ}C$	67	73	78	%
Data Threshold as % of ALBO Voltage	V_{TL}	$T_A = 25^{\circ}C$	46	54	58	%
ALBO ON Voltage	V_{O16}	Measured at pin 16, $[V_{p4} - V_{p5}] = \text{ALBO Threshold}$	1.0	1.7	2.5	V
ALBO OFF Voltage	V_{F16}	Measured at pin 16 and pin 1 $T_A = 25^{\circ}C$ (Note 1)	—	—	75	mV
Minimum ALBO Diode Resistance	R_D MIN		—	8	—	Ω
Maximum ALBO Diode Impedance	R_D MAX	$f = 1.544\text{MHz}$	—	30	—	k Ω
ALBO Gain Range	A_m	(Note 3)	36	48	—	dB

NOTES:1. $V_{pin 2} = 2.5V$; adjust $V_{pin 3}$ until $V_{pin 4} = V_{pin 5}$.

2. Sample tested.

3. Guaranteed by design.

FUNCTIONAL DESCRIPTION

Bipolar-pulse transmission, the transmission of alternately positive and negative pulses, is used on repeater lines to remove the DC component present in unipolar PCM pulse trains. This also places the principal energy components in the 0-1.544MHz band, as opposed to the 0-3.088MHz band for

unipolar pulse trains. The absence of a DC component in bipolar pulse trains permits the repeater to be transformer-coupled to the repeater line and helps prevent time-shifting of the regenerator firing levels with variations in input pulse density (see Figure 1).

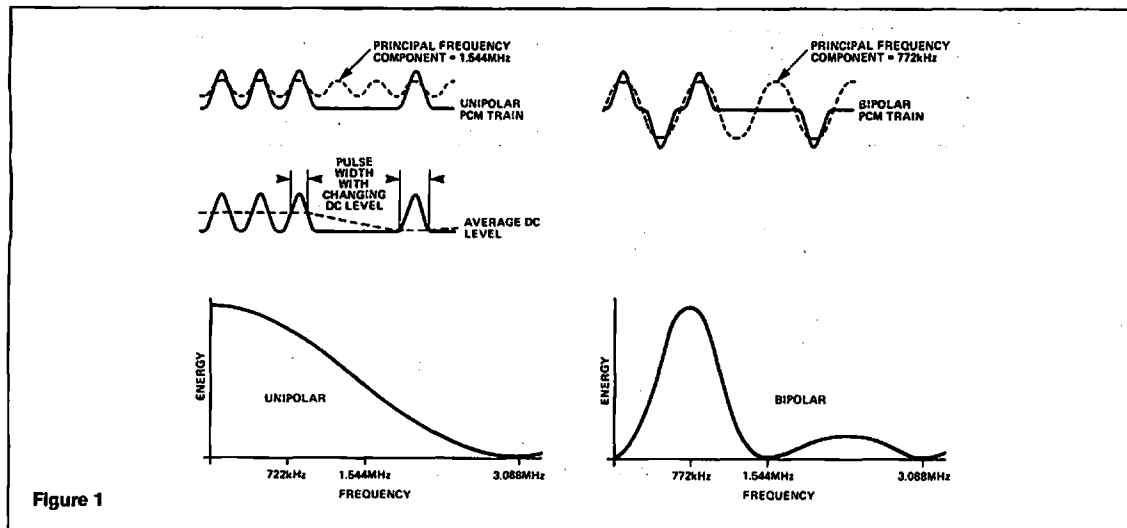
ENERGY SPECTRA OF BIPOLAR AND UNIPOLAR PULSE TRAINS

Figure 1

FUNCTIONAL BLOCK DIAGRAM

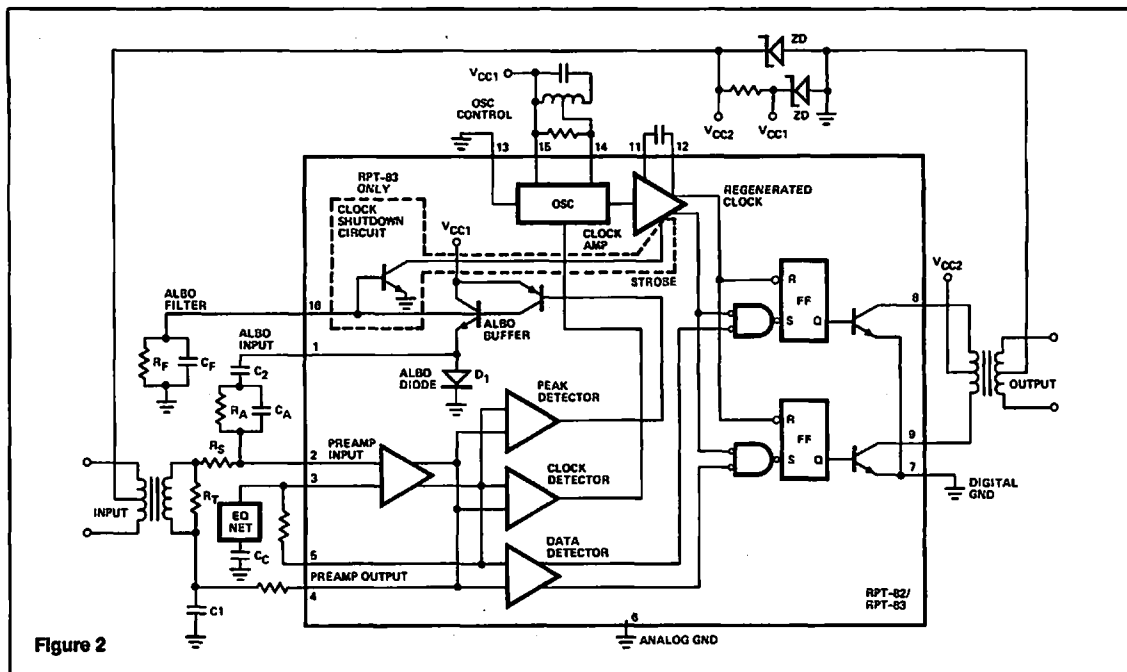


Figure 2

The bipolar-PCM pulse train is transformer-coupled into the preamplifier as shown in the functional block diagram (Figure 2). The secondary of the input transformer is loaded with the proper terminating resistor, R_T , to match the line impedance. One side of the transformer secondary is AC-coupled to ground by capacitor C_1 ; the other side of the secondary winding is in series with resistance R_S . Resistor R_S and the RC network $R_A C_A$ are AC-coupled to the ALBO input by capacitor C_2 . The impedance of the ALBO (Automatic Line Build-Out) input to ground is governed by the amount of current through the ALBO diode. R_S , in series with $R_A C_A$, provides signal attenuation proportional to the current flowing through the ALBO diode. When minimum current flows through the ALBO diode, C_2 is effectively isolated from ground and the input signal attenuation is minimal. The ALBO diode range of 8Ω to $30k\Omega$ provides compensation for line losses of approximately 5dB to 41dB.

The preamplifier stage amplifies the input signal and applies it to the three comparators labeled data detector, clock detector, and peak detector, respectively. Each comparator provides an output whenever the signal exceeds the trip point on both positive and negative pulses. Each comparator trips at a different threshold. The data detector is set to trip at the 54% point; the clock detector trips at the 73% point; and the peak detector trips at peak amplitude. Thresholds and waveforms are shown in Figure 3.

Current pulses from the peak detector are integrated by the capacitor in the ALBO filter. This causes a relatively constant

current to flow through the emitter follower and D_1 . In the RPT-83, a low voltage at the ALBO filter enables the clock-shutdown circuit when there is no input signal. The clock-shutdown circuit turns off the clock amplifier so that neither the regenerated clock, nor the strobe outputs, are sent to the flip-flops. This prevents the RPT-83 from sending noise or cross-talk out as valid-appearing data pulses when the incoming data level is too low.

The clock detector output locks the oscillator to the input frequency. The following amplifier stages shape the oscillator

THRESHOLDS AND WAVEFORMS

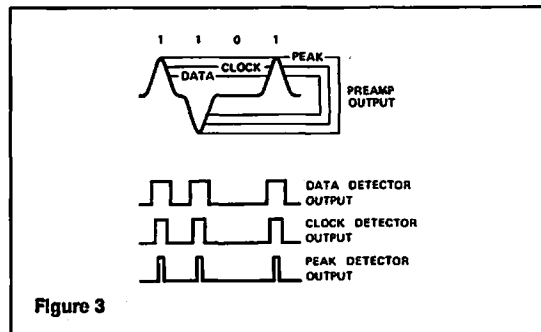


Figure 3

output and shift it in time. The phase-shift capacitor is selected to provide additional phase-shift so that the strobe pulses will occur at the center of the incoming pulses. This provides optimum timing for determining if a "1" or a "0" is present. A 0-to-30pF capacitor (10pF is typical at 1.544MHz) will optimize the performance of the complete repeater.

The delayed regenerated clock and the data-detector outputs drive the input flip-flops and output transistors. The output transistors are coupled to the transmission line through an output transformer.

DETAILED DESCRIPTION

PREAMPLIFIER

The preamplifier performs two basic functions. The first is to raise the level of the incoming signal to the correct level to trip the comparators. The second is to provide frequency/gain compensation to enhance the signal-to-noise ratio of the incoming signal. The preamp is designed to be operated in a near open-loop condition. A limited amount of feedback is used to control the frequency response. The gain-phase relationship of the preamp (see Figures 4 and 5) implies that the feedback network must have 40dB attenuation or more at 20MHz and above to ensure stability.

ALBO

To enable the preamp to operate open-loop with a wide range of signal levels, the ALBO diode is connected between the preamp input and ground. Since the ALBO-diode conductance is directly proportional to the ALBO-diode current, and the ALBO diode is driven by the peak detector, any signal in excess of that required to trip the peak detector will be shunted to ground through the ALBO diode. This automatic-gain-control function maintains the signal at the optimum level to operate the clock and data detectors.

The combination of R_S and R_A , in parallel with both C_A and the series impedance of the ALBO diode, perform the following two functions: 1) the automatic-gain-control function previously described, and 2) the frequency/phase compensation for transmission-line losses.

FREQUENCY/PHASE COMPENSATION

Frequency/phase compensation is desirable for three reasons:

1. If the bandwidth is wider than necessary, noise and cross-talk outside of the signal-frequency band will appear at the threshold detectors. Out-of-band signals increase the probability that an incorrect logic decision will be made. These incorrect logic decisions will increase the bit error rate.
2. Nonlinear phase-shifts in the transmission line may cause the signal to be distorted to the extent that bit errors occur. Phase compensation in the repeater can partly correct for this problem.
3. Large phase-shifts in the preamplifier at high frequencies can cause instability if not compensated for by the feedback network. (See Figures 4 and 5).

CLOCK DETECTOR

The clock detector drives the clock-tank circuit with a pulse each time that the incoming signal is greater than 73% of the average peak signal.

PEAK DETECTOR

The peak detector drives the ALBO buffer and ALBO diode at the peak of the amplified "1" bits. Whenever the preamp AC-signal-output exceeds about 1.5V peak-to-peak, the ALBO buffer becomes forward biased and drives current into both the ALBO diode and the ALBO filter. This closed-loop AGC action maintains the preamp input signal at about 5mVp-p.

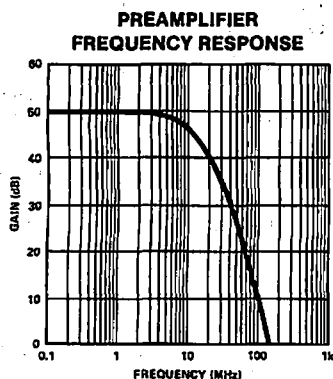


Figure 4

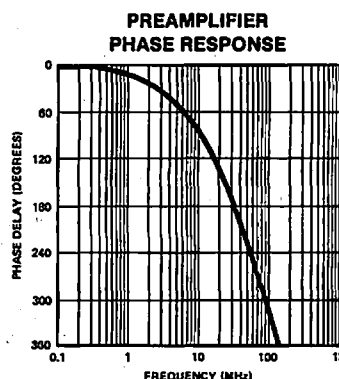


Figure 5

RPT-82/83 IN TYPICAL 1.544MHz T1 REPEATER SYSTEM

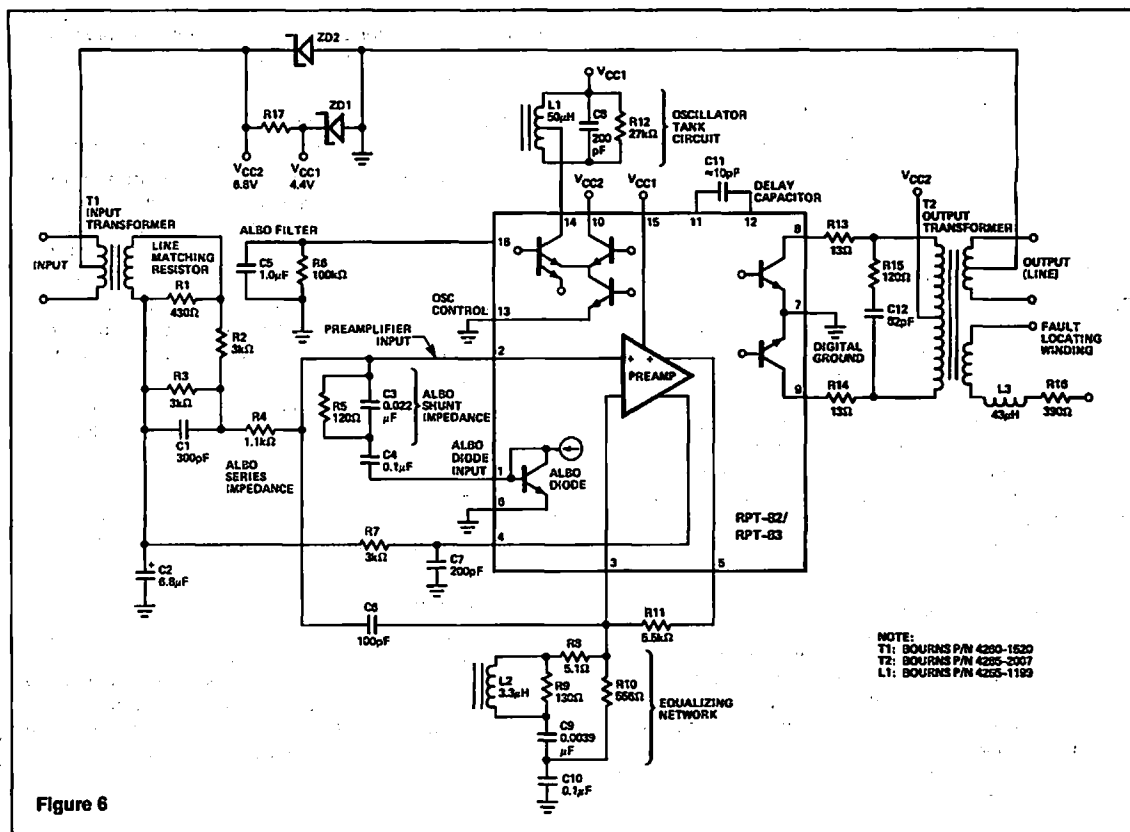


Figure 6

APPLICATION

In a typical T1, 1.544MHz repeater system (see Figure 6), the repeater is placed in series with a twisted-pair transmission line at distances of up to approximately 6000 feet. The power is supplied by a constant current of 60mA that is sent common-mode down the transmission line. This constant current is separated from the signal by input transformer T1 and output transformer T2, and is converted to voltages V_{CC1} and V_{CC2} by zener diodes ZD_1 and ZD_2 . The signal is coupled into the input network by T1. One end of T1 is held at AC ground by C2; and the other end is terminated by the line-matching resistor R1. The line-matching resistor is followed with a resistive attenuator consisting of R2 and R3, and the ALBO series impedance R4. The two resistors, R2 and R3, isolate the changing ALBO-diode impedance from the transmission line such that the transmission line is always correctly terminated. Resistor R4, in series with the shunt ALBO-diode impedance, determines the amount of attenuation provided at any given ALBO-diode current. Capacitor C1 provides a shunt path to ground for signals that are above the signal frequency.

When the ALBO-diode impedance is high, the ALBO series and shunt impedances have very little effect, so the unattenuated signal is applied to the preamp input with only C1 affecting the frequency response. When the ALBO-diode input impedance is reduced by higher signal levels, more of the input signal is shunted to ground through the ALBO shunt impedance.

The ALBO shunt impedance, C3 and R5, changes the input attenuation vs. frequency such that the system has more high frequency response at low signal levels, and less high frequency response at high signal levels. This change in bandwidth with signal level is intended to partially compensate for the increased high-frequency losses that occur in long transmission lines.

The bias feedback components between pin 4 and pin 2, consisting of C7, R7, and C2, operate as a DC self-biasing network. This C-R-C network prevents AC feedback and allows the preamp to establish a balanced input-and-output DC bias of 2.5 to 2.6 volts. Resistor R11 provides the DC path for biasing between pins 5 and 3.

Resistor R11 and capacitor C6 provide an AC feedback path. Resistors R10 and R11 act as an AC voltage divider that is shunted by the variable impedance of the resonant circuit comprised of L2 and C9. This frequency-selective feedback path, between pin 5 and pin 3, increases preamp gain at approximately 900kHz which further improves the system signal-to-noise ratio. The beneficial effect of the frequency-selective network is shown in Figure 7. The lower trace is a typical input signal (all 1's in this example) and the upper trace is the preamp output.

Figures 8 and 9 show the appearance of different preamp inputs measured at pin 5. Figure 8 is typical of an all 1's signal pattern with very little cross-talk or noise. Figure 9 shows a normal pattern of random 1's and 0's.

Due to the automatic-gain-control action of the ALBO circuitry, the peak amplitude is held constant for line losses of approximately 5dB to greater than 36dB. These signals are superimposed on a DC level of approximately 2.5V.

The preamp output drives the clock detector (reference Figures 2 and 6) which drives the clock-tank circuitry (L1, C8, and R12). The signal at pin 14, a sine wave of 0.2 to 1.0Vp-p (depending upon the percentage of 1-bits), drives the clock amplifier. The phase-shift capacitor, C11, provides the additional phase shift so that this integrated and phase-shifted signal (Figure 10) will strobe the output flip-flops at the optimum time to determine if a 1-bit is present. If a 1-bit is present, outputs from the data detector and the strobe cause the flip-flops to drive alternate output transistors. This signal is coupled through the output transformer into the next section of transmission line (see Figure 11, all 1's; and Figure 12, a random 1-0 pattern).



Figure 7

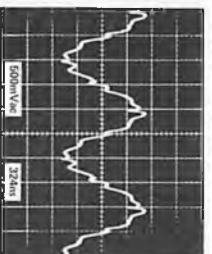


Figure 8

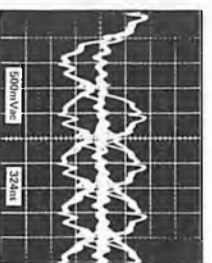


Figure 9

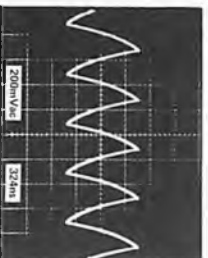


Figure 10

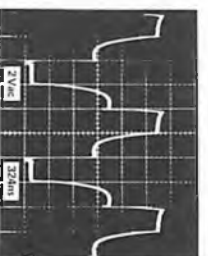


Figure 11

Figure 13 is a scope photograph of the signals as observed at several locations in the system. All traces are DC coupled and referenced to zero volts at the bottom graticule line. All signals, except the output, are displayed at 1-volt-per-division. The output is shown at 2-volts-per-division. The signal is all 1's. The phase relationships are typical for this type of repeater.

The signals shown are:

1. The preamp output at pin 5.
2. The clock-tank at pin 14.
3. The phase-shifted clock at pin 11.
4. The output signal at pin 8.
5. R13, 14, 15, and C12 control ringing and overshoot in the output waveform.

The fault-locating winding with L3 and R16 is used in long-line systems to determine which repeater, in a large series of repeaters, has become defective.

The RPT-82 and RPT-83 can be used in a variety of systems over a wide range of frequencies. The low-frequency response is limited by the difficulty in maintaining useable Q in the clock-tank circuit and by transformer-coupling losses. At high frequencies, the major limitation is the output-pulse rise-and-fall time.

The preamp is a high-gain, wide-bandwidth linear amplifier. Analog circuits do not have the noise rejection that is common with most digital circuits. To obtain best performance, certain precautions should be observed.

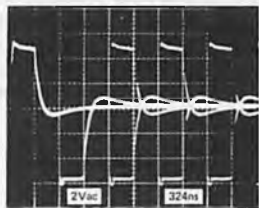


Figure 12

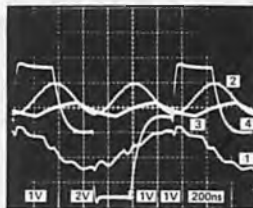


Figure 13

Circuit layout techniques used for R.F. amplifiers should be followed. Use of double-sided boards with all unused circuit-board area made into a ground plane is highly recommended. Keep input and output leads as far apart as possible, and signal runs as short as possible. Locate the attenuator network and the ALBO series impedance R4 as close to pin 2 as possible.

Power supply voltages V_{CC1} and V_{CC2} should be bypassed near pins 10 and 15. A bypass capacitor between the V_{CC2} connection on T_2 and pin 7 is also recommended.



Precision Monolithics Inc.

RPT-86/RPT-87

LOW POWER
PCM REPEATERS

PRELIMINARY

FEATURES

- Low Power Consumption (56mW)
- Single-Supply Operation
- Wide Data Rate Range < 100kbps to >3Mbps
- Dual ALBO Diodes; Dynamic Range >50dB
- Clock-Shutdown Circuit (RPT-87)

ORDERING INFORMATION†

PACKAGE		OPERATING TEMPERATURE RANGE
CERDIP	PLASTIC	
RPT86FQ	RPT86FS††	XIND
RPT87FQ	RPT87FS††	XIND

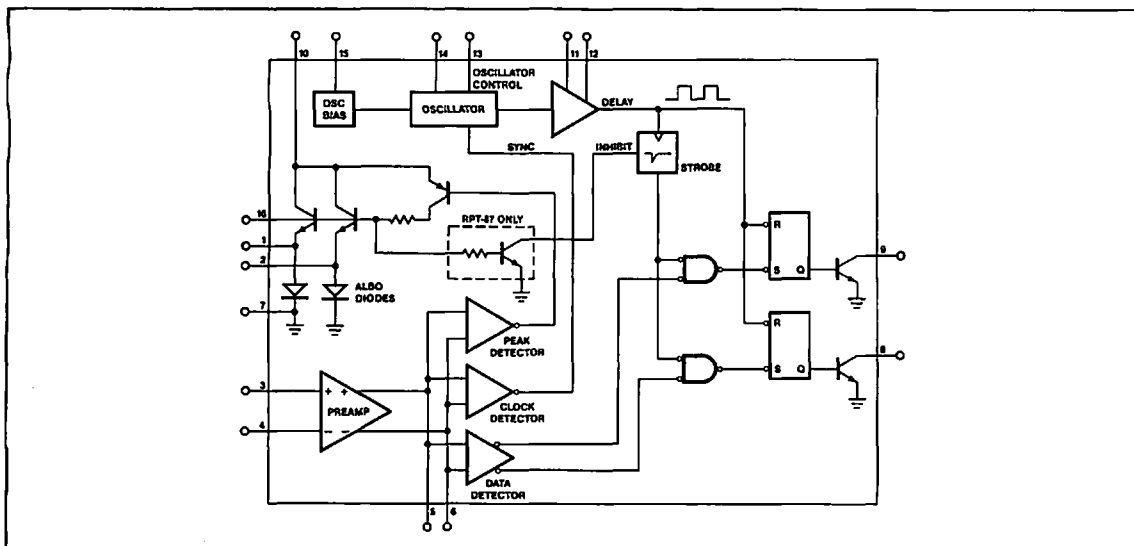
† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

The RPT-86 and RPT-87 are monolithic repeater circuits containing all the active functions required in regenerative PCM repeaters. These devices automatically adjust gain to optimize signal levels, determine if a pulse is present, and retransmit the reconstructed pulses. The RPT-86 and RPT-87 operate at data rates from under 100kbps to over 3Mbps and are compatible with T1 (1.544Mbps), T148 (2.048Mbps), and T1C(3.152Mbps) systems.

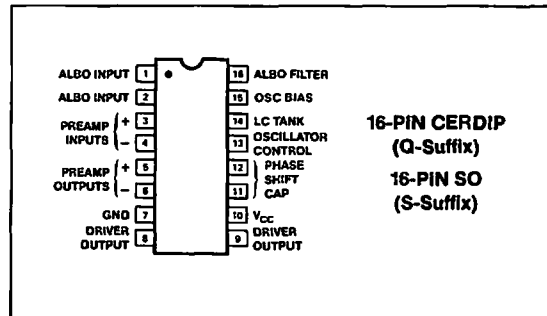
FUNCTIONAL BLOCK DIAGRAM



A key feature of the RPT-86/RPT-87 repeaters is the ability to operate on a single supply of 5.6V with a typical quiescent supply current of only 10mA. In addition, the RPT-86 and RPT-87 have two automatic line build-out diodes coupled with a high gain preamplifier that allows for a dynamic input signal range exceeding 50dB.

The RPT-87 also contains a clock-shutdown circuit. This shutdown circuit senses the incoming signal level and disables the clock drive to the output latches if the incoming signal is below the level where accurate pulse reconstruction is possible. This prevents noise or crosstalk from being mistaken as valid data and retransmitted.

PIN CONNECTIONS



COMMUNICATIONS PRODUCTS

15

This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.

**ABSOLUTE MAXIMUM RATINGS**

Voltage Pin 10 to Pin 7, 20ms Pulse,	
Duty Cycle ≤ 0.1	35V, -1.0V
Voltage Pin 10 to Pin 7, Continuous 50Hz	
Half-Wave Sinusoid	25V, -1.0V
Pin 10 to Pin 7, Continuously	13.5V, -0.7V
Voltage Pins 8 or 9 to Pin 7, Continuously	35V, -1.0V

Voltage Pins 3, 4, 5, 6, 11, 12, 14 to Pin 7	V_{CC}
Sinking Current at Pin 8 or 9	300mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	500mW
Lead Soldering Temperature	300°C

ELECTRICAL CHARACTERISTICS at $V_{CC} = 5.6V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$, unless otherwise noted. $V_{PIN 7} = V_{PIN 13} = GND$.

			RPT-86F/RPT-87F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Supply Current	I _{CC}	(Note 1)	5	10	12	mA
PREAMPLIFIER						
Preamplifier Open-Loop Gain	A _O		44	48	51	dB
Preamplifier Bandwidth	B _W	−3dB (Note 3)	3	5	—	MHz
Preamplifier Input Impedance, Differential	Z _{IN}	f = 1.544MHz	—	50	—	kΩ
Preamplifier Input Offset Voltage	V _{OS}	(Note 1)	—	1	5	mV
Preamplifier Output Impedance	Z _{OUT}		—	50	100	Ω
Preamplifier Output High	V _{OHA}	T _A = +25°C	3.35	3.45	—	V
Preamplifier Output Low	V _{OLA}	T _A = +25°C	—	1.4	1.45	V
Preamplifier Input Bias Current	I _B	(Note 1)	—	1	4	μA
Preamplifier Input Offset Current	I _{OS}	(Note 1)	—	0.02	0.2	μA
Preamplifier Output Self-Bias Voltage	V _{DC}	T _A = +25°C (Note 1)	2.4	2.5	2.6	V
OUTPUT DRIVE						
Output Voltage Low	V _{OL}	I _{LOAD} = 20mA	0.7	0.9	1.1	V
Differential Output Voltage, Low	V _{OLD}	I _{LOAD} = 20mA	—	0.02	0.15	V
Output Leakage Current	I _{OH}	V _{PIN 14} = 4.9V, V _{PIN 8} = V _{PIN 9} = 20V (Note 1)	—	0.05	50	μA
Output Pulse Rise-Time	T _{OR}	(Note 2)	—	30	50	ns
Output Pulse Fall-Time	T _{OF}	(Note 2)	—	10	60	ns
Output Pulse Width	P _w	f = 1.544MHz	—	324	—	ns
Pulse-Width Differential	P _{wD}	(Note 2)	—	3	12	ns
CLOCK CIRCUIT						
Tank Emitter-Follower Base Current	I _{TB}	I _{PIN 14} , V _{PIN 14} = 4.9V (Note 1)	—	4	15	μA
Oscillator Bias Current	I _{OSC}	V _{PIN 14} = 3.9V, (I _{OSC} − I _{TB}) (Note 1)	10	30	50	μA
Oscillator Injection Current	I _{INJ}	Set V _{PIN 8} − V _{PIN 5} = ±1.4V, V _{PIN 14} = 3.9V, (I _{INJ} − I _{OSC})	60	160	190	μA
Data Sampling Interval	T _{DS}	(Note 3)	—	70	95	ns
Delay Circuit Resistor	R _d	Measured from pin 11, or pin 12 to pin 15 T _A = +25°C	3.2	4.0	4.8	kΩ
Oscillator Bias Voltage	V _{BIAS}	V _{PIN 15}	—	4.4	—	V

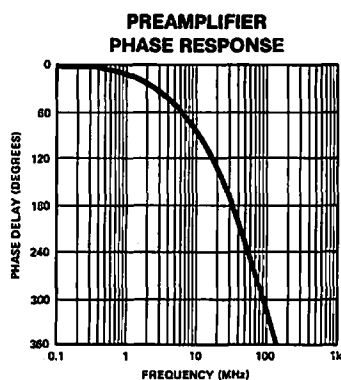
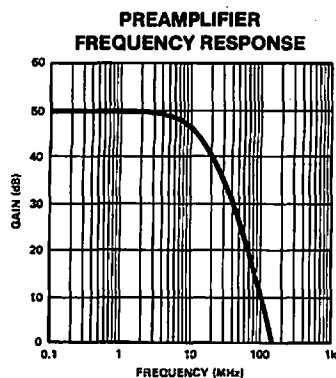


ELECTRICAL CHARACTERISTICS at $V_{CC} = 5.6V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$, unless otherwise noted. $V_{PIN7} = V_{PIN13} = GND$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	RPT-86F/RPT-87F			UNITS
			MIN	TYP	MAX	
ALBO						
ALBO Threshold	V _{TA}	Differential voltage, measured between pins 6 and 5, required to activate the Peak Detector.	1.35	1.5	1.65	V
ALBO Threshold ±Differential	V _{TAD}		—	—	75	mV
ALBO ON Voltage	V _{O16}	Measured at pin 16, [V _{PIN 6} – V _{PIN 5}] = ALBO Threshold	1.0	1.7	2.5	V
ALBO OFF Voltage	V _{F16}	Measured at pin 16 and pin 1 (Note 1)	—	—	75	mV
Minimum ALBO Diode Resistance	R _D MIN		—	6	10	Ω
Maximum ALBO Diode Impedance	R _D MAX	f = 1.544MHz (Note 4)	20	30	—	kΩ
ALBO Diode Impedance Matching		R _D MIN ≤ R _D ≤ R _D MAX	—	10	—	%
DATA/CLOCK THRESHOLDS						
Clock Threshold	V _{TC}	Differential voltage, measured between pins 6 and 5, required to activate the Clock Detector.	0.85	1.0	1.15	V
Clock Threshold as % of ALBO Voltage	V _{TC}		64	67	70	%
Clock Threshold ±Differential %	V _{TCD}		—	—	3	%
Data Threshold	V _{TL}	Differential voltage, measured between pins 6 and 5, required to activate the Data Detector.	0.65	0.75	0.85	V
Data Threshold as % of ALBO Voltage	V _{TL}		47	50	53	%
Data Threshold ±Differential %	V _{TLD}		—	—	3	%

NOTES:

1. Preamplifier self-biased. $V_{PIN3} \approx V_{PIN4} \approx V_{PIN5} \approx V_{PIN6}$
2. Sample tested.
3. Guaranteed by correlation to other tested parameters.
4. Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS



LIU-01

SERIAL
DATA RECEIVER

Precision Monolithics Inc.

PRELIMINARY

FEATURES

- Wide Data Rate Range, < 50kbps to >4Mbps
- Accepts RZ and NRZ Data Formats
- Accepts Unipolar and Bipolar Transmissions
- Single +5 Volt Operation
- Automatic Gain/Equalization Control; Dynamic Range >60dB
- TTL/CMOS Compatible Clock and Data Outputs
- Provides LOSS-OF-CARRIER Output
- Suitable for T1, T148, T1C, and LAN Applications
- Meets CCITT and ATT Specifications for ISDN Compatibility

APPLICATIONS

- PBXs and LANs Using Twisted-Pair, Coax, or Fiber Optic Cable
- ISDN Compatible Equipment: Computers, FAX Machines, Test Equipment
- Industrial Communications/Process Control
- Digital Multiplexers, CSUs, and Switching Equipment

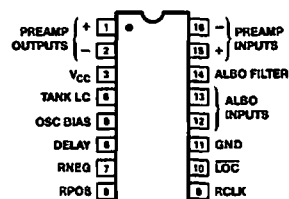
GENERAL DESCRIPTION

The LIU-01 is a versatile monolithic receiver for use in serial data transmission networks. It accepts both RZ and NRZ input signals, separates the clock and data, and presents both clock and data as TTL/CMOS compatible outputs. A LOSS-OF-CARRIER output is also provided to indicate that the incoming signal has fallen below a usable level. The LIU-01 incorporates a high gain preamplifier and dual ALBO ports enabling it to

automatically adjust for the signal attenuation and frequency distortion encountered at varying lengths of twisted-pair, coax, or fiber optic transmission lines. It will tolerate an input signal range of over 60dB and can handle data rates ranging from less than 50kbps to greater than 4Mbps.

The LIU-01 meets all CCITT and ATT specifications for an ISDN compatible receiver interface. Additionally, it is directly compatible with the R8070 and, with one additional inverter gate, the DS2180 digital T1 transceivers.

PIN CONNECTIONS

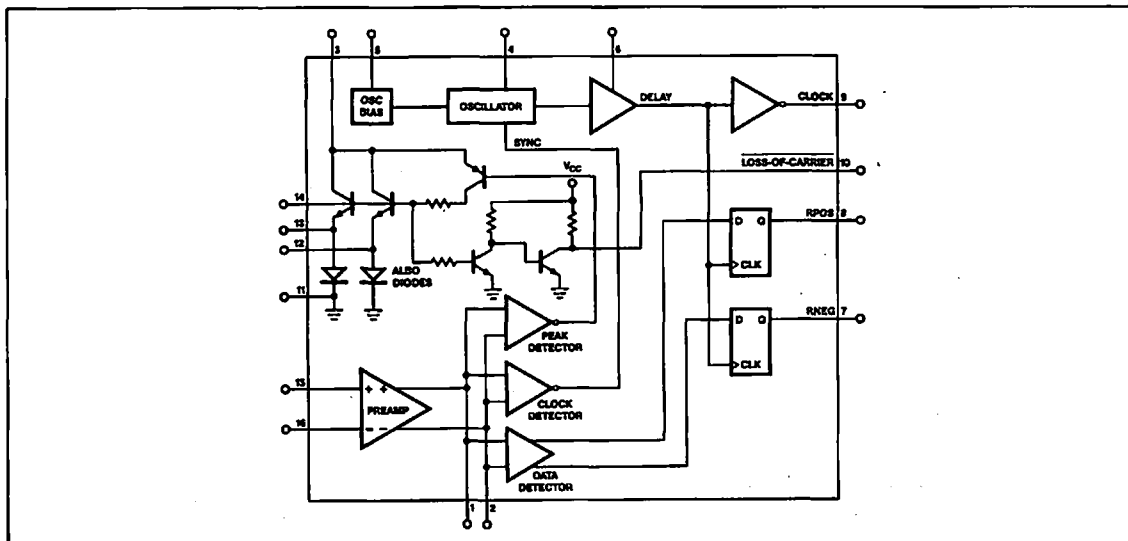


16-PIN CERDIP
(Q-Suffix)

16-PIN SOL
(S-Suffix)

16-PIN PLASTIC DIP
(P-Suffix)

FUNCTIONAL BLOCK DIAGRAM



This preliminary product information is based on testing of a limited number of devices. Final specifications may vary. Please contact local sales office or distributor for final data sheet.



ORDERING INFORMATION†

PACKAGE		OPERATING TEMPERATURE RANGE
CERDIP	PLASTIC	
LIU01FQ	LIU01FP	XIND
—	LIU01FS††	XIND

† Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS

Maximum Voltage, Pin 3 to Pin 7	6.5V, -0.5V
Maximum Voltage, Any Pin Except 12 and 13	V_{CC}
Maximum Sinking Current, Any Pin	20mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Power Dissipation	500mW
Lead Soldering Temperature	300°C

ELECTRICAL CHARACTERISTICS at $V_{CC} = 5V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	LIU-01F TYP	MAX	UNITS
SUPPLY						
Supply Current	I_{CC}	(Note 1)	—	20	—	mA
PREAMPLIFIER						
Preamplifier Open-Loop Gain	A_O		—	56	—	dB
Preamplifier Bandwidth	B_W	-3dB (Note 3)	6	9	—	MHz
Preamplifier Input Impedance, Differential	Z_{IN}	$f = 1.544\text{MHz}$	—	50	—	k Ω
Preamplifier Input Offset Voltage	V_{OS}	(Note 1)	—	1	10	mV
Preamplifier Output Impedance	Z_{OUT}		—	50	100	Ω
Preamplifier Output High	V_{OHA}	$T_A = +25^{\circ}C$	—	4.0	—	V
Preamplifier Output Low	V_{OLA}	$T_A = +25^{\circ}C$	—	1.2	—	V
Preamplifier Input Bias Current	I_B	(Note 1)	—	1	4	μA
Preamplifier Input Offset Current	I_{OS}	(Note 1)	—	0.02	0.5	μA
Preamplifier Output Self-Bias Voltage	V_{OC}	$T_A = +25^{\circ}C$ (Note 1)	—	2.5	—	V
OUTPUT DRIVE						
Output High Voltage, LOC	V_{OHC}	$I_L = 100\mu A$	—	4.0	—	V
Output Low Voltage, LOC	V_{OLC}	$I_L = 5\text{mA}$	—	0.25	—	V
Output High Voltage, RPOS, RNEG, RCLK	V_{OHD}	$I_L = 400\mu A$	—	3.5	—	V
Output Low Voltage, RPOS, RNEG, RCLK	V_{OLD}	$I_L = 5\text{mA}$	—	0.25	—	V
Output Pulse Rise-Time	T_{ON}	(Note 2)	—	20	—	ns
Output Pulse Fall-Time	T_{OF}	(Note 2)	—	20	—	ns
Output Pulse-Width, RPOS, RNEG	P_{WP}	$f = 1.544\text{MHz}$	—	648	—	ns
Output Pulse-Width, RCLK	P_{WD}	$f = 1.544\text{MHz}$	—	324	—	ns
CLOCK CIRCUIT						
Oscillator Bias Voltage	V_{BIAS}	$V_{PIN 5}$	—	3	—	V
Tank Emitter-Follower Base Current	I_{TB}	(Note 1)	—	10	—	μA
Oscillator Bias Current	I_{OSC}		—	30	—	μA
Oscillator Injection Current	I_{INJ}		—	200	—	μA
Data Sampling Interval	T_{DS}	(Note 3)	—	20	—	ns
Delay Circuit Resistor	R_D	Measured from pin 6 to pin 3 $T_A = +25^{\circ}C$	700	1000	1300	Ω

**ELECTRICAL CHARACTERISTICS** at $V_{CC} = 5V$, $-40^{\circ}C \leq T_A \leq +85^{\circ}C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	LIU-01F TYP	MAX	UNITS
ALBO						
ALBO Threshold	V_{TA}	Differential voltage, measured between pins 1 and 2, required to activate the Peak Detector	1.35	1.5	1.65	V
ALBO Threshold $\pm$ Differential	V_{TAD}		—	—	75	mV
ALBO ON Voltage	V_{O14}	Measured at Pin 14, [$V_{PIN\ 1} - V_{PIN\ 2}$] = ALBO Threshold	1.0	1.7	4.0	V
ALBO OFF Voltage	V_{FH}	Measured at Pins 12, 13, 14 (Note 1)	—	—	75	mV
Minimum ALBO Diode Resistance	$R_D\ MIN$		—	5	8	Ω
Maximum ALBO Diode Impedance	$R_D\ MAX$	$f = 1.544MHz$ (Note 4)	20	30	—	k Ω
ALBO Diode Impedance Matching		$R_{D\ MIN} \leq R_D \leq R_{D\ MAX}$	—	10	—	%
DATA/CLOCK THRESHOLDS						
Clock Threshold	V_{TC}	Differential voltage, measured between pins 1 and 2, required to activate the Clock Detector.	0.85	1.0	1.15	V
Clock Threshold as % of ALBO Voltage	V_{TC}		64	67	70	%
Clock Threshold $\pm$ Differential %	V_{TCD}		—	—	3	%
Data Threshold	V_{TL}	Differential voltage, measured between pins 1 and 2, required to activate the Data Detector.	0.65	0.75	0.85	V
Data Threshold as % of ALBO Voltage	V_{TL}		47	50	53	%
Data Threshold $\pm$ Differential %	V_{TLD}		—	—	3	%

NOTES:

1. Preamplifier self-biased. $V_{PIN\ 1} = V_{PIN\ 2} = V_{PIN\ 15} = V_{PIN\ 16}$
2. Sample tested.
3. Guaranteed by correlation to other tested parameters.
4. Guaranteed by design.

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Precision Monolithics Inc.

PACKAGE INFORMATION

PMI Letter Designator	Package Description	38510 Applicable Configuration	Page	PMI Letter Designator	Package Description	38510 Applicable Configuration	Page
Package Dimensions — Metal Cans				Package Dimensions — Cerpacks			
H	6-Lead TO-78 Metal Can	—	16-4	L	10-Lead Cerpack	—	16-20
J	8-Lead TO-99 Metal Can	A1	16-4	M	14-Lead Cerpack	—	16-20
K	10-Lead TO-100 Metal Can	A2	16-4	F	16-Lead Cerpack	—	16-21
Package Dimensions — Ceramic DIPs				N	24-Lead Cerpack	—	16-21
Z	8-Lead Ceramic DIP	D4-1	16-5	Package Dimensions — Flatpacks			
Y	14-Lead Ceramic DIP	D1-1	16-5	L*	10-Lead Flatpack	F4-1	16-22
Q	16-Lead Ceramic DIP	D2-1	16-6	LB*	10-Lead Flatpack, Bottom-Brazed	F4-2	16-22
X	18-Lead Ceramic DIP	D6-1	16-6	M*	14-Lead Flatpack	F1-1	16-22
R	20-Lead Ceramic DIP	D8-1	16-7	MB*	14-Lead Flatpack, Bottom-Brazed	F1-2	16-22
W	24-Lead Narrow-Body Ceramic DIP	D9-1	16-8	F*	16-Lead Flatpack	F5-1	16-23
V	24-Lead Ceramic DIP	D3-1	16-9	FB*	16-Lead Flatpack, Bottom-Brazed	F5-2	16-23
T	28-Lead Ceramic DIP	—	16-10	N*	24-Lead Flatpack	F8-1	16-23
Package Dimensions — Side-Brazed DIPs				NB*	24-Lead Flatpack, Bottom-Brazed	F8-2	16-23
YB*	14-Lead Side-Brazed DIP	D1-3	16-11	Package Dimensions — Leadless Chip Carriers			
QB*	16-Lead Side-Brazed DIP	D2-3	16-11	RC	20-Position Chip Carrier	C-2	16-24
XB*	18-Lead Side-Brazed DIP	D6-3	16-12	TC	28-Position Chip Carrier	C-4	16-25
RB*	20-Lead Side-Brazed DIP	D8-3	16-12	Package Dimensions — Plastic Leaded Chip Carriers			
VB*	24-Lead Side-Brazed DIP	D3-3	16-13	PC	20-Lead Plastic Leaded Chip Carrier	—	16-26
TB*	28-Lead Side-Brazed DIP	—	16-14	PC	28-Lead Plastic Leaded Chip Carrier	—	16-27
Package Dimensions — Epoxy DIPs				Package Dimensions — Small Outline ICs			
P	8-Lead Epoxy DIP	—	16-15	S	8-Lead Narrow-Body SO	—	16-28
P	14-Lead Epoxy DIP	—	16-15	S	14-Lead Narrow-Body SO	—	16-28
P	16-Lead Epoxy DIP	—	16-16	S	16-Lead Narrow-Body SO	—	16-29
P	18-Lead Epoxy DIP	—	16-16	S	16-Lead Wide-Body SO	—	16-30
P	20-Lead Epoxy DIP	—	16-17	S	18-Lead Wide-Body SO	—	16-31
P	24-Lead Narrow-Body Epoxy DIP	—	16-18	S	20-Lead Wide-Body SO	—	16-32
P	24-Lead Epoxy DIP	—	16-19	S	24-Lead Wide-Body SO	—	16-33
				S	28-Lead Wide-Body SO	—	16-34

*Special Order Only.



PACKAGE INFORMATION

Precision Monolithics Inc.

Dimensioning Symbols

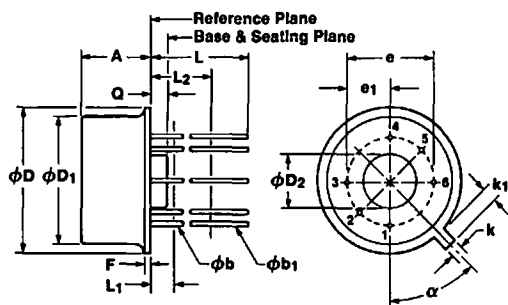
The symbols to be used for dimensioning case outlines will be as listed below. To designate the dimension as a diameter, the lower-case Greek letter ϕ (phi) will be added in front of the dimension symbol.

- A — Body dimensions.
- ϕb — Terminal lead diameters.
- b — Terminal lead widths.
- c — Terminal lead thicknesses.
- ϕD — Body diameters.
- D — Body lengths.
- E — Body Widths.
- e — Terminal lead spacings.
- F — Flange dimensions.
- H — Tip to tip lead span.
- h — Body bevel width.
- k — Index dimensions, length.
- L — Terminal lead lengths.
- Q — Standoff height. The height from the seating plane or a reference plane parallel to the seating plane.
- R — Radius dimensions.
- S — Distance between terminal leads and the body end.
- α — Angular dimensions.

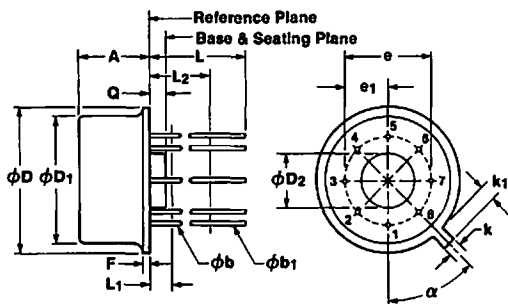
Standard lead finish is matte tin/lead. Other lead finishes per MIL-M-38510 are available on special orders. Standard 883 product meets lead finish requirements per MIL-M-38510.

PACKAGE DIMENSIONS — METAL CANS

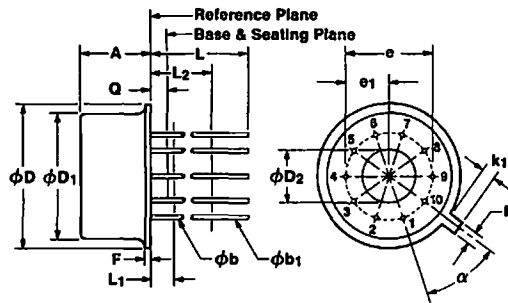
6-Lead TO-78 Metal Can (H-Suffix)



8-Lead TO-99 Metal Can (J-Suffix)



10-Lead TO-100 Metal Can (K-Suffix)



6 & 8-Lead Can Dimensions

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	—
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.335	0.370	8.51	9.40	—
ϕD_1	0.305	0.335	7.75	8.51	—
ϕD_2	0.110	0.160	2.79	4.06	—
e	0.200 BSC		5.08 BSC		3
e ₁	0.100 BSC		2.54 BSC		3
F	—	0.040	—	1.02	—
k	0.027	0.034	0.69	0.86	—
k ₁	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L ₁	—	0.050	—	1.27	1
L ₂	0.250	—	6.35	—	1
Q	0.010	0.045	0.25	1.14	—
α	45° BSC		45° BSC		3

10-Lead Can Dimensions

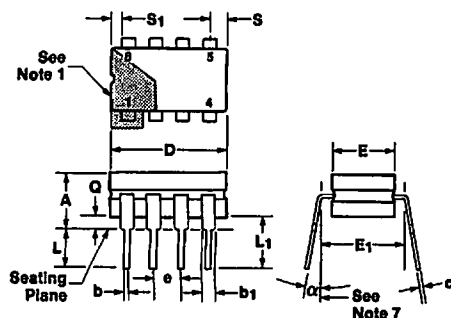
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	—
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.335	0.370	8.51	9.40	—
ϕD_1	0.305	0.335	7.75	8.51	—
ϕD_2	0.110	0.160	2.79	4.06	—
e	0.230 BSC		5.84 BSC		3
e ₁	0.115 BSC		2.92 BSC		3
F	—	0.040	—	1.02	—
k	0.027	0.034	0.69	0.86	—
k ₁	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L ₁	—	0.050	—	1.27	1
L ₂	0.250	—	6.35	—	1
Q	0.010	0.045	0.25	1.14	—
α	36° BSC		36° BSC		3

NOTES:

- (All leads) ϕb applies between L₁ and L₂. ϕb_1 applies between L₂ and 0.500 (12.70 mm) from the reference plane. Diameter is uncontrolled in L₁ and beyond 0.500 (12.70 mm) from the reference plane.
- Measured from the maximum diameter of the product.
- Leads having a maximum diameter 0.019 (0.48 mm) measured in gaging plane 0.054 (1.37 mm) + 0.001 (0.03 mm) - 0.000 (0.00 mm) below the base plane of the product is within 0.007 (0.18 mm) of their true position relative to a maximum width tab.

PACKAGE DIMENSIONS — CERAMIC DIPS

8-Lead Ceramic Dip (Z-Suffix)

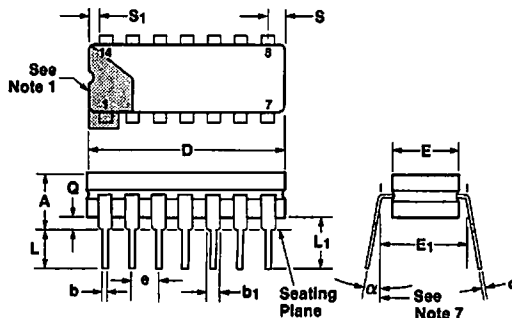


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.405	—	10.29	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.055	—	1.35	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

- Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
- The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
- Dimension Q shall be measured from the seating planes to the base plane.

14-Lead Ceramic Dip (Y-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.785	—	19.94	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic lead spacing is 0.100 (2.54 mm) between centerlines.
- Applies to all four corners.
- Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

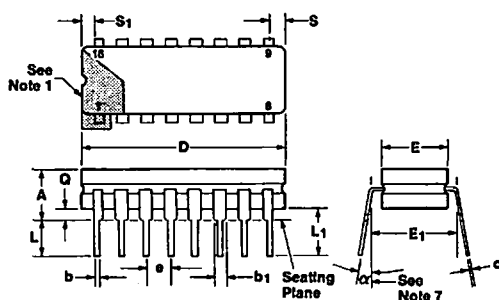


Precision Monolithics Inc.

PACKAGE INFORMATION

PACKAGE DIMENSIONS — CERAMIC DIPS

**16-Lead Ceramic Dip
(Q-Suffix)**

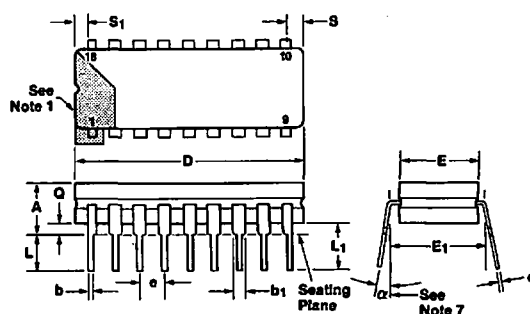


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.38	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.840	—	21.34	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.

**18-Lead Ceramic Dip
(X-Suffix)**



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.960	—	24.38	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

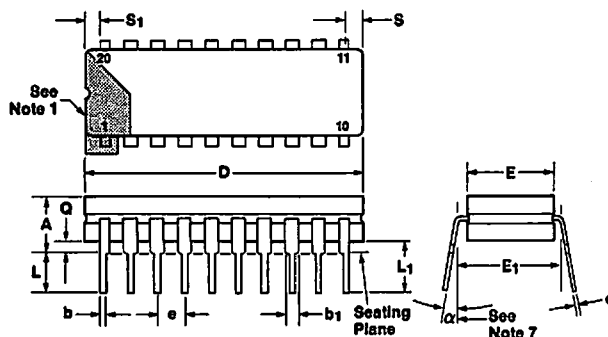


Precision Monolithics Inc.

PACKAGE INFORMATION

PACKAGE DIMENSIONS — CERAMIC DIPS

20-Lead Ceramic Dip
(R-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S ₁	0.005	—	0.13	—	8
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

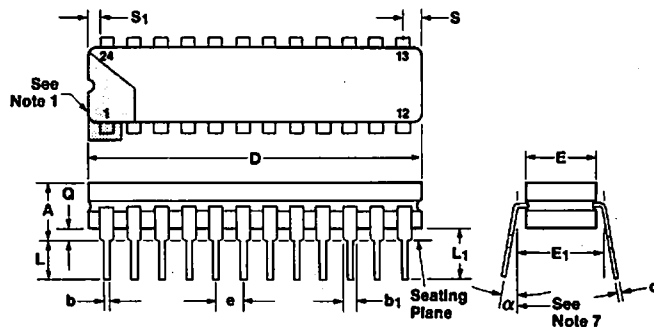


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — EPOXY DIPS

24-Lead Narrow-Body Ceramic Dip (W-Suffix)



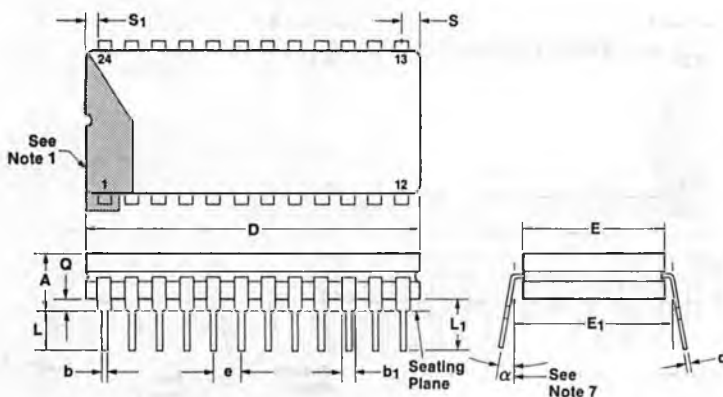
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.280	—	32.51	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimensions b₁ may be 0.023 (0.58 mm) for leads number 1, 12, 13 and 24 only.
3. Dimensions Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is 0.100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±0.010 (0.25 mm) of its exact longitudinal position relative to pins 1 and 24.
6. Applies to all four corners (leads number 1, 12, 13 and 24), and 40.5 shall apply.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — CERAMIC DIPS

24-Lead Ceramic Dip (V-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

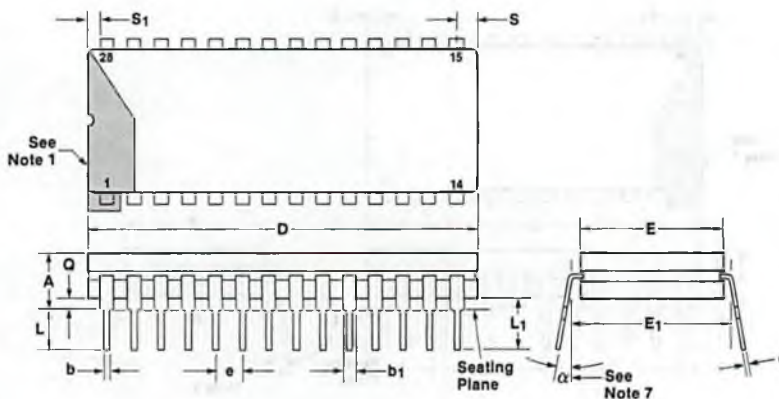


Precision Monolithics Inc.

PACKAGE INFORMATION

PACKAGE DIMENSIONS — CERAMIC DIPS

28-Lead Ceramic Dip (T-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.490	—	37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for leads number 1, 12, 13 and 24 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is 0.100 (2.54 mm) between centerlines. Each pin centerline shall be located within ± 0.010 (0.25 mm) of its exact longitudinal position relative to pins 1 and 24.
6. Applies to all four corners (leads number 1, 12, 13 and 24), and 40.5 shall apply.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

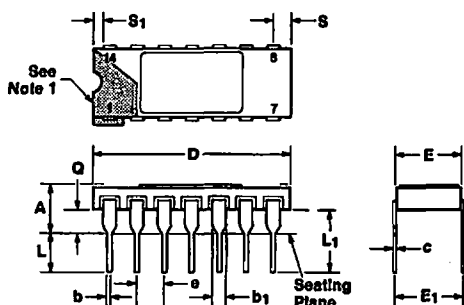


Precision Monolithics Inc.

PACKAGE INFORMATION

PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

**14-Lead Side-Brazed Dip
(YB-Suffix)**

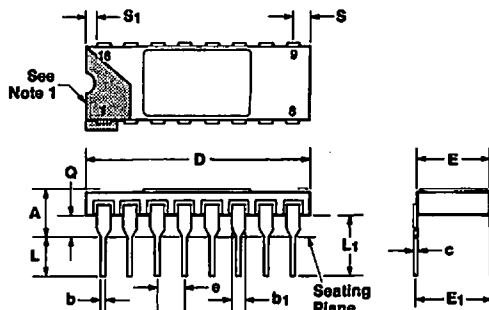


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.785	—	19.94	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.088	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum (limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.

**16-Lead Side-Brazed Dip
(QB-Suffix)**



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.840	—	21.34	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.080	—	2.03	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

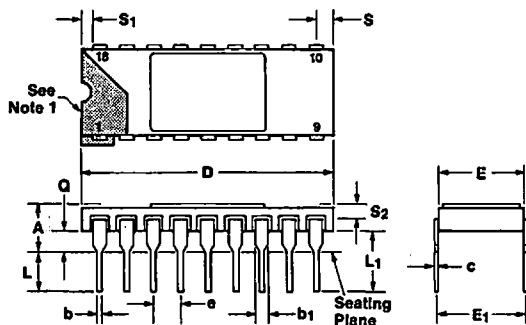
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

18-Lead Side-Brazed Dip (XB-Suffix)

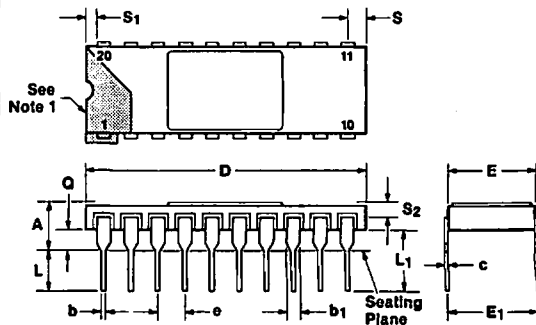


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	0.960	—	24.38	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.

20-Lead Side-Brazed Dip (RB-Suffix)

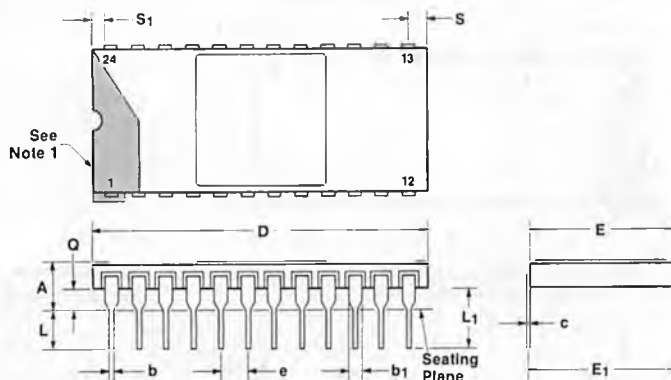


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.200	—	5.08	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.060	—	26.92	4
E	0.220	0.310	5.59	7.87	4
E ₁	0.290	0.320	7.37	8.13	7
e	0.100 BSC		2.54 BSC		5
L	0.125	0.200	3.18	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.060	0.38	1.52	3
S	—	0.098	—	2.03	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

24-Lead Side-Brazed Dip
(VB-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b ₁	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.290	—	32.77	4
E	0.500	0.610	12.70	15.49	4
E ₁	0.590	0.620	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L ₁	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.098	—	2.49	6
S ₁	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b₁ may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E₁ shall be measured at the centerline of the leads.

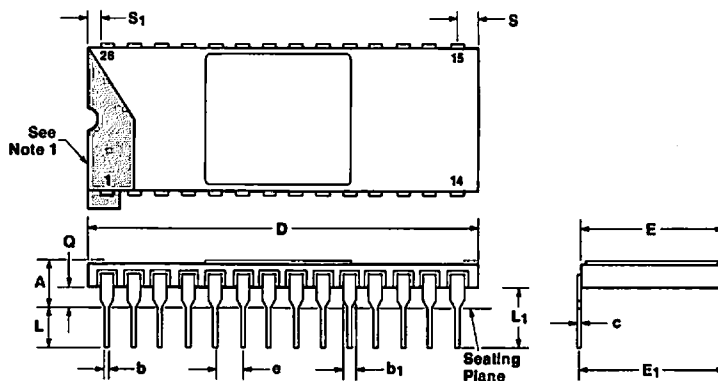


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — SIDE-BRAZED DIPS

28-Lead Side-Brazed Dip (TB-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.225	—	5.72	—
b	0.014	0.023	0.36	0.58	—
b_1	0.030	0.070	0.76	1.78	2
c	0.008	0.015	0.20	0.38	—
D	—	1.490	—	37.85	4
E	0.500	0.810	12.70	15.49	4
E_1	0.590	0.820	14.99	15.75	7
e	0.100 BSC		2.54 BSC		5
L	0.120	0.200	3.05	5.08	—
L_1	0.150	—	3.81	—	—
Q	0.015	0.075	0.38	1.91	3
S	—	0.088	—	2.49	6
S_1	0.005	—	0.13	—	6
α	0°	15°	0°	15°	—

NOTES:

1. Index area; a notch is or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic lead spacing is 0.100 (2.54 mm) between centerlines.
6. Applies to all four corners.
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.

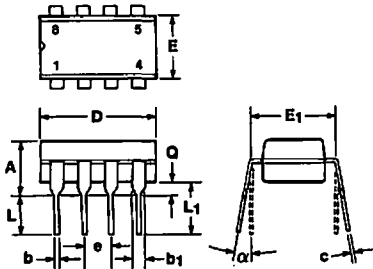


Precision Monolithics Inc.

PACKAGE INFORMATION

PACKAGE DIMENSIONS — EPOXY DIPS

**8-Lead Epoxy Dip
(P-Suffix)**

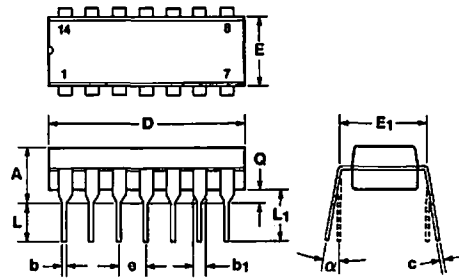


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.210	—	5.33	—
b	0.014	0.022	0.356	0.558	—
b ₁	0.045	0.070	1.15	1.77	—
c	0.008	0.015	0.203	0.381	—
D	0.348	0.430	8.84	10.92	3
E	0.240	0.280	6.10	7.11	3
E ₁	0.300	0.325	7.62	8.25	2
e	0.100 BSC		2.54 BSC		—
L	0.115	0.160	2.92	4.06	—
L ₁	0.130	—	3.30	—	—
Q	0.015 TYP		0.381 TYP		—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.
3. D and E dimensions do not include mold flash or protrusions.

**14-Lead Epoxy Dip
(P-Suffix)**



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.210	—	5.33	—
b	0.014	0.022	0.356	0.558	—
b ₁	0.045	0.070	1.15	1.77	—
c	0.008	0.015	0.203	0.381	—
D	0.725	0.795	18.41	20.19	3
E	0.240	0.280	6.10	7.11	3
E ₁	0.300	0.325	7.62	8.25	2
e	0.100 BSC		2.54 BSC		—
L	0.115	0.160	2.92	4.06	—
L ₁	0.130	—	3.30	—	—
Q	0.015	—	0.381	—	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.
3. D and E dimensions do not include mold flash or protrusions.

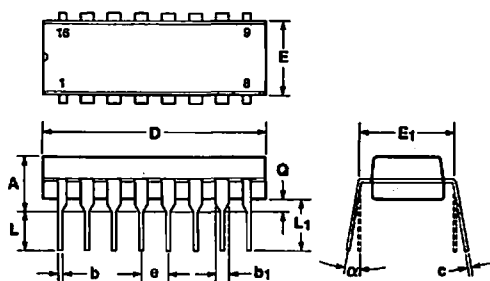


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — EPOXY DIPS

16-Lead Epoxy Dip
(P-Suffix)

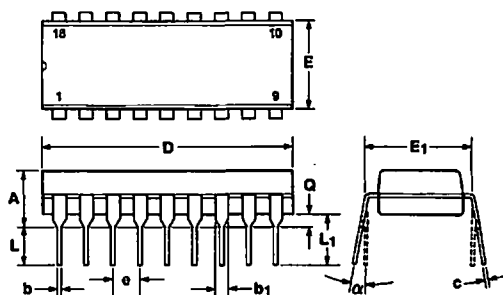


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.210	—	5.33	—
b	0.014	0.022	0.356	0.558	—
b ₁	0.045	0.070	1.15	1.77	—
c	0.008	0.015	0.20	0.38	—
D	0.745	0.840	18.92	21.33	3
E	0.240	0.280	6.10	7.11	3
E ₁	0.300	0.325	7.62	8.25	2
e	0.100 BSC		2.54 BSC		—
L	0.115	0.160	2.92	4.06	—
L ₁	0.130	—	3.30	—	—
Q	0.015	—	0.38	—	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.
3. D and E dimensions do not include mold flash or protrusion.

18-Lead Epoxy Dip
(P-Suffix)



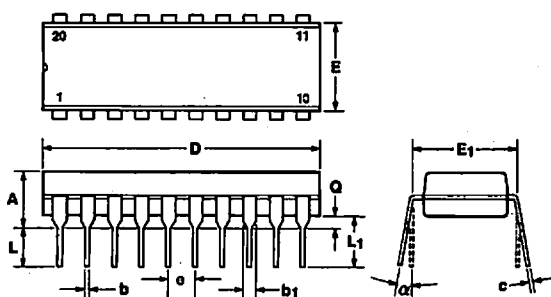
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.210	—	5.33	—
b	0.014	0.022	0.356	0.558	—
b ₁	0.045	0.070	1.15	1.77	—
c	0.008	0.015	0.20	0.38	—
D	0.845	0.925	21.46	23.49	3
E	0.240	0.280	6.10	7.11	3
E ₁	0.300	0.325	7.62	8.25	2
e	0.100 BSC		2.54 BSC		—
L	0.115	0.160	2.92	4.06	—
L ₁	0.130	—	3.30	—	—
Q	0.015	—	0.38	—	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.
3. D and E dimensions do not include mold flash or protrusion.

PACKAGE DIMENSIONS — EPOXY DIPS

20-Lead Epoxy Dip (P-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.210	—	5.33	—
b	0.014	0.022	0.356	0.558	—
b ₁	0.045	0.070	1.15	1.77	—
c	0.008	0.015	0.203	0.381	—
D	0.925	1.060	23.49	26.92	3
E	0.240	0.280	6.10	7.11	3
E ₁	0.300	0.325	7.62	8.25	2
o	0.100 BSC		2.54 BSC		—
L	0.115	0.160	2.92	4.06	—
L ₁	0.130	—	3.30	—	—
Q	0.015	—	0.38	1.52	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.
3. D and E dimensions do not include mold flash or protrusion.

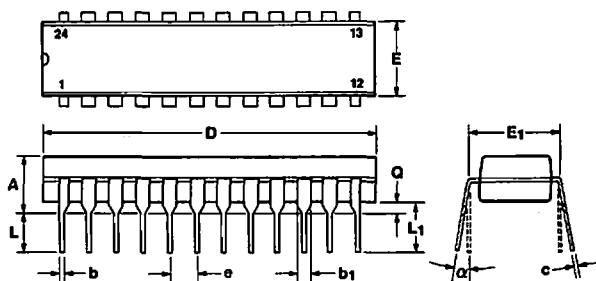


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — EPOXY DIPS

24-Lead
Narrow-Body Epoxy Dip
(P-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.210	—	5.33	—
b	0.014	0.022	0.356	0.558	—
b ₁	0.045	0.070	1.15	1.77	—
c	0.008	0.015	0.203	0.381	—
D	1.125	1.275	28.6	32.3	3
E	0.240	0.280	6.10	7.11	3
E ₁	0.300	0.325	7.62	8.25	2
e	0.100 BSC		2.54 BSC		—
L	0.115	0.160	2.92	4.06	—
L ₁	0.130	—	3.30	—	—
Q	0.015	—	0.38	—	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.
3. D and E dimensions do not include mold flash or protrusions.

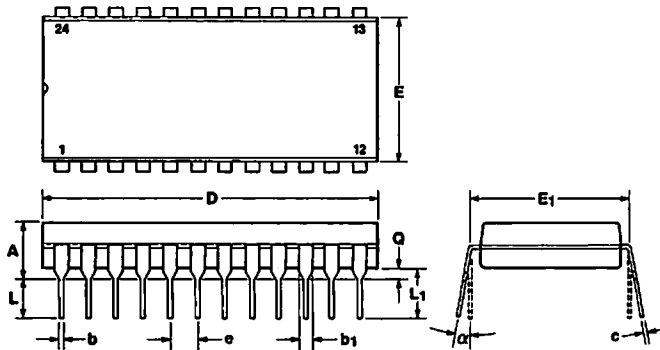


Precision Monolithics Inc.

PACKAGE INFORMATION

PACKAGE DIMENSIONS — EPOXY DIPS

24-Lead Epoxy Dip
(P-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	—	0.250	—	6.35	—
b	0.014	0.022	0.36	0.558	—
b ₁	0.030	0.070	0.76	1.78	—
c	0.008	0.015	0.203	0.381	—
D	1.150	1.290	29.3	32.7	3
E	0.485	0.580	12.32	14.73	3
E ₁	0.600	0.625	15.24	15.87	2
e	0.100 BSC		2.54 BSC		—
L	0.115	0.200	2.93	5.08	—
L ₁	0.130	—	3.30	—	—
Q	0.015	—	0.38	—	—
α	0°	15°	0°	15°	—

NOTES:

1. Minor changes in dimensions may occur without advance notice.
2. Dimension "E₁" to center of leads when formed parallel.
3. D and E dimensions do not include mold flash or protrusion.

PACKAGE INFORMATION

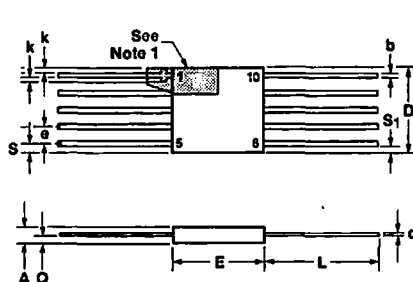


Precision Monolithics Inc.

PACKAGE INFORMATION

PACKAGE DIMENSIONS — CERPACKS

**10-Lead Cerpack
(L-Suffix)**

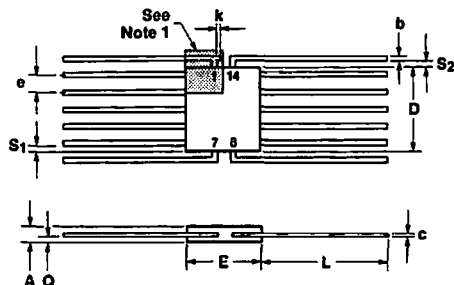


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	—
b	0.010	0.019	0.25	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.290	—	7.37	3
E	0.240	0.260	6.10	6.60	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S	—	0.045	—	1.14	5
S ₁	0.005	—	0.13	—	5, 6

NOTES:

1. Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic lead spacing is 0.050 (1.27 mm) between centerlines.
5. Applies to all four corners.

**14-Lead Cerpack
(M-Suffix)**

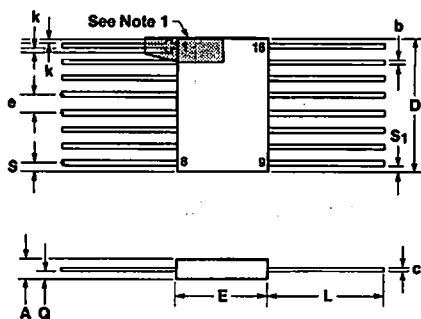


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	—
b	0.010	0.019	0.25	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.280	—	7.11	3
E	0.240	0.260	6.10	6.60	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S ₁	0.005	—	0.13	—	5, 6
S ₂	0.004	—	0.10	—	—

6. Dimension S₁ (See 40.3) may be 0.000 (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
7. Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
8. Optional, see note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

PACKAGE DIMENSIONS — CERPACKS

16-Lead Cerpack (F-Suffix)

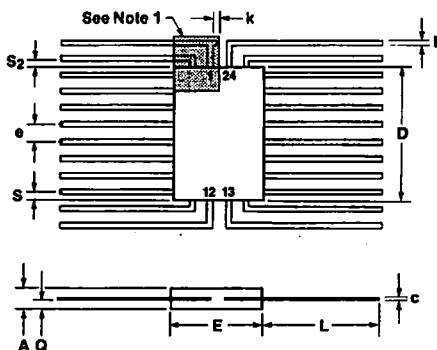


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.085	1.14	2.16	—
b	0.015	0.019	0.38	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.440	—	11.18	3
E	0.245	0.285	6.22	7.24	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
O	0.010	0.040	0.23	1.02	2
S	—	0.045	—	1.14	5
S ₁	0.005	—	0.13	—	5, 6

NOTES:

- Index area: a notch or a lead one identification mark is located adjacent to lead one and is located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
- Dimension Q shall be measured at the point of exit of the lead from the body.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic lead spacing is 0.050 (1.27 mm) between centerlines.
- Applies to all four corners.

24-Lead Cerpack (N-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.080	1.14	2.29	—
b	0.015	0.019	0.38	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.430	—	10.92	3
E	0.245	0.285	6.22	7.24	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
O	0.010	0.040	0.25	1.02	2
S	0.005	—	0.13	—	5, 6
S ₂	0.004	—	0.10	—	—

- Dimension S₁ (See 40.3) may be 0.000 (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
- Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
- Optional, see note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

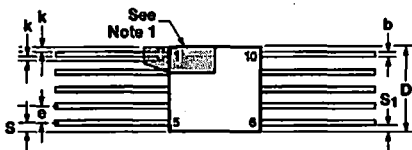


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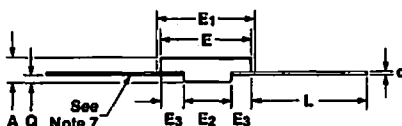
PACKAGE INFORMATION

PACKAGE DIMENSIONS — FLATPACKS

10-Lead Flatpack (L-Suffix)



Bottom-Brazed (LB-Suffix)

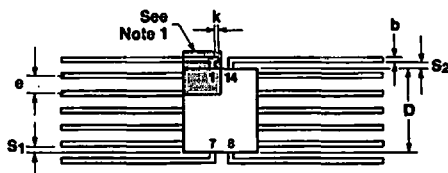


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	—
b	0.010	0.019	0.25	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.290	—	7.37	3
E	0.240	0.260	6.10	6.60	—
E ₁	—	0.280	—	7.11	3
E ₂	0.125	—	3.18	—	—
E ₃	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S	—	0.045	—	1.14	5
S ₁	0.005	—	0.13	—	5, 6

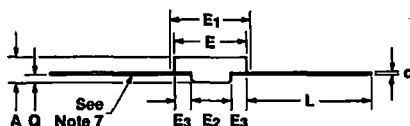
NOTES:

- Index area; a notch or a lead one identification mark is located adjacent to lead one and shall be located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
- Dimension Q shall be measured at the point of exit of the lead from the body.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic lead spacing is 0.050 (1.27 mm) between centerlines.
- Applies to all four corners.

14-Lead Flatpack (M-Suffix)



Bottom-Brazed (MB-Suffix)

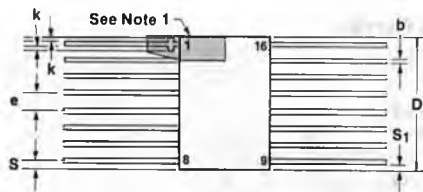


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.030	0.085	0.76	2.16	—
b	0.010	0.019	0.25	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.280	—	7.11	3
E	0.240	0.260	6.10	6.60	—
E ₁	—	0.280	—	7.11	3
E ₂	0.125	—	3.18	—	—
E ₃	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S ₁	0.005	—	0.13	—	5, 6
S ₂	0.004	—	0.10	—	—

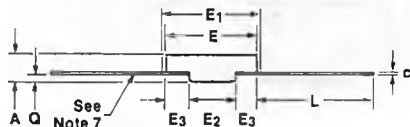
- Dimension S₂ (See 40.3) may be 0.000 (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
- Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
- Optional, see note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

PACKAGE DIMENSIONS — FLATPACKS

16-Lead Flatpack (F-Suffix)



Bottom-Brazed (FB-Suffix)

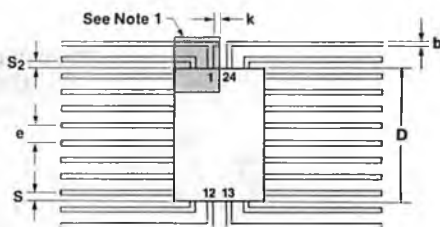


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.085	1.14	2.16	—
b	0.015	0.019	0.38	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.440	—	11.18	3
E	0.245	0.285	6.22	7.24	—
E ₁	—	0.305	—	7.75	3
E ₂	0.130	—	3.30	—	—
E ₃	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.23	1.02	2
S	—	0.045	—	1.14	5
S ₁	0.005	—	0.13	—	5, 6

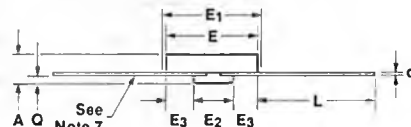
NOTES:

- Index area; a notch or a lead one identification mark is located adjacent to lead one and is located within the shaded area shown. Alternatively, a tab (dim. k) may be used to identify lead one. This tab may be located on either side as shown.
- Dimension Q shall be measured at the point of exit of the lead from the body.
- This dimension allows for off-center lid, meniscus and glass overrun.
- The basic lead spacing is 0.050 (1.27 mm) between centerlines.
- Applies to all four corners.

24-Lead Flatpack (N-Suffix)



Bottom-Brazed (NB-Suffix)

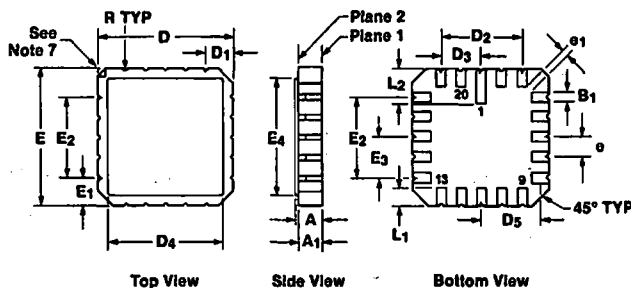


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.090	1.14	2.29	—
b	0.015	0.019	0.38	0.48	—
c	0.003	0.006	0.08	0.15	—
D	—	0.430	—	10.92	3
E	0.245	0.285	6.22	7.24	—
E ₁	—	0.305	—	7.75	3
E ₂	0.125	—	3.18	—	—
E ₃	0.030	—	0.76	—	—
e	0.050 BSC		1.27 BSC		4
k	0.008	0.015	0.20	0.38	8
L	0.250	0.370	6.35	9.40	—
Q	0.010	0.040	0.25	1.02	2
S	0.005	—	0.13	—	5, 6
S ₂	0.004	—	0.10	—	—

- Dimension S₂ (See 40.3) may be 0.000 (0.00 mm) if corner leads bend toward the cavity of the package within one lead's width from the point of entry of the lead into body.
- Optional configuration. If this configuration is used, no organic or polymeric materials are molded to the bottom of the package to cover the leads.
- Optional, see note 1. If a lead one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.

PACKAGE DIMENSIONS — LEADLESS CHIP CARRIERS

20-Position Chip Carrier (RC-Suffix)



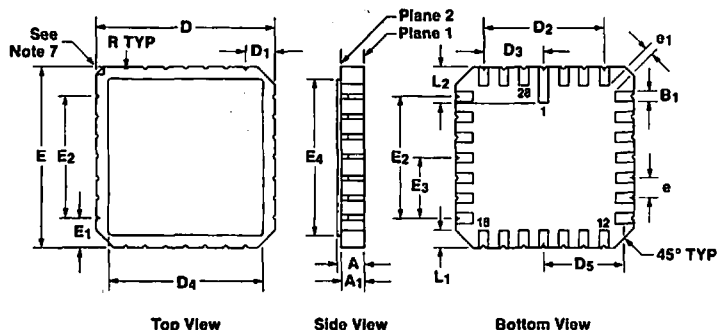
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	5
A ₁	0.054	0.088	1.37	2.24	—
B ₁	0.022	0.028	0.56	0.71	2
D	0.342	0.358	8.69	9.09	—
D ₁	0.075 REF		1.91 REF		—
D ₂	0.200 REF		5.08 REF		—
D ₃	0.100 REF		2.54 REF		—
D ₄	—	0.358	—	9.09	3
D ₅	0.150 BSC		3.81 BSC		—
E	0.342	0.358	8.69	9.09	—
E ₁	0.075 REF		1.91 REF		—
E ₂	0.200 REF		5.08 REF		—
E ₃	0.100 REF		1.91 REF		—
E ₄	—	0.358	—	9.09	3
e	0.050 BSC		1.27 BSC		—
e ₁	0.015	—	0.38	—	1
L ₁	0.045	0.055	1.14	1.40	—
L ₂	0.077	0.093	1.96	2.36	4
R	0.007	0.011	0.18	0.28	—

NOTES:

1. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.
2. Electrical connection is required on plane 1. Metallization is optional on plane 2. However, if plane 2 is metallized it must be electrically connected.
3. A minimum clearance of 0.020" (0.508 mm) is maintained between overall dimensions D₄ × E₄ and all other features, including metallization, chamfers and edges.
4. Non-electrical features for No. 1 terminal identification, optical orientation or handling purposes shall be within the shaded area shown on plane 2.
5. Dimension A controls the overall package thickness.
6. Length of pad metallization may increase only toward package periphery.
7. When space is available, the index corner may be metallized on either or both planes 1 and 2. The package edge at the index corner shall not be metallized.

PACKAGE DIMENSIONS — LEADLESS CHIP CARRIERS

28-Position Chip Carrier (TC-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	5
A ₁	0.054	0.088	1.37	2.24	—
B ₁	0.022	0.028	0.56	0.71	2
D	0.442	0.458	11.23	11.63	—
D ₁	0.075 REF		1.91 REF		—
D ₂	0.300 REF		7.62 REF		—
D ₃	0.150 REF		3.81 REF		—
D ₄	—	0.458	—	11.63	3
D ₅	0.200 BSC		5.08 BSC		—
E	0.442	0.458	11.23	11.63	—
E ₁	0.075 REF		1.91 REF		—
E ₂	0.300 REF		7.62 REF		—
E ₃	0.150 REF		3.81 REF		—
E ₄	—	0.458	—	11.63	3
e	0.050	—	1.27	—	—
e ₁	0.015	—	0.38	—	1
L ₁	0.045	0.055	1.14	1.40	—
L ₂	0.077	0.093	1.96	2.36	4
R	0.007	0.011	0.18	0.28	—

NOTES:

1. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.
2. Electrical connection is required on plane 1. Metallization is optional on plane 2. However, if plane 2 is metallized it must be electrically connected.
3. A minimum clearance of 0.020" (0.508 mm) is maintained between overall dimensions D₄ × E₄ and all other features, including metallization, chamfers and edges.
4. Non-electrical features for No. 1 terminal identification, optical orientation or handling purposes shall be within the shaded area shown on plane 2.
5. Dimension A controls the overall package thickness.
6. Length of pad metallization may increase only toward package periphery.
7. When space is available, the index corner may be metallized on either or both planes 1 and 2. The package edge at the index corner shall not be metallized.

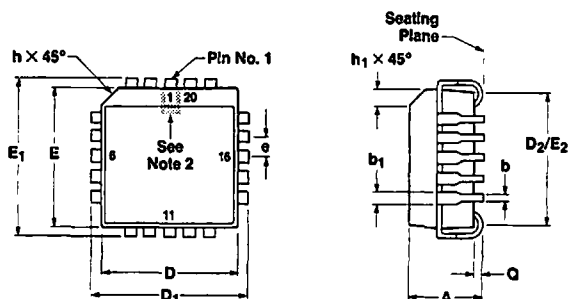


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — PLASTIC LEADED CHIP CARRIERS

PLCC-20 20-Lead Plastic Leaded Chip Carrier (PC-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.200	4.570	
b	0.013	0.021	0.331	0.533	
b ₁	0.028	0.032	0.661	0.812	
D	0.350	0.356	8.890	9.042	
D ₁	0.385	0.395	9.780	10.030	
D ₂	0.290	0.330	7.370	8.380	3
E	0.350	0.356	8.890	9.042	
E ₁	0.385	0.395	9.780	10.030	
E ₂	0.290	0.330	7.370	8.380	3
e	0.050 BSC		1.270 BSC		
h	0.042	0.048	1.067	1.219	
h ₁	0.042	0.056	1.070	1.420	
Q	0.020	—	0.510	—	

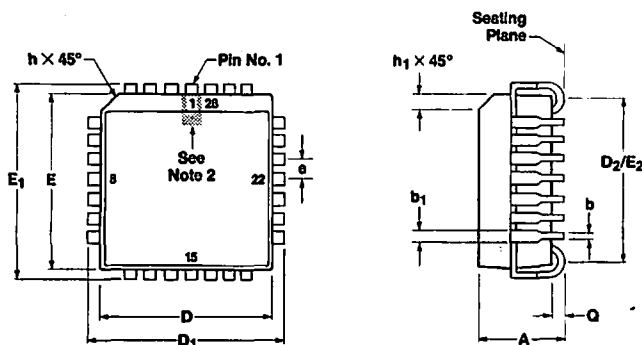
NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AA (Issue A, October 31, 1984).
2. Index area; a dimple or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
3. Overall distance between leads at tangent points to seating plane.

Precision Monolithics Inc.

PACKAGE DIMENSIONS — PLASTIC LEADED CHIP CARRIERS

PLCC-28 28-Lead Plastic Leaded Chip Carrier (PC-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.200	4.570	
b	0.013	0.021	0.331	0.533	
b ₁	0.026	0.032	0.661	0.812	
D	0.450	0.456	11.430	11.582	
D ₁	0.485	0.495	12.320	12.570	
D ₂	0.390	0.430	9.910	10.920	3
E	0.450	0.456	11.430	11.582	
E ₁	0.485	0.495	12.320	12.570	
E ₂	0.390	0.430	9.910	10.920	3
e	0.050 BSC		1.270 BSC		
h	0.042	0.048	1.067	1.219	
h ₁	0.042	0.056	1.070	1.420	
Q	0.020	—	0.510	—	

NOTES:

1. Package dimensions conform to JEDEC specification MO-047-AB (Issue A, October 31, 1984).
2. Index area; a dimple or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
3. Overall distance between leads at tangent points to seating plane.

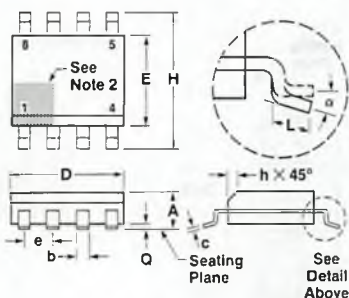


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — SMALL OUTLINE ICs

SO-8
8-Lead Narrow-Body SO
(S-Suffix)

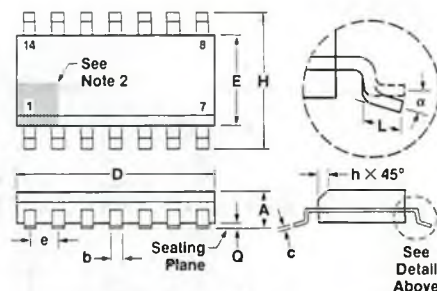


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AA (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

SO-14
14-Lead Narrow-Body SO
(S-Suffix)



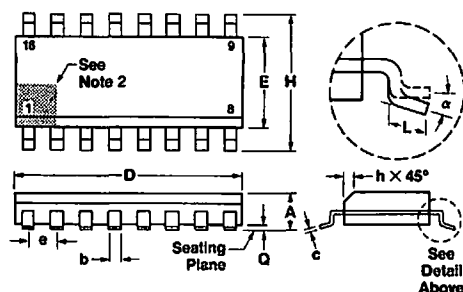
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AB (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

PACKAGE DIMENSIONS — SMALL OUTLINE ICs

SO-16 16-Lead Narrow-Body SO (S-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0099	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES:

1. Package dimensions conform to JEDEC specification MS-012-AC (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

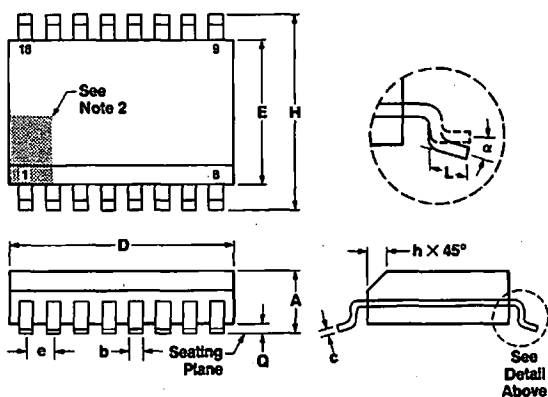


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — SMALL OUTLINE ICs

SOL-16 16-Lead Wide-Body SO (S-Suffix)



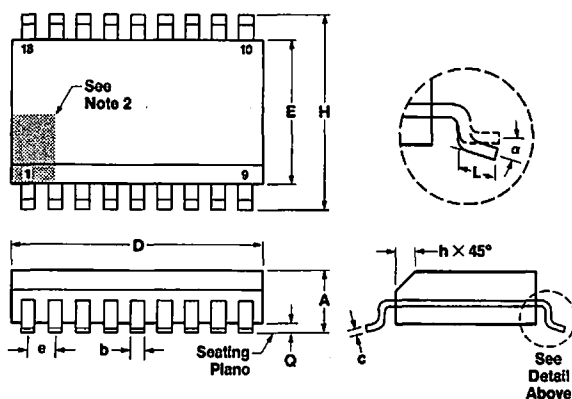
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AA (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

PACKAGE DIMENSIONS — SMALL OUTLINE ICs

SOL-18 18-Lead Wide-Body SO (S-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.4469	0.4625	11.35	11.75	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AB (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

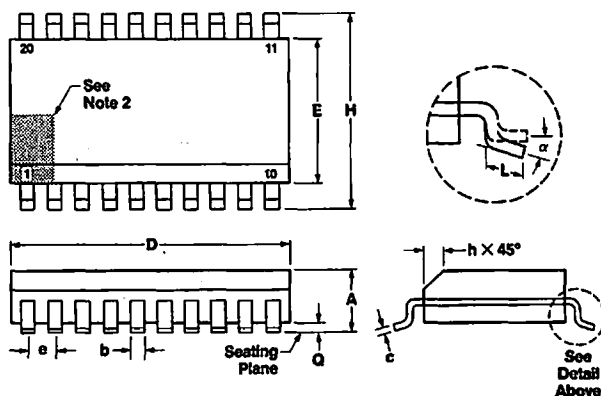


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — SMALL OUTLINE ICs

SOL-20 20-Lead Wide-Body SO (S-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0136	0.0182	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.4961	0.5118	12.60	13.00	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AC (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

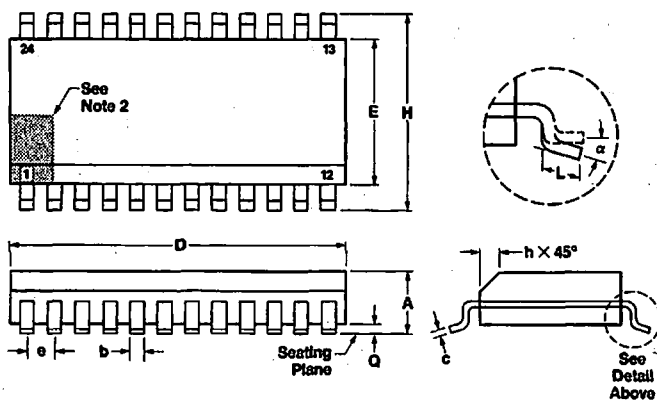


Precision Monolithics Inc.

PACKAGE INFORMATION

PACKAGE DIMENSIONS — SMALL OUTLINE ICs

SOL-24 24-Lead Wide-Body SO (S-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AD (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

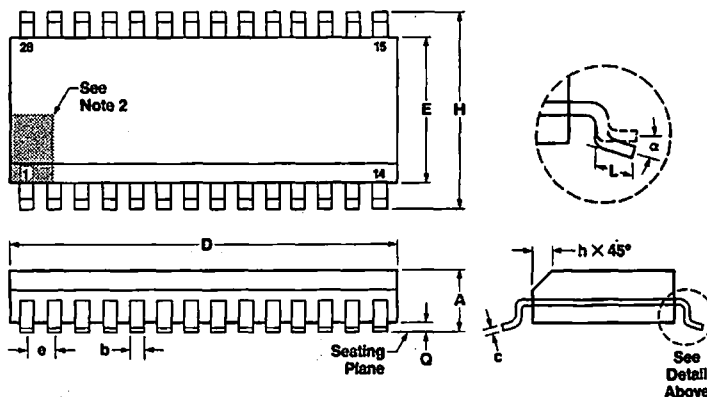


PACKAGE INFORMATION

Precision Monolithics Inc.

PACKAGE DIMENSIONS — SMALL OUTLINE ICs

SOL-28 28-Lead Wide-Body SO (S-Suffix)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.6969	0.7125	17.70	18.10	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES:

- Package dimensions conform to JEDEC specification MS-013-AE (Issue A, June 1985).
- Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

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Authorized Distributors
North America 17-5

Sales Offices, Representatives
International 17-11

Authorized Distributors
International 17-12



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